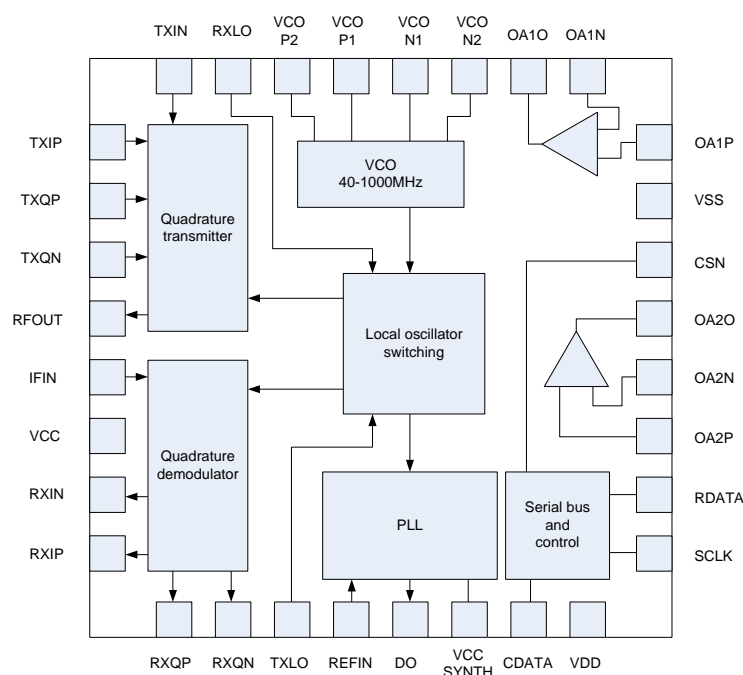


### Features

- 20 – 300MHz IF/RF Demodulator
- 10MHz Rx and 25MHz Tx I/Q Bandwidth
- 20 – 1000 MHz RF Modulator
- 0dBm Modulator Output
- < 1 degree I/Q Phase Matching
- < 0.5 dB I/Q Gain Matching
- Low Power, 3.0V – 3.6V Operation
- Small 32-lead VQFN Package

### Applications

- Wireless Data Terminals
- HF/VHF and UHF Mobile Radio
- Avionics Radio Systems
- Telemetry Modems
- Wireless Microphones
- Software Defined Radio (SDR)
- Satellite Terminals



## 1 Brief Description

The CMX973 integrates a quadrature (I/Q) modulator and a low-power quadrature IF/RF demodulator, both featuring a wide operating frequency range and optimised power consumption. The demodulator is suitable for superheterodyne architectures with IF frequencies up to 300MHz and the device may be used in low IF systems or those converting down to baseband. The modulator converts directly from baseband to the desired transmit frequency and features quadrature phase correction to minimise unwanted spectral components. An on-chip PLL and VCO, together with uncommitted baseband differential amplifiers, provide additional flexibility. Control of the CMX973 is by serial bus. The CMX973 is supplied in an RF-optimised 32-lead VQFN package.

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## 1.1 History

Version	Changes	Date
13	<ul style="list-style-type: none"> <li>Section 7.6: updated input 1dB compression point</li> <li>Section 7.6: new Figure 22 Gain v Input level at IF of 45MH</li> </ul>	08/04/22
12	<ul style="list-style-type: none"> <li>Adjustment of receive current consumption values (no change in overall performance).</li> <li>Typical equivalent output IP3 specification changed from 21 dBm to 14 dBm.</li> </ul>	23/4/19
11	<ul style="list-style-type: none"> <li>LO Input impedance: Smith chart added in section 7.1.2</li> </ul>	12/02/15
10	<ul style="list-style-type: none"> <li>Information added on modulator harmonics (section 7.7.3).</li> </ul>	25/2/13
9	<ul style="list-style-type: none"> <li>Gain compression information added (section 7.6); related clarifications.</li> </ul>	16/11/12
8	<ul style="list-style-type: none"> <li>PLL spurious issue noted in section 5.4.3.</li> </ul>	10/10/12
7	<ul style="list-style-type: none"> <li>Rx Operation to 300MHz and PLL to 1GHz.</li> </ul>	8/6/12
6	<ul style="list-style-type: none"> <li>Note on I/Q Tx bandwidth performance added.</li> </ul>	17/5/12
5	<ul style="list-style-type: none"> <li>Editorial correction and extra information added.</li> </ul>	23/4/12
4	<ul style="list-style-type: none"> <li>Changes to document style.</li> </ul>	14/12/11
3	<ul style="list-style-type: none"> <li>Document revised based on test results from first silicon.</li> </ul>	10/10/11
2	<ul style="list-style-type: none"> <li>Typographical error in naming of PLL registers corrected.</li> </ul>	9/5/11
1	<ul style="list-style-type: none"> <li>Original document, first approved.</li> </ul>	3/3/11

## 2 Block Diagram

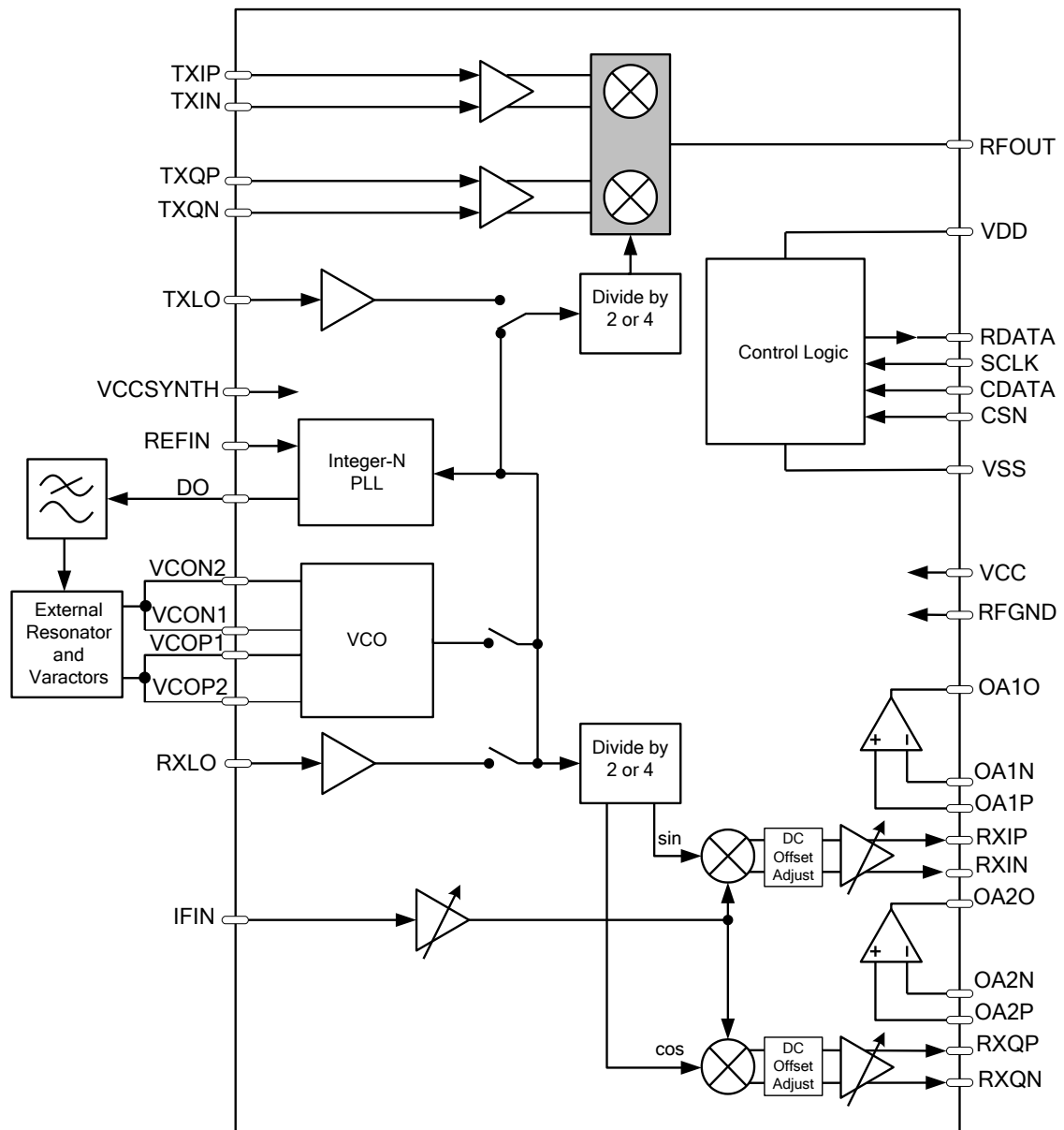


Figure 1 Block Diagram

### 3 Pin List

Pin	Name	Type	Function
1	TXIP	IP	Analogue input for baseband transmit I signal (positive)
2	TXQP	IP	Analogue input for baseband transmit Q signal (positive)
3	TXQN	IP	Analogue input for baseband transmit Q signal (negative)
4	RFOUT	OP	RF output
5	IFIN	IP	IF/RF input signal
6	VCC	PWR	Analogue and RF supply
7	RXIN	OP	Analogue output for baseband receive I signal (negative)
8	RXIP	OP	Analogue output for baseband receive I signal (positive)
9	RXQP	OP	Analogue output for baseband receive Q signal (positive)
10	RXQN	OP	Analogue output for baseband receive Q signal (negative)
11	TXLO	IP	Input for modulator local oscillator
12	REFIN	IP	PLL frequency reference input
13	DO	OP	PLL charge pump output
14	VCCSYNTH	PWR	RF supply for synthesiser
15	CDATA	IP	C-BUS data input
16	VDD	PWR	C-BUS and digital supply
17	SCLK	IP	C-BUS clock input
18	RDATA	TSOP	C-BUS data output
19	OA2P	IP	Baseband amplifier 2 positive input
20	OA2N	IP	Baseband amplifier 2 negative input
21	OA2O	OP	Baseband amplifier 2 output
22	CSN	IP	C-BUS chip select
23	VSS	PWR	C-BUS and digital ground
24	OA1P	IP	Baseband amplifier 1 positive input
25	OA1N	IP	Baseband amplifier 1 negative input
26	OA1O	OP	Baseband amplifier 1 output
27	VCON2	NR	VCO negative port 2
28	VCON1	NR	VCO negative port 1
29	VCOP1	NR	VCO positive port 1
30	VCOP2	NR	VCO positive port 2
31	RXLO	IP	Input for demodulator local oscillator
32	TXIN	IP	Analogue input for baseband transmit I signal (negative)
33*	RFGND	PWR	Analogue and RF ground

Notes: IP = Input

OP = Output

TSOP = Three-state output

PWR = Power connection

NR = Negative resistance VCO port

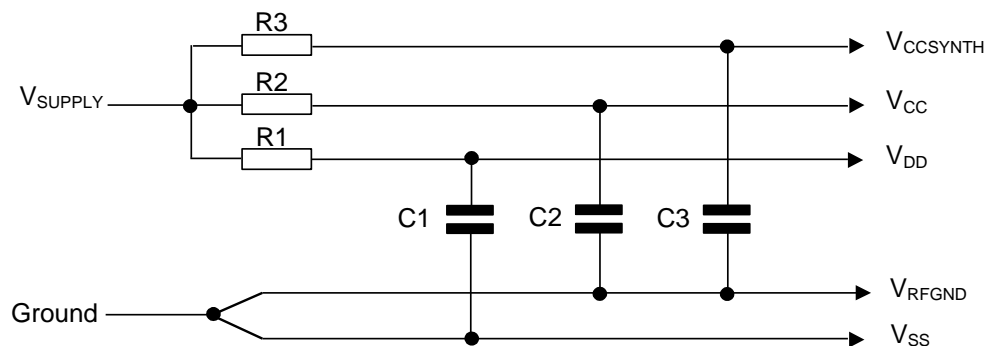
\* Pin 33 is the exposed metal pad on the back of the package and should be connected to the RF Ground Plane (V<sub>RFGND</sub>).

**Table 1 Pin List**

## 4 External Components

### 4.1 Power Supply Decoupling

This device has separate supply pins for the analogue and digital circuitry; a 3.3V nominal supply is recommended.



**Figure 2 Power Supply Connections and Decoupling**

C1	10nF	R1	10Ω
C2	10nF	R2	3.3Ω
C3	10nF	R3	10Ω

Resistors  $\pm 1\%$ , capacitors  $\pm 20\%$

**Table 2 Power Supply Component Values**

Note:

It is expected that low-frequency interference on the 3.3V supply will be removed by active regulation. A large capacitor is an alternative but may require more board space and so may not be preferred. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively by using the resistor as shown. The use of resistors results in small dc voltage drops. Choosing resistor values approximately inversely proportional to the dc current requirements of each supply pin ensures the dc voltage drop on each supply is reasonably matched. In any case, the dc voltage change that results are well within the design tolerance of the device. If higher impedance resistors are used then greater care will be needed to ensure that the supply voltages are maintained within tolerance, including when parts of the device are enabled or disabled.

4.2 Quadrature Modulator

Typical circuit for the quadrature modulator output is shown in Figure 3/Table 3.

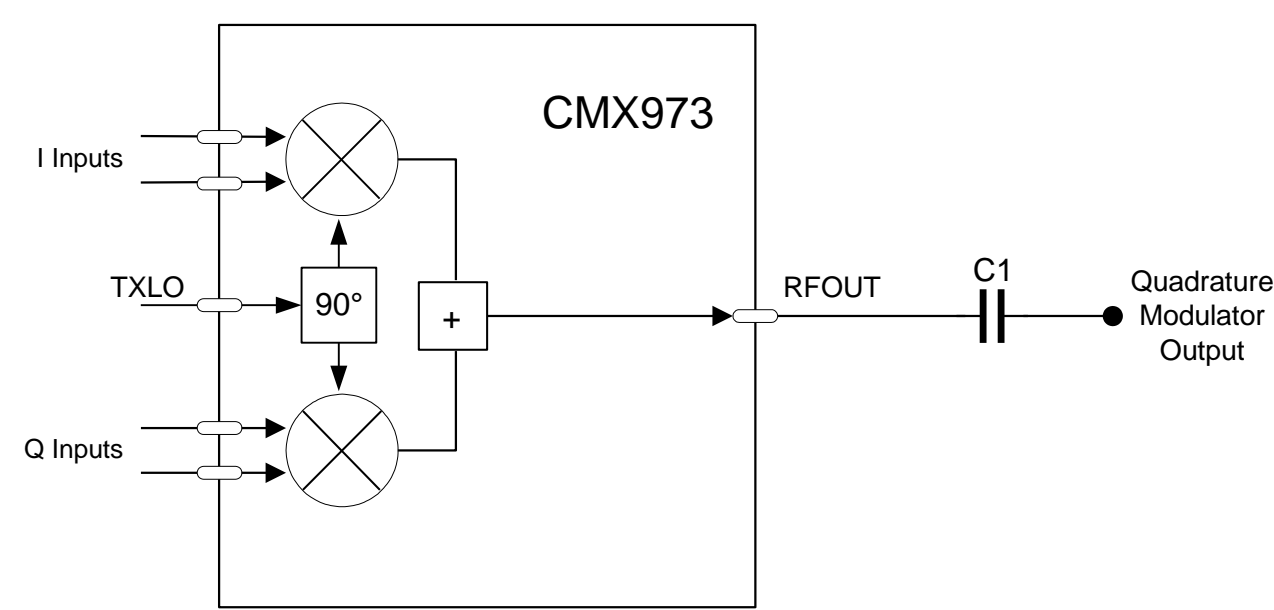


Figure 3 Quadrature Modulator Output External Components (20MHz to 1GHz)

C1	1nF
----	-----

Table 3 Quadrature Modulator Output Components

4.3 Quadrature Demodulator

The input impedance of the quadrature demodulator section is shown in section 7.1. The input can be driven from a 50 Ohm source or can be matched to 50 Ohms. A typical 50 Ohm matching circuit is shown in Figure 4 for operation at 45MHz.

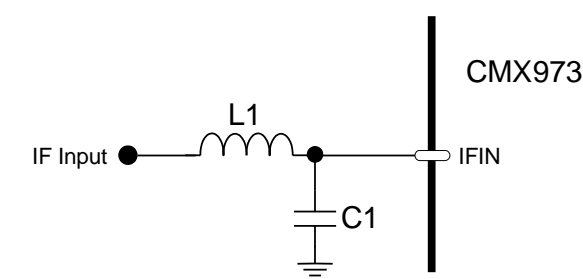


Figure 4 IF Input Match Circuit

L1	910nH
C1	10pF

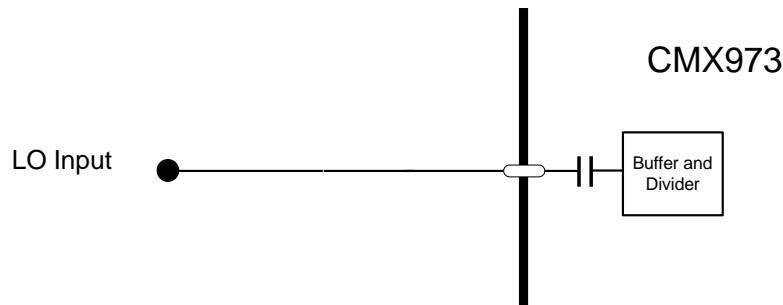
Table 4 Quadrature Demodulator Input Components



#### 4.4 Local Oscillator (LO) Input

The CMX973 has single-ended TXLO and RXLO inputs. The CMX973 transmit modulator LO can come from either the on-chip VCO/PLL or from an external source (TXLO). Likewise, the receive demodulator LO can come from either the on-chip VCO/PLL or from an external source (RXLO), see section 5.4.

Users should be aware that the presence of high levels of harmonics in the signals applied to the LO inputs might degrade quadrature accuracy.



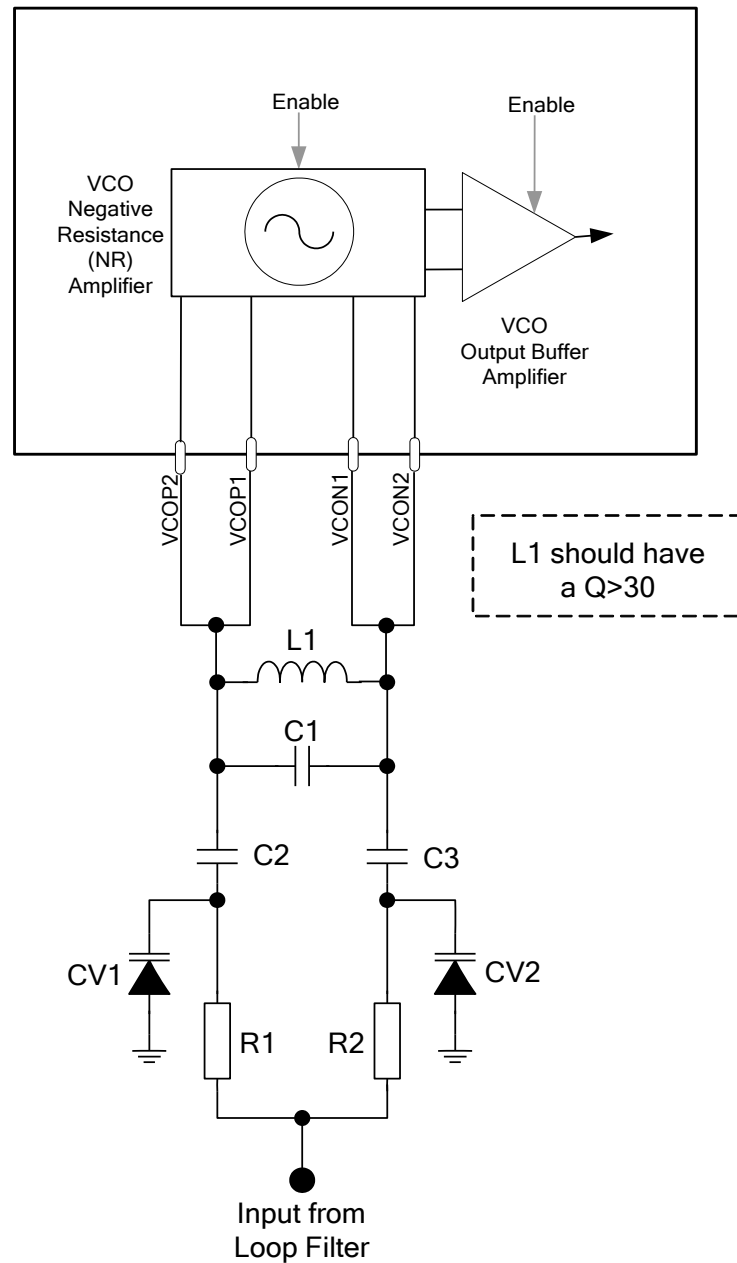
**Figure 5 LO Input Configuration**

#### 4.5 VCO and PLL

A typical configuration for using the internal VCO negative resistance amplifier at 180MHz is shown in Figure 6. The other external components required to complete the PLL are the loop filter components, see Figure 7 – which shows a 3<sup>rd</sup> order loop filter; typical values for a 300Hz bandwidth are given in Table 6.

VCOP1 should be connected to VCOP2 and similarly VCON1 to VCON2 in order to form the negative resistance loop. It is recommended that the parallel LC tank (L1/C1) is situated as close to the package as possible, with the inductor closest to the device pins. Also the shorting of VCOP1 to VCOP2 and of VCON1 to VCON2 occurs as close as possible to the tank circuit – this minimises the effects of series inductance on the oscillator behaviour.

For further information see also section 7.8.



**Figure 6 Example External Components – VCO External Tank Circuit**

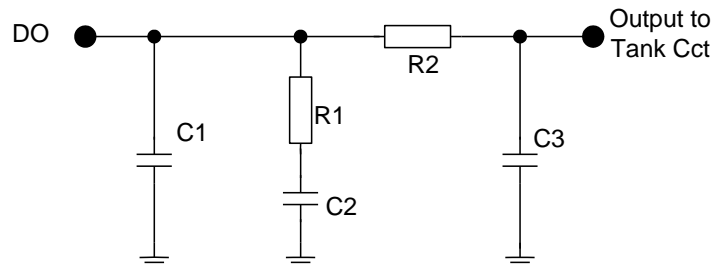
L1	51nH (Note 1)	CV1	SMV1705-079LF
C1	8.2pF (Note 2)	CV2	SMV1705-079LF
C2	27pF	R1	10k $\Omega$
C3	27pF	R2	10k $\Omega$

Note 1: Tolerance of 2% or better recommended

Note 2: Tolerance of 5% or better recommended

**Table 5 Internal VCO Amplifier Tank Circuit for 180MHz Operation**

Alternative diodes may be used for CV1,CV2, for example the Toshiba 1SV305 (for which no other value changes should be necessary). For increased tuning range the Skyworks SMV1249-079LF can be used: in this case changing the tank circuit values is recommended. For operation at 180MHz, make  $L1 = 56\text{nH}$  and  $C1=6.8\text{pF}$ , then  $C2$  and  $C3$  can be adjusted to give the desired tuning range: with  $C2, C3 = 27\text{pF}$  the VCO gain ( $K_v$ ) = 15 MHz/V and with  $C2, C3 = 12\text{pF}$ ,  $K_v = 8\text{MHz/V}$ . For  $C2,C3 = 12\text{pF}$ , the value of  $C1$  should be changed to  $8.2\text{pF}$ , to give a control voltage closer to the centre of the tuning range.



**Figure 7 Example External Components – PLL Loop Filter**

C1	150nF	R1	1.5k $\Omega$
C2	1 $\mu$ F	R2	2.4k $\Omega$
C3	15nF		

**Table 6 3<sup>rd</sup> Order Loop Filter Circuit for 180MHz Operation**

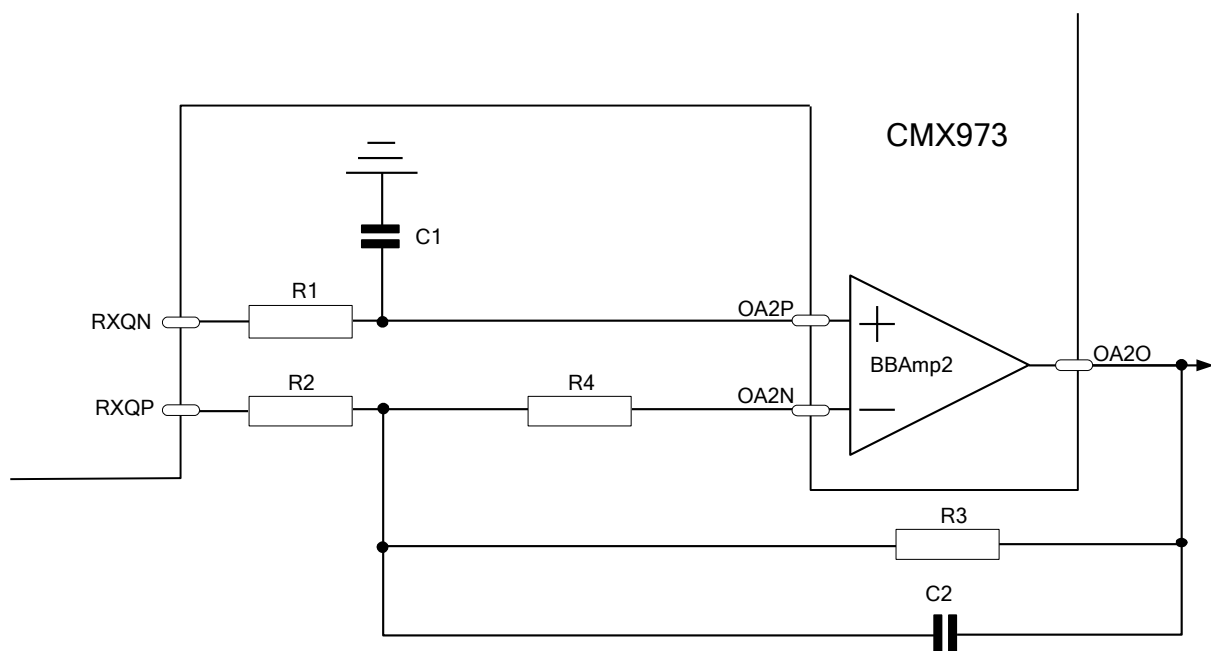
## 4.6 Differential Amplifiers

The CMX973 provides two uncommitted differential amplifiers which may be used for a range of purposes. Two possible configurations are shown in the following sections, however other uses include buffering or level shifting of the modulator I/Q signals.

### 4.6.1 I/Q Output Amplifiers

The uncommitted differential amplifiers may be used to convert the differential I/Q output signals to a single-ended output. A typical configuration of the amplifier on the Q channel (the I channel is identical) is shown in Figure 8. This circuit has a linear gain of 1.5. Although the circuit is not optimum for rejection of common mode signals, in practice performance is generally still satisfactory if R4 is omitted (i.e. replaced with a 0 Ohm link). Users should note that the gain and bandwidth of this stage can be adjusted by altering the component values and should be configured to suit a particular application.

C1 and C2 may be fitted to provide filtering if required.



**Figure 8 Example External Components – Receive I/Q Output**

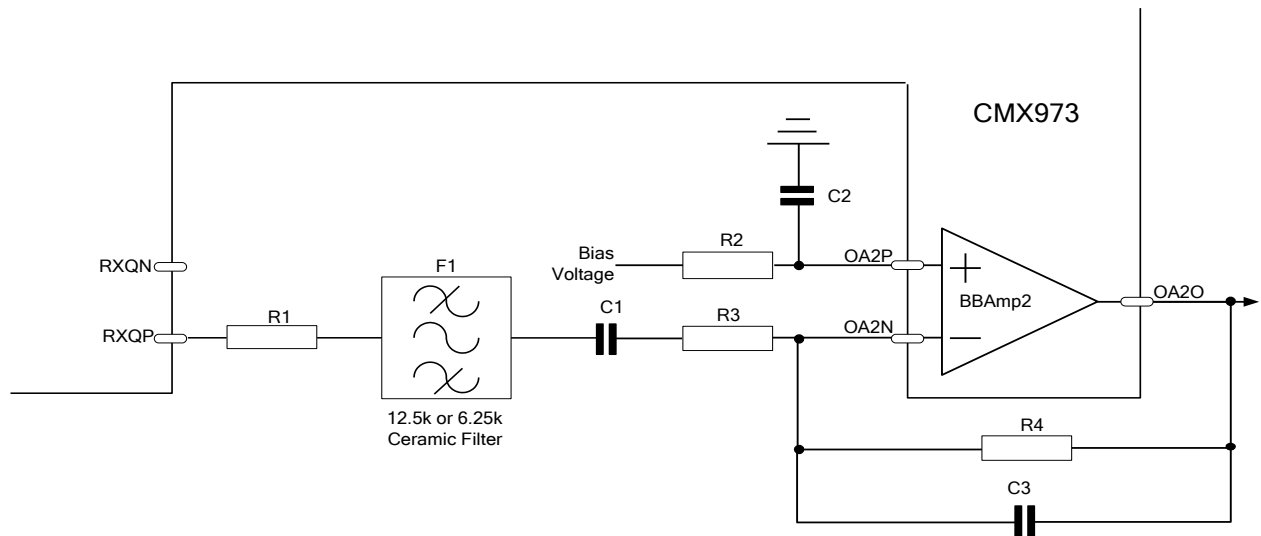
C1	NF	R2	10kΩ
C2	NF	R3	10kΩ
R1	10kΩ	R4	5kΩ Note 1

Note 1: The value of R4 should be calculated from the value of the other resistors using the calculation  $R4 = R1 - ((R2 \cdot R3) / (R2 + R3))$ .

**Table 7 Rx I/Q Differential to Single-ended Amplifier Components**

#### 4.6.2 Low IF Output

The quadrature demodulator output bandwidth is at least 5MHz, (see section 8.1.3.4), so the output of each quadrature demodulator mixer can be configured to mix down to a low IF and use one of the differential amplifiers to provide gain. A possible configuration for the Q channel is shown in Figure 9.



**Figure 9 Example External Components – Receive Low IF Output**

C1	100nF	R1	1.5kΩ
C2	47nF	R2	1.5kΩ
C3	33pF	R3	1.5kΩ
F1	CFWL455KEFA-B0	R4	4.7kΩ

**Table 8 Rx Low IF (455kHz) Components**

The components above specify, as an example, a particular ceramic filter (F1) that would typically be used in a 25kHz channel application in a system with an IF frequency of 455kHz. The other component values specified (e.g. R1, R3) are determined by the input/output impedance of the filter used. The filter and other components can be easily changed to allow for other bandwidths and IF frequencies.

A different external IF filter, e.g. of different bandwidth, could similarly be connected to the I channel output to support a second modulation bandwidth mode, e.g. to receive a 6.25kHz channel signal. The channel to be used is selectable via the Rx Mode register (\$1D), section 6.4.1, the unused channel being powered-down.

## 5 General Description

The CMX973 is an RF integrated circuit providing a quadrature modulator, demodulator, integer-N synthesiser and an IF VCO. Additional features include gain control and uncommitted differential amplifiers. A detailed block diagram for the IC is shown in section 2. The device can support a wide range of modulation formats and standards. The following sections describe the functionality of the CMX973.

### 5.1 Quadrature Modulator

The quadrature modulator provides translation from baseband I/Q signals to a modulated RF signal. The wideband inputs can be driven in a differential or single-ended configuration. In the case of single-ended operation a reference voltage equal to the nominal dc level of the modulation must be supplied on the unused input pin.

#### 5.1.1 Local Oscillator (LO)

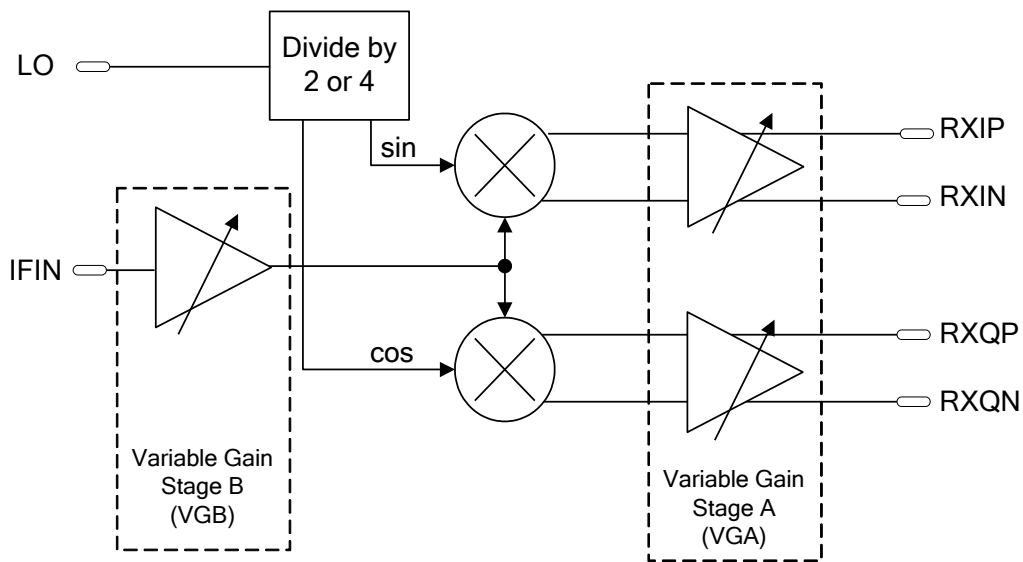
The modulator requires a Local Oscillator signal applied at twice or four times the desired output frequency, see section 5.4 for further details of LO configurations supported by the CMX973.

#### 5.1.2 DC Offsets and Carrier Leakage

The modulator inputs (TXIN/TXIP and TXQN/TXQP) are differential and require a common dc level or common mode voltage. Differences in the bias voltages on the pins will result in an increased level of carrier present at the output. Care should be taken to minimise offsets, thereby minimising carrier leakage.

### 5.2 Quadrature Demodulator

The quadrature demodulator is designed for IF/RF operation, having very low power consumption. Input frequencies in the range 20MHz to 300MHz are allowed. The demodulator system has two gain-controlled stages, one before and one after the I/Q down-converters, as shown in Figure 10. The two gain control elements can be independently controlled (see section 6.3.1). This adjustability allows users to optimise characteristics depending on their system requirements. Minimum noise figure can be maintained by decreasing gain in VGA with VGB at maximum gain. Intermodulation performance can be optimised by decreasing gain in VGA or VGB. A lower gain in VGA will tend to reduce dc offsets in the output I/Q signal. For further information on the effects of control of VGA and VGB see section 7.4.



**Figure 10 Demodulator Gain Control**

The output of the quadrature demodulator is provided as a differential signal (pins RXIP, RXIN, RXQP and RXQN). The bandwidth of the I/Q signals depends on the OUTDRV bit (b7, \$1C, Rx Control Register, see section 6.3.1). The intermodulation performance of the CMX973 also depends on the OUTDRV bit, see section 7.2 for further details.

The CMX973 provides for an optimisation of receiver intermodulation using the “IMD” bits in the VCO control register, further details can be found in section 7.2.

### 5.2.1 I/Q Amplitude and Phase Correction

The LO path includes a correction circuit for the quadrature demodulator, which may be enabled or disabled using the COR bit (b6 in the Rx Control Register \$1C), see section 6.3.1. This will improve the I/Q balance of the demodulator particularly when using the local oscillator divide by two (LO/2) mode; enabling this mode (COR='1') will give a small increase in current consumption of typically 0.5mA. The improvement is most noticeable with higher frequency signals, e.g. circa 200 - 300MHz; at 45MHz the improvement is negligible.

Condition	250MHz		45MHz	
	RXIP/RXQP	RXIN/RXQN	RXIP/RXQP	RXIN/RXQN
\$1C, b6 = '0'	92.0°	92.0°	90.1°	90.2°
\$1C, b6 = '1'	89.8°	89.8°	89.9°	89.9°

**Table 9 Typical Phase Balance, LO/2 Mode**

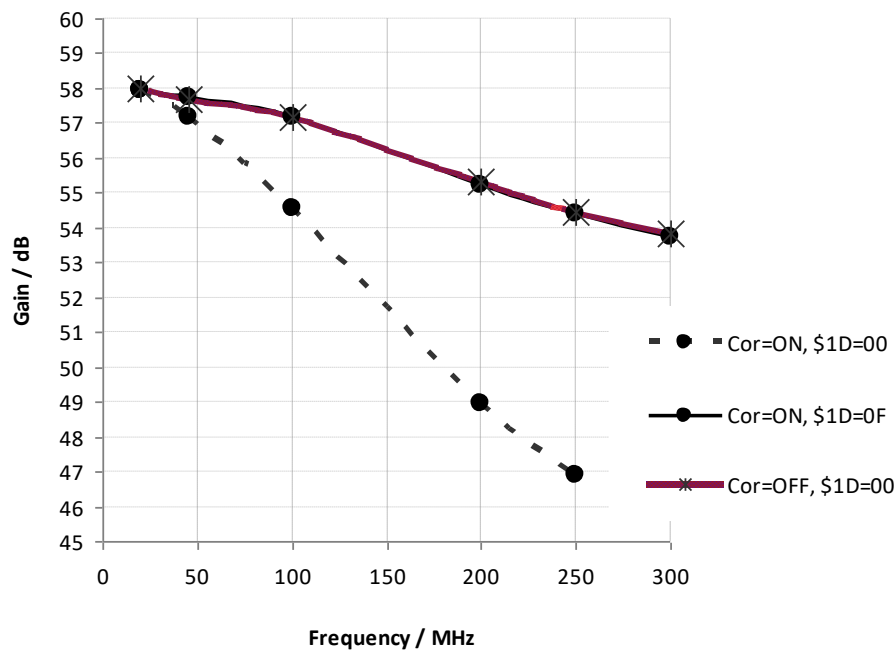
At 250MHz I/Q amplitude balance is typically 0.12dB with COR = '0' and 0.04dB with COR = '1'. Enabling the correction circuit also reduces the I/Q path gain, particularly at higher frequencies. This can be compensated by setting the FREQ bits (b3-0 in the Rx Mode register \$1D) to '1111', instead of the default value of '0000'. I/Q path gain is restored at the expense of a slight degradation in I/Q phase balance of  $\approx 0.5^\circ$ . For many applications, the '1111' setting will be adequate.

At all frequencies, phase correction accuracy is improved by using a lower setting of the FREQ bits (b3-0 in the Rx Mode register \$1D). However, care should be taken to avoid significant gain degradation, which

occurs if a setting near '0000' is chosen for a high frequency. Table 10 is a guide for the appropriate setting of the FREQ bits, so as to obtain the best phase balance (typically better than  $0.06^\circ$ ) with only a small gain reduction (typically less than 0.6dB). Where frequency ranges overlap, either setting of the FREQ bits can be used.

Bit	b3	b2	b1	b0	Frequency
	0	1	0	0	20MHz to 40MHz
	1	0	0	0	40MHz to 80MHz
	1	1	0	0	80MHz to 200MHz
	1	1	0	1	200MHz to 240MHz
	1	1	1	0	240MHz to 300MHz

**Table 10 Recommended FREQ bit Settings in the Rx Mode Register**



**Figure 11 Frequency Response, showing effect of COR bit (\$1C, b6) and FREQ bits(\$1D, b3-b0)**

Condition	Typical I/Q Phase Balance
COR = '0' \$1D = 0x00	87.95°
COR = '1' \$1D = 0x00	90.06°
COR = '1' \$1D = 0x0F	90.49°

**Table 11 Effect of FREQ bits (\$1D, b3-b0) on I/Q Phase Balance at 250MHz**

Condition	Typical I/Q Phase Balance
COR = '0' \$1D = 0x00, +20°C	87.3°
COR = '1' \$1D = 0x0F, -20°C	90.6°
COR = '1' \$1D = 0x0F, +20°C	90.6°
COR = '1' \$1D = 0x0F, +55°C	90.5°

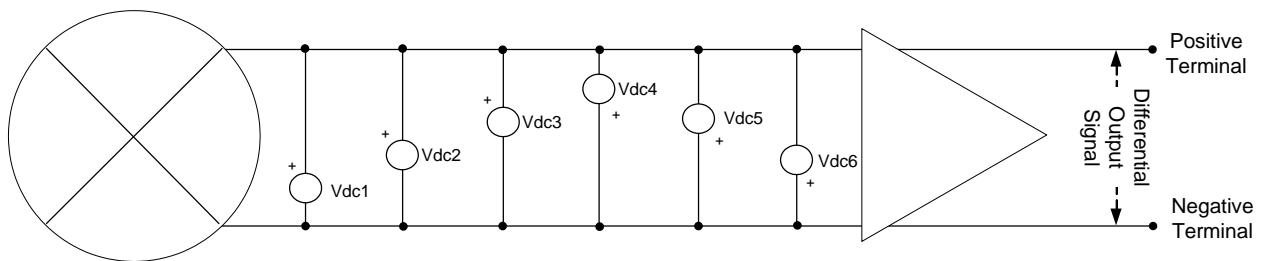
**Table 12 Effect of FREQ bits (\$1D, b3-b0) on I/Q Phase Balance at 300MHz with Temperature**



### 5.2.2 DC Offset Correction

Digitally-controlled dc offset correction is provided which is capable of reducing the offset to 60mV or less for errors of up to +/-420mV. This represents a reduction in dynamic range of about 0.3dB for a typical ADC input signal range (2Vp-p) and is therefore negligible. The required correction must be measured externally as such measurements are application specific. The correction is applied close to the start of the I/Q baseband chain and therefore maximises dynamic range in the analogue sections.

The correction is applied in a differential manner so positive and negative corrections are possible, see Figure 12. This allows the dc to be corrected to the nominal dc bias level. The voltage sources are scaled in a binary fashion so multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels.



**Figure 12 Simplified Schematic DC Offset Correction Circuit**

Source	Voltage Correction at Output for Maximum Gain in Baseband Amplifiers	Correction Polarity
Vdc1	60mV	Positive terminal increase, Negative terminal decrease
Vdc2	120mV	Positive terminal increase, Negative terminal decrease
Vdc3	180mV	Positive terminal increase, Negative terminal decrease
Vdc4	60mV	Negative terminal increase, Positive terminal decrease
Vdc5	120mV	Negative terminal increase, Positive terminal decrease
Vdc6	180mV	Negative terminal increase, Positive terminal decrease

**Table 13 DC Offset Correction Adjustments**

### 5.3 Differential Amplifiers

A pair of differential amplifiers are provided which may be used to implement filtering or buffering. These uncommitted amplifiers may be used to implement Sallen-Key or Multiple Feedback (MFB) style filters, buffering or configured as needed.

The amplifiers are low power and are enabled using the General Control Register (see section 6.2.1). It is also possible for the amplifiers to be enabled with individual I and Q paths, see section 6.4.1.

## 5.4 Local Oscillator (LO)

The device allows for a flexible choice of routing for the LO inputs to both the modulator and demodulator, to suit a variety of applications.

The options available, controlled by the General Control Register (see section 6.2.1), are as follows:

- The demodulator LO may be derived from the external input (RXLO) or from the internal VCO/PLL.
- The modulator LO may be derived from the external input (TXLO) or from the internal VCO/PLL, although care would be needed to ensure that the phase noise from the internal VCO is adequate for this use and that sufficient isolation from the PA output signal is achieved to prevent VCO-pulling degrading the signal.
- The selected LO source is fed back to an integer-N PLL circuit which may be used to control the on-chip (or an external) VCO from its Charge Pump output (DO).

The most common configuration would be to use the on-chip VCO and PLL connected to the demodulator for the Intermediate Frequency (IF) of a superheterodyne receiver with the TXLO sourced externally for the modulator.

Four bits in the General Control Register and one bit in the Tx Control Register are used to define the allowed states (X = don't care). The permitted combinations are shown in Table 14.

LOS S1E, b7	RXEN \$1B, b1	TXEN \$1B, b0	VCOEN \$1B, b3	PLEN \$1B, b2	Function
0	0	0	0	0	All features disabled for low power
0	0	1	0	0	Use of modulator with signal from TXLO pin
0	0	1	0	1	Use of modulator with external VCO connected to TXLO pin using on-chip PLL
1	0	1	1	1	Use of modulator with LO supplied by on-chip VCO and PLL
X	1	0	0	0	Use of demodulator with signal from RXLO pin
X	1	0	0	1	Use of demodulator with external VCO connected to RXLO using on-chip PLL
X	1	0	1	1	Use of demodulator with LO supplied by on-chip VCO and PLL
0	1	1	0	0	Modulator uses signal from TXLO pin; demodulator uses signal from RXLO pin
0	1	1	1	1	Modulator uses signal from TXLO pin; demodulator uses signal from on chip VCO and PLL
<b>Note:</b> Other combinations of control bit are illegal states and should not be used.					

**Table 14 LO Connections**

### 5.4.1 Demodulator LO Input

The RXLO pin is a single-ended input for the demodulator LO signal. Internal ac coupling is provided so an external dc blocking capacitor is not required. Note that the LO should be at twice or four times the desired input frequency.

### 5.4.2 Modulator LO Input

The TXLO pin is a single-ended input for the modulator LO signal, internal ac coupling is provided so an external dc blocking capacitor is not required. Note that the LO should be at twice or four times the desired RF output frequency.

### 5.4.3 VCO and PLL

The internal VCO may be connected to the internal PLL and the demodulator or modulator. If required, an external VCO can be connected to the PLL using either of the LO inputs, in this case the on-chip VCO must be disabled using bit 3 in the General Control Register (see section 6.2.1 and Table 14).

#### 5.4.3.1 PLL

The PLL functions are shown in Figure 13. The output frequency of the PLL is set by the following calculation:

$$f_{\text{out}} = f_{\text{ref}} \times (M / R)$$

where

$f_{\text{out}}$  = The desired output frequency in MHz

$f_{\text{ref}}$  = The reference frequency supplied to the PLL on pin REFIN in MHz

M = Divider value programmed in the M divider register (see section 6.7.1)

R = Divider value programmed in the R divider register (see section 6.8.1)

also note that  $f_{\text{comparison}} = f_{\text{ref}} / R$

The PLL only supports VCOs with a positive tuning slope, i.e. a high tuning voltage from DO results in a higher oscillation frequency from the VCO.

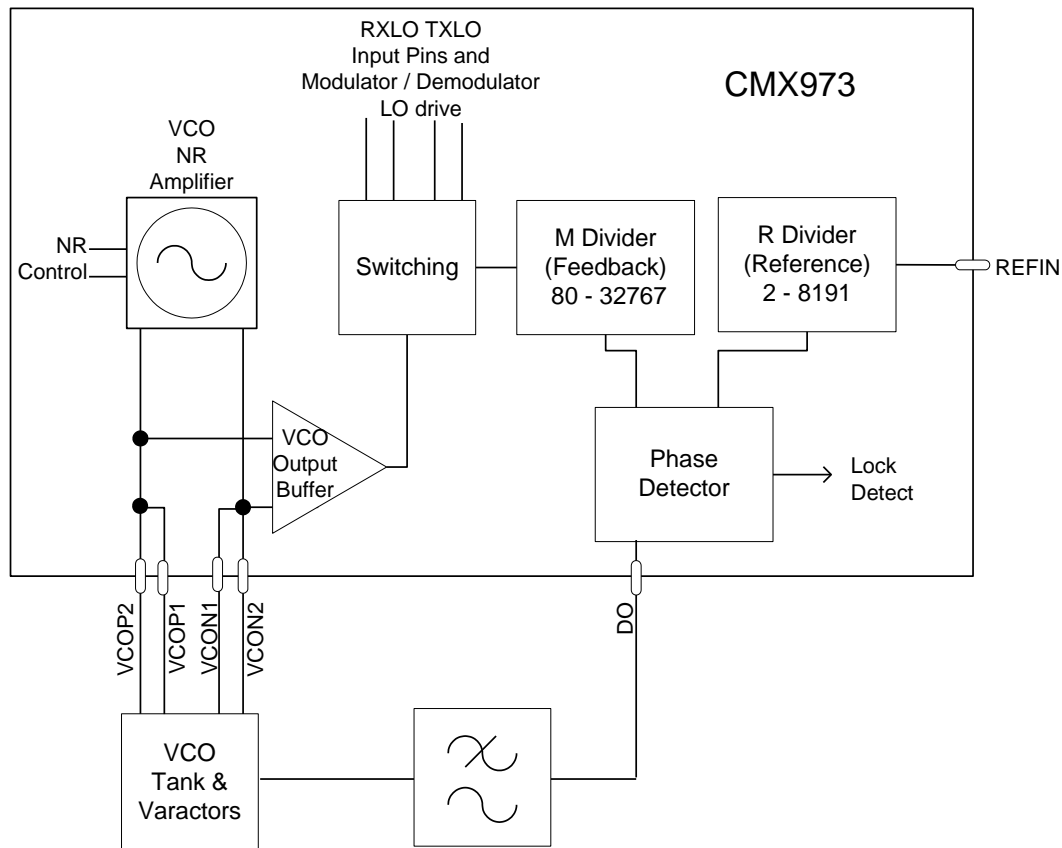


Figure 13 PLL Architecture

The PLL block has to be enabled from the General Control Register \$1B, b2 (section 6.2.1) and the PLL R Divider Register \$2C, b7 (section 6.8.1), i.e. an AND function is performed on these two bits.

General Control Register \$1B, b2	PLL R Divider Register \$2C, b7	PLL Enable
0	0	No
0	1	No
1	0	No
1	1	Yes

**Table 15 PLL Control**

The PLL provides a lock detect function which can be read via C-BUS register \$DC bit 6, see section 6.7.2. Register \$2C provides the facility for the PLL charge pump to be placed in a high-impedance state, this mode can be used, for example, to allow pre-steering of the VCO.

When using the CMX973 PLL, spurious products (spurs) in the receiver I/Q output may be observed. The level of the spurs varies and is typically different in I and Q channels. The frequency of the spurs is linked to the PLL M divider value, thus the comparison frequency and which of the divider modes (divide-by-2 or -4) is selected for the receiver LO circuits. Operation in divide-by-2 mode is most predictable: all even division ratios are problem free and all odd division ratios will give a spurious product at:

$$f_{\text{spur}} = f_{\text{lo}} / (M * 2)$$

In divide-by-4 mode odd divisions will produce a spur although at some low frequencies (e.g circa 100MHz) spur levels are much lower. At circa 300 MHz and above, even divisions are also problematic (in divide-by-4 mode).

It is recommended that for safe operation of the CMX973 PLL, receiver LO divide-by-2 with even division ratios, should be used.

Using the CMX973 PLL for Tx operation is not normally recommended (section 5.4) however if it is used spurious can also be observed in the output. In this case the spurs are at small offsets from the wanted signal – the offset is linked to the PLL comparison frequency. The level of these spurs is typically relatively low and therefore less problematic than in the receiver.

#### 5.4.3.2 VCO

The CMX973 VCO is a reflection oscillator that requires an external resonator circuit (see section 4.5) with the negative resistance (NR) generator on the device. The VCO Control Register (\$2F, section 6.9.1) provides a control of the magnitude of the negative transconductance for optimum phase noise performance. The NR minimum mode should be used with the low Q external tank circuit and NR maximum with the higher Q circuits. For further information see section 7.8.

## 6 C-BUS Interface and Register Description

The C-BUS serial interface supports the transfer of control and status information between the CMX973's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or one data bytes that are written into the corresponding CMX973 register, as illustrated in Figure 14.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX973 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common  $\mu$ C/DSP serial interfaces and may also be easily implemented with general-purpose I/O pins controlled by a simple software routine. Section 8.1.3.6 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of read or write type is fixed for a given C-BUS register address, thus it is not possible to read from and write to the same C-BUS register address.

In order to provide ease of addressing when using this device with other CML RF devices, the C-BUS addresses below are arranged so as not to overlap those used on the existing CML RF Devices. Thus, a common chip select (CSN) signal can be used, as well as common CDATA, RDATA and SCLK signals. Also note that the General Reset (\$1A) command on the CMX973 differs from other CML devices (such as CMX991/CMX992/CMX993/CMX998), which use \$01 or \$10 for this function.

The following C-BUS register addresses are used:

### *Write Only register:*

General Reset Register (Address only, no data)	Address \$1A
General Control Register, 8-bit write only	Address \$1B
Rx Control Register, 8-bit write only	Address \$1C
Rx Mode Register, 8-bit write only	Address \$1D
Tx Control Register, 8-bit write only	Address \$1E
Rx Offset Correction Register, 8-bit write only	Address \$1F
IF PLL M Divider Register, 8-bit write only	Address \$2A-\$2C
IF PLL R Divider Register, 8-bit write only	Address \$2D-\$2E
VCO Control Register, 8-bit write only	Address \$2F

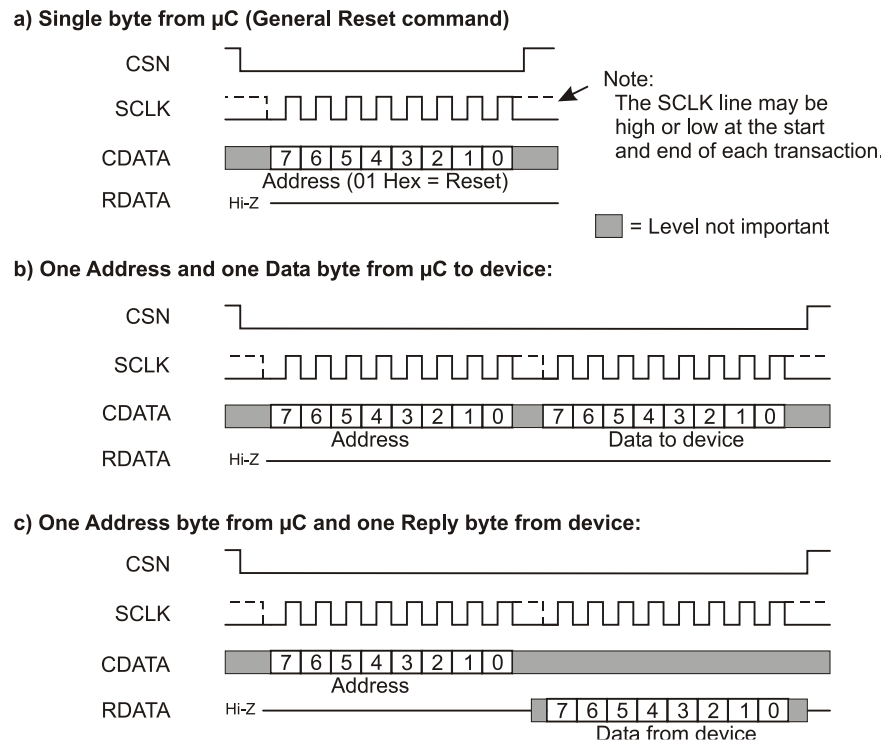
### *Read Only register:*

General Control Register, 8-bit read only	Address \$EB
Rx Control Register, 8-bit read only	Address \$EC
Rx Mode Register, 8-bit read only	Address \$ED
Tx Control Register, 8-bit read only	Address \$EE
Rx Offset Correction Register, 8-bit read only	Address \$EF
IF PLL M Divider Register, 8-bit read only	Address \$DA-\$DC
IF PLL R Divider Register, 8-bit read only	Address \$DD-\$DE
VCO Control Register, 8-bit read only	Address \$DF

### Notes:

- All registers will retain data if VDD pin is held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices VDD must be maintained in its normal operating range otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK, RDATA and CDATA pins, preventing correct programming of other devices.

Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.



**Figure 14 C-BUS Transactions**

## 6.1 General Reset Command

### 6.1.1 General Reset Command - \$1A: no data

This command resets the device and clears all bits of all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the VDD pin, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command.

## 6.2 General Control Register

### 6.2.1 General Control Register - \$1B: 8-bit write

This register controls general features such as powersave.

All bits of this register are cleared to '0' during a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	RXDIV	TXDIV	DIFAMP	ENBIAS	VCOEN	PLLEN	RXEN	TXEN

#### General Control Register b7

Writing b7 = '1' the receiver LO is divided by 2; writing b7 = '0' the LO is divided by 4.

#### General Control Register b6

Writing b6 = '1' the transmitter LO is divided by 2; writing b6 = '0' the LO is divided by 4.

#### General Control Register b5 - b0

These bits control power up/power down of the various blocks of the IC.  
In all cases '1' = power up, '0' = power down.

b5	Enable differential amplifiers (see also section 6.4.1)
b4	Enable bias
b3	Enable VCO (this bit also disables the RXLO and TXLO inputs)
b2	PLL enable (see Table 15 and section 6.7.1) Note: To enable the PLL b7 of the PLL M-Divider Register (\$2C) also needs to be set.
b1	Enable quadrature demodulator
b0	Enable quadrature modulator

**Note:** b0-b3 also controls local oscillator signal routing, see section 5.4 and Table 14.

### 6.2.2 General Control Register - \$EB: 8-bit read

This register reads the value in register \$1B, see section 6.2.1 for details of bit functions.

## 6.3 Rx Control Register

### 6.3.1 Rx Control Register - \$1C: 8-bit write

This register controls operational modes of the receiver such as gain setting.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	OUTDRV	COR	0	VGB2	VGB1	VGB0	VGA1	VGA0

#### Rx Control Register b7

Writing b7 = '1' the output drive capability of the demodulator I/Q output is increased, this mode allows the CMX973 to support wider bandwidth modulation and/or driver lower impedance loads; b7 = '0' is the default condition with best power efficiency.

#### **Rx Control Register b6**

Writing b6 = '1' enables the correction circuit in the quadrature demodulator. This will improve the I/Q phase balance of the demodulator particularly in LO/2 mode; enabling this mode increases the current consumption slightly. For further information see section 5.2.1.

With b6 = '0' this enhanced mode is disabled for optimum current consumption.

#### **Rx Control Register b5**

Reserved, must be cleared to '0' for correct operation.

#### **Rx Control Register b4 – b2**

Variable Gain (VGB) Control; these bits control the gain of the IF/RF amplifier reducing the gain from the maximum in 6dB steps.

Bit	b4	B3	b2	
	1	1	1	Reserved do not use
	1	1	0	Reserved do not use
	1	0	1	VG = -30dB
	1	0	0	VG = -24dB
	0	1	1	VG = -18dB
	0	1	0	VG = -12dB
	0	0	1	VG = -6dB
	0	0	0	VG = 0dB (maximum gain)

#### **Rx Control Register b1 – b0**

Variable Gain (VGA) control; this bits control the gain of the post-I/Q mixer baseband amplifiers reducing the gain from the maximum in 6dB steps.

Bit	b1	B0	
	1	1	VG = -18dB
	1	0	VG = -12dB
	0	1	VG = -6dB
	0	0	VG = 0dB (maximum gain)

### **6.3.2 Rx Control Register - \$EC: 8-bit read**

This read-only register mirrors the value in register \$1C; see section 6.3.1 for details of bit functions.

## **6.4 Rx Mode Register**

### **6.4.1 Rx Mode Register - \$1D: 8-bit write**

This register controls operational modes of the receiver.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
------	---	---	---	---	---	---	---	---



M1	M0	DIFAMPI	DIFAMPQ	FREQ3	FREQ2	FREQ1	FREQ0
----	----	---------	---------	-------	-------	-------	-------

### **Rx Mode Register b7 – b6**

Bit	b7	B6	
	0	0	I and Q channels enabled
	0	1	Only I channel enabled
	1	0	Only Q channel enabled
	1	1	Reserved do not use

### **Rx Mode Register b5 - b4**

With b4, b5 = '0' both differential amplifiers are enabled/disabled by the DIFAMP bit in the General Control Register (section 6.2.1). With b4 = '1' the Q channel differential amplifier control by the DIFAMP bit will be inverted. With b5 = '1' the I channel differential amplifier control by the DIFAMP bit will be inverted. This aids the applications where the amplifiers are associated with either the I or Q channels.

Bit	\$1B, b5	b5	b4	
	0	0	0	Diff Amp 1 = 'OFF'; Diff Amp 2 = 'OFF'
	0	0	1	Diff Amp 1 = 'OFF'; Diff Amp 2 = 'ON'
	0	1	0	Diff Amp 1 = 'ON'; Diff Amp 2 = 'OFF'
	0	1	1	Diff Amp 1 = 'ON'; Diff Amp 2 = 'ON'
	1	0	0	Diff Amp 1 = 'ON'; Diff Amp 2 = 'ON'
	1	0	1	Diff Amp 1 = 'ON'; Diff Amp 2 = 'OFF'
	1	1	0	Diff Amp 1 = 'OFF'; Diff Amp 2 = 'ON'
	1	1	1	Diff Amp 1 = 'OFF'; Diff Amp 2 = 'OFF'

### **Rx Mode Register b3 – b0**

These bits optimise the operation of the receiver quadrature demodulator mixers by adjusting the LO signal. The bits adjust LO amplitude, which has an impact on mixer gain, but the adjustment also has an effect on quadrature accuracy. See also section 5.2.1. Note that if \$1C b6 is set to 0, so that phase correction is not used, the setting of these FREQ bits has no effect.

A setting of '0000' represents the optimum value for phase accuracy.

## **6.4.2 Rx Mode Register - \$ED: 8-bit read**

This read-only register mirrors the value in register \$1D; see section 6.4.1 for details of bit functions.

## **6.5 Tx Control Register**

### **6.5.1 Tx Control Register - \$1E: 8-bit write**

This register controls transmitter features.  
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	LOS	0	0	0	F3	F2	F1	F0

**Tx Control Register b7**

This bit determines the source of the LO, see Table 14.

**Tx Control Register b6 – b4**

Reserved, clear to '0'.

**Tx Control Register b3 - b0**

These bits optimise the performance of the Transmitter LO path. The best intermodulation performance is achieved at the lowest control setting ('0000') and the best wideband noise can be achieved at the highest setting ('1111').

Bit:	b3	b2	b1	b0	
	0	0	0	0	best intermodulation
	0	0	0	1	intermediate value
	0	0	1	0	intermediate value
	0	0	1	1	intermediate value
	0	1	0	0	intermediate value
	0	1	0	1	intermediate value
	0	1	1	0	intermediate value
	0	1	1	1	intermediate value
	1	0	0	0	intermediate value
	1	0	0	1	intermediate value
	1	0	1	0	intermediate value
	1	0	1	1	intermediate value
	1	1	0	0	intermediate value
	1	1	0	1	intermediate value
	1	1	1	0	intermediate value
	1	1	1	1	best wideband noise

**6.5.2 Tx Control Register - \$EE: 8-bit read**

This read-only register mirrors the value in register \$1E; see section 6.5.1 for details of bit functions.

## 6.6 Rx Offset Register

### 6.6.1 Rx Offset Register - \$1F: 8-bit write

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	QDC3	QDC2	QDC1	QDC0	IDC3	IDC2	IDC1	IDC0

#### **Rx Offset Register b7 – b0**

I/Q DC offset correction, see section 5.2.2 for further details.

Bit	b3 b7	b2 b6	b1 b5	b0 b4	I Channel Q Channel
	1	1	1	1	-420mV
	1	1	1	0	-360mV
	1	1	0	1	-300mV
	1	1	0	0	-240mV
	1	0	1	1	-180mV
	1	0	1	0	-120mV
	1	0	0	1	-60mV
	1	0	0	0	No correction
	0	1	1	1	+420mV
	0	1	1	0	+360mV
	0	1	0	1	+300mV
	0	1	0	0	+240mV
	0	0	1	1	+180mV
	0	0	1	0	+120mV
	0	0	0	1	+60mV
	0	0	0	0	No correction

### 6.6.2 Rx Offset Register - \$EF: 8-bit read

This read-only register mirrors the value in register \$1F; see section 6.6.1 for details of bit functions.

## 6.7 PLL M Divider

### 6.7.1 PLL M Divider - \$2C - \$2A: 8-bit write

These registers set the M divider value for the PLL (Feedback divider). The PLL dividers are only updated when \$2C has been written, so this register should be written to last. Bits 7 and 5 also control the PLL and charge-pump blocks and these control bits are active as soon as \$2C is written. (Note: To enable the PLL, b2 of the General Control Register (\$1B) also needs to be set).

Bit:

\$2C								\$2B							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
E	LD_Synth	CP	0	0	0	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8

\$2A							
7	6	5	4	3	2	1	0
M7	M6	M5	M4	M3	M2	M1	M0

#### **M17:M0**

Phase Locked Loop M divider value.

#### **CP**

\$2C, b5 = '1' enables the charge pump, \$2C b5 = '0' puts the charge pump into high-impedance mode.

#### **LD\_Synth**

Only write '0' to b6 of \$2C (when read, this shows the PLL lock status, see section 6.7.2).

#### **E**

\$2C, b7 = '1' enables the PLL; b7 = '0' disables the PLL – in this mode an external local oscillator may be supplied to the CMX973, see also section 5.4.3 and Table 15. (Note: To enable the PLL b2 of the General Control Register (\$1B) also needs to be set).

#### **\$2C b4-b2**

Reserved, set to '0'.

### 6.7.2 PLL M Divider - \$DC - \$DA: 8-bit read

These registers read the respective values in registers \$2C, \$2B and \$2A (\$DC reads back \$2C and \$DB reads back \$2B etc.); see section 6.7.1 for details of bit functions.

**N.B. \$DC b6 indicates the Synthesiser lock detect status.**

## 6.8 PLL R Divider

### 6.8.1 PLL R Divider - \$2E - \$2D: 8-bit write

These registers set the R divider value for the PLL (Reference divider). The PLL dividers are only updated when \$2E has been written, so this register should be written to last.

Bit:	\$2E								\$2D							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

**R15:R0**

Phase Locked Loop R divider value.

**6.8.2 PLL R Divider - \$DE - \$DD: 8-bit read**

These registers read the respective values in registers \$2E and \$2D (\$DE reads back \$2E and \$DD reads back \$2D); see section 6.8.1 for details of bit functions.

**6.9 VCO Control Register****6.9.1 VCO Control Register - \$2F: 8-bit write**

This register optimises the operation of the VCO. Note the VCO is enabled when b3 = '1' in the General Control register (\$1B), as detailed in section 6.2.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	IMD5	IMD4	IMD3	IMD2	IMD1	IMD0	VCONR2	VCONR1

**VCO Control Register b7 – b2**

These bits allow the user to adjust the intermodulation performance of the Rx I/Q mixers. The default value is '0' for all the bits. Improved intermodulation can be achieved with a particular value in these bits. The recommended value for optimum performance is '111111'. This value does not vary between devices or with frequency. For further details see section 7.2.

**VCO Control Register b1 – b0**

VCO amplifier Negative Resistance (NR) control for optimum phase noise performance, see section 5.4.3.2.

Bit:	b2	b1	
	0	0	NR maximum (highest Q tank circuit)
	0	1	NR Intermediate value
	1	0	NR Intermediate value
	1	1	NR minimum (lowest Q tank circuit)

**6.9.2 VCO Control Register - \$DF: 8-bit read**

This register reads the value in register \$2F, see section 6.9.1 for details of bit functions.

## 7 Application Notes

### 7.1 Impedance Matching Information

#### 7.1.1 IF/RF Input Matching

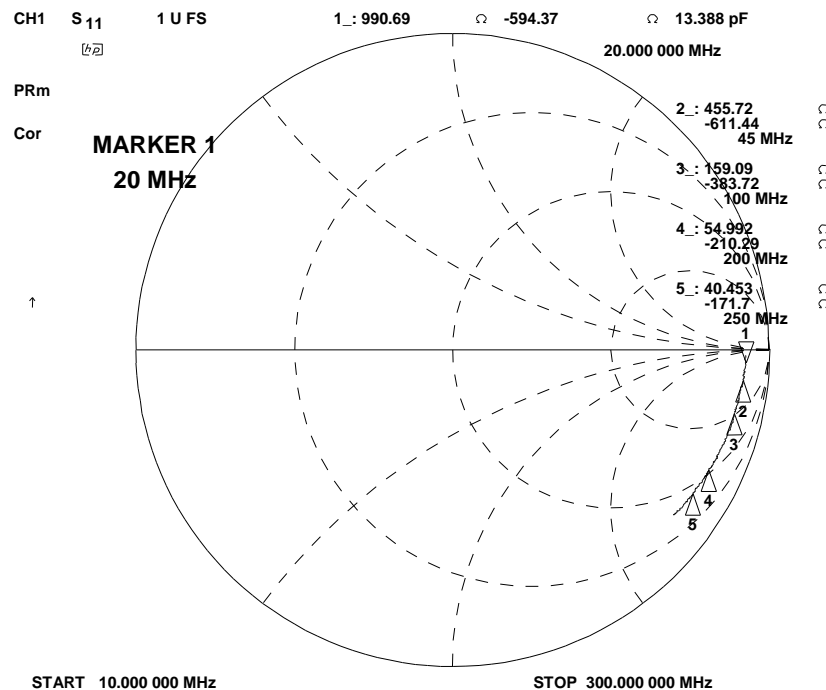


Figure 15 Quadrature Demodulator Input Impedance (10MHz to 300MHz)

Frequency (MHz)	Typical Impedance ( $\Omega$ -/+j $\Omega$ )	Parallel Equivalent Circuit (R//pF)
20	991 - j594	1.35kR // 3.5pF
45	456 - j611	1.28kR // 3.7pF
100	159 - j384	1.08kR // 3.5pF
200	55 - j210	860.5R // 3.5pF
250	41 - j172	768.4R // 3.5pF

Table 16 Quadrature Demodulator Input Impedances and Parallel Equivalent Circuit

The typical input impedance of the IFIN port is shown in Figure 15 and Table 16. The configuration of the IF input has a significant effect on the measured performance. This is demonstrated in Table 17, where the receiver is measured with a 50 Ohm source and three different input conditions. A matched network (e.g. as shown in section 4.3) provides the best noise figure and maximum gain, however intermodulation will be degraded in this condition due to the larger signal levels indicated by the extra gain. The 'straight in' condition means that the 50 Ohm signal source was connected directly at IFIN.

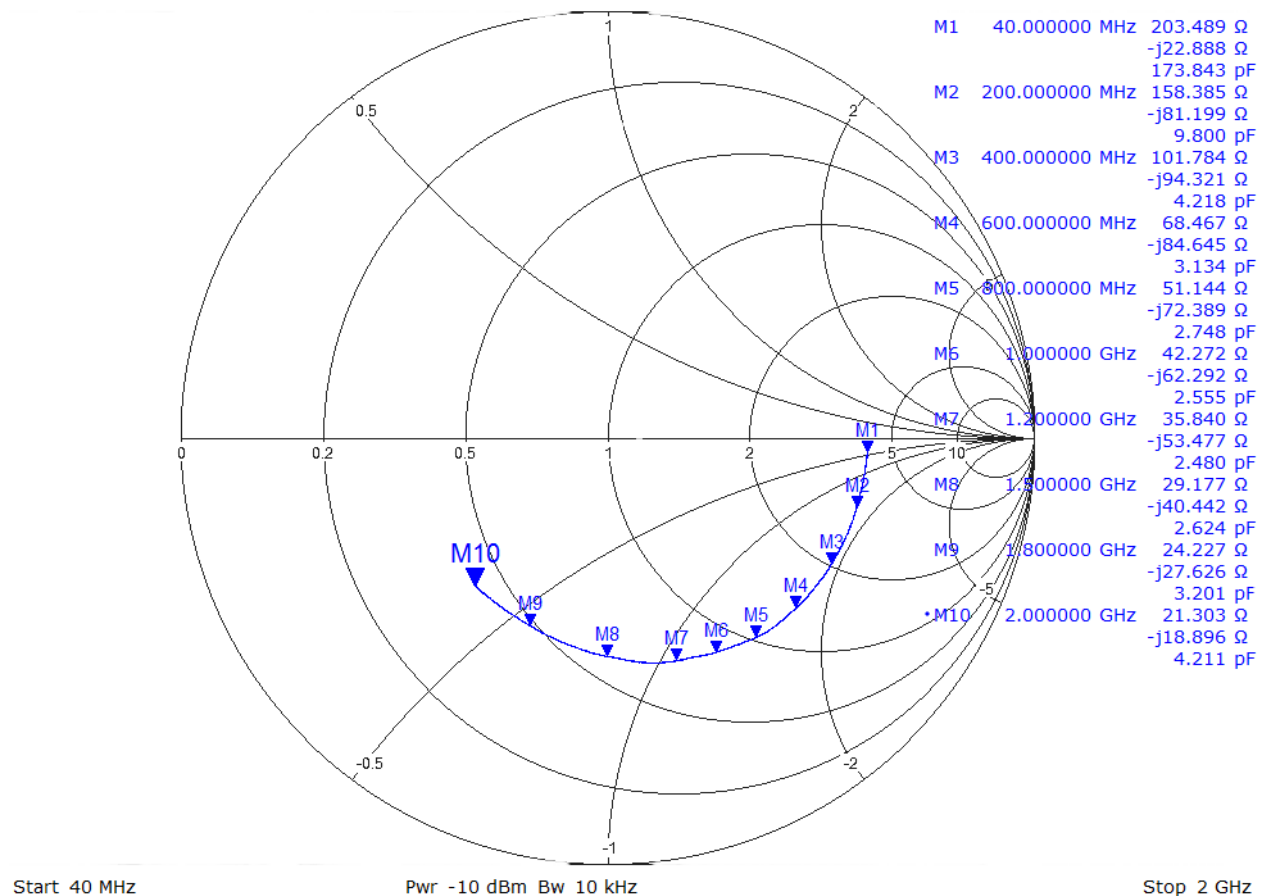
Input Condition	Noise Figure / dB	Gain / dB
50R shunt resistor	16.3	50.5
matched network	7.8	64
straight in	10	56

**Table 17 Typical Noise Figure and Gain of IF Amp, VGA and I/Q Mixer**

The gain in the 'straight in' case is based on direct conversion of the signal generator power to a voltage and calculating the gain based on the output voltage. The output signal is the differential signal at RXIN and RXIP (or RXQN and RXQP) so if the voltage is measured at a single pin the signal level must be doubled to get the appropriate differential signal level. Also it should be noted that making a simple conversion of the power in the 'straight in' case is erroneous as the voltage calculated will be a potential difference. As the circuit is unmatched an e.m.f. would be more appropriate (i.e. twice the potential difference value).

### 7.1.2 TXLO Input

The impedance to the transmitter LO input (TXLO pin) is shown in Figure 16.



**Figure 16 – TXLO Impedance**

## 7.2 Receiver Intermodulation and Output Drive Capability

The intermodulation performance of the receiver path may be optimised by use of the output drive bit (register \$1C b7, see section 6.3.1). Performance can be further optimised by setting the IMD bits in the VCO register (register \$2F b2 to b7) to '111111' = 63 decimal.

IMD bits setting (register \$2F b2 to b7) decimal value	\$1C, b7='0' 50kHz and 100kHz tones	\$1C, b7='1' 50kHz and 100kHz tones	\$1C, b7='0' 500kHz and 1MHz tones	\$1C, b7='1' 500kHz and 1MHz tones
0	-23 dBm	-12 dBm	-24 dBm	-12 dBm
63	-19 dBm	-11 dBm	-24 dBm	-11 dBm

**Table 18 Typical Third Order Intercept Performance of Receiver at 45MHz (straight-in case)**



### 7.3 Receiver Variation with Temperature

The CMX973 demodulator exhibits excellent temperature stability. Typical variation of the receive path gain is shown in Figure 17. The I/Q gain/phase balance (see Table 11), dc level and attenuator steps also show only small variations with temperature.

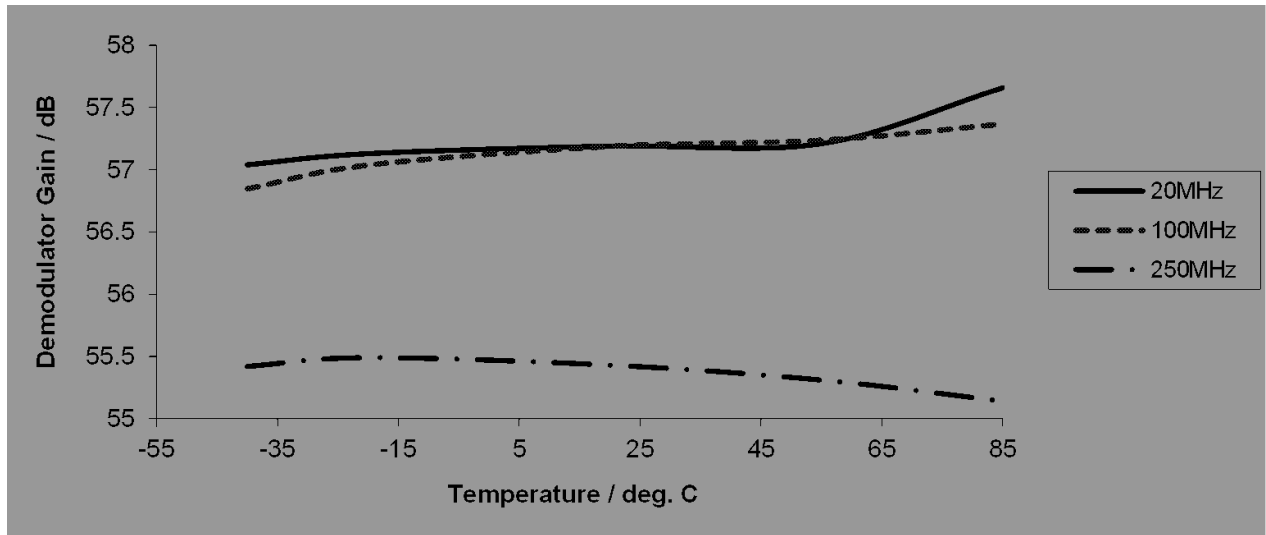


Figure 17 Demodulator Gain Variation With Temperature

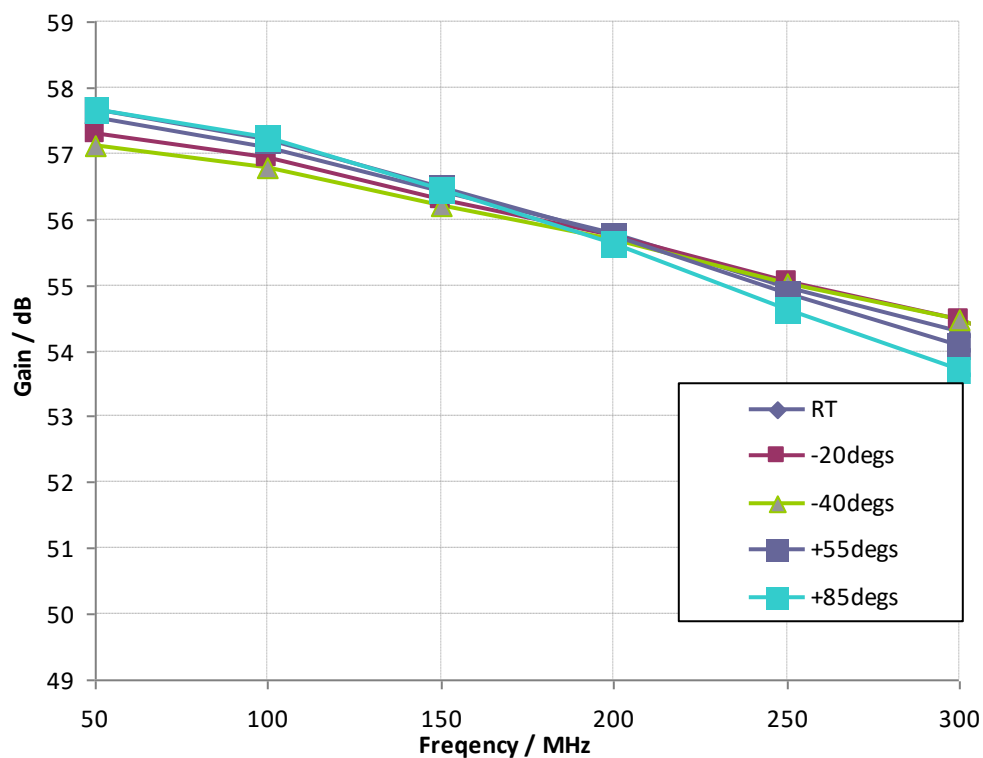


Figure 18 Variation in Gain with Temperature (COR = '0' \$1D = 0x00)

## 7.4 Effect of Gain Control on Receiver Performance

The CMX973 has two independent gain control elements: VGA is gain control applied in the I/Q sections and VGB is gain control in the RF/IF sections. Further details can be found in section 5.2. The gain can be controlled in 6dB steps via the Rx Control Register (see section 6.3).

The control of gain using VGA and VGB has an impact on the performance of the CMX973 demodulator section. The variation in noise figure (NF) is straightforward, with the RF/IF gain control (VGB) having a direct impact on NF but, due to the gain before the I/Q section, VGA has little impact on NF (see Figure 19). The variation of intermodulation (IMD) is more complex, as shown in Figure 20, where performance is characterised by 'Input Third Order Intercept Point' (IIP3). At maximum gain IIP3 is at a minimum and as would be expected, the IIP3 increases as the RF/IF gain is reduced (VGB). The improvement plateaus beyond the -18dB gain setting as the input stages limit performance at this level. Reduction in gain with VGA (I/Q gain control) also has a positive effect on IIP3. This is perhaps less intuitive but indicates that the intermodulation performance of the CMX973 demodulator chain is dominated by the output stages rather than RF/IF or mixer stages. Thus -6dB or even -12dB VGA gain control settings can be used to achieve improved IMD performance for negligible change in noise figure (Figure 19), as long as the reduction in gain can be tolerated.

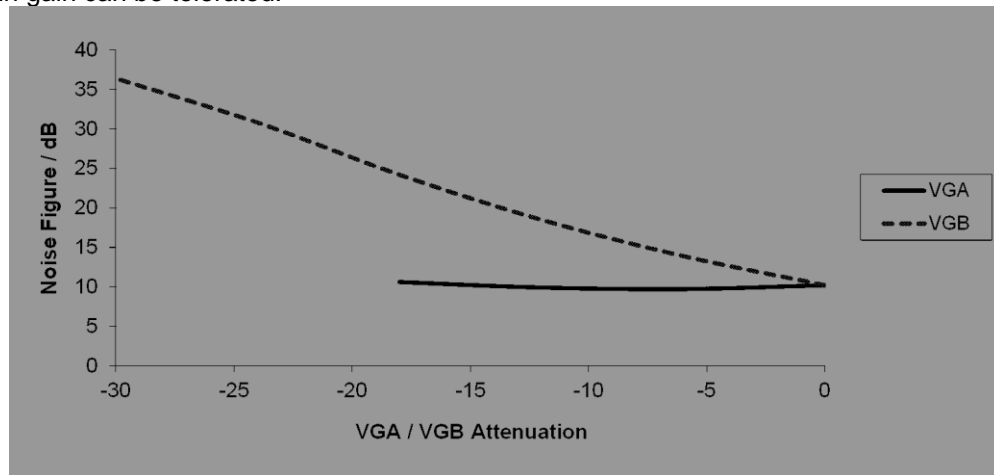


Figure 19 Variation in CMX973 Demodulator Noise Figure with VGA/VGB Control

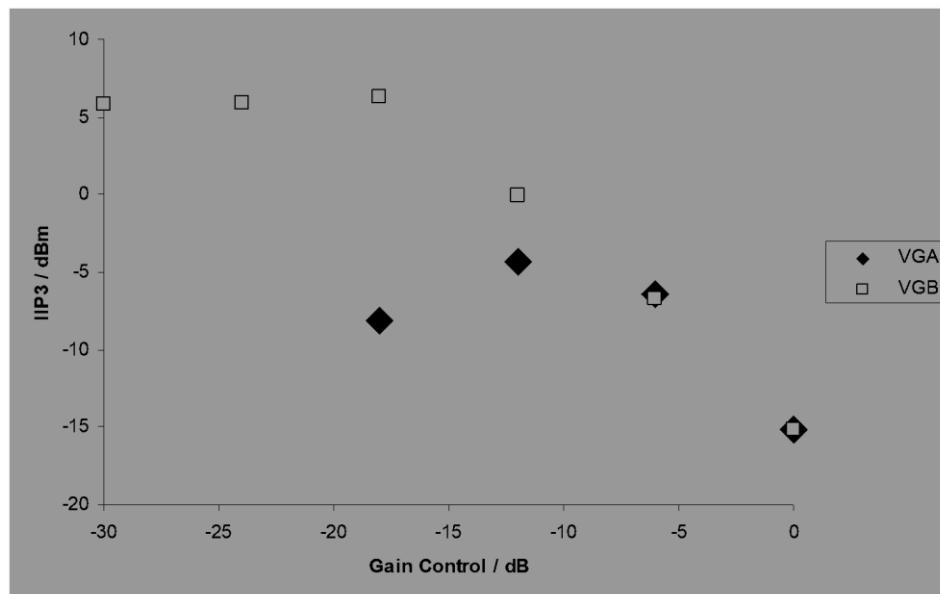


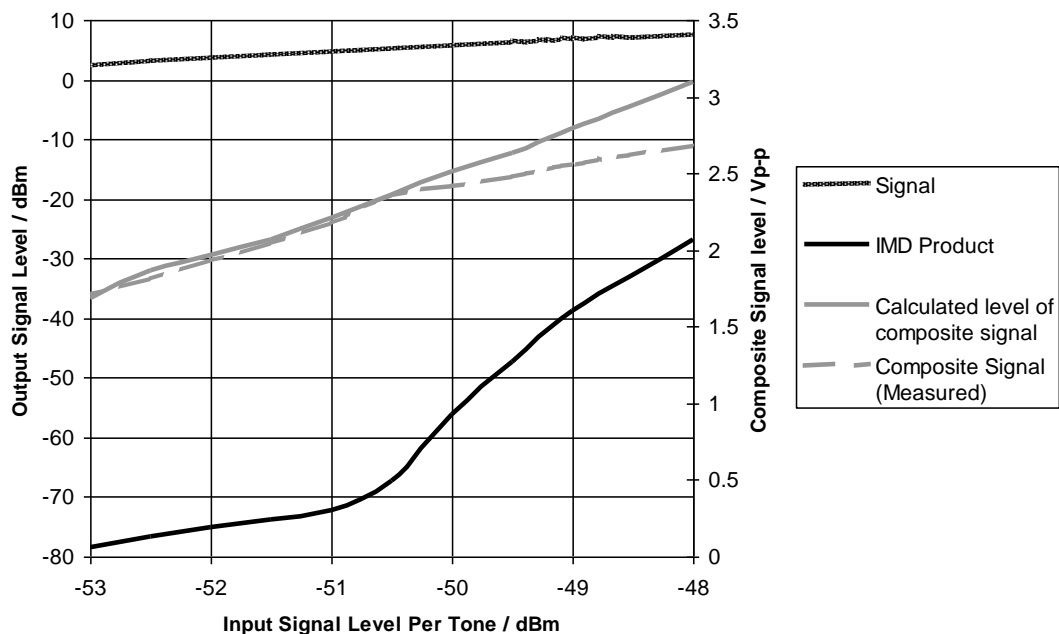
Figure 20 Variation in Input Third Order Intercept Point with VGA/VGB Control

## 7.5 Measurement of CMX973 Demodulator Intermodulation Performance

The measurement of the intermodulation (IMD) performance of the CMX973 demodulator requires great care because generally the IMD products are at a very low level. As a result, it is important to ensure products being measured are generated by the CMX973, not the measurement instrument or the test system.

It is also important to ensure that measurements are taken before the onset of clipping in the I/Q output stages – the effect is shown in Figure 21. Considering the graph, at signal levels below  $-51\text{dBm}$  per tone (two tone signal, tones of equal amplitude) the measured IMD product rises at the classical rate of  $2\text{dB}$  for every  $1\text{dB}$  increase in tone level. For input levels above  $-51\text{dBm}$  the rate of increase rises dramatically due to the onset of clipping. The effect can be seen in the plots of the composite signal: the calculated line is based on a calculation of the peak-to-peak swing of the output I/Q voltage from measured tone level at the output of the CMX973, however the actual output level is also plotted and the two lines deviate at the on-set of clipping.

It will be apparent that any calculation of IMD parameters, e.g. input third order intercept point, from measurements taken after the onset of clipping will give erroneous results if trying to characterise receiver operation at normal signal levels.



(Note: the two curves 'Signal' and 'IMD Product' are levels in dBm so should be referenced to the left hand Y-axis; the other curves are output voltages and use the right hand Y-axis.)

**Figure 21 Variations in Signal and IMD Product Levels**

Typical IMD measurements for the CMX973 demodulator usually involve IMD products at least  $75\text{dB}$  below the wanted signal.

The input level where compression commences will vary somewhat from device to device, the value of  $-44.5\text{dBm}^1$  (Figure 21) is typical but should only be used as an initial guide.

<sup>1</sup> Note:  $-50.5\text{ dBm per tone} = -44.5\text{ dBm PEP}$ ,

## 7.6 Operation with large input signals

The input 1dB gain compression point of the CMX973 will vary depending on the settings of the VGA and VGB gain stages. Typical results with a 45 MHz signal, 50 ohm source, 'straight in' are as follows:

VGA = 0dB, VGB = 0dB	Input 1dB compression point = -42dBm
VGA = -18dB, VGB = 0dB	Input 1dB compression point = -25dBm
VGA = -18dB, VGB = -12dB	Input 1dB compression point = -12dBm
VGA = -18dB, VGB = -24dB	Input 1dB compression point = -8dBm

The above results are with the OUTDRV bit set to '1' and the IMD5-IMD0 bits in register \$2F='000000'. For optimum intermodulation performance the IMDn bits should be set to '111111' which has the effect of reducing the gain by about 1dB thus improving the input compression point by 1dB.

Typical performance at maximum and minimum gain settings, plus some interim attenuator settings, is shown in Figure 22, measured at 45MHz, setting as above. The output is measured by buffering the differential I/Q output signals (voltage), converting to single-ended and then measuring as power based on 50 Ohms.

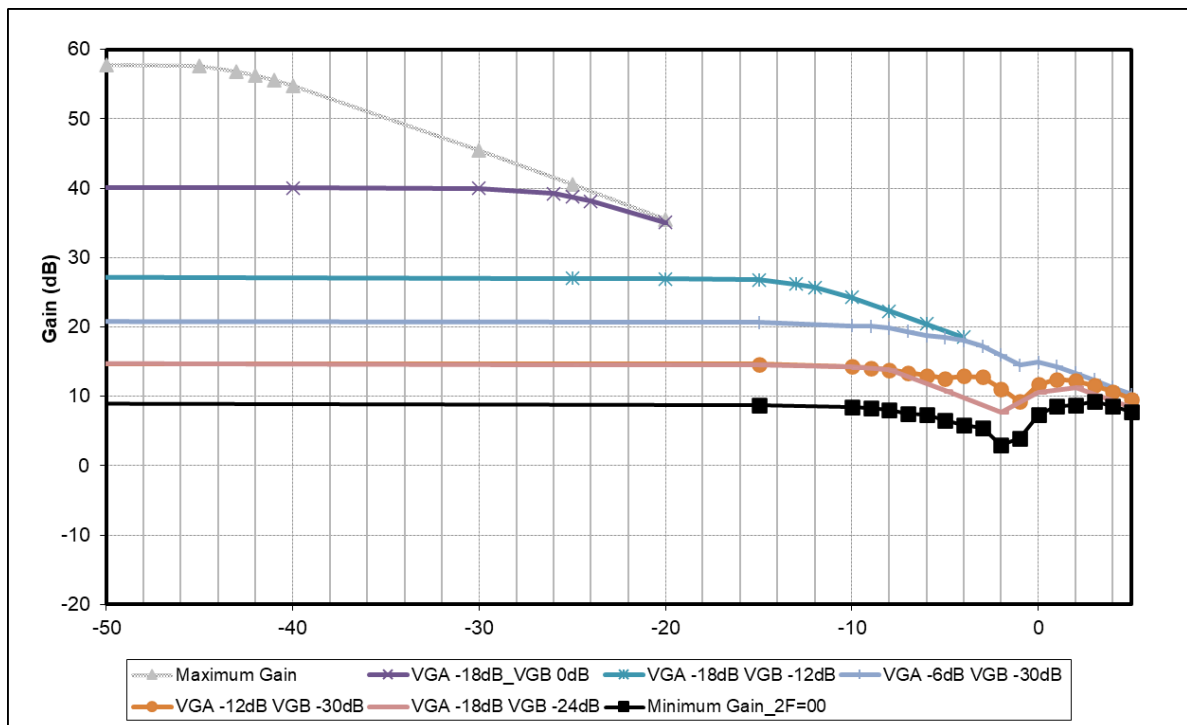
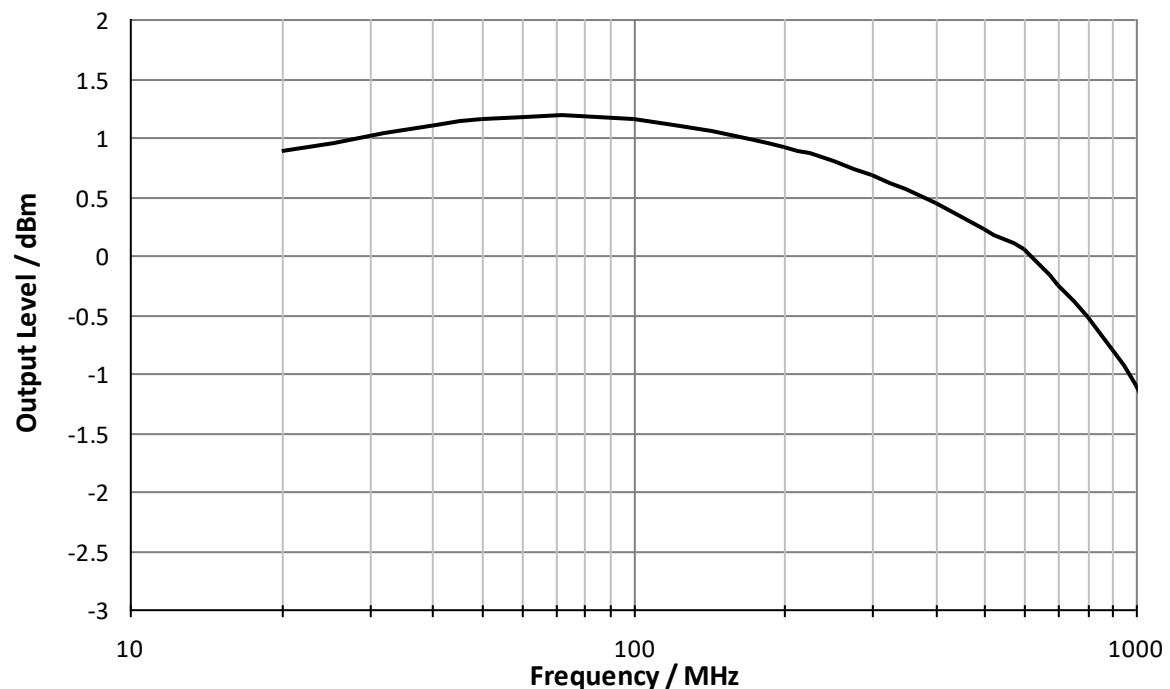


Figure 22 Gain v Input level at IF of 45MHz

## 7.7 Modulator Operation

The quadrature modulator section of the CMX973 is designed to operate with a maximum I/Q input level of 1Vp-p for either single-ended or differential operation. The device offers excellent modulation accuracy with accurate phase and amplitude balance and also low carrier leakage.

The variation in output level with frequency is typically 2dB, as shown in Figure 23 – where the output level is shown for an I/Q input of 1Vp-p 7kHz sine and cosine waves. The LO input level is -10dBm.



**Figure 23 Typical Variation in Modulator Output Level with Frequency**

### 7.7.1 Quadrature Accuracy

The modulation accuracy of the CMX973 is excellent and consistent with frequency. The I/Q phase and amplitude balance can be measured as a combined result in terms of image suppression when sine and cosine waves are applied to the I and Q channels. Typical results for 7kHz I/Q signals are shown in Figure 24.

The CMX973 can be used to generate a wide range of modulations including those with stringent adjacent channel requirements, for example C4FM modulation for the APCO P25 system – see Figure 25. In this figure, the I/Q input level is 700mVp-p and the measured adjacent channel power is -70dB.

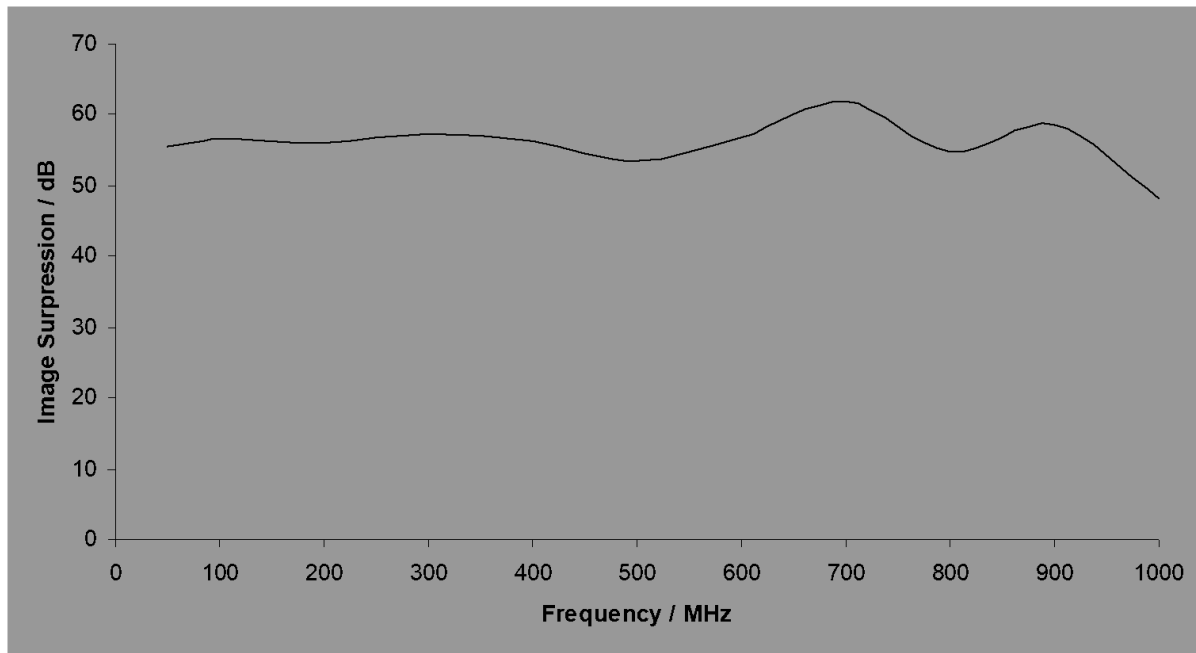


Figure 24 Modulator Accuracy with Frequency

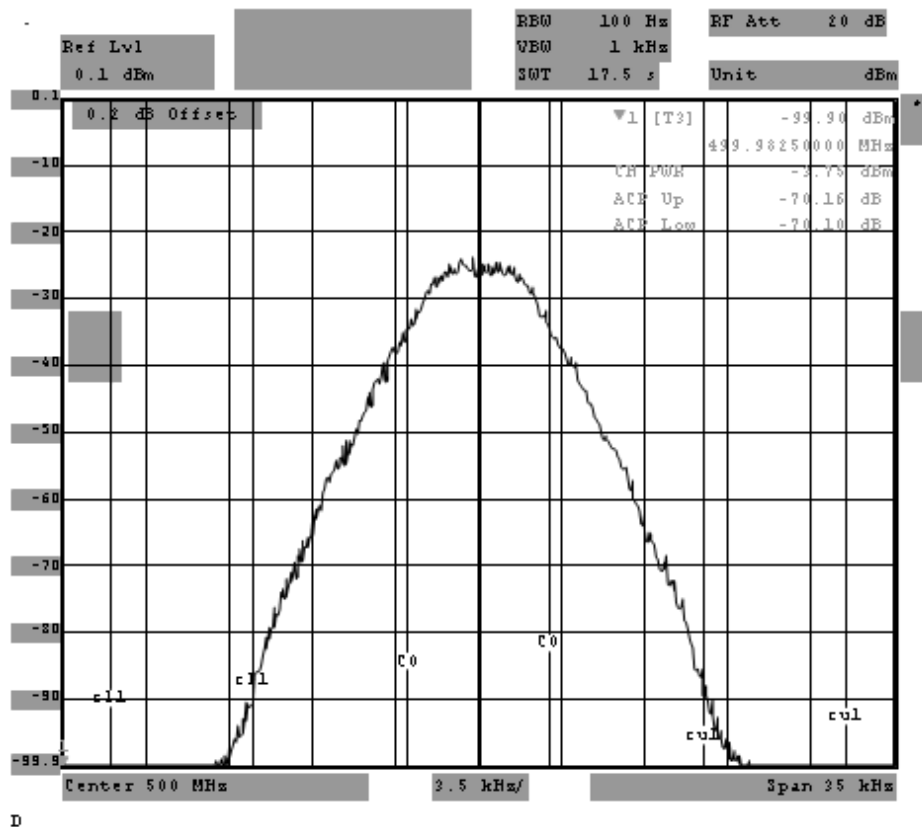


Figure 25 Typical Spectrum with APCO C4FM (TIA/EIA 102.CAAB-B) at 500MHz

### 7.7.2 Wideband Noise

The CMX973 noise floor does not vary significantly with LO input level: with LO levels between -5dBm and -15dBm, less than 0.5dB of variation from the typical value of -150dBm/Hz can be expected.

For optimum wideband noise during modulation the F bits in the Tx Control Register (\$1E, b3-b0) should be set to '1111'. Wideband noise during modulation measured at a 5MHz offset from a 390MHz signal is shown Table 19.

Freq Setting (\$1E, b3-b0)	Output Level (dBm)	Noise at 5 MHz offset (dBc/Hz)
'0000'	3.9	-143.7
'1111'	4.2	-146

**Table 19 Typical Wideband Noise at 5MHz Offset with Different Frequency Control Settings**

### 7.7.3 Harmonics

The typical levels of modulator harmonics are summarised in Table 20 for an I/Q modulator output level of circa 0dBm; the LO level was -10dBm.

Variation of the LO level +/-10dB does not change the CMX973 modulator harmonic levels significantly. Whether the divide-by-2 or divide-by-4 mode is used also does not materially effect the level of the harmonics.

Harmonic	100MHz / dBc	400MHz / dBc	500MHz / dBc	1GHz / dBc
2 <sup>nd</sup>	-37	-37	-36	-34
3 <sup>rd</sup>	-10	-15	-17	-28
4 <sup>th</sup>	-40	-36	-39	-47
5 <sup>th</sup>	-15	-27	-33	-46
6 <sup>th</sup>	-41	-48	-53	-57
7 <sup>th</sup>	-19	-40	-51	-59
8 <sup>th</sup>	-42	-55	-61	-68
9 <sup>th</sup>	-23	-51	-64	
10 <sup>th</sup>	-45	-66	-74	

**Table 20 Typical Modulator Harmonic Levels for Given Output Frequency**

## 7.8 VCO Phase Noise

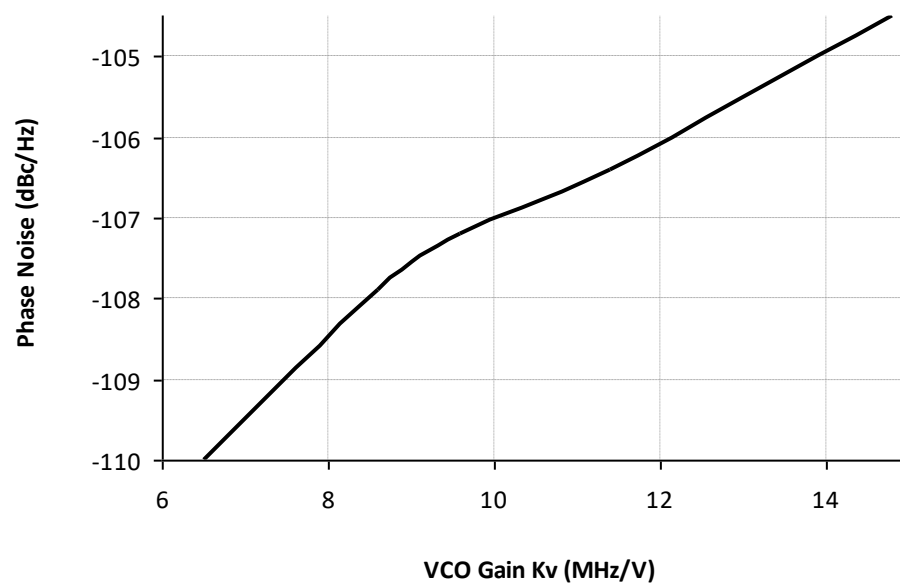
The performance of the negative resistance VCO can be optimised by use of the VCONR bits in the VCO control register (\$2F, b1-b0, see section 6.9.1). For example, the typical change in phase noise and tuning voltage with VCONR setting is shown in Table 21 for the 180 MHz VCO described in Figure 6 / Table 5.

VCONR setting (\$2F, b1-b0)	V <sub>tune</sub> (V)	Phase Noise at 10kHz offset, from $f_{vco}/2$ (dBc/Hz)
Maximum	2.425	-105.7
Intermediate 1	2.335	-107.1
Intermediate 2	2.235	-109.0
Minimum	2.183	-110.0

**Table 21 Effect of VCONR bits,  $f_{vco}$  = 180 MHz, divide-by-2**

The phase noise achieved by the CMX973 VCO depends on the VCO gain ( $K_v$ ). The effect is shown in Figure 26, which plots the phase noise measured at 90 MHz (180 MHz VCO as Figure 6 / Table 5, divide-by-2 mode) as a function of the VCO gain.





**Figure 26 Effect of VCO Gain on Phase Noise**

## 8 Performance Specification

### 8.1 Electrical Performance

#### 8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ ) or ( $V_{CC} - V_{RFGND}$ ) or ( $V_{CCSYNTH} - V_{RFGND}$ )	-0.3	+4.0	V
Voltage on any pin to $V_{SS}$ or $V_{RFGND}$	-0.3	$V_{DD} + 0.3$	V
Voltage between pins RFGND and VSS	-50	+50	mV
Voltage between pins VCC and VCCSYNTH	-0.3	+0.3	V
Current into or out of RFGND, VSS, VCC, VCCSYNTH or VDD pins	-75	+75	mA
Current into or out of any other pin	-30	+30	mA

Q5 Package	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$	–	1410	mW
... Derating (see Note below)	–	14.1	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

#### 8.1.2 Operating Limits

	Notes	Min.	Max.	Units
Analogue Supply ( $V_{CC} - V_{RFGND}$ )		3.0	3.6	V
Digital Supply ( $V_{DD} - V_{SS}$ )		3.0	3.6	V
Operating Temperature (see Note above)		-40	+85	$^{\circ}\text{C}$

### 8.1.3 Operating Characteristics

#### 8.1.3.1 DC Parameters

For the following conditions unless otherwise specified:

$V_{CC} = V_{CCSYNTH} = V_{DD} = 3.3V$ ;  $V_{RFGND} = V_{SS} = 0V$ . LO Level = -10dBm and  $T_{AMB} = +25^{\circ}C$ .

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption	1				
Powersave Mode	2	–	7	70	$\mu A$
Bias Only		–	1.7	2	mA
Operating Currents					
Tx Only	3	–	63	75	mA
Rx Only	4	–	15	19	mA
PLL and VCO	5	–	9	12	mA
Additional Current with DIFFAMP='1'	6	–	0.85	1.5	mA
Logic '1' Input Level		70%	–	–	$V_{DD}$
Logic '0' Input Level		–	–	30%	$V_{DD}$
Logic Input Leakage Current ( $V_{in} = 0$ to $V_{DD}$ )		-1.0	–	+1.0	$\mu A$
Output Logic '1' Level ( $I_{OH} = 0.6$ mA)		80%	–	–	$V_{DD}$
Output Logic '0' Level ( $I_{OL} = -1.0$ mA)		–	–	+0.4	V
Power Up Time					
Voltage Reference	7	–	–	0.5	ms
All Blocks Except Voltage Reference	7	–	–	10	$\mu s$

#### Notes:

1. Total current,  $V_{DD}$ ,  $V_{CC}$  and  $V_{CCSYNTH}$ .
2. Clock input (REFIN pin) not active; powersave mode includes the case after general reset with all analogue and digital supplies applied and also the case with  $V_{DD}$  applied but with  $V_{CC}$  and  $V_{CCSYNTH}$  supplies disconnected (i.e. in this latter scenario power from  $V_{DD}$  will not exceed the specified value, whatever the state of the registers), not including any current drawn from device pins by external circuitry.
3. Only Tx and Bias sections active.
4. Only Rx and Bias sections active.
5. Only Bias, PLL and VCO sections active.
6. DIFFAMP bit in General Control Register, see section 6.2.1, combined current for both differential amplifiers
7. Time from the rising edge of the last serial clock input following CSN being asserted for a write to the appropriate control register.

### 8.1.3.2 AC Parameters

For the following conditions unless otherwise specified:

$V_{CC} = V_{CCSYNTH} = V_{DD} = 3.3V$ ;  $V_{RFGND} = V_{SS} = 0V$ . LO Level = -10dBm and  $T_{AMB} = +25^{\circ}C$ .

AC Parameters	Notes	Min.	Typ.	Max.	Units
<b>Modulator Local Oscillator Input</b>					
Frequency Range	10	40	—	2000	MHz
LO Input Impedance	12	—	—	—	$\Omega$
LO Input Level		—	-10	—	dBm
<b>Differential Amplifiers</b>					
Gain Bandwidth Product		40	70	—	MHz
Input Offset Voltage		—	1	—	mV
Input Common Mode Range		1.0	1.6	2.5	V
Input Bias Current		—	0.4	—	$\mu A$
Input Resistance		—	160	—	k $\Omega$
Slew Rate		—	6	—	V/ $\mu s$
Differential Input Voltage		—	—	2	Vp-p
Input Referred Noise at 1kHz		—	15	—	nV/ $\sqrt{Hz}$
DC Output Range		$V_{RFGND+}$ 0.1	—	$V_{RFGND-}$ 0.1	V
Output Load	11	—	1k $\Omega$ //100pF	—	

#### Notes:

10. Local oscillator input frequency twice or four times the required operating frequency.
11. Operating into a virtual earth (not ground).
12. See section 7.1.2.

### 8.1.3.3 AC Parameters – Modulator

For the following conditions unless otherwise specified:

$V_{CC} = V_{CCSYNTH} = V_{DD} = 3.3V$ ;  $V_{RFGND} = V_{SS} = 0V$ . LO Level = -10dBm and  $T_{AMB} = +25^{\circ}C$ .

Quadrature Modulator	Notes	Min.	Typ.	Max.	Units
I/Q Input Common Mode Voltage		–	1.6	–	V
I/Q Mixer Input Voltage		–	–	1	Vp-p
Modulator Input Bandwidth		–	25	–	MHz
Gain from I/Q Input to Output	23	–	-4	–	dB(V/V)
Output Frequency Range		20	–	1000	MHz
Transmit Output Power (PEP)	20	–	0	–	dBm
Noise Floor	22	–	-150	–	dBm/Hz
Wideband Noise During Modulation	24	–	-146	–	dBc/Hz
Image Suppression					
At 100MHz		–	50	40	dB
At 500MHz		–	52	–	dB
At 1GHz		–	44	40	dB
I/Q Gain Matching Error		–	–	0.5	dB
I/Q Phase Matching Error		–	–	1	degree
Carrier Suppression					
At 100MHz		–	-50	-40	dBm
At 500MHz		–	-50	–	dBm
At 1000MHz		–	-49	-40	dBm
Equivalent Output IP3	20, 25, 26	–	14	–	dBm
Load Impedance		–	50	–	$\Omega$
Discrete Unwanted Emissions (other than harmonics of the output) in the Frequency Range 9kHz –12.75GHz.	21	–	–	-70	dBc

#### Notes:

20. Typical output power and OIP3 is achieved with the typical input drive level stated on I/Q channels, operation at 500MHz (sine and cosine waveforms on I/Q respectively).
21. With a spurious-free LO input and -10dBm output level.
22. Measured with TXIN, TXIP, TXQN, TXQP connected to 1.6V with 10 $\Omega$  resistors decoupled by 33nF capacitors; measured at 20MHz offset from the operating frequency of 380MHz.
23. Voltage gain measured from modulator input to output using 7kHz sine/cosine waves on TXIN/TXQN, at 500MHz.
24. Tx Control Register (\$1E), b3-b0 = '1111'.
25. Tx Control Register (\$1E), b3-b0 = '0000'.
26. Optimum performance for I/Q signals up to 2 MHz.

### 8.1.3.4 AC Parameters – Demodulator

For the following conditions unless otherwise specified:

$V_{CC} = V_{CCSYNTH} = V_{DD} = 3.3V$ ;  $V_{RFGND} = V_{SS} = 0V$ . LO Level = -10dBm and  $T_{AMB} = +25^{\circ}C$ .

IF Amplifier and Quadrature Demodulator	Notes	Min.	Typ.	Max.	Units
Gain	30,31	–	56	–	dB(V/V)
Noise Figure	30,31	–	10	–	dB
Input Third Order Intercept Point	30,34	–	-15	–	dBm
Input Frequency Range		20	–	300	MHz
LO Frequency Range		40	–	600	MHz
Input Impedance	31	–	1000	–	$\Omega$
Output Impedance		–	200	–	$\Omega$
Output Load					
Resistance (differential)	33	10	–	–	k $\Omega$
Capacitance per Pin	33	–	–	10	pF
Differential Output Voltage	33	2	–	–	Vp-p
Output Common Mode Voltage		$V_{CC} - 1.9$	$V_{CC} - 1.7$	$V_{CC} - 1.5$	V
LO Leakage at Input		–	-80	-40	dBm
Input 1dB Compression Point	30, 34,35	–	-41	–	dBm
VGA Control Range	32	–	18	–	dB
VGB Control Range	32	–	30	–	dB
VGA and VGB Step Size		4	6	8	dB
I/Q Gain Matching Error		–	0.1	0.5	dB
I/Q Phase Matching Error		–	0.1	1	degree
I/Q Output Bandwidth (-3dB)	33	5	10	–	MHz

#### Notes:

30. Measured from an unmatched 50 $\Omega$  input source to a differential I or Q output voltage; test frequency = 45MHz. Note that values include combined response of IF amplifier, quadrature demodulator and I/Q amplifier stages; at maximum VGA and VGB setting (0dB).
31. See also section 7.1.
32. Four VGA steps and six VGB steps, see Rx Control Register, section 6.3.1.
33. Differential Output Voltage is achieved with default output drive setting (register \$1C, b7='0', see section 6.3.1), for given output load and for at least the minimum I/Q output bandwidth; typical I/Q output bandwidth is achieved with increased drive capability selected (register \$1C, b7='1', see section 6.3.1) and with the same output load specification.
34. With increased output drive setting (register \$1C, b7='1').
35. With IMD5 – IMD0 (b7 – b2 of register \$2F) set to '111111'

### 8.1.3.5 AC Parameters – Integer N PLL and VCO

For the following conditions unless otherwise specified:

$V_{CC} = V_{CCSYNTH} = V_{DD} = 3.3V$ ;  $V_{RFGND} = V_{SS} = 0V$ . LO Level = -10dBm and  $T_{amb} = +25^{\circ}C$ .

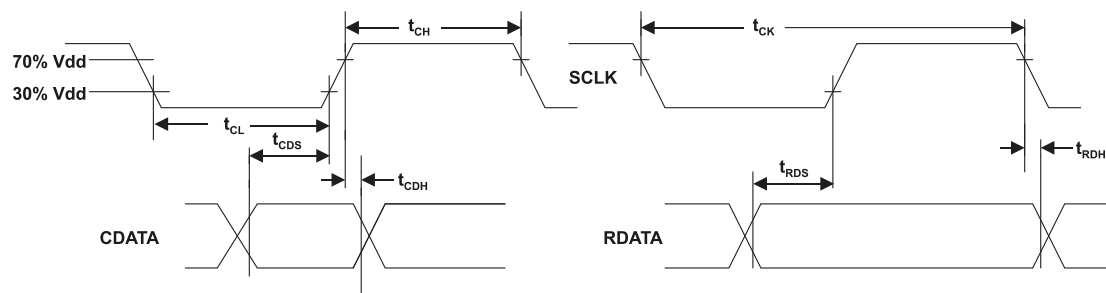
	Notes	Min.	Typ.	Max.	Unit
<b>Phase Locked Loop</b>					
<i>Reference Input</i>					
Frequency		5	–	30	MHz
Level	40	–	0.5	–	Vp-p
Divide Ratios (R Counter)		2	–	8191	
<i>Synthesiser</i>					
Comparison Frequency ( $f_{comparison}$ )		1	–	500	kHz
Input Frequency Range		40	–	1000	MHz
Input Level		-20	–	-5	dBm
Divide Ratios (M Counter)		80	–	32767	
Charge Pump Current		–	$\pm 2.5$	–	mA
1Hz Normalised Phase Noise Floor	43	–	-216	–	dBc/Hz
<b>Negative Resistance VCO</b>					
Supply Current (Enabled)		–	3	–	mA
Frequency Range	41	40	–	1000	MHz
Phase Noise at 10kHz Offset	42	–	-104	–	dBc/Hz
Phase Noise at 100kHz Offset	42	–	-118	–	dBc/Hz
<b>LO Input</b>					
Input Level		–	-10	–	dBm
Frequency Range		40	–	1000	MHz

#### Notes:

40. Sinewave or clipped sinewave.
41. Operation will depend on the choice and layout of external resonant components.
42. With external components from section 4.5 (Table 5) forming a 180MHz VCO; negative resistance bits set to minimum (\$2F, b1-b0 = '11'); phase noise quoted at VCO operating frequency but will normally be improved by the divider circuits in modulator/demodulator LO paths.
43. 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop bandwidth by: Measured Phase Noise (in 1Hz) =  $PN1Hz + 20\log_{10}(M) + 10\log_{10}(f_{comparison})$ .

C-BUS Timings (See Figure 27)		Notes	Min.	Typ.	Max.	Units
t <sub>CSE</sub>	CSN-enable to clock-high time		100	—	—	ns
t <sub>CSH</sub>	Last clock-high to CSN-high time		100	—	—	ns
t <sub>LOZ</sub>	Clock-low to reply output enable time		0.0	—	—	ns
t <sub>HIZ</sub>	CSN-high to reply output 3-state time		—	—	1.0	μs
t <sub>CSOFF</sub>	CSN-high time between transactions		1.0	—	—	μs
t <sub>NXT</sub>	Inter-byte time		200	—	—	ns
t <sub>CK</sub>	Clock-cycle time		200	—	—	ns
t <sub>CH</sub>	Serial clock-high time		100	—	—	ns
t <sub>CL</sub>	Serial clock-low time		100	—	—	ns
t <sub>CDS</sub>	Command data set-up time		75.0	—	—	ns
t <sub>CDH</sub>	Command data hold time		25.0	—	—	ns
t <sub>RDS</sub>	Reply data set-up time		50.0	—	—	ns
t <sub>RDH</sub>	Reply data hold time		0.0	—	—	ns

Timing diagram for CS, SCLK, CSDATA, and RDATA signals. The diagram shows the relationship between these signals during data transfer. CS (Chip Select) is active low. SCLK (Serial Clock) is a periodic clock signal. CSDATA (Chip Select Data) and RDATA (Read Data) are 8-bit data buses. The diagram illustrates the timing for reading 1 byte and 2 bytes of data. Key timing parameters are labeled:  $t_{CSE}$  (CS to SCLK setup),  $t_{CK}$  (SCLK period),  $t_{NXT}$  (SCLK to CS hold),  $t_{CSH}$  (SCLK to CSDATA setup),  $t_{CSOFF}$  (SCLK to CSDATA hold),  $t_{LOZ}$  (CSDATA to RDATA delay), and  $t_{HIZ}$  (RDATA to CSDATA delay). A legend indicates that shaded gray boxes represent levels that are not important or undefined.



### Figure 27 C-BUS Timing



## 8.2 Packaging

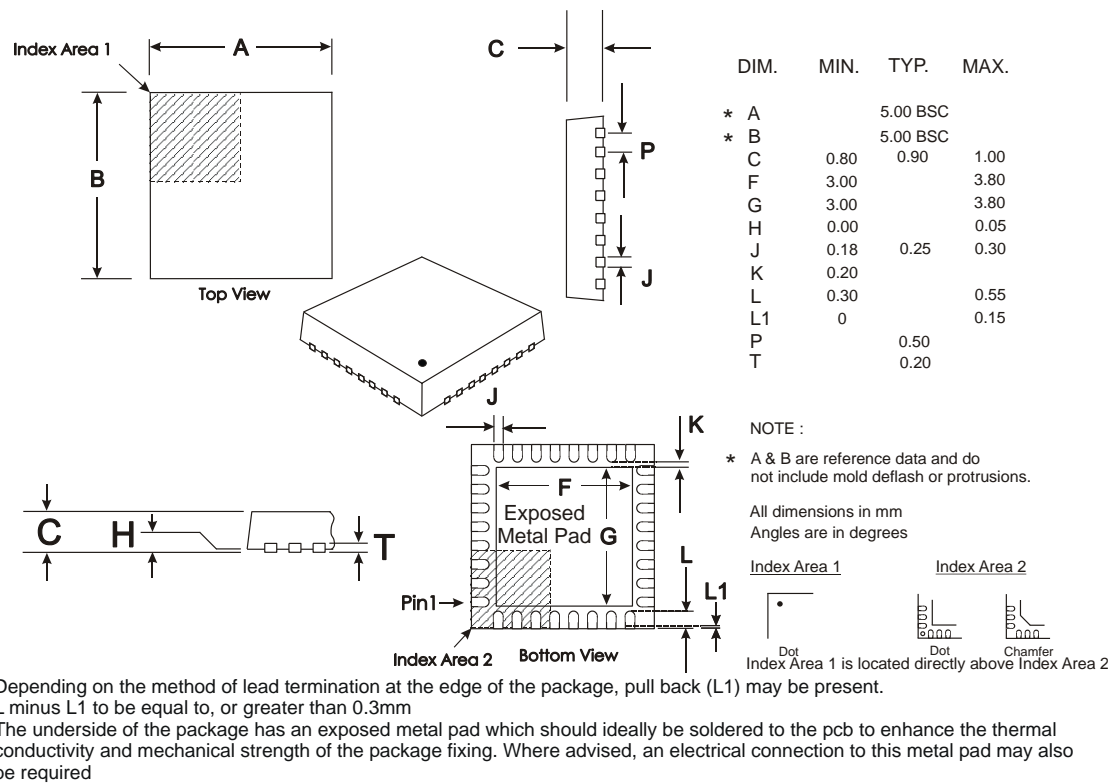


Figure 28 Q5 Mechanical Outline Order as part no. CMX973Q5

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



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