FEATURES

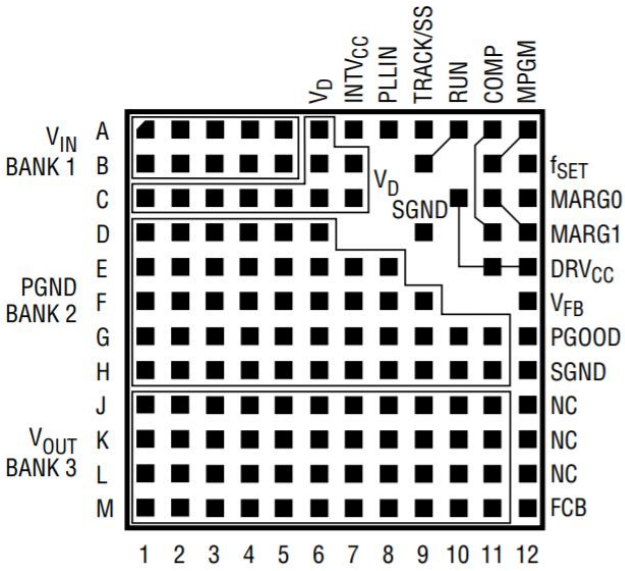
- Wide Input Voltage Range: 5V to 30V
- 8A Output Current
- 3.3V to 15V Output Voltage Range
- High efficiency
- Current Mode Control
- Output Voltage Tracking and Margining
- PLL Frequency Synchronization
- Output Overvoltage Protection
- Overcurrent protection
- Short-current protection
- External RUN control
- power good signal port
- 15mm x 15mm x 6mm LGA and
  15mm x 15mm x 6.6mm BGA Packages

DESCRIPTION

LTM4613CN is a complete 8A switch mode DC/DC power supply. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage range of 5V to 30V, the LTM4613CN supports an output voltage range of 3.3V to 15V, set by a single external resistor. Only bulk input and output capacitors are needed to finish the design. High switching frequency and an adaptive on-time current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

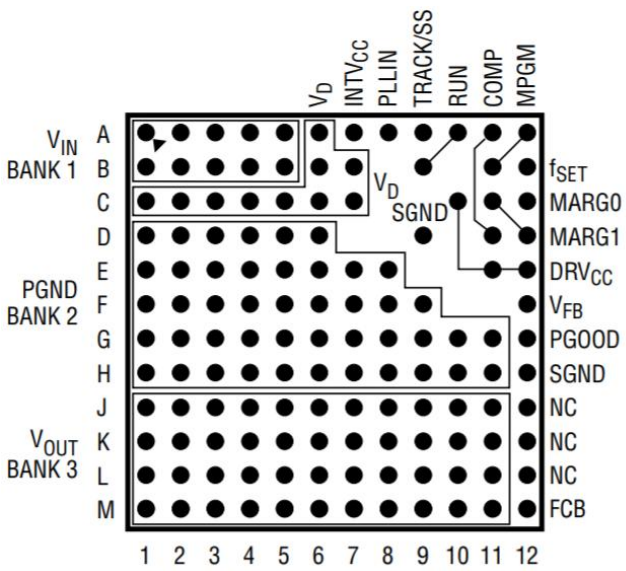
The LTM4613CN can provide high reliability power supply solutions for telecom and networking equipment,industrial equipment and RF systems.

PIN CONFIGURATION



LGA PACKAGE
133-LEAD (15mm × 15mm × 6 mm)

Fig.1 LTM4613CN LGA Package top view



BGA PACKAGE
133-LEAD (15mm × 15mm × 6.6mm)

Fig.2 LTM4613CN BGA Package top view

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}	-0.3V to 30V	Operating Temperature Range	-55℃ to 125℃
V_{OUT}	-0.3V to 16V	Junction Temperature	125℃
RUN	-0.3V to 5V	Storage Temperature Range	-55℃ to 125℃
V_{FB}, COMP	-0.3V to 5V	INTVCC,DRVCC,TRACK/SS, MPGM,MARG0,MARG1, PGOOD	-0.3V to INTVCC+0.3V
Peak Solder Reflow Package Body Temperature	220℃		

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Specifications					
Input DC Voltage $V_{IN(DC)}$		5	-	30	V
Undervoltage Lockout Threshold $V_{IN(UVLO)}$	I_{OUT}=0A	-	3.2	4	V
Internal VCC Voltage V_{INTVCC}	V_{IN}=30V, RUN>2 I_{OUT}=0A	4.7	5	5.5	V
$I_{INRUSH(VIN)}$	V_{OUT}=12V	-	-	-	-
	V_{IN}=24V	-	150	-	mA
	V_{IN}=30V	-	120	-	mA
Input Supply Bias Current $I_{Q(VIN)}$	$V_{IN\backslash}$=30V	-	80	-	mA
	V_{IN}=24V	-	60	-	mA
	Shut down RUN=0V	-	50	-	μA
Output Specifications					
Output Voltage $V_{OUT(DC)}$		11.83	12.07	12.31	V
Output Current Range $I_{OUT(DC)}$	V_{IN}=24V, V_{OUT}=12V	0	-	8	A
$\Delta V_{OUT(LINE)}/V_{FBOUT}$	V_{OUT}=12V, V_{FCB}=0V V_{IN}=24V-30V, I_{OUT}=0A	-	0.05	0.3	%
$\Delta V_{OUT(LOAD)}/V_{FBOUT}$	V_{IN}=30V	-	0.5	0.75	%

	V_{IN}=24V	-	0.5	0.75	%
fs	V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0A	-	600	-	kHz
Turn-On Time $t_{(START)}$	V_{IN}=24V-30V	-	0.3	-	ms
Settling Time for Dynamic Load Step $t_{(SETTLE)}$	V_{IN}=12V, V_{OUT}=3.3V	-	100	-	μs
Control Section					
Voltage at VFB Pin V_{FB}	V_{OUT}=12V, I_{OUT}=0A	0.591	0.6	0.609	V
RUN Pin On/Off Threshold V_{RUN}		1	1.5	1.9	V
Soft-Start Charging Current $I_{TRACK/SS}$	$V_{TRACK/SS}$=0V	-1	-1.5	-2	μA
Forced Continuous Threshold V_{FCB}		0.57	0.6	0.63	V
Forced Continuous Pin Current I_{FCB}	V_{FCB}=0V	-	-1	-2	μA
$t_{ON(MIN)}$		-	50	100	ns
$t_{OFF(MIN)}$		-	250	400	ns
R_{PLLIN}		-	50	-	kΩ
R_{FBHI}		99.5	100	100.5	kΩ
PGOOD					
ΔV_{FBH}		7	10	13	%
ΔV_{FBL}		-7	-10	-13	%
$\Delta V_{FB(HYS)}$		-	1.5	-	%
V_{PGL}	I_{PGOOD}=5mA	-	0.2	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

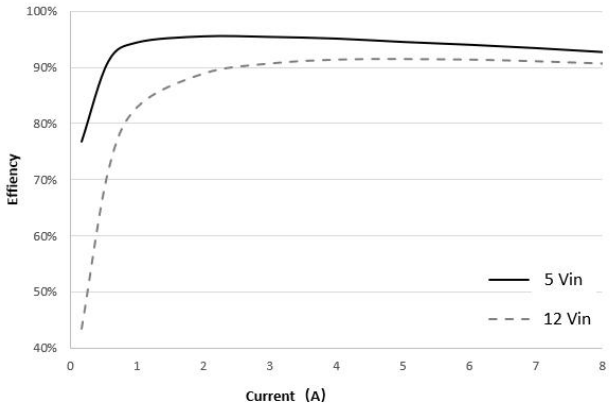


Fig.3 Efficiency vs Load Current with 3.3VOUT

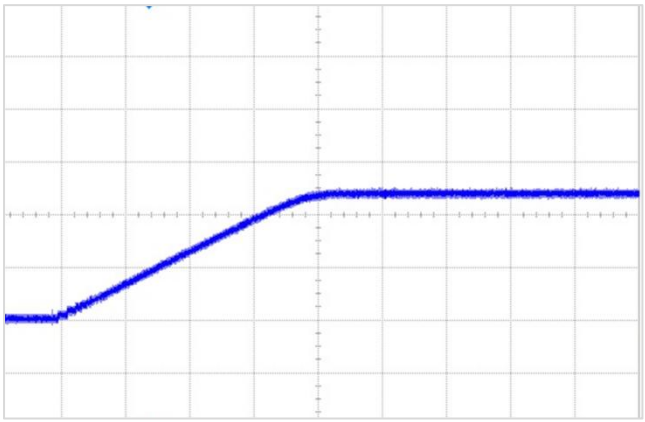


Fig.6 Start-Up with 24V_{IN} to 12V_{OUT} at I_{OUT} = 0A

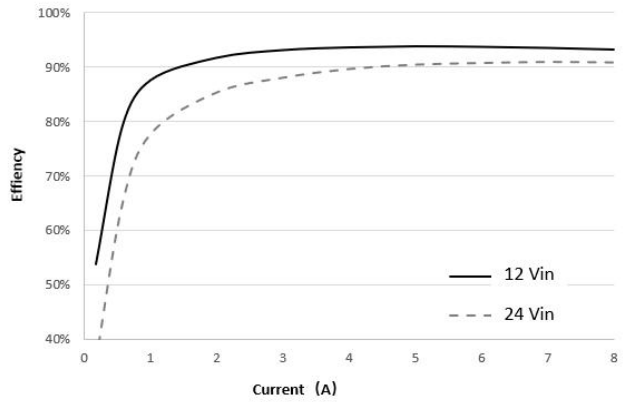


Fig.4 Efficiency vs Load Current with 5.0VOUT

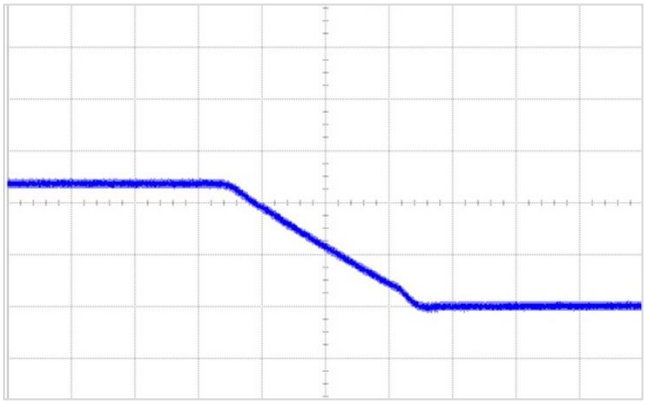


Fig.7 Shut-Down with 24V_{IN} to 12V_{OUT} at I_{OUT} = 8A

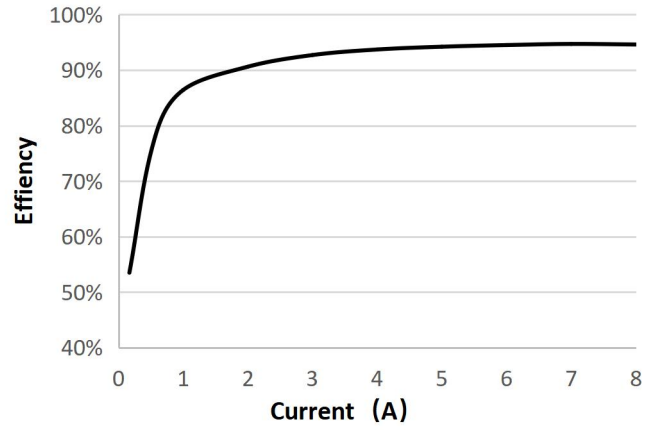


Fig.5 Efficiency vs Load Current with 24V_{IN} to 12V_{OUT}

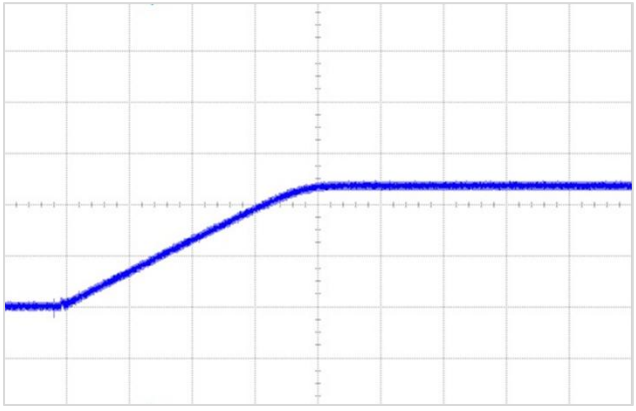


Fig.8 Start-Up with 24V_{IN} to 12V_{OUT} at I_{OUT} = 8A

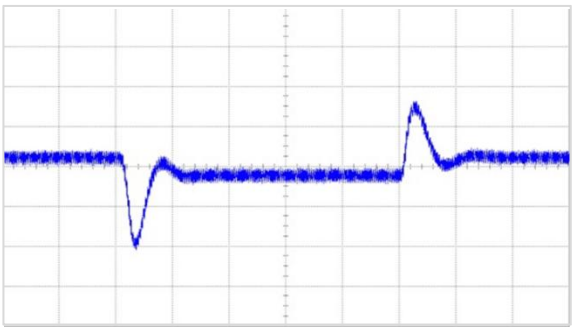


Fig.9 Transient Response from $12V_{IN}$ to $5V_{OUT}$

Load step: 0A to 4A

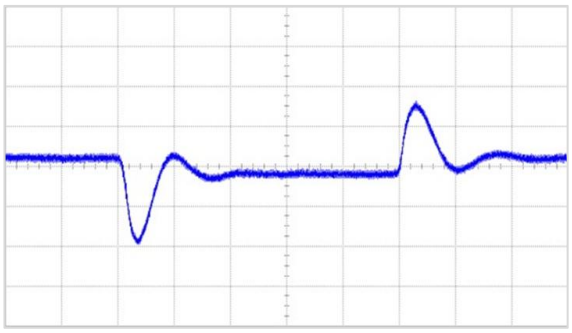


Fig.11 Transient Response from $24V_{IN}$ to $12V_{OUT}$

Load step: 0A to 4A

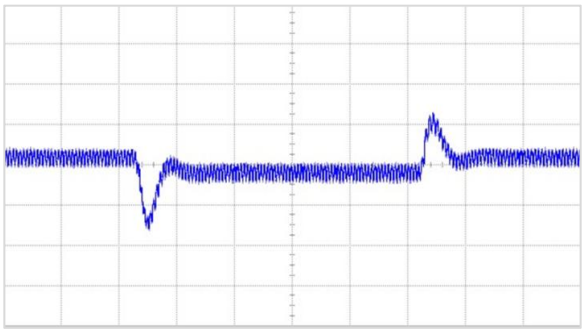


Fig.10 Transient Response from $12V_{IN}$ to $3.3V_{OUT}$

Load step: 0A to 4A

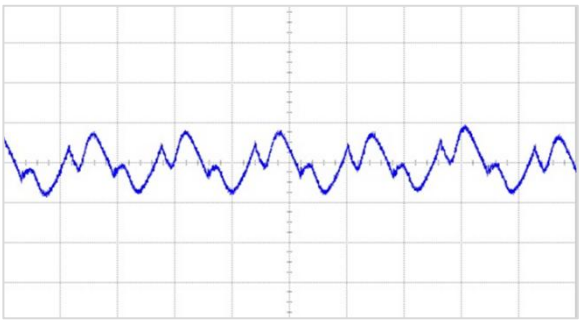


Fig.12 Output Ripple from $24V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 8A

PIN FUNCTIONS

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

PGND (Bank 2): Power Ground Pins for Both Input and Output Returns.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins (see the LTM4613CN Pin Configuration below).

V_D (Pins C1 to C7, B6 to B7, A6): Top FET Drain Pins. Add more high frequency ceramic decoupling capacitors between V_D and PGND to handle the input RMS current and reduce the input ripple further.

DRV_{CC} (Pins C10, E11, E12): These pins normally connect to $INTV_{CC}$ for powering the internal MOSFET drivers. They can be biased up to 6V from an external supply with about 50mA capability. This improves efficiency at the higher input voltages by reducing power dissipation in the module. See the Applications Information section.

$INTV_{CC}$ (Pin A7): This pin is for additional decoupling of the 5V internal regulator.

PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock above 2V and below $INTV_{CC}$ subject to minimum on-time and minimum off-time requirements. See the Applications Information section.

FCB (Pin M12): Forced Continuous Input. Connect this pin to SGND to force continuous synchronization operation at light load or to $INTV_{CC}$ to enable discontinuous mode operation at light load.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn-on as a standalone regulator. Slave operation is performed by putting a resistor divider from the master output to the ground, and connecting the center point of the divider to this pin. See the Applications Information section.

MPGM (Pins A12, B11): Programmable Margining Input. A resistor from these pins to ground sets a current that is equal to 1.18V/R. This current multiplied by 10k will equal a value in millivolts that is a percentage of the 0.6V reference voltage. Leave floating if margining is not used. See the Applications Information section. To parallel LTM4613CNs , each requires anindividual MPGM resistor. Do not tie MPGM pins together.

f_{SET} (Pin B12): Frequency Set Internally to 600kHz at 12V Output. An external resistor can be placed from this pin to ground to increase frequency or from this pin to V_{IN} to reduce frequency. See the Applications Information section for frequency adjustment.

VFB (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 100k 0.5% precision resistor. Different output voltages can be programmed with an additional resistor between the V_{FB} and SGND pins. See the Applications Information section.

MARG0 (Pin C12): LSB Logic Input for the Margining Function. Together with the MARG1 pin, the MARG0 pin will determine if a margin high, margin low, or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

MARG1 (Pins C11, D12): MSB Logic Input for the Margining Function. Together with the MARG0 pin, the MARG1 pin will determine if a margin high, margin low, or no margin state is applied. The pins have an internal pull-down resistor of 50k. See the Applications Information section.

SGND (Pins D9, H12): Signal Ground Pins. These pins connect to PGND at output capacitor point.

COMP (Pins A11, D11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after a 25µs power bad mask timer expires.

RUN (Pins A10, B9): Run Control Pins. A voltage above 1.9V will turn on the module, and below 1V will turn off the module. A programmable UVLO function can be accomplished with a resistor from VIN to this pin. Maximum pin voltage is 5V.

MTP (Pins J12, K12, L12): No Connect Pins. Leave floating. Used for mounting to PCB.

OPERATION

The LTM4613CN is a standalone nonisolated switch mode DC/DC power supply. It can deliver 8A of DC output current with minimal external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from 3.3V_{DC} to 15V_{DC} over a 5V to 30V input voltage.

Current mode control provides cycle-by-cycle fast current limiting. Moreover, foldback current limiting is provided in an overcurrent condition when V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET M1 is turned off and bottom FET M2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both M1 and M2. At light load currents, discontinuous mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting FCB pin higher than 0.6V.

When the DRV_{CC} pin is connected to $INTV_{CC}$, an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher input voltage range.

The MPGM, MARG0, and MARG1 pins are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, while the MARG0 and MARG1 select positive or negative margining. The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

APPLICATIONS INFORMATION

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. A 100k 0.5% internal feedback resistor connects the V_{OUT} and V_{FB} pins together. Adding a resistor, R_{FB}, from the V_{FB} pin to the SGND pin programs the output voltage.

$$V_{OUT} = 0.6V \cdot \frac{100 + R_{FB}}{R_{FB}}$$

or equivalently,

$$R_{FB} = \frac{100k}{\frac{V_{OUT}}{0.6V} - 1}$$

Table 1. R_{FB} Standard 1% Resistor Values vs V_{OUT}

V_{OUT} (V)	3.3	5	6	8	10	12	14	15
R_{FB} (kΩ)	22.1	13.7	11.0	8.06	6.34	5.23	4.42	4.12

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference ± offset for margining. A 1.18V reference divided by the R_{PGM} resistor on the MPGM pin programs the current.

Calculate V_{OUT}(MARGIN):

$$V_{OUT\ (MARGIN)} = V_{OUT} \cdot (\frac{\%V_{OUT}}{100})$$

Where %V_{OUT} is the percentage of V_{OUT} to be margined, and V_{OUT}(MARGIN) is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \cdot \frac{1.18V}{V_{OUT(MARGIN)}} \cdot 10K$$

Where R_{PGM} is the resistor value to place on the MPGM pin to ground.

The margining voltage, V_{OUT}(MARGIN), will be added or subtracted from the nominal output voltage as determined by the state of the MARG0 and MARG1 pins. See the table 2 below:

Table 2:

MARG1	MARG 0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Parallel Operation

The LTM4613CN devic e is an inherently current mode controlled device. This allows the paralleled modules to have very good current sharing and balanced thermals on the design. The voltage feedback equation changes with the variable N as modules are paralleled:

$$R_{FB} = \frac{\frac{100k}{N}}{\frac{V_{OUT}}{0.6V} - 1}$$

Operating Frequency

The operating frequency of the LTM4613CN is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. If lower output ripple is required, the operating frequency f can be increased by adding a resistor R_{fSET} between f_{SET} pin and SGND, as shown in Figure 16.

$$f = \frac{V_{OUT}}{1.5 \cdot 10^{-10}\ (R_{PGM}||133K)}\ [\text{Hz}]$$

For output voltages more than 12V, the frequency can be higher than 600kHz, thus reducing the efficiency significantly. Additionally, the minimum off-time of 400ns normally limits the operation when the input voltage is close to the output voltage. Therefore, it is recommended to lower the frequency in these conditions by connecting a resistor (R_{fSET}) from the f_{SET} pin to V_{IN} as shown in Figure 15, where:

$$f = \frac{V_{OUT}}{5 \cdot 10^{-11}(\frac{3 \cdot R_{fSET} \cdot 133K}{R_{fSET} - 2 \cdot 133K})}\ [\text{Hz}]$$

The load current can affect the frequency due to its constant on-time control. If constant frequency is a necessity, the PLLIN pin can be used to synchronize the frequency of the LTM4613CN to an external clock.

Input Capacitors

LTM4613CN is designed to achieve low input conducted. EMI noise due to the fast switching of turn-onand turnoff. Additionally, a high-frequency inductor is integrated into the input line fornoise attenuation. V_D and V_{IN} pins are available for external input capacitors to form a high frequency π filter.The ceramic capacitors, C1-C3, on the V_D pins are used to handle most of the RMS current into the converter, so careful attention is needed for capacitors C1-C3 selection.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \cdot \sqrt{D \cdot (1 - D)}$$

In this equation, η is the estimated efficiency of the power module. Note the capacitor ripple current ratings are often based on temperature

and hours of life. This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In a typical 8A output application, three very low ESR, X5R or X7R, 10μF ceramic capacitors are recommended for C1-C3. This decoupling capacitance should be placed directly adjacent to the module V_D pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10μF ceramic is typically good for 2A of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

Output Capacitors

The LTM4613CN is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements . C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical capacitance is 4×47μF if all ceramic output capacitors are used. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

Multiphase operation with multiple 4613 devices in parallel will also lower the effective output ripple current due to the phase interleaving operation. Pick the corresponding duty cycle and the number of phases to get the correct output ripple current value.

Fault Conditions: Current Limit and Overcurrent Foldback

LTM4613CN has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady state operation, but also in response to transients. To further limit current in the event of an overload condition, the LTM4613CN provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.5μA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal voltage reference plus or minus any margin delta. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \cdot (0.6 \pm V_{OUT(MARGIN)}) \cdot \left(\frac{C_{SS}}{1.5\mu A}\right)$$

If the RUN pin falls below 1.5V, then the TRACK/SS pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and forced continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp rise time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in Volts/ Time. The equation:

$$\frac{MR}{SR} \cdot 100k = R2$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R2 is equal to 100k. R1 is derived from equation:

$$R1 = \frac{0.6V}{\frac{V_{FB}}{100k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R2}}$$

where VFB is the feedback voltage reference of the regulator, and VTRACK is 0.6V. Since R2 is equal to the 100k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R1 is equal to RFB with VFB = VTRACK. In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R2 can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output

voltage will reach its final value before the master output. For example, MR = 1.5V/1ms, and SR = 1.2V/1ms. Then R2 = 125k. Solve for R1 to equal 5.18k.

Each of the TRACK/SS pins will have the 1.5μA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK/SS pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 100k is used then a 10k value can be used to reduce the TRACK/SS pin offset to a negligible value.

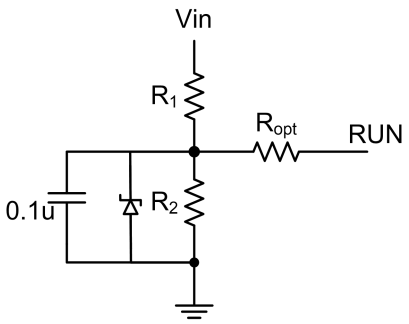
RUN Enable

The RUN pin is used to enable the power module. The pin can be driven with 5V logic levels.

The RUN pin can also be used as an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin. The equation for UVLO threshold:

$$V_{UVLO}=\frac{R_1+R_2}{R_2}\cdot 1.5V$$

It is recommended to connect a 5.1V Zener diode to protect this pin.



POWER GOOD

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point and tracks with margining.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages.

FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.6V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. FCB pin below the 0.6V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

PLLIN PIN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of an external clock. The external clock frequency range must be within ±30% around the set operating frequency. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock low level below 0.3V. The PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. During the start-up of the regulator, the phase-locked loop function is disabled.

$INTV_{CC}$ and DRV_{CC} Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV_{CC} for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4613CN can be directly powered by V_{IN}. The gate driver current through the LDO is about 20mA.The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 20mA \cdot (V_{IN} - 5V)$$

The LTM4613CN also provides the external gate driver voltage pin DRV_{CC}. If there is a 5V rail in the system, it is recommended to connect the DRV_{CC} pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV_{CC} pin.

Safety Considerations

The LTM4613CN does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse.If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Typical Application Circuit

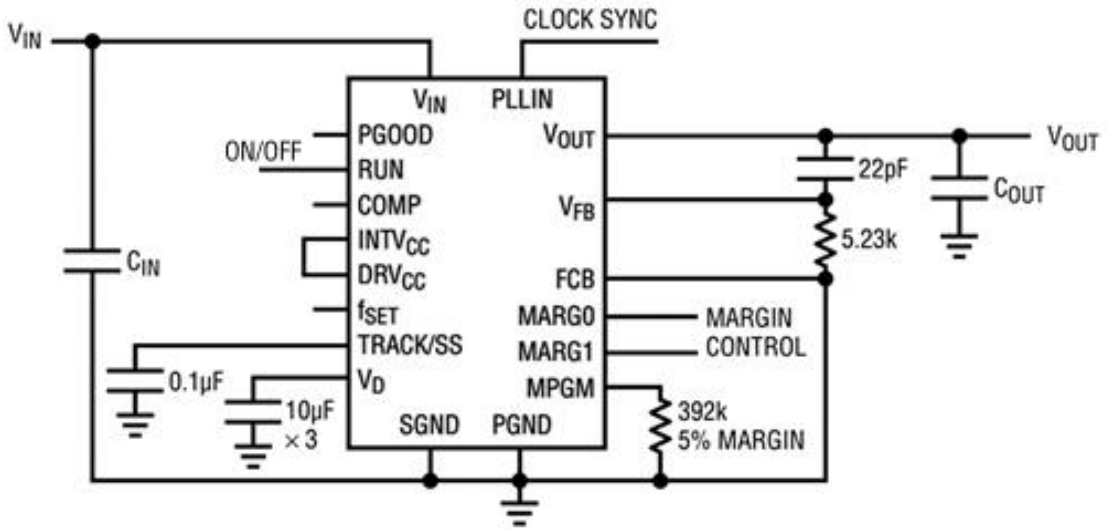


Fig.13 Typical 24V to 30V_{IN}, 12 V_{OUT} at 8A Design

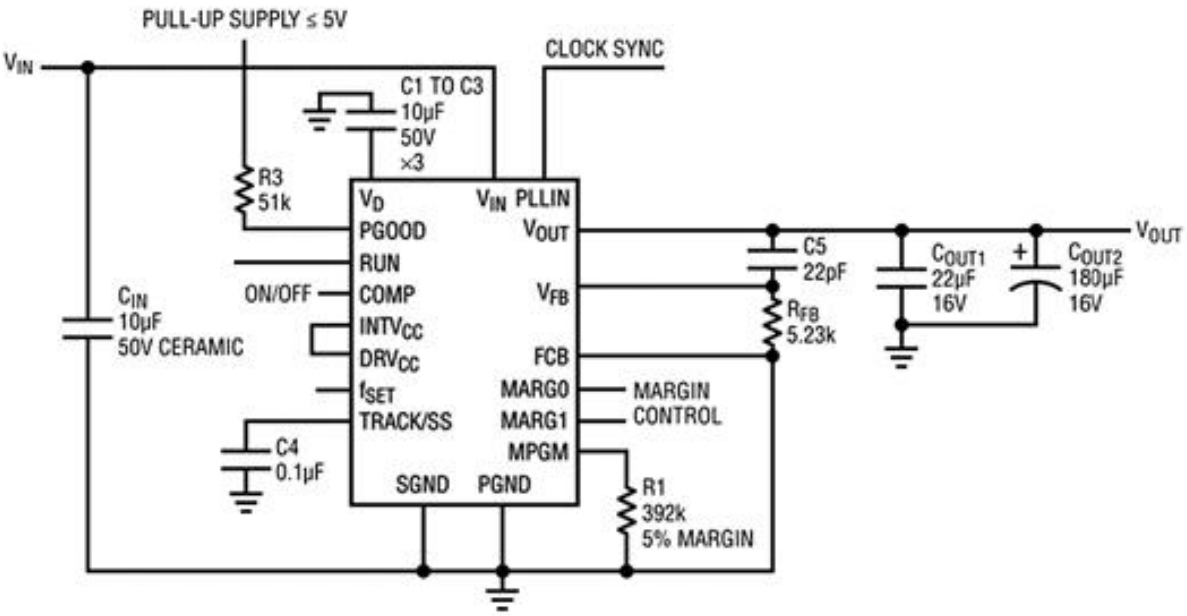


Fig.14 Typical 22V to 30V_{IN}, 12 V_{OUT} at 8A Design

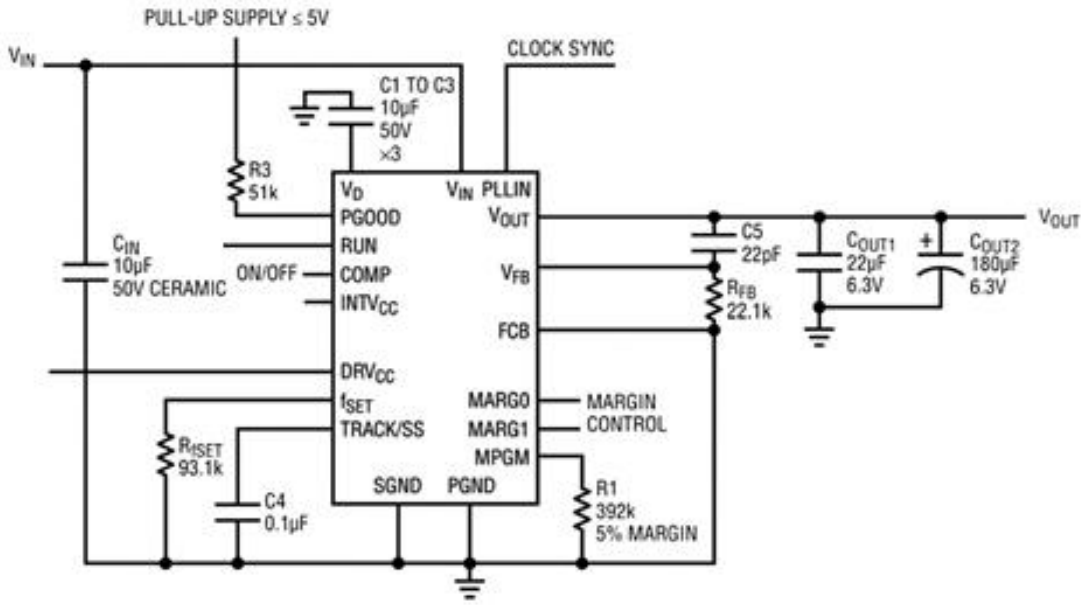


Fig.15 Typical 5V to 30V_{IN}, 3.3 V_{OUT} at 4A Design with 400kHz Frequency

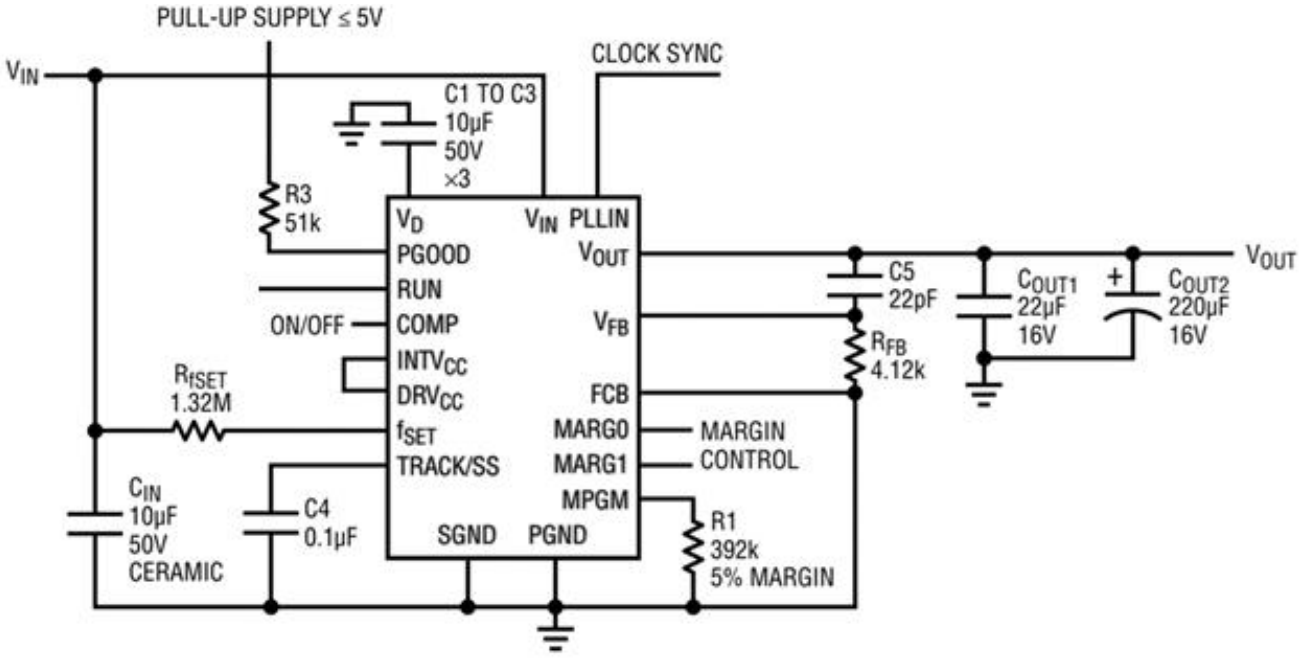


Fig.16 Typical 26V to 30V_{IN}, 15 V_{OUT} at 5A Design with 600kHz Frequency

Humidity sensitivity before SMT upper plate

LTM4613CN products must be dried before plate, otherwise it may cause poor welding or even damage due to moisture. According to JEDEC standard J-STD-033 "Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices" , please use the following conditions to baking the module: The temperature is 125 °C for 48 hours or more. Please refer to Fig.17 for the temperature curve of SMT reflow soldering.

A reminder: Please try to avoid using high temperature welding methods (such as high temperature heat gun, high temperature hot plate, etc.) that exceed the peak temperature of SMT reflow soldering to solder the upper plate, or disassemble the LTM4613CN product module. Any high temperature welding and disassembly methods that exceed the peak temperature of SMT reflow soldering may cause irreversible damage to the product. For products that exceed the peak temperature of SMT reflow soldering and disassembling, manufacturers will not guarantee the performance of the product, and it is difficult to make an accurate failure analysis.

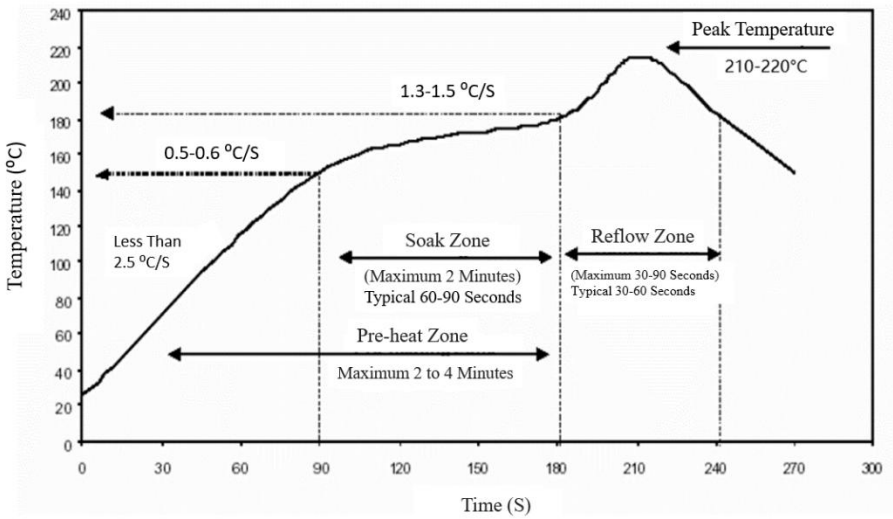
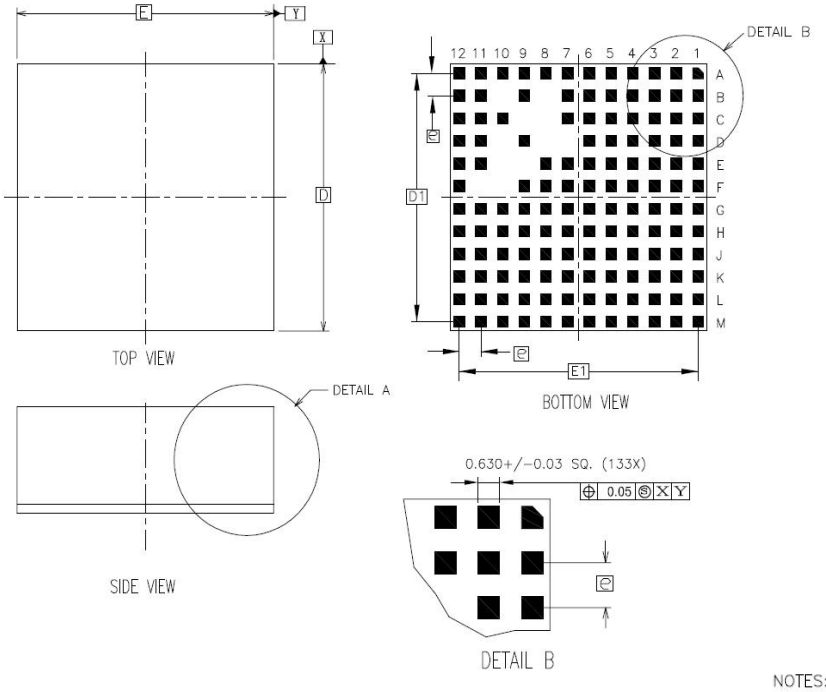
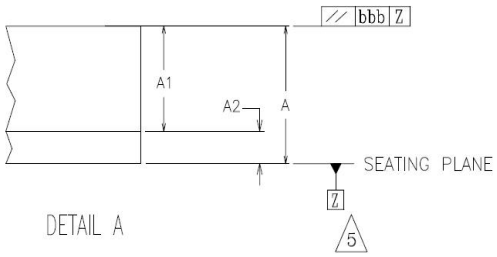


Fig.17 Reflow Soldering Temperature Curve

Packaging Description



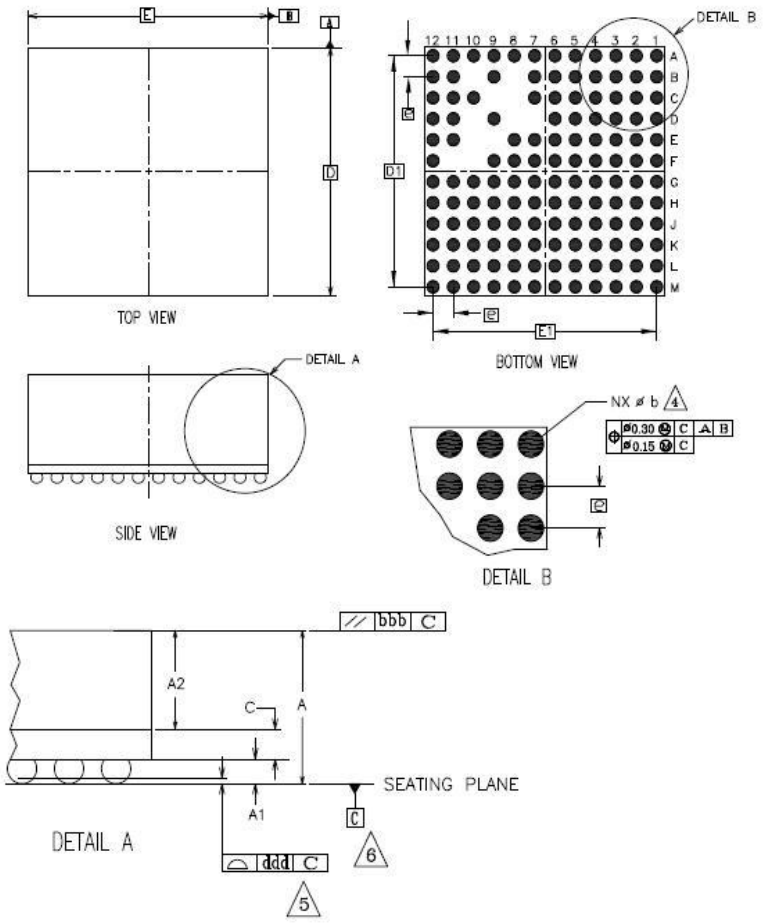
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	5.85	6.00	6.15
A1	5.40	5.50	5.60
A2		0.50 Ref.	
D	14.85	15.00	15.15
D1		13.97 BSC.	
E	14.85	15.00	15.15
E1		13.97 BSC.	
bbb		0.10	
e		1.27 BSC.	
MD/ME		12/12	
N		133	



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC LGA PITCH.
3. 'M' REPRESENTS THE BASIC LGA MATRIX SIZE.
   AND SYMBOL 'N' IS THE NUMBER OF LGA AFTER DEPOPULATING.
4. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
5. PRIMARY DATUM 'Z' IS SEATING PLANE.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
7. LAND DESIGNATION PER JESD MO−222.

Packaging Description



DIMENSIONAL REFERENCES				
REF.	MIN.	NOM.	MAX.	
A	6.35	6.60	6.85	10
A1	0.50	0.60	0.70	
A2	5.40	5.50	5.60	
c	0.45	0.50	0.55	
D	14.85	15.00	15.15	
D1	13.97 BSC.			
E	14.85	15.00	15.15	
E1	13.97 BSC.			
b	0.60	0.75	0.90	
bbb	0.25			
ddd	0.20			
e	1.27 BSC.			
M	12			
N	133			
REF: JEDEC MS-028				10

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'N' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DAIUM C
5. DIMENSION 'ddd' IS MEASURED PARALLEL TO PRIMARY DATUM C
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. SUBSTRATE MATERIAL BASE IS BT RESIN.
9. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
10. CONFORM TO JEDEC MS-028, EXCEPT DIMENSION 'A'.

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