

PROTECTION PRODUCTS

Description

RClamp®1265P provides dedicated surge and ESD protection for uUSB ports. It features low capacitance TVS diodes for protection of the USB data (DP, DM) and USB ID pins operating up to +/- 6.5 volts. These diodes provide ESD protection to $\pm 25\text{kV}$ contact discharge per IEC 61000-4-2. Loading capacitance on these lines is 0.95pF (maximum). An integrated 12 volt TVS diode is used for protection of the USB voltage bus. The VBus TVS is designed with a high surge current capability of 100A ($t_p=8/20\mu\text{s}$) and low clamping voltage.

RClamp1265P is in a 6-pin SLP2018P6 package measuring 2.0 x 1.8 mm with a nominal height of 0.57mm. Leads are finished with NiPdAu. This highly integrated device requires less board space than existing solutions. The combination of small size, low capacitance, and high level of surge and ESD protection makes this device a flexible solution for protection of USB interfaces in mobile phones, laptops, and other portable electronics.

Features

- High ESD withstand voltage
 - IEC 61000-4-2 (ESD) 30kV (air), 25kV (contact)
- Surge protection for USB voltage bus to 100A (8/20 μs) and data pins to 8A (8/20 μs)
- USB DP, DM, and ID Pin operating voltage: +/- 6.5V
- USB VBus operating voltage: 12V
- Low ESD clamping
- Low capacitance: 0.95pF maximum
- Dynamic resistance: 0.55 Ohms (Typ)
- Solid-state silicon-avalanche technology

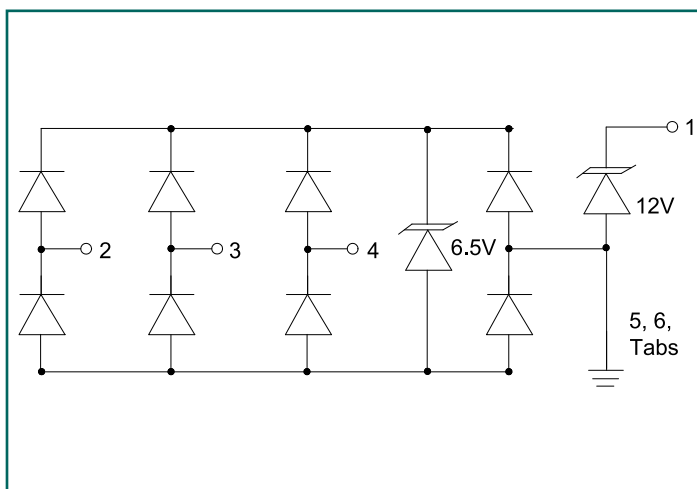
Mechanical Characteristics

- SLP2018P6 6L package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.0 x 1.8 x 0.57 mm
- Lead Finish: NiPdAu
- Marking : Marking code + date code
- Packaging : Tape and Reel

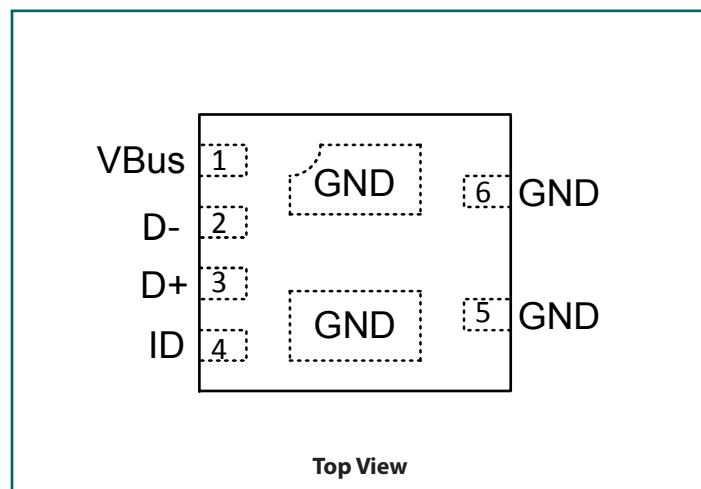
Applications

- USB Type C
- USB 2.0
- USB OTG
- uUSB

Circuit Diagram



Pin Configuration



Absolute Maximum Ratings

Rating	Symbol	Value	Units
DP, DM, USB ID TVS (Pins 2, 3, 4)			
Peak Pulse Power (tp = 8/20μs)	P _{PK}	160	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	8	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±30 ±25	kV
Operating Temperature	T _J	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C
VBus TVS (Pin 1)			
Peak Pulse Power (tp = 8/20μs)	P _{PK}	3000	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	100	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±30 ±30	kV
Operating Temperature	T _J	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

VBus TVS (Pin 1)							
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}	-40°C to 85°C Pin 1 to GND				12	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA, Pin 1 to GND	-40°C to 85°C	13	16	19	V
Reverse Leakage Current	I _R	V _{RWM} = 12V	T = 25°C		0.002	0.100	μA
			T = 85°C		0.01	0.250	μA
Forward Voltage	V _F	I _F = 10mA GND to Pin 1			0.75	1.1	V
Clamping Voltage	V _C	I _{pp} = 40A, tp = 8/20μs Pin 1 to GND				20	V
Clamping Voltage	V _C	I _{pp} = 100A, tp = 8/20μs Pin 1 to GND				30	V
Dynamic Resistance ^{2, 3}	R _{DYN}	tp = 0.2/100ns (TLP) Pin 1 to GND			0.06		Ohms
Junction Capacitance	C _J	V _R = 0V, f = 1MHz Pin 1 to GND	T = 25°C			650	pF

Electrical Characteristics (T=25°C unless otherwise specified)

DP, DM, USB ID TVS (Pin 2, 3, 4)						
Parameter	Symbol	Conditions		Min.	Typ.	Max. Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 85°C Pin 2, 3, 4 to GND				6.5 V
Reverse Breakdown Voltage	V_{BR}	$I_t = 10\text{mA}$, Pin 2, 3, 4 to GND	-40°C to 85°C	7.5	9.5	11.5 V
Reverse Leakage Current	I_R	$V_{RWM} = 6.5\text{V}$	T = 25°C		0.01	0.100 μA
			T = 85°C		0.02	0.250 μA
Clamping Voltage	V_C	$I_{pp} = 8\text{A}$, $t_p = 8/20\mu\text{s}$, Pin 2, 3, 4 to GND				20 V
ESD Clamping Voltage ²	V_C	$I_{pp} = 4\text{A}$, $t_p = 0.2/100\text{ns}$ (TLP) Pin 2, 3, 4 to GND			13.5	V
ESD Clamping Voltage ²	V_C	$I_{pp} = 16\text{A}$, $t_p = 0.2/100\text{ns}$ (TLP) Pin 2, 3, 4 to GND			20	V
Dynamic Resistance ^{2,3}	R_{DYN}	$t_p = 0.2/100\text{ns}$ (TLP) Pin 2, 3, 4 to GND			0.55	Ohms
Junction Capacitance	C_J	$V_R = 0\text{V}$, $f = 1\text{MHz}$ Pin 2, 3, 4 to GND	T = 25°C		0.85	0.95 pF

Notes:

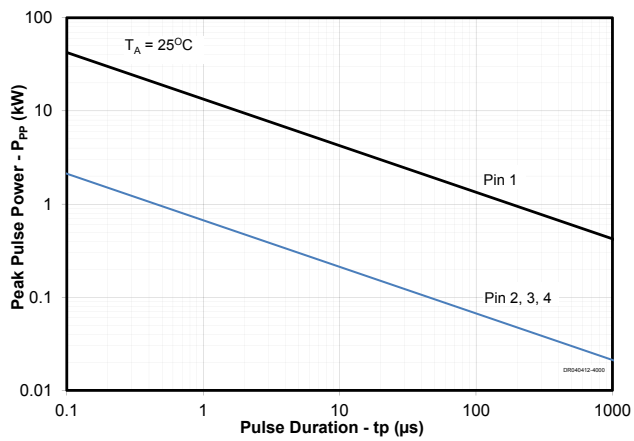
(1): Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane

(2): Transmission Line Pulse Test (TLP) Settings: $t_p = 100\text{ns}$, $t_r = 0.2\text{ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70\text{ns}$ to $t_2 = 90\text{ns}$

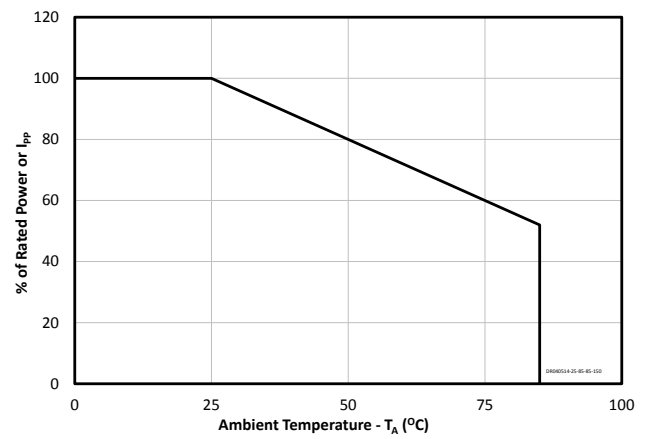
(3): Dynamic resistance calculated from $I_{TLP} = 4\text{A}$ to $I_{TLP} = 16\text{A}$

Typical Characteristics

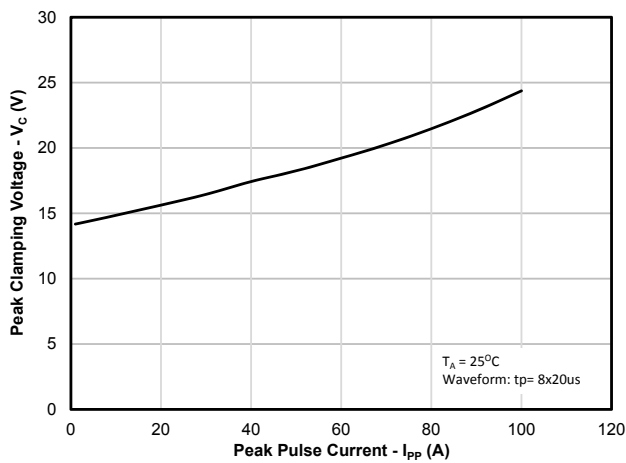
Non-Repetitive Peak Pulse Power vs. Pulse Time



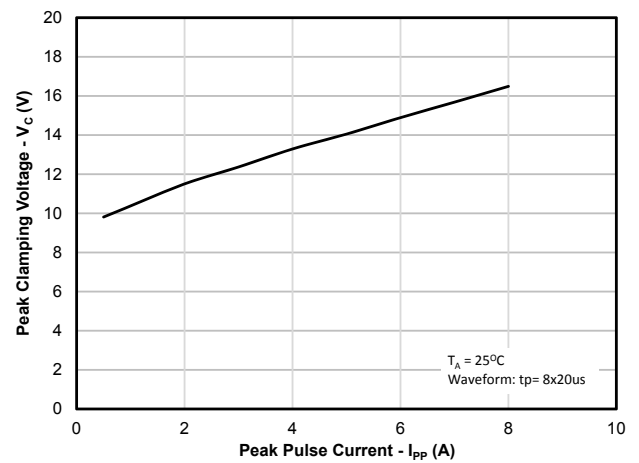
Pulse Derating Curve vs. Temperature



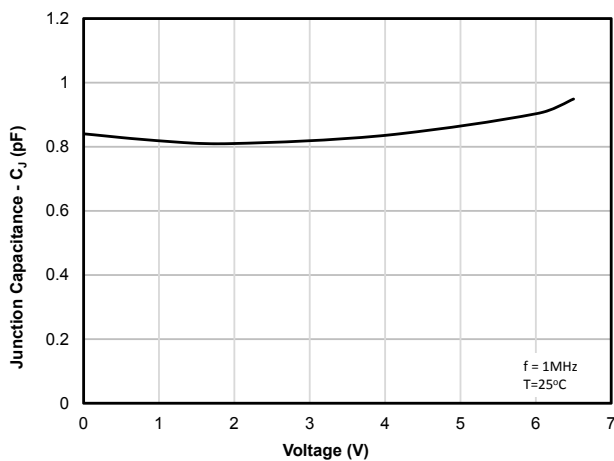
Clamping Voltage vs. Peak Pulse Current - Pin 1



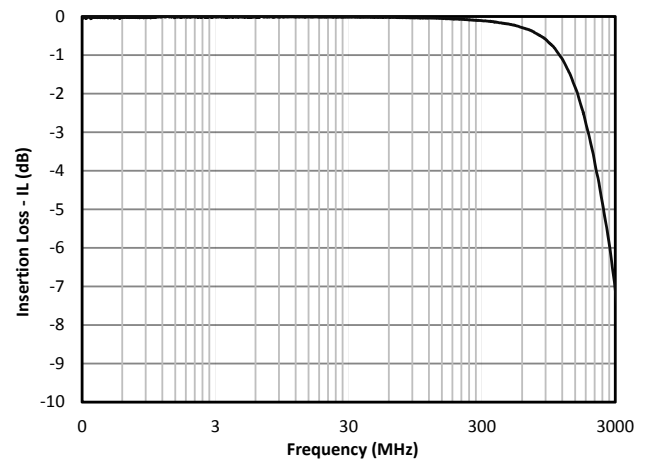
Clamping Voltage vs. Peak Pulse Current - Pin 2, 3, 4



Capacitance vs. Reverse Voltage - Pin 2, 3, 4

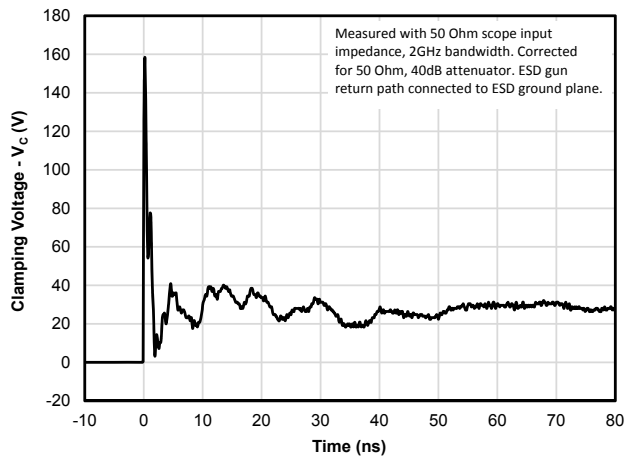


Insertion Loss - S21 (dB) - Pin 2, 3, 4

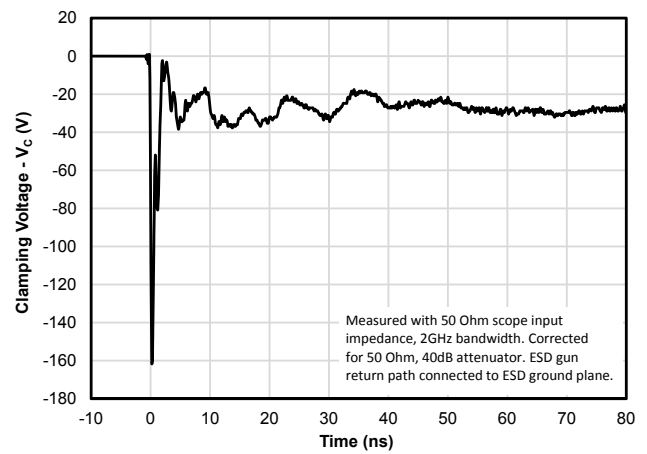


Typical Characteristics (Continued)

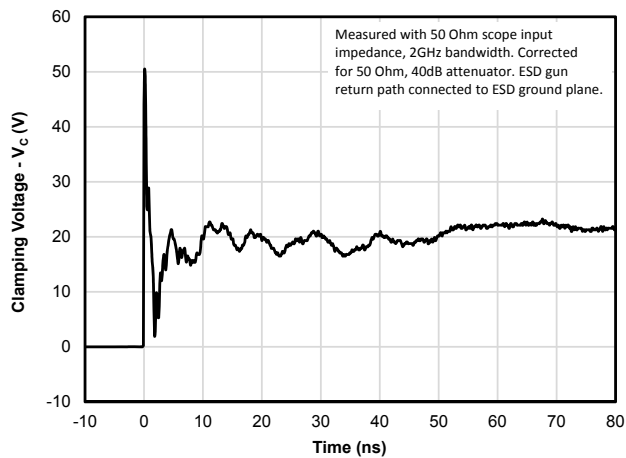
ESD Clamping (+8kV Contact per IEC 61000-4-2) - Pin 2, 3, 4



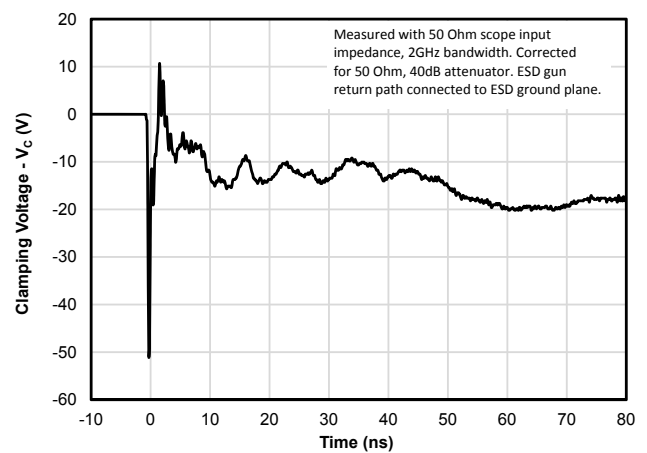
ESD Clamping (-8kV Contact per IEC 61000-4-2) - Pin 2, 3, 4



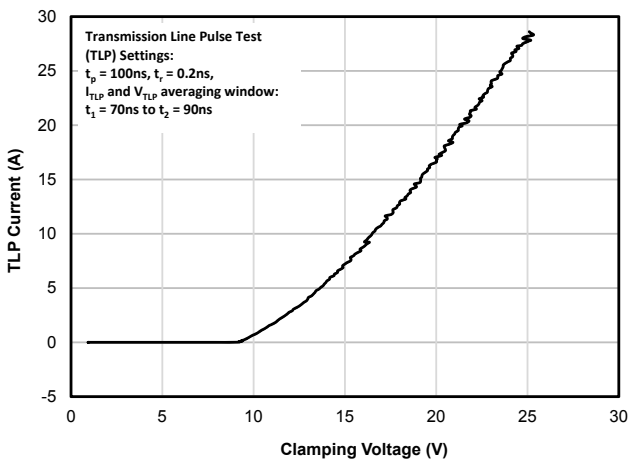
ESD Clamping (+8kV Contact per IEC 61000-4-2) - Pin 1



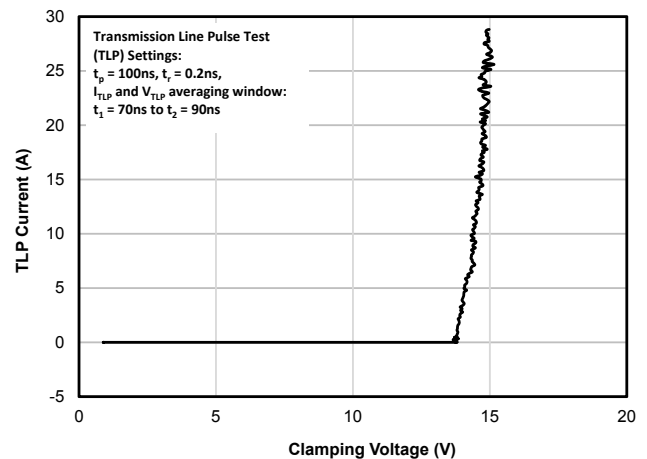
ESD Clamping (-8kV Contact per IEC 61000-4-2) - Pin 1



TLP Characteristic - Pin 2, 3, 4

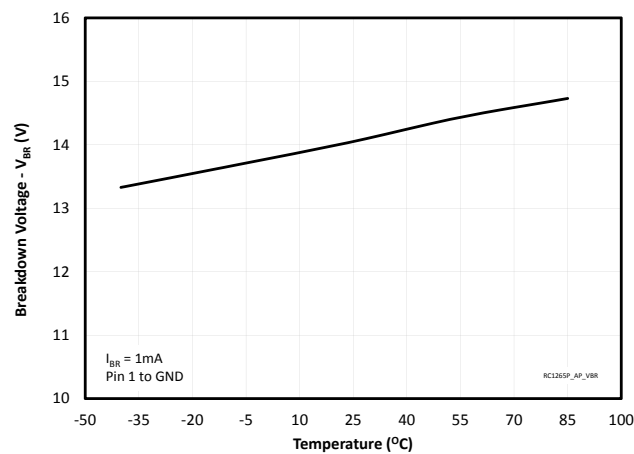


TLP Characteristic - Pin 1

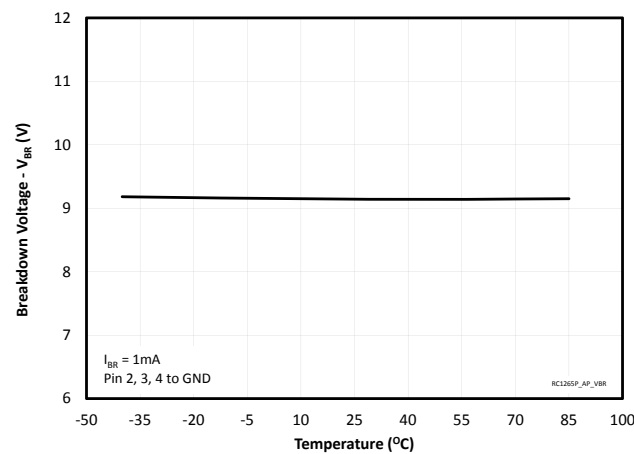


Typical Characteristics (Continued)

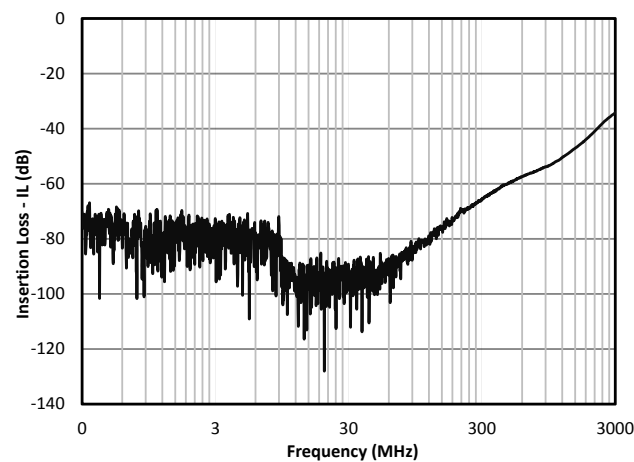
VBR vs. Temperature - Pin 1



VBR vs. Temperature - Pin 2, 3, 4



Analog Crosstalk - Pin 2, 3, 4



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the aperture size, a solder paste with Type 3 or smaller particles are recommended.

Recommended Mounting Pattern

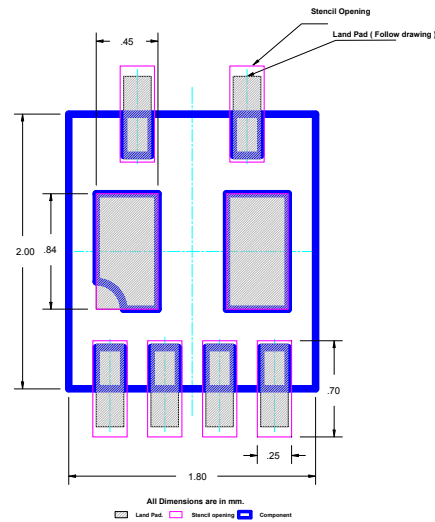
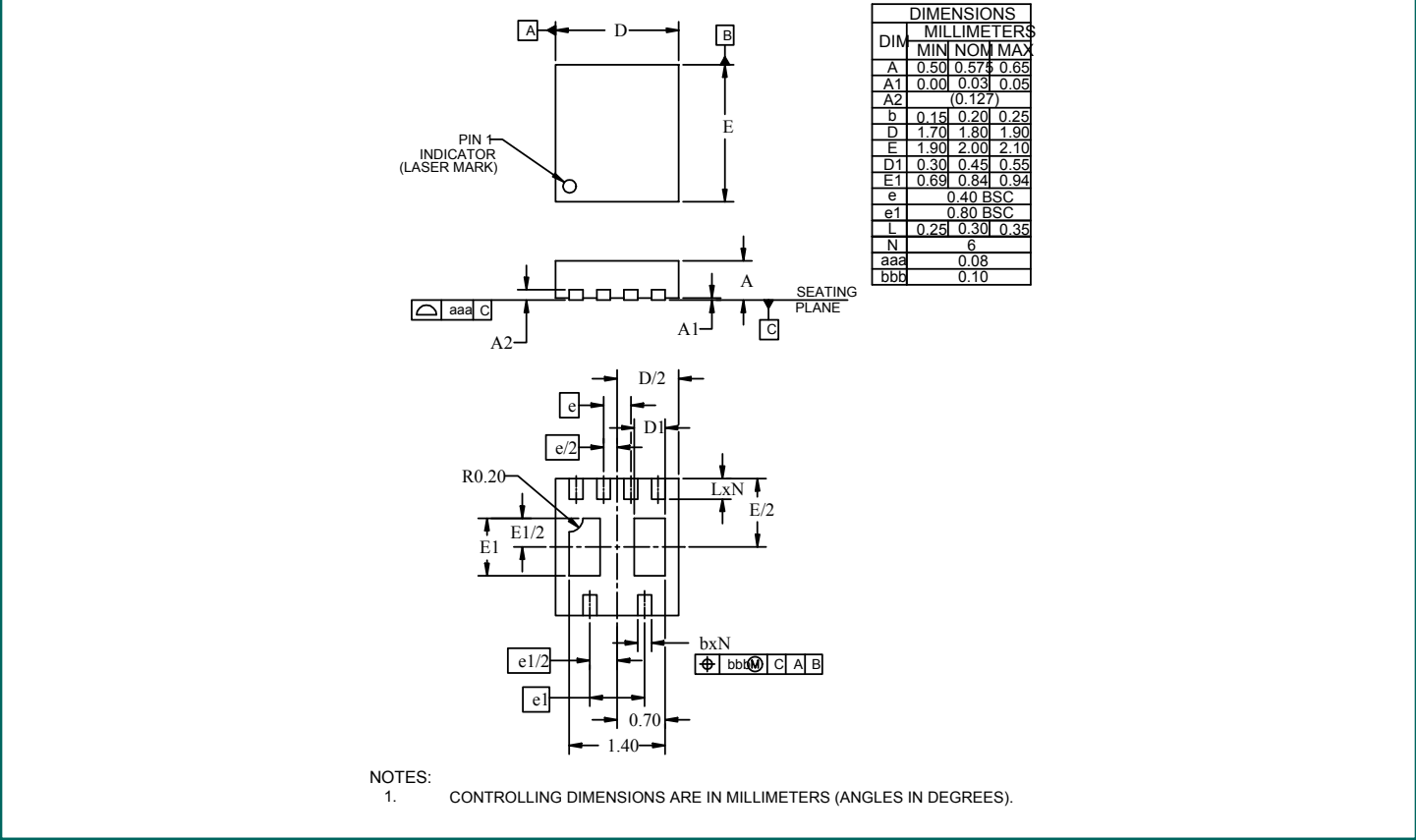
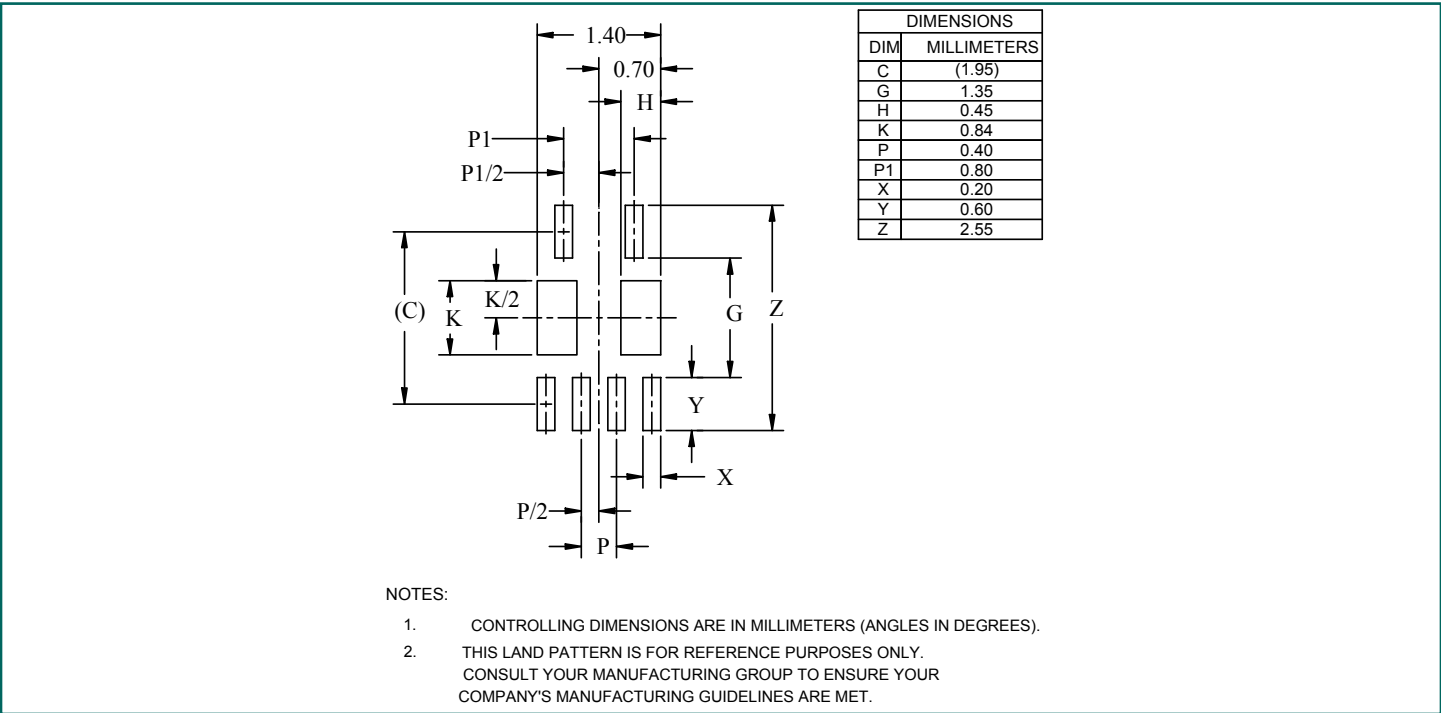


Table 1 - Recommended Assembly Guidelines	
Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 3 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

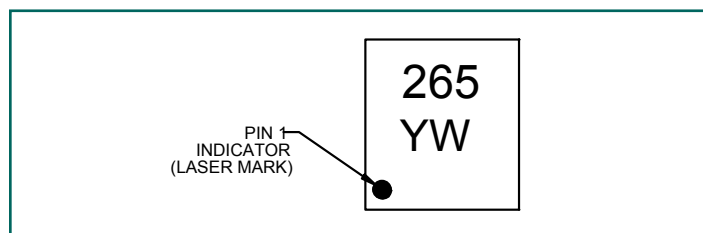
Outline Drawing - SLP2018P6



Land Pattern - SLP2018P6

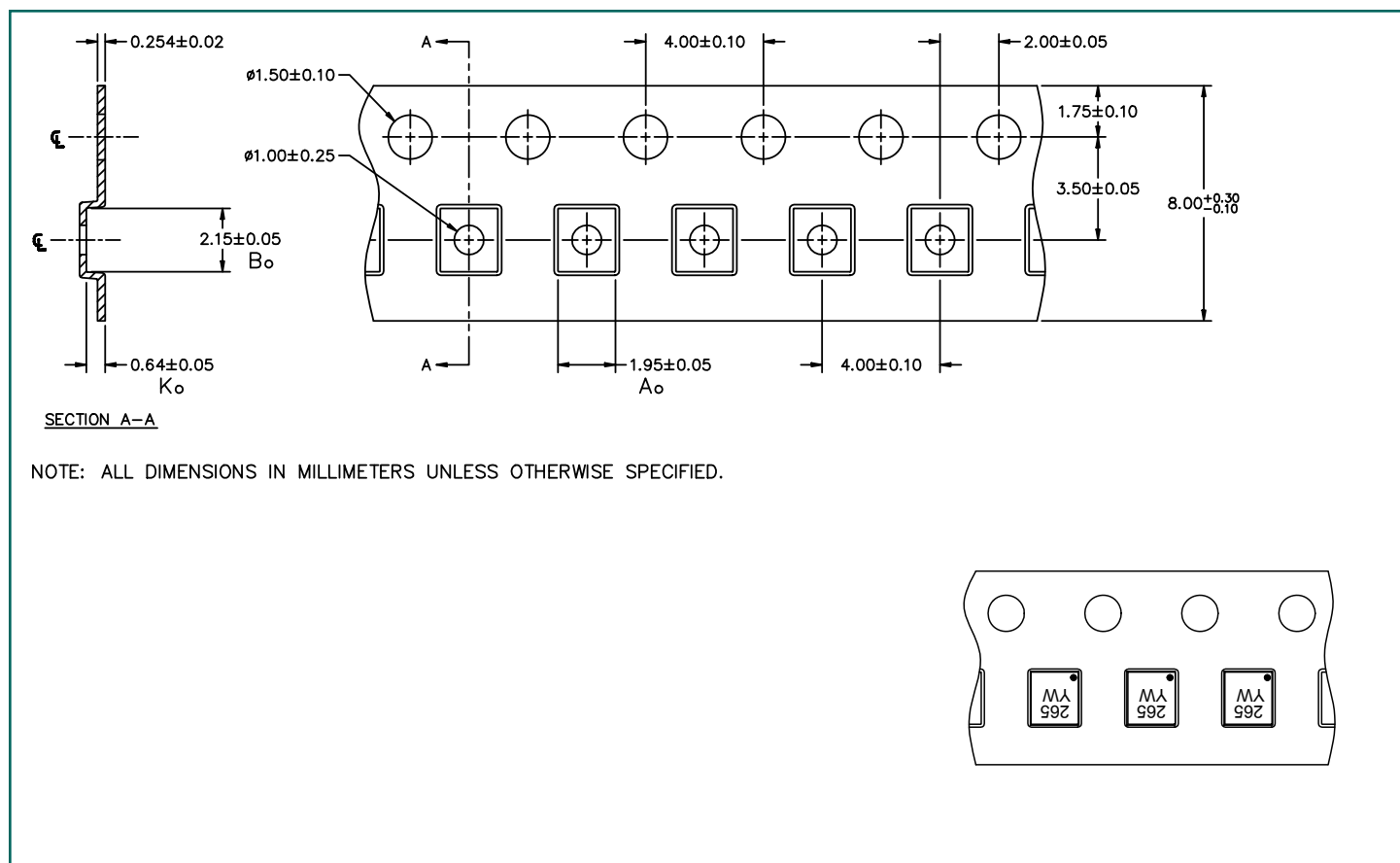


Marking Code



Notes: YW = Date Code

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp1265P.TGT	10000	13 Inch
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