

2ED314xMC12L (2ED-X3 Compact)

Dual channel isolated gate driver IC with dead-time control

Features

- Dual-channel isolated gate driver
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to 6.5 A typical peak output current
- 40 ns propagation delay with 6 ns channel-to-channel delay mismatch (skew)
- 35 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 200 kV/μs
- Active shutdown and short circuit clamping
- Galvanically isolated coreless transformer gate driver
- 3.3 V and 5 V input supply voltage
- 8 mm input-to-output and 3.3 mm channel-to-channel creepage and clearance
- Safety certification
 - UL 1577 (pending) with $V_{ISO,test} = 6840$ V (rms) for 1 s, $V_{ISO} = 5700$ V (rms) for 60 s
 - Reinforced insulation according to IEC 60747-17 (planned) with $V_{IORM} = 1767$ V (peak)



Potential applications

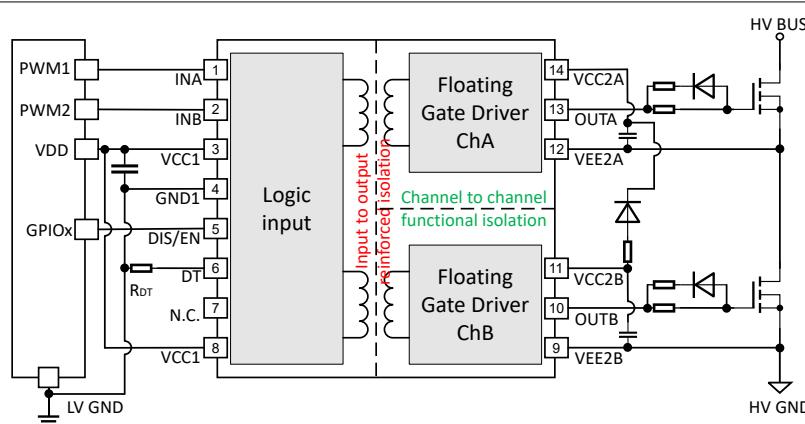
- EV charging
- Energy storage systems
- Solar inverters
- Server and telecom switched mode power supplies (SMPS)
- UPS-systems
- AC and brushless DC motor drives
- Commercial air-conditioning (CAC)
- High voltage DC-DC converter and DC-AC inverter

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The EiceDRIVER™ 2ED314xMC12L is a family of dual-channel isolated gate driver ICs, designed to drive Si, SiC and IGBT power switches. All products are available in a 14-pin DSO package with 8 mm input-to-output creepage and provide reinforced isolation. All variants offer dead-time control (DTC) functionality and independent channel operation. This allows the operation as dual-channel low-side driver, dual-channel high-side driver or half-bridge gate driver with a configurable dead-time. With excellent common-mode transient immunity (CMTI), low part-to-part propagation delay mismatch and fast signal propagation, the products are best suited for use in fast-switching applications.



Typical application diagram using bootstrap biasing

Table 1 Ordering information

Product type	Typical UVLO (V_{UVLOL2}/V_{UVLOH2})	Typical output current source/sink	Functionality	Certification (pending/planned)	Package marking
2ED3140MC12L	8.5 V / 9.3 V	6 A / 6.5 A	DISABLE	UL 1577, IEC 60747-17	3140MC12
2ED3141MC12L	11 V / 12 V	6 A / 6.5 A	DISABLE	UL 1577, IEC 60747-17	3141MC12
2ED3142MC12L	12.5 V / 13.6 V	6 A / 6.5 A	DISABLE	UL 1577, IEC 60747-17	3142MC12
2ED3143MC12L	14.7 V / 16 V	6 A / 6.5 A	DISABLE	UL 1577, IEC 60747-17	3143MC12
2ED3144MC12L	8.5 V / 9.3 V	6 A / 6.5 A	ENABLE	UL 1577, IEC 60747-17	3144MC12
2ED3145MC12L	11 V / 12 V	6 A / 6.5 A	ENABLE	UL 1577, IEC 60747-17	3145MC12
2ED3146MC12L	12.5 V / 13.6 V	6 A / 6.5 A	ENABLE	UL 1577, IEC 60747-17	3146MC12
2ED3147MC12L	14.7 V / 16 V	6 A / 6.5 A	ENABLE	UL 1577, IEC 60747-17	3147MC12

Table 2 Related evaluation boards

Board name	Gate driver	Power transistor	Short description
EVAL-2ED3146MC12L-SIC	2ED3146MC12L	IMZA120R020M1H	Half bridge board with the 2ED3146MC12L gate driver and paired with CoolSiC™ in PG-T0-247-4 package

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1 Block diagram reference

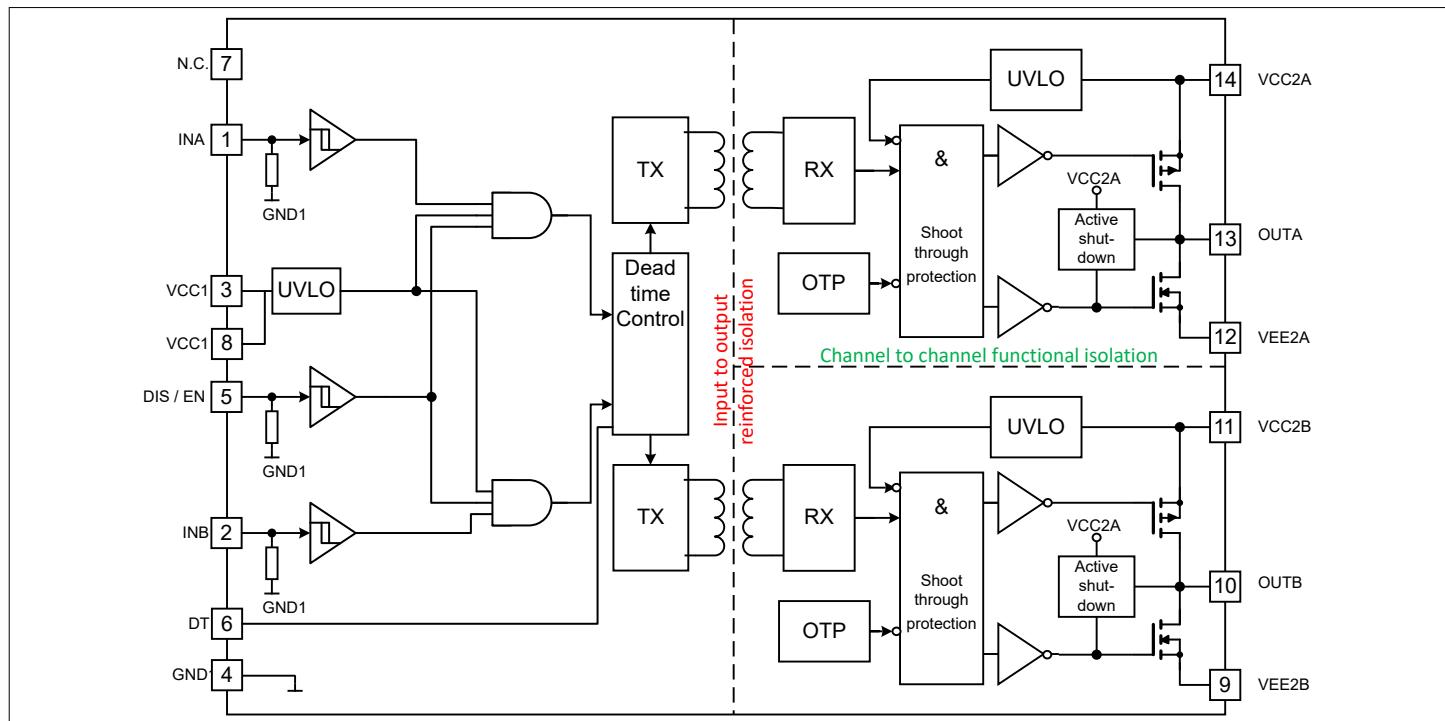


Figure 2 Block diagram

2 Pin configuration and description

Pin configuration

Table 3 Pin configuration

Pin No.	Name	Function
1	INA	Input signal channel A
2	INB	Input signal channel B
3,8	VCC1	Positive power supply input side
4	GND1	Ground reference input side
5	DIS	DISABLE input channel A and B (low active)
5	EN	ENABLE input channel A and B (high active)
6	DT	Dead-time control
7	N.C.	No internal connection
9	VEE2B	Ground reference output channel B
10	OUTB	Gate driver output channel B
11	VCC2B	Positive power supply output channel B
12	VEE2A	Ground reference output channel A
13	OUTA	Gate driver output channel A
14	VCC2A	Positive power supply output channel A

2 Pin configuration and description

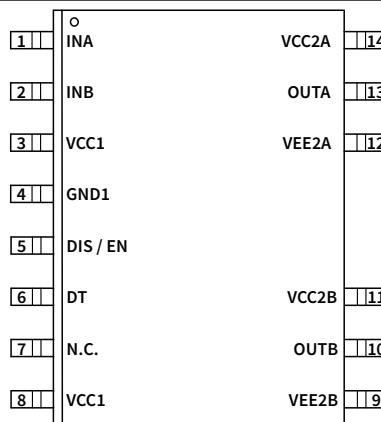


Figure 3 DSO-14-71 (top view)

Pin description

- **VCC1:** Input supply voltage. Connect to 3.3 V or 5 V and decouple with a capacitor to *GND1*. Use a low ESR and ESL capacitor placed as close as possible to the device
- **GND1:** Input ground. All the input side signals, *VCC1*, *IN+* and *IN-* are referenced to this ground
- **INA:** Non-inverted control signal for output channel A. An internal filter provides robustness against noise at *INA*
- **INB:** Non-inverted control signal for output channel B. An internal filter provides robustness against noise at *INB*
- **DIS (2ED3140-2ED3143):** Disable input pin. When at logic high, it switches *OUTA* and *OUTB* off, at logic low the output levels are controlled by their individual input pins
- **EN (2ED3144-2ED3147):** Enable input pin. When at low, it switches *OUTA* and *OUTB* off, at logic high the output levels are controlled by their individual input pins
- **DT:** Dead-time control. The feature is active if the pin is connected to *GND1* via a resistor, inactive if tied to *VCC1* or left open. It is not recommended to connect capacitive loads to this pin. The configured dead-time should be reasonably smaller than the minimum pulse width
- **VCC2A:** Channel A positive power supply rail. Connect a decoupling capacitor from this pin to *VEE2A*. Use low ESR and ESL capacitors placed as close as possible to the device
- **VEE2A:** Channel A output ground. *VCC2A* and *OUTA* are referenced to this ground. In case of a bipolar supply (positive and negative voltage referred to the IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- **OUTA:** Channel A output pin used to charge and discharge the gate of the external transistor (IGBT or MOSFET). During the on-state this output is connected to *VCC2A* and during the off-state to *VEE2A*. This output is controlled by *INA* and will be turned off by an UVLO or OTP event
- **VCC2B:** Channel B positive power supply rail. Connect a decoupling capacitor from this pin to *VEE2B*. Use low ESR and ESL capacitors placed as close as possible to the device
- **VEE2B:** Channel B output ground. *VCC2B* and *OUTB* are referenced to this ground. In case of a bipolar supply (positive and negative voltage referred to the IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- **OUTB:** Channel B output pin used to charge and discharge the gate of the external transistor (IGBT or MOSFET). During the on-state this output is connected to *VCC2A* and during the off-state to *VEE2B*. This output is controlled by *INB* and will be turned off by an UVLO or OTP event

3 Electrical characteristics and parameters

3.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	-0.3		17	V	$V_{VCC1} - V_{GND1}$
Power supply output side voltage	V_{VCC2}	-0.3		35	V	$V_{VCC2A} - V_{VEE2A}, V_{VCC2B} - V_{VEE2B}$
Gate driver output voltage	V_{OUT}	$V_{VEE2A/B} - 0.3$		$V_{VCC2A/B} + 0.3$	V	
Logic input voltages (INA, INB, DIS/EN)	V_{IN}	-0.3		17	V	
Dynamic logic input voltages (INA, INB, DIS/EN)	V_{INdyn}	-5		17	V	¹⁾ $t_{IN} < 50$ ns
Dead time control (DT)	V_{DT}	-0.3		$V_{VCC1} + 0.3$	V	
Input to output offset voltage	V_{OFFSET}			2300	V	²⁾ $V_{OFFSET} = V_{VEE2A/B} - V_{GND1} $
ESD robustness - human body model	$ V_{ESD,HBM} $			2	kV	³⁾
ESD robustness - charged device model	ESD,CDM			TC500		⁴⁾
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{Stg}	-65		150	°C	

PG-DSO-14-71 Thermal characteristics

Power dissipation (input side)	$P_{D,IN}$			66	mW	⁵⁾ $T_A = 85$ °C
Power dissipation (output side)	$P_{D,OUT}$			900	mW	⁶⁾ ⁷⁾ $T_A = 85$ °C
Thermal resistance junction-case (top)	R_{thJC}		46		K/W	
Thermal resistance junction ambient	R_{thJA25}		69		K/W	⁸⁾ $T_A = 25$ °C
Thermal resistance junction ambient	R_{thJA85}		65		K/W	⁸⁾ $T_A = 85$ °C
Thermal resistance junction board	R_{thJB}		27		K/W	⁹⁾
Characterization parameter junction-top	Ψ_{thJT}		12		K/W	¹⁰⁾
Characterization parameter junction-board	Ψ_{thJB25}		23		K/W	¹⁰⁾

1) Parameter is not subject to production test - verified by design/characterization

2) for functional operation only

3 Electrical characteristics and parameters

3) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

4) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

5) *IC input-side power dissipation is derated linearly with 14 mW/°C above 145 °C*

6) *IC output-side power dissipation is derated linearly with 14 mW/°C above 85 °C*

7) For both channels in total

8) 2s2p high-K board, as specified in JESD51-7, in an environment described in JESD51-2

9) 2s2p high-K board, as specified in JESD51-7, in an environment described in JESD51-8 with a ring cold plate fixture to control the PCB temperature

10) Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7)

3.2 Recommended operating conditions

Table 5 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	3		16.5	V	$V_{VCC1} - V_{GND1}$
Power supply output side voltage	V_{VCC2}	V_{UVLOL2}		32	V	¹⁾ $V_{VCC2A/B} - V_{VEE2A/B}$
Logic input voltages (INA, INB, DIS/EN)	V_{IN}	0		5.5	V	
Dead time control (DT)	V_{DT}	0		V_{VCC1}	V	
Switching frequency	f_{SW}			1	MHz	max P_D applies
Ambient temperature	T_A	-40		125	°C	-
Junction temperature	T_J	-40		150	°C	-

1) $V_{VCC2A/B} - V_{VEE2A/B}$ must first rise above V_{UVLOH2} .

3.3 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are tested in production at $T_A = 25$ °C. Typical values represent the median values measured at $V_{VCC1} = 3.3$ V, $V_{VCC2A/B} - V_{VEE2A/B} = 15$ V, and $T_A = 25$ °C. Minimum and maximum values in characteristics are verified by characterization/design. This is valid for all electrical characteristics unless specified otherwise.

3.3.1 Power supply

Table 6 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}		2.85	3	V	$V_{VCC1} - V_{GND1}$
UVLO threshold input side (off)	V_{UVLOL1}	2.55	2.7		V	$V_{VCC1} - V_{GND1}$
UVLO hysteresis input side	V_{HYS1}	0.1	0.15	0.2	V	$V_{UVLOH1} - V_{UVLOL1}$
Quiescent current input side	I_{Q1}		1.67	2.12	mA	INA = Low, INB = Low, DT = VCC1

(table continues...)

3 Electrical characteristics and parameters

Table 6 (continued) Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Quiescent current output side, ON state	$I_{Q2,ON}$			1.35	mA	¹⁾ INA = High, INB = Low or INA = Low, INB = High, $V_{VCC2A/B} - V_{VEE2A/B} < 18$ V
Quiescent current output side, OFF state	$I_{Q2,OFF}$			1.0	mA	¹⁾ INA = Low, INB = Low, $V_{VCC2A/B} - V_{VEE2A/B} < 18$ V

2ED3140 / 2ED3144

UVLO threshold output side (on)	V_{UVLOH2}		9.3	9.6	V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO threshold output side (off)	V_{UVLOL2}	8.25	8.55		V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO hysteresis output side	V_{HYS2}		0.75		V	$V_{UVLOH2} - V_{UVLOL2}$

2ED3141 / 2ED3145

UVLO threshold output side (on)	V_{UVLOH2}		12	12.35	V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO threshold output side (off)	V_{UVLOL2}	10.7	11.05		V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO hysteresis output side	V_{HYS2}		0.95		V	$V_{UVLOH2} - V_{UVLOL2}$

2ED3142 / 2ED3146

UVLO threshold output side (on)	V_{UVLOH2}		13.6	14	V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO threshold output side (off)	V_{UVLOL2}	12.15	12.55		V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO hysteresis output side	V_{HYS2}		1.05		V	$V_{UVLOH2} - V_{UVLOL2}$

2ED3143 / 2ED3147

UVLO threshold output side (on)	V_{UVLOH2}		16	16.45	V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO threshold output side (off)	V_{UVLOL2}	14.30	14.75		V	$V_{VCC2A/B} - V_{VEE2A/B}$
UVLO hysteresis output side	V_{HYS2}		1.25		V	$V_{UVLOH2} - V_{UVLOL2}$

1) Per channel

3.3.2 Logic input**Table 7 Logic input**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INA,INB, DIS / EN low input threshold voltage	$V_{IN,L}$	0.9	1.2	1.6	V	
INA, INB, DIS / EN high input threshold voltage	$V_{IN,H}$	1.73	2.0	2.36	V	
INA, INB, DIS / EN low/high hysteresis	$V_{IN,HYS}$	0.38	0.8	1.2	V	
INA, INB, DIS / EN input current	I_{IN}		22	27	μ A	$V_{VCC1} = 3.3$ V; $V_{IN} \leq V_{VCC1}$
INA, INB, DIS / EN pull down resistor	$R_{IN,PD}$		150		k Ω	-

3.3.3 Gate driver

Table 8 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	3.5	6		A	¹⁾ $V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, INA/B = High, $C_L = 100 \text{ nF}$
High level output on resistance	$R_{DSON,H}$	0.3	0.9	2.2	Ω	$I_{OUTH} = 0.1 \text{ A}$
Low level output peak current	I_{OUTL}	3.5	6.5		A	¹⁾ $V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, INA/B = Low, $C_L = 100 \text{ nF}$
Low level output on resistance	$R_{DSON,L}$	0.2	0.5	1.1	Ω	$I_{OUTL} = 0.1 \text{ A}$
Clamp voltage between OUTA/B and VCC2A/B	V_{CLP_OUTH}			1.0	V	$V_{OUTA/B} - V_{VCC2A/B}$, $I_{OUTA/B} = -500 \text{ mA}$, $t < 10 \mu\text{s}$, INA/B = High
Clamp voltage between VEE2A/B and OUTA/B	V_{CLP_OUTL}			1.0	V	$V_{VEE2A/B} - V_{OUTA/B}$, $I_{OUTA/B} = -500 \text{ mA}$, $t < 10 \mu\text{s}$, INA/B = Low

1) Parameter is not subject to production test - verified by design/characterization

3.3.4 Dead-time and shoot-through protection

Table 9 Dead-time and shoot-through protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dead-time	t_{DT}	85	100	115	ns	¹⁾ $R_{DT} = 10 \text{ k}\Omega$
Dead-time	t_{DT}	255	300	345	ns	¹⁾ $R_{DT} = 30 \text{ k}\Omega$
Dead-time	t_{DT}	800	950	1100	ns	^{1) 2)} $R_{DT} = 100 \text{ k}\Omega$
Dead-time to resistor value ratio	K_{DT_R}	8	10	12	ns/ $\text{k}\Omega$	$1.2\text{k}\Omega \leq R_{DT} \leq 100\text{k}\Omega$; $t_{DT} = K_{DT_R} \times R_{DT} + M_{DT_R}$
Dead-time offset	M_{DT_R}		0		ns	$t_{DT} = K_{DT_R} \times R_{DT} + M_{DT_R}$
Dead-time resistor range	R_{DT}	1.2		100	$\text{k}\Omega$	
Ch-to-ch dead-time matching	$\Delta t_{DT,Ch-Ch}$			10	ns	$R_{DT} = 10 \text{ k}\Omega$; $\Delta t_{DT,Ch-Ch} = t_{DT,A-B} - t_{DT,B-A} $
Ch-to-ch dead-time matching	$\Delta t_{DT,Ch-Ch}$			14	ns	$R_{DT} = 30 \text{ k}\Omega$; $\Delta t_{DT,Ch-Ch} = t_{DT,A-B} - t_{DT,B-A} $
Ch-to-ch dead-time matching	$\Delta t_{DT,Ch-Ch}$			40	ns	²⁾ $R_{DT} = 100 \text{ k}\Omega$; $\Delta t_{DT,Ch-Ch} = t_{DT,A-B} - t_{DT,B-A} $
Part-to-part dead-time matching	$\Delta t_{DT,P-P}$			20	ns	$R_{DT} = 10 \text{ k}\Omega$
Part-to-part dead-time matching	$\Delta t_{DT,P-P}$			55	ns	$R_{DT} = 30 \text{ k}\Omega$
Part-to-part dead-time matching	$\Delta t_{DT,P-P}$			105	ns	²⁾ $R_{DT} = 100 \text{ k}\Omega$

1) Input filter time not included

2) Parameter is not subject to production test - verified by design/characterization

3.3.5 Dynamic characteristics

Table 10 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	30	39	50	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, $C_L = 100 \text{ pF}$, valid for INA, INB and DIS/EN, $V_{DT} = V_{VCC1}$
Input to output propagation delay OFF	t_{PDOFF}	30	39	50	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, $C_L = 100 \text{ pF}$, valid for INA, INB and DIS/EN, $V_{DT} = V_{VCC1}$
Input to output propagation delay distortion	$ t_{PDISTO} $		0	5	ns	¹⁾ $ t_{PDOFF} - t_{PDON} $
Input to output turn-on, part to part propagation delay variation	$\Delta t_{PDON,P-P}$			6	ns	¹⁾ $C_L = 100 \text{ pF}$, $V_{DT} = V_{VCC1}$
Input to output turn-off, part to part propagation delay variation	$\Delta t_{PDOFF,P-P}$			8	ns	¹⁾ $C_L = 100 \text{ pF}$, $V_{DT} = V_{VCC1}$
Input to output turn-on, channel to channel propagation delay variation	$\Delta t_{PDON,Ch-Ch}$			5	ns	$V_{DT} = V_{VCC1}$; $\Delta t_{PDON,Ch-Ch} = t_{PDON,A} - t_{PDON,B} $
Input to output turn-off, channel to channel propagation delay variation	$\Delta t_{PDOFF,Ch-Ch}$			5	ns	$V_{DT} = V_{VCC1}$; $\Delta t_{PDOFF,Ch-Ch} = t_{PDOFF,A} - t_{PDOFF,B} $
Input pulse suppression time (filter time)	t_{INFLT}	10	17	25	ns	²⁾
Dead-time distortion	$ t_{DTD} $			5	ns	$t_{PDOFF,A} - t_{PDON,B}$ or $t_{PDOFF,B} - t_{PDON,A}$; $V_{DT} = V_{VCC1}$
Rise time	t_{RISE}			20	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, $C_L = 1 \text{ nF}$, valid for all parts, except 2ED3143 and 2ED3147
Rise time	t_{RISE}			20	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 18 \text{ V}$, $C_L = 1 \text{ nF}$, valid for 2ED3143 and 2ED3147
Fall time	t_{FALL}			20	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 15 \text{ V}$, $C_L = 1 \text{ nF}$, valid for all parts, except 2ED3143 and 2ED3147
Fall time	t_{FALL}			20	ns	$V_{VCC2A/B} - V_{VEE2A/B} = 18 \text{ V}$, $C_L = 1 \text{ nF}$, valid for 2ED3143 and 2ED3147
Input-side start-up time	$t_{START,VCC1}$		3.5	5	μs	³⁾ INA/B = High, DT = VCC1, DIS = low / EN = high, $V_{VCC2A/B} > V_{UVLOH2}$, $C_L = 100\text{pF}$
Input-side deactivation time	$t_{STOP,VCC1}$	600	750		ns	³⁾ INA/B = High, DT = VCC1, DIS = low / EN = high, $V_{VCC2A/B} > V_{UVLOH2}$, $C_L = 100\text{pF}$

(table continues...)

3 Electrical characteristics and parameters

Table 10 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output-side start-up time	$t_{\text{START},\text{VCC2}}$		5	10	μs	³⁾ INA/B = High, DIS = Low / EN = High, DT = VCC1, $V_{\text{VCC1}} > V_{\text{UVLOH1}}$, $C_L = 100\text{pF}$
Output-side deactivation time	$t_{\text{STOP},\text{VCC2}}$	0.5		1	μs	³⁾ INA/B = High, DIS = Low / EN = High, DT = VCC1, $V_{\text{VCC1}} > V_{\text{UVLOH1}}$, $C_L = 100\text{pF}$
High-level common-mode transient immunity	$ \text{CM}_H $	200			kV/μs	³⁾ $V_{\text{CM}} = 1500\text{ V}$; INA/B tied to VCC1, DT = VCC1
Low-level common-mode transient immunity	$ \text{CML} $	200			kV/μs	³⁾ $V_{\text{CM}} = 1500\text{ V}$; INA/B tied to GND1, DT = VCC1
Dynamic common-mode transient immunity	$ \text{CMDYN} $	200			kV/μs	³⁾ $V_{\text{CM}} = 1500\text{ V}$; INA/B = 10 MHz square wave, DT = VCC1

1) value at same ambient and operating conditions.

2) Valid for INA, INB and DIS/EN, $V_{\text{DT}} = V_{\text{VCC1}}$. The pulse is generated outside the DT window; shorter pulses will not propagate to the output.

3) Parameter is not subject to production test - verified by design/characterization

3.3.6 Active shut down

Table 11 Active shut down

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	$V_{\text{OUTA/B}} - V_{\text{VEE2A/B}}$, $I_{\text{OUTL}} = 500\text{ mA}$, VCC2A/B open

3.3.7 Overtemperature protection

Table 12 Overtemperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature protection level	T_{OTPOFF}	150	160	175	°C	¹⁾
Overtemperature protection release level	T_{OTPREL}	130	140	150	°C	¹⁾
Overtemperature protection hysteresis	T_{OTPHYS}		20		°C	¹⁾

1) Parameter is not subject to production test - verified by design/characterization

4 Insulation characteristics (IEC 60747-17, UL 1577) for DSO-14-71 package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 13 Insulation specification for DSO-14-71 package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25^\circ\text{C}$ ¹⁾	P_{SI}	66	mW
Maximum output-side power dissipation at $T_A = 25^\circ\text{C}$ ²⁾	P_{SO}	1600	mW
Package specific insulation characteristics			
External clearance	CLR	> 8	mm
Channel-to-channel creepage	$CLR_{\text{Ch-Ch}}$	> 3.3	mm
External creepage	CPG	> 8	mm
Channel-to-channel creepage	$CPG_{\text{Ch-Ch}}$	> 3.3	mm
Comparative tracking index	CTI	> 600	–
Isolation capacitance	C_{IO}	0.9	pF
Reinforced insulation according to IEC 60747-17 (planned)			
Installation classification per EN 60664-1, Table 1			–
for rated mains voltage $\leq 150 \text{ V (rms)}$		I-IV	
for rated mains voltage $\leq 300 \text{ V (rms)}$		I-IV	
for rated mains voltage $\leq 600 \text{ V (rms)}$		I-III	
for rated mains voltage $\leq 1000 \text{ V (rms)}$		I-II	
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Apparent charge, method a	q_{pd}	< 5	pC
$V_{pd(\text{ini}),a} = V_{IOTM}, V_{pd(m)} = 1.6 \times V_{IORM}, t_{\text{ini}} = 1 \text{ min}, t_m = 10 \text{ s}$			
Apparent charge, method b	q_{pd}	< 5	pC
$V_{pd(\text{ini}),b} = V_{IOTM} \times 1.2, V_{pd(m)} = 1.875 \times V_{IORM}, t_{\text{ini}} = 1 \text{ s}, t_m = 1 \text{ s}$			
Isolation resistance at $T_{A,\text{max}}; V_{IO} = 500 \text{ V}_{\text{DC}}, T_A = 125^\circ\text{C}$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at $T_S; V_{IO} = 500 \text{ V}_{\text{DC}}, T_S = 150^\circ\text{C}$	R_{IO_S}	$> 10^9$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1250	V (rms)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced isolation; $V_{\text{TEST}} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577 (pending)			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,\text{TEST}}$	6840	V (rms)

1) IC input-side power dissipation is derated linearly at 14 mW/°C above 145 °C

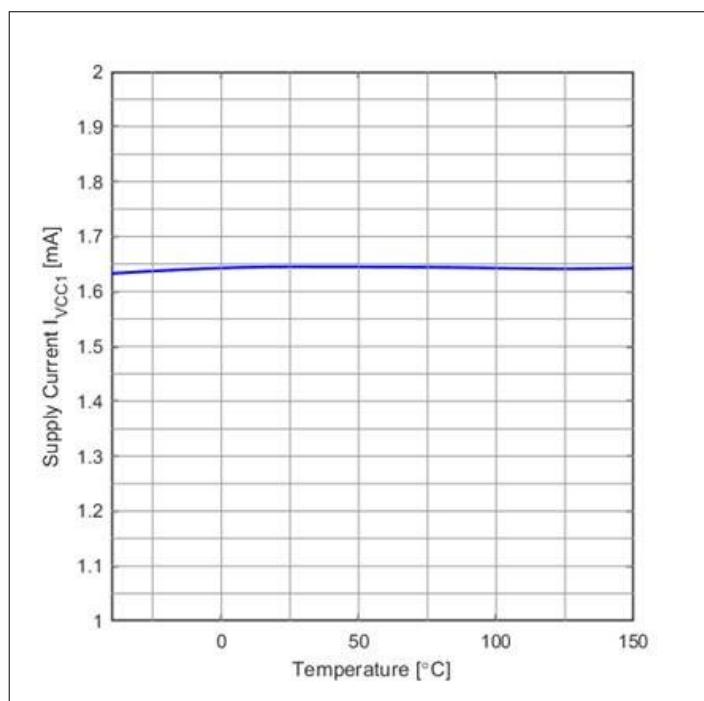
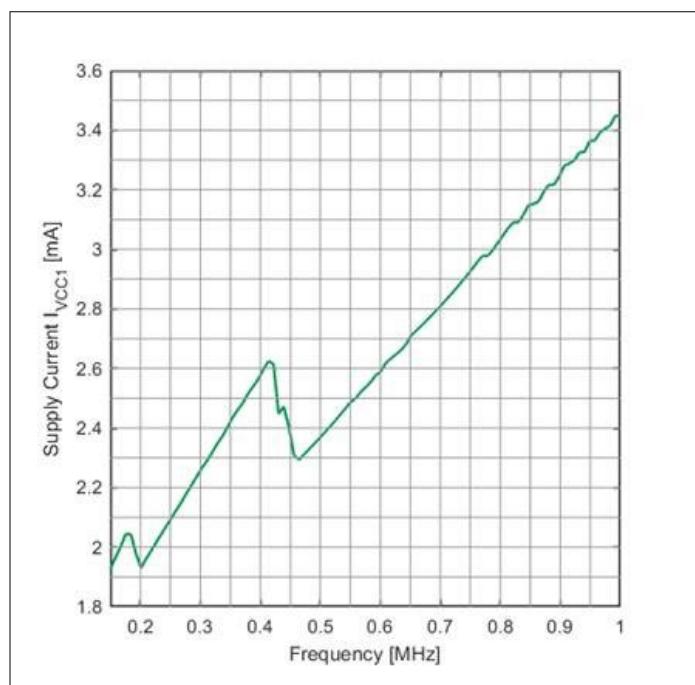
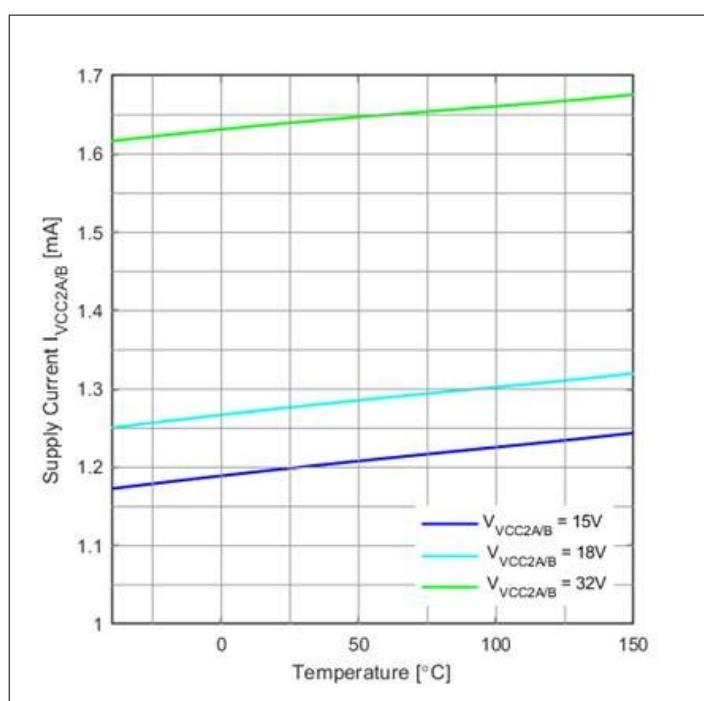
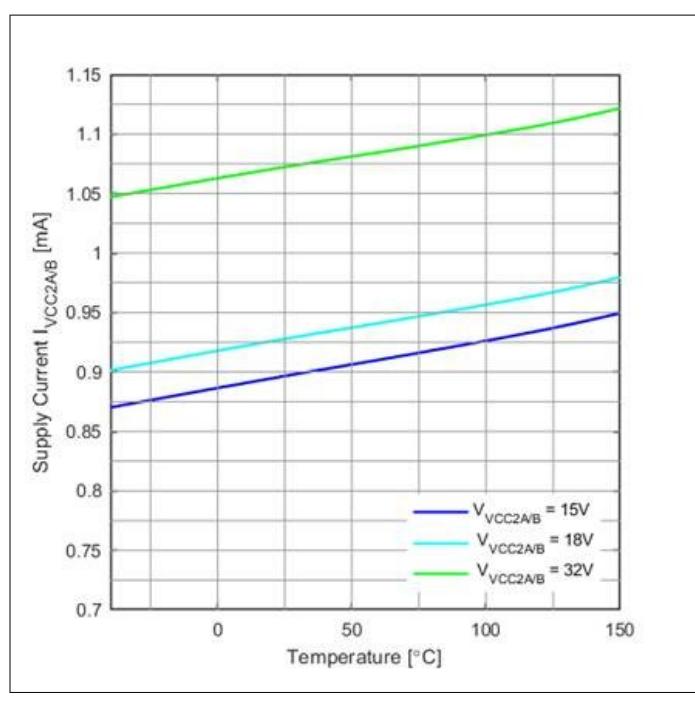
2) IC output-side power dissipation is derated linearly at 12.6 mW/°C above 25 °C

5 Typical characteristics

5 Typical characteristics

Unless otherwise noted, the measurements are done with $V_{VCC1} = 3.3$ V, 100 nF capacitor connected between $VCC1$ and $GND1$, 4.7 μ F capacitor between $VCC2A/B$ and $VEE2A/B$.

Table 14

Figure 4 I_{Q1} vs. temperatureFigure 5 I_{Q1} vs. frequency @ $T_A = 25^\circ\text{C}$ Figure 6 $I_{Q2,ON}$ vs. temperatureFigure 7 $I_{Q2,OFF}$ vs. temperature

(table continues...)

Table 14 (continued)

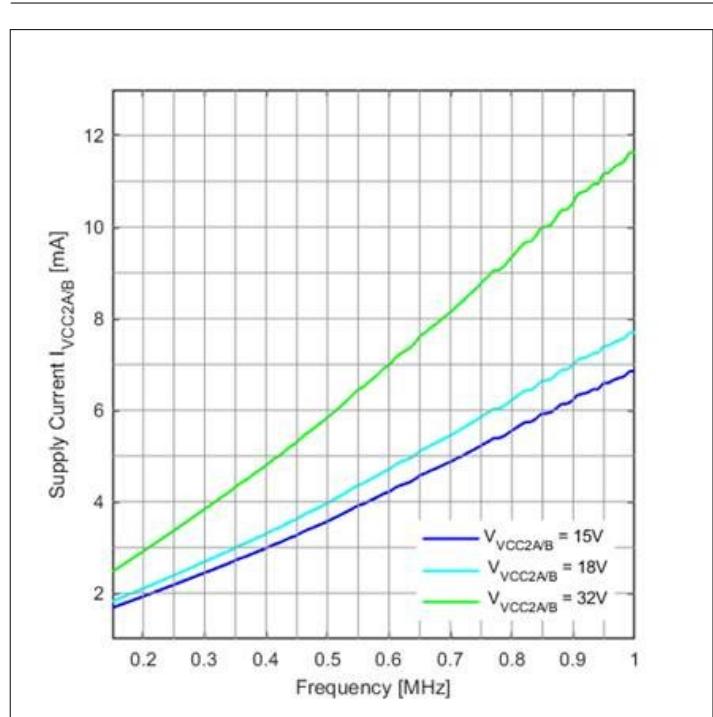


Figure 8 I_{Q2} vs. frequency @ $C_{load} = 100\text{pF}$ & $T_A = 25^\circ\text{C}$

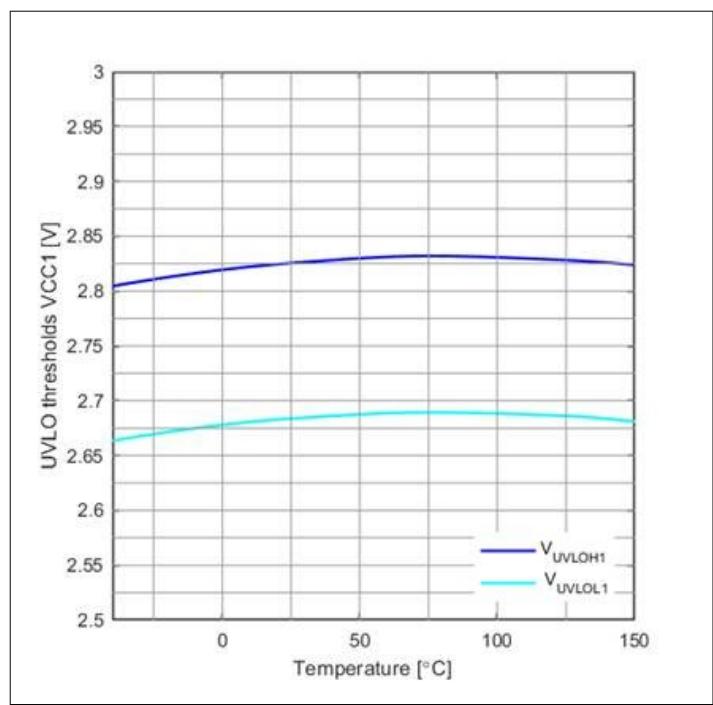


Figure 9 V_{UVLOH1} and V_{UVLOL1} vs. temperature

(table continues...)

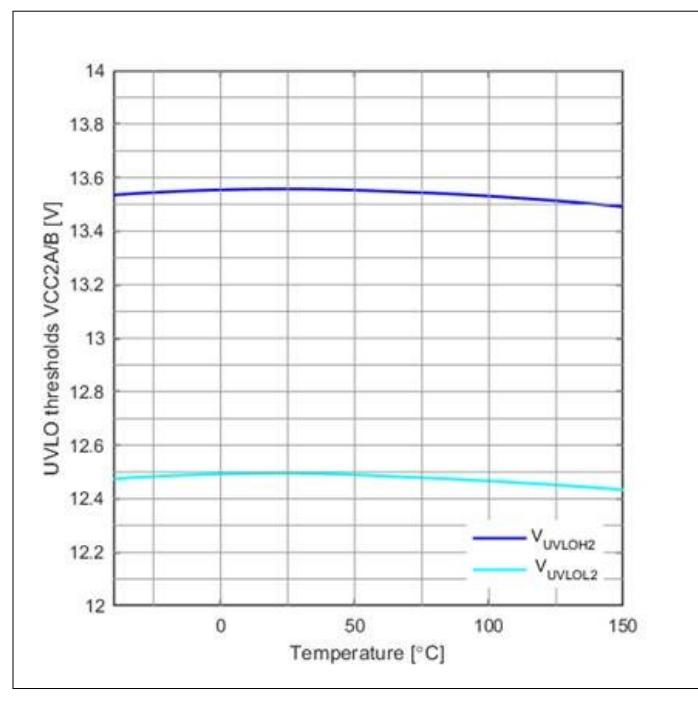


Figure 10 V_{UVLOH2} and V_{UVLOL2} (2ED3146MC12L) vs. temperature

5 Typical characteristics

Table 14 (continued)

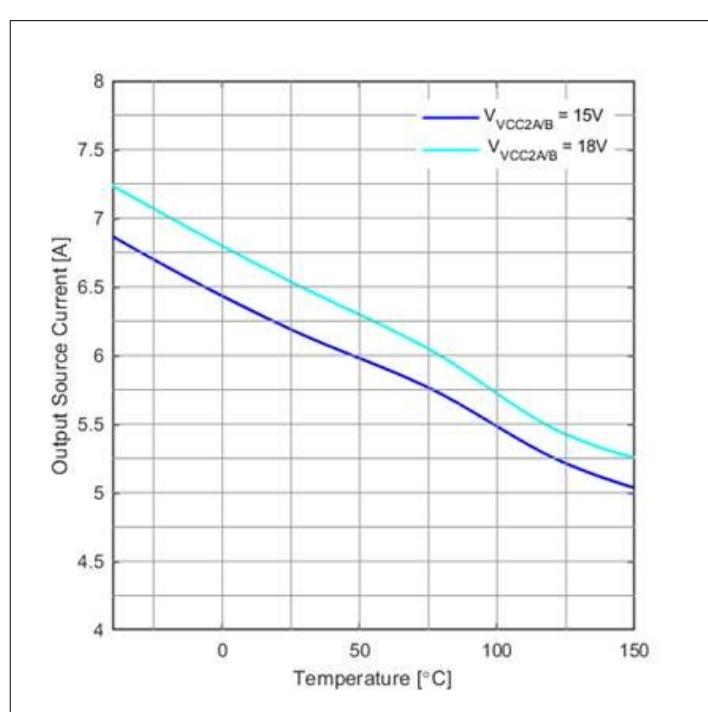


Figure 11 I_{OUTH} vs. temperature

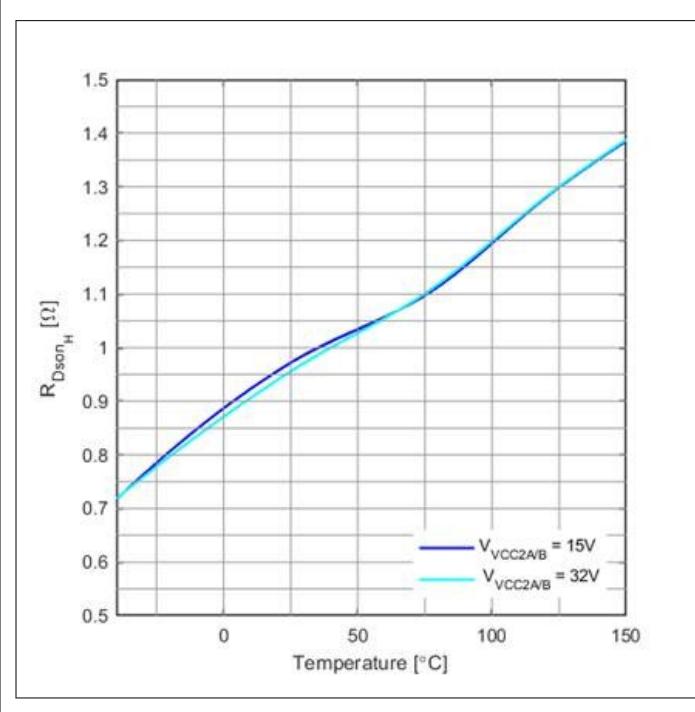


Figure 12 $R_{DSon,H}$ vs. temperature

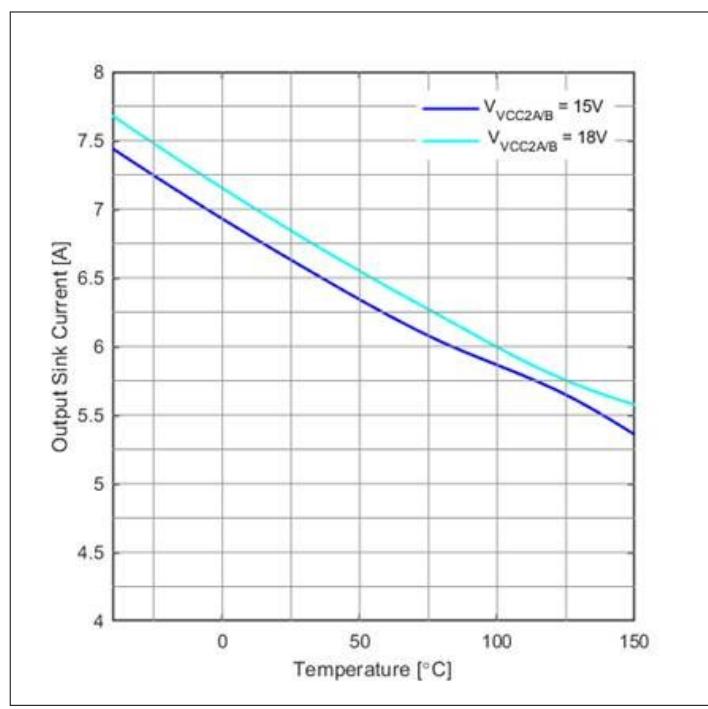


Figure 13 I_{OUTL} vs. temperature

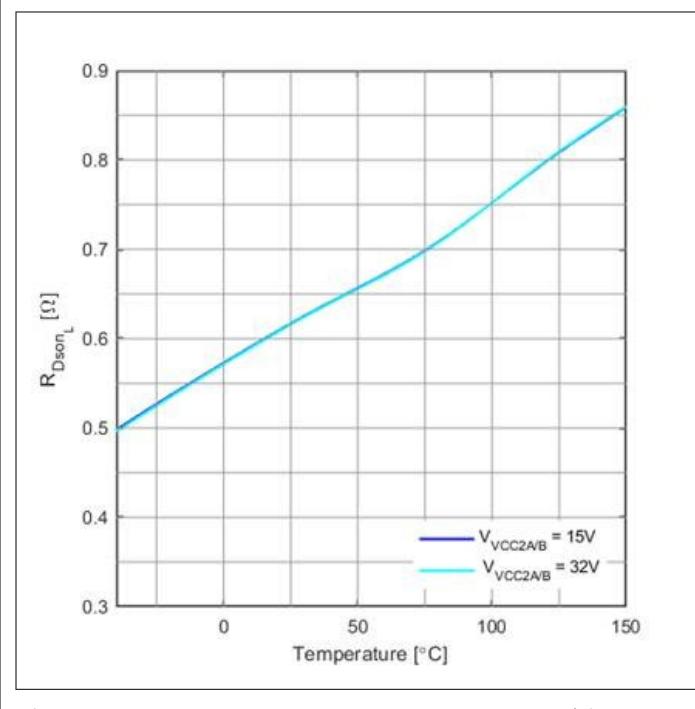


Figure 14 $R_{DSon,L}$ vs. temperature (lines are overlapping)

(table continues...)

5 Typical characteristics

Table 14 (continued)

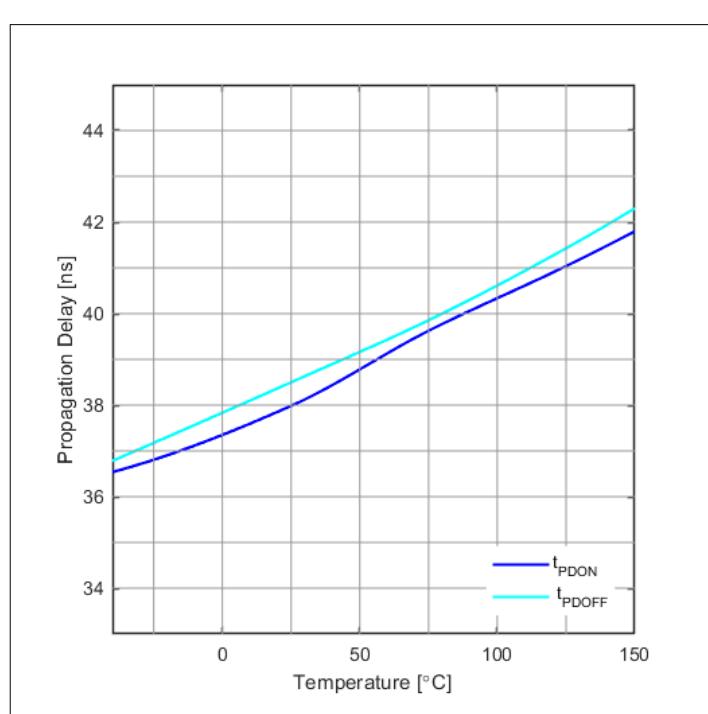


Figure 15 t_{PDON} & t_{PDOFF} vs. temperature

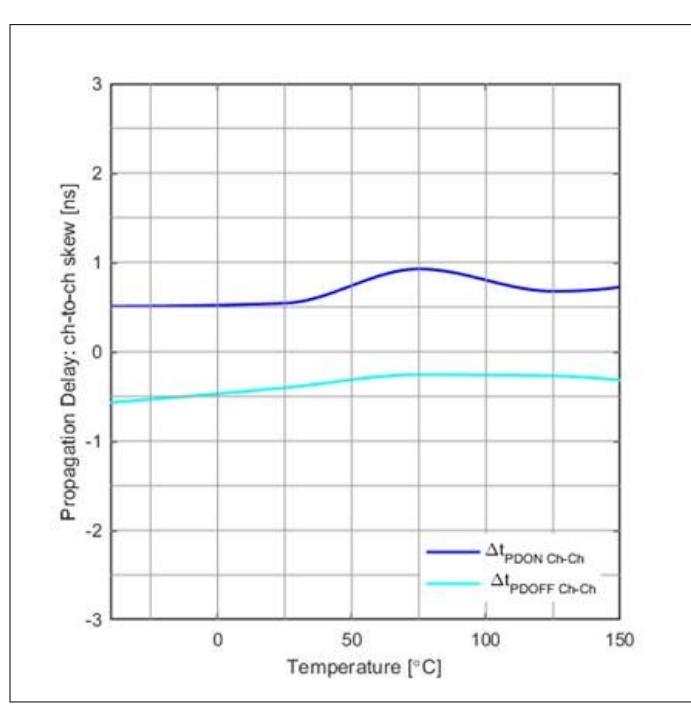


Figure 16 $\Delta t_{PDON,Ch-Ch}$ & $\Delta t_{PDOFF,Ch-Ch}$ vs. temperature

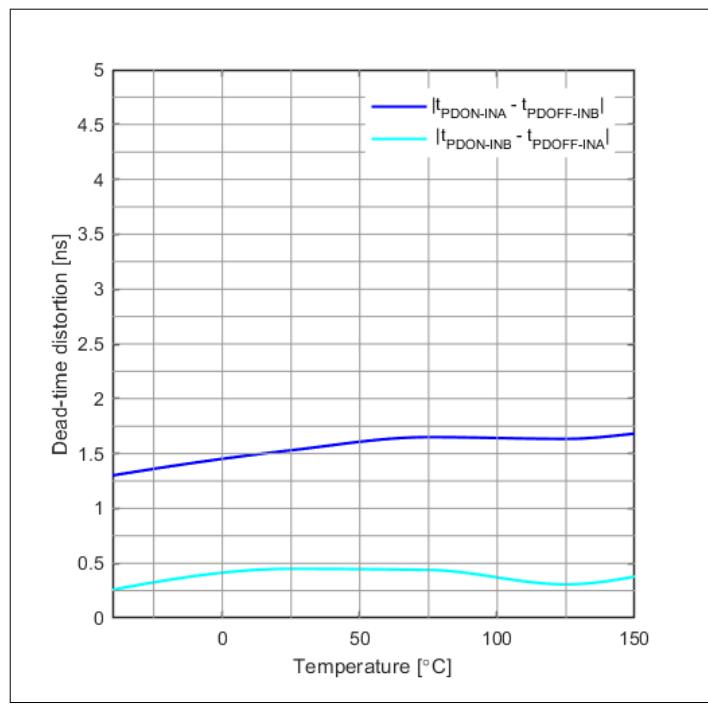


Figure 17 $|t_{DTD}|$ vs. temperature

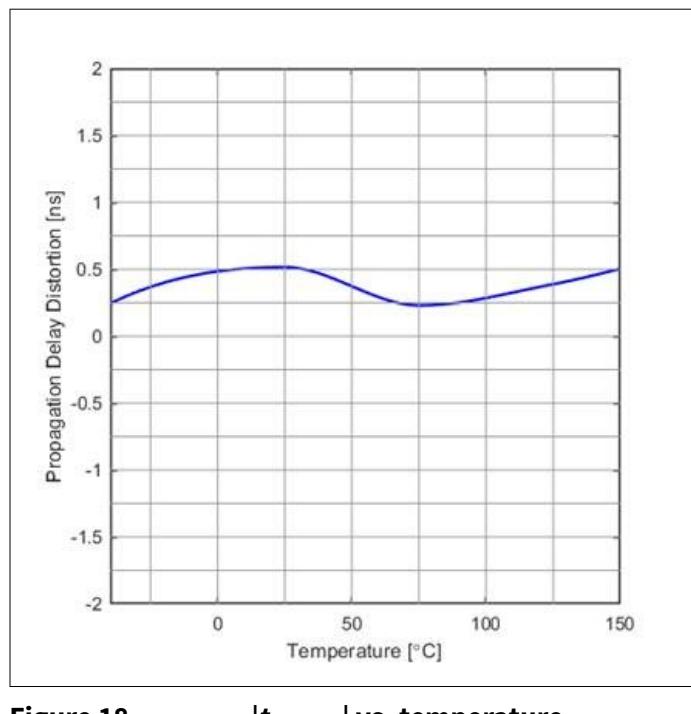


Figure 18 $|t_{PDISTO}|$ vs. temperature

(table continues...)

5 Typical characteristics

Table 14 (continued)

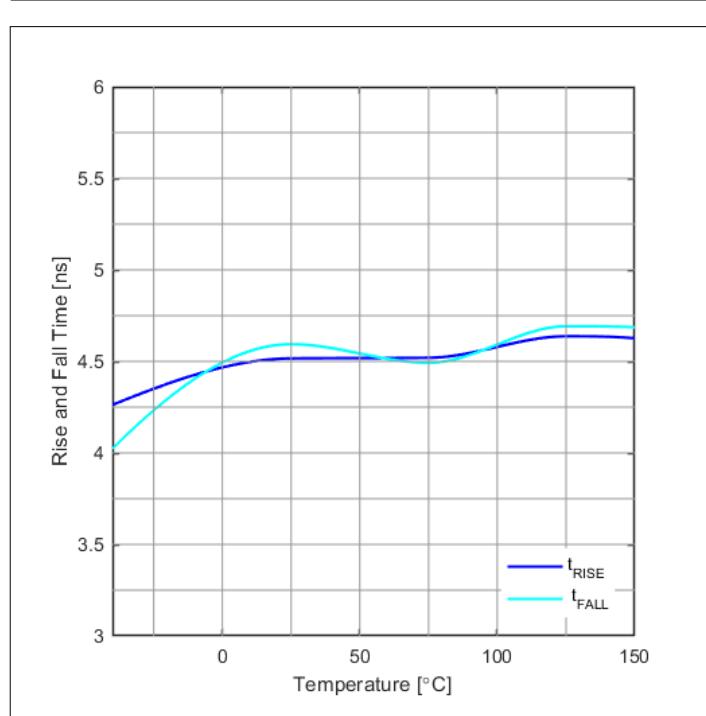


Figure 19 t_{RISE} & t_{fall} vs. temperature @ $C_{LOAD} = 1 \text{ nF}$

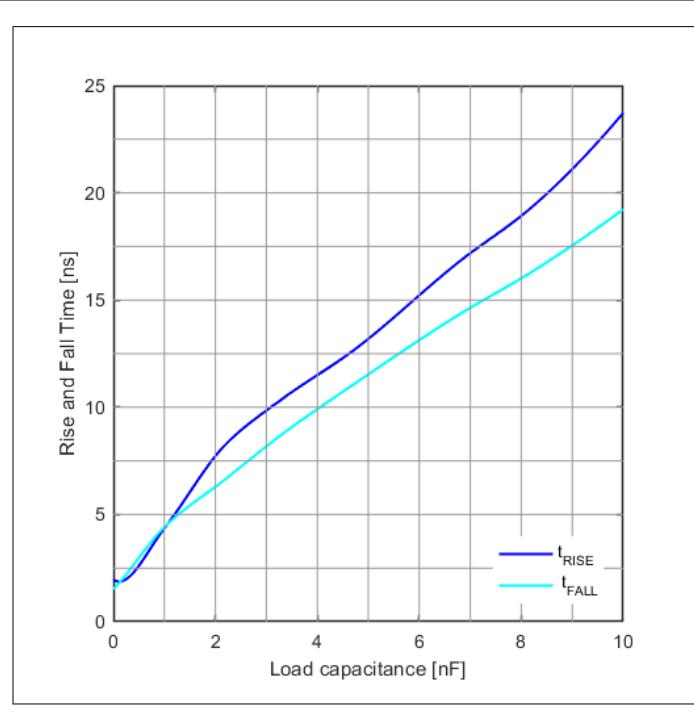


Figure 20 t_{RISE} & t_{fall} vs. C_{LOAD}

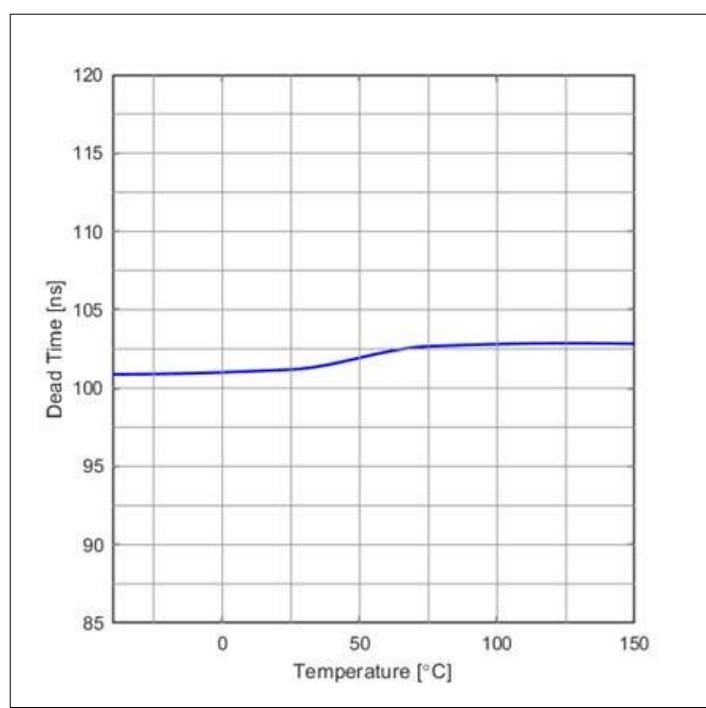


Figure 21 t_{DT} vs. temperature @ $R_{DT} = 10 \text{ k}\Omega$

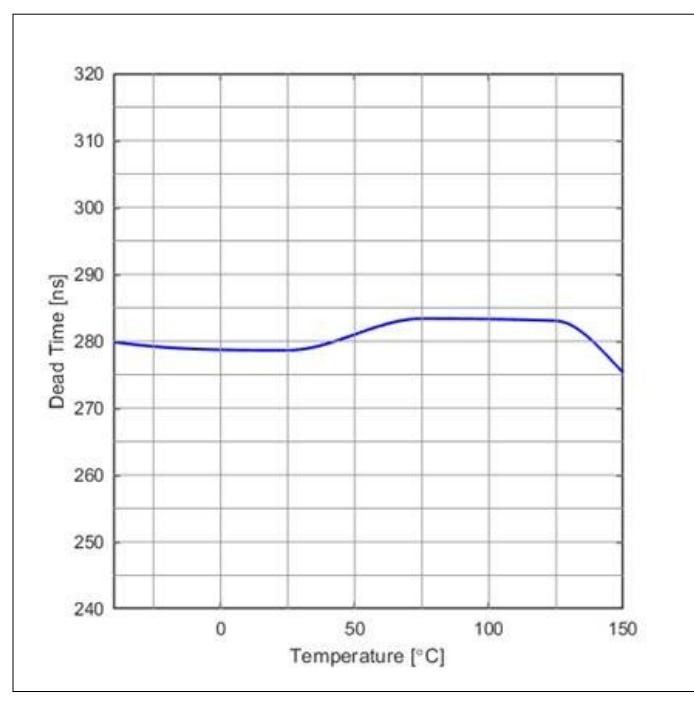


Figure 22 t_{DT} vs. temperature @ $R_{DT} = 30 \text{ k}\Omega$

(table continues...)

Table 14 (continued)

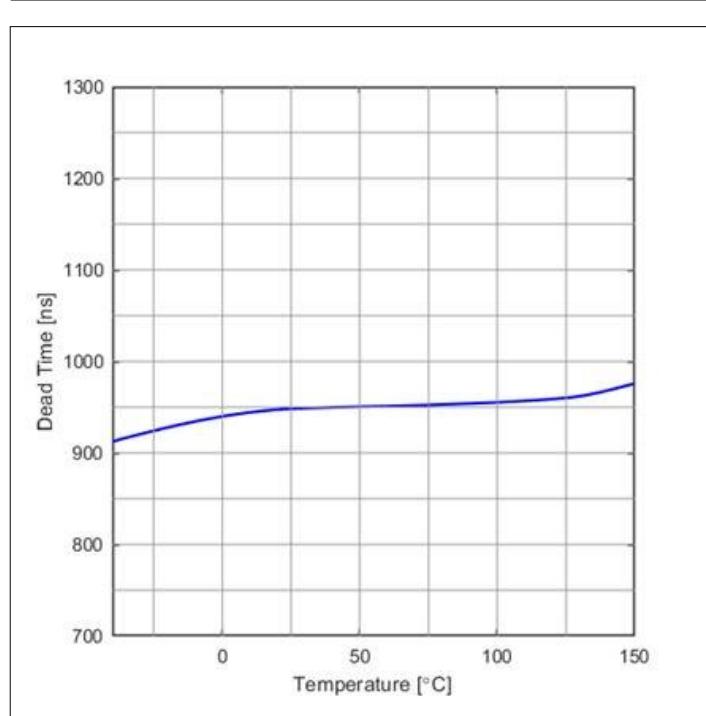


Figure 23 t_{DT} vs. temperature @ $R_{DT} = 100\text{k}\Omega$

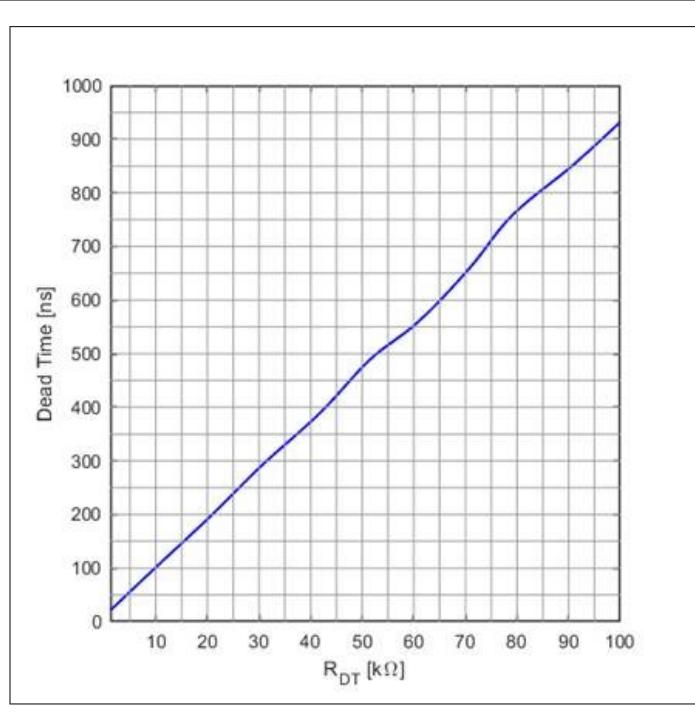


Figure 24 t_{DT} vs. R_{DT}

6 Parameter measurement

6.1 CMTI measurement setup

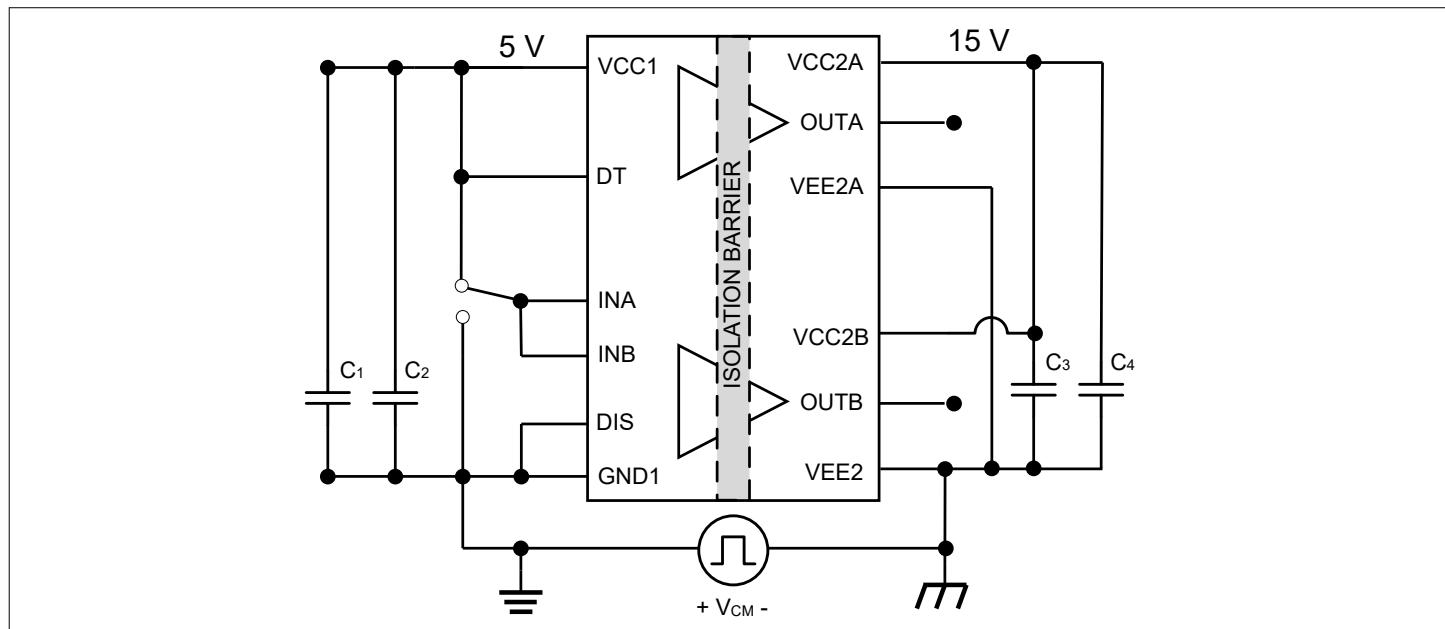


Figure 25 Static CMTI test circuit

The figure above shows the test setup for static common mode transient immunity

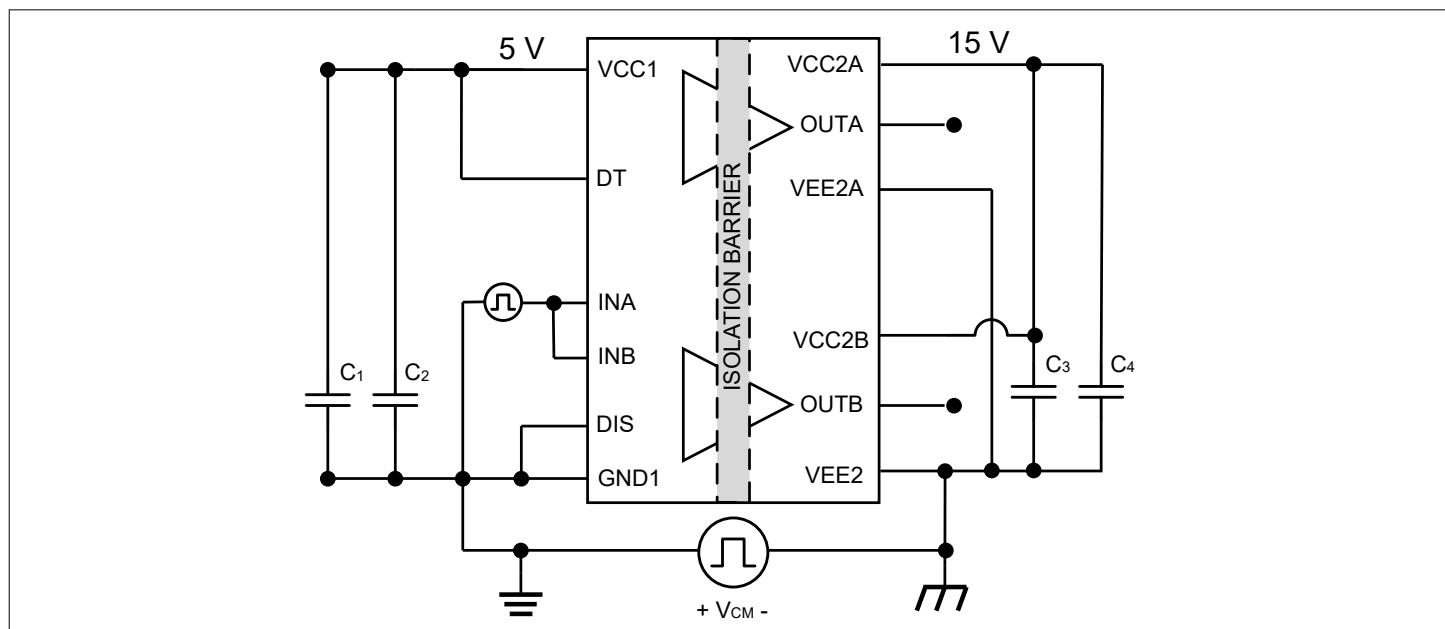


Figure 26 Dynamic CMTI test circuit

The figure above shows the test setup for dynamic common mode transient immunity

6.2 Undervoltage lockout (UVLO)

The following diagram shows the behavior of the channel outputs under UVLO conditions. In order to measure the thresholds, *INA* and *INB* are held at logic high and then the power supply voltages V_{VCC1} and V_{VCC2x} are ramped down

6 Parameter measurement

and up. When the voltages decrease below the V_{UVLOLx} levels, the channels turn off, allowing the threshold to be measured. Increasing the voltages, once they go above the V_{UVLOHx} , the channel turn on, again allowing the thresholds to be measured. All these thresholds are measured using slow ramps on all supplies.

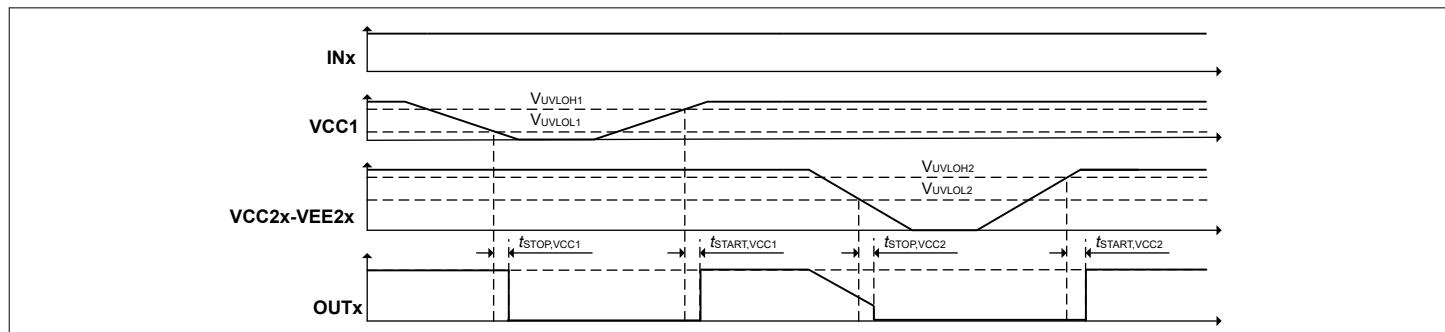


Figure 27 UVLO behavior

6.3 Propagation delay, rise and fall time

The following diagrams show the propagation delays t_{PDON} and t_{PDOFF} for the INA and INB , as well as DIS , including the rise time, t_{RISE} , and fall time, t_{FALL} .

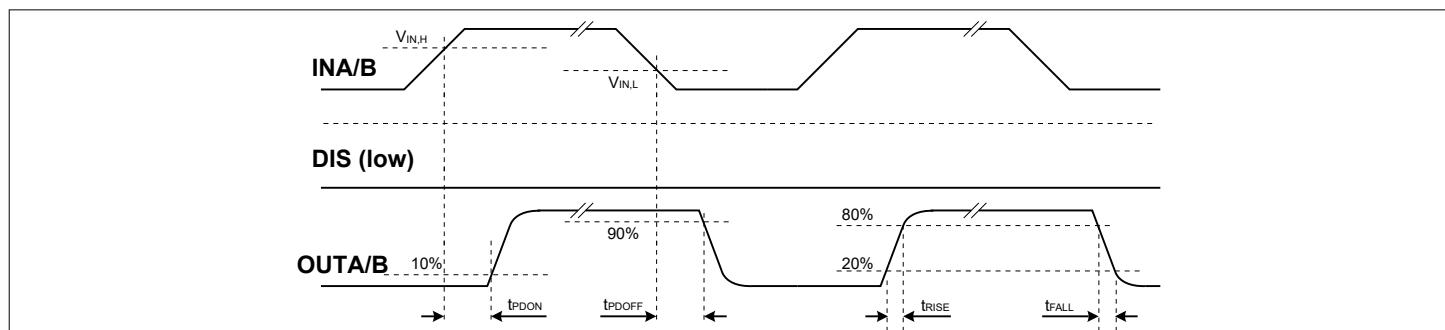


Figure 28 Propagation delay for DIS variants

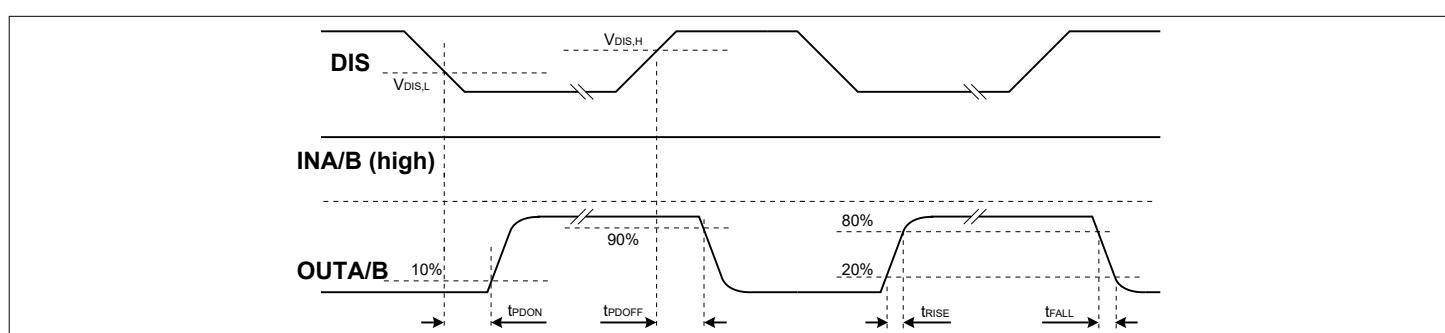
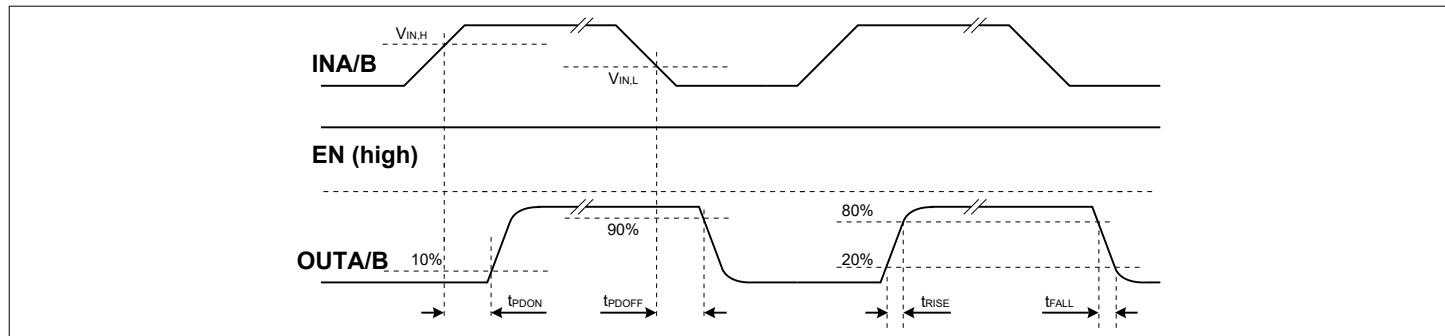
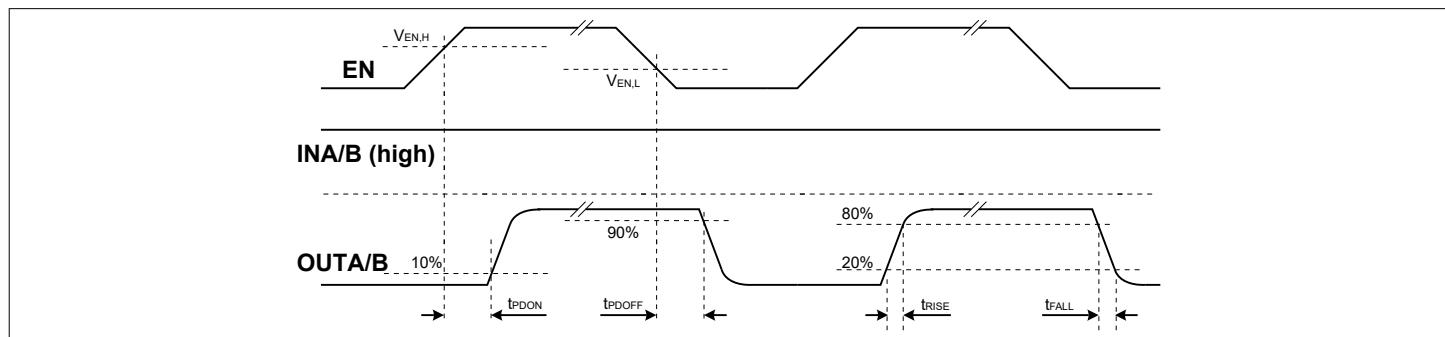


Figure 29 Propagation delay for the DIS pin

The following diagrams show the propagation delays t_{PDON} and t_{PDOFF} for the INA and INB , as well as EN , including the rise time, t_{RISE} , and fall time, t_{FALL} .

Figure 30 Propagation delay for *EN* variantsFigure 31 Propagation delay for the *EN* pin

6.4 Deadtime matching

The channel-to-channel deadtime matching $\Delta t_{DT,Ch-Ch}$ is defined as the absolute difference between the deadtimes generated by the falling edges of the 2 channels *INA* and *INB*.

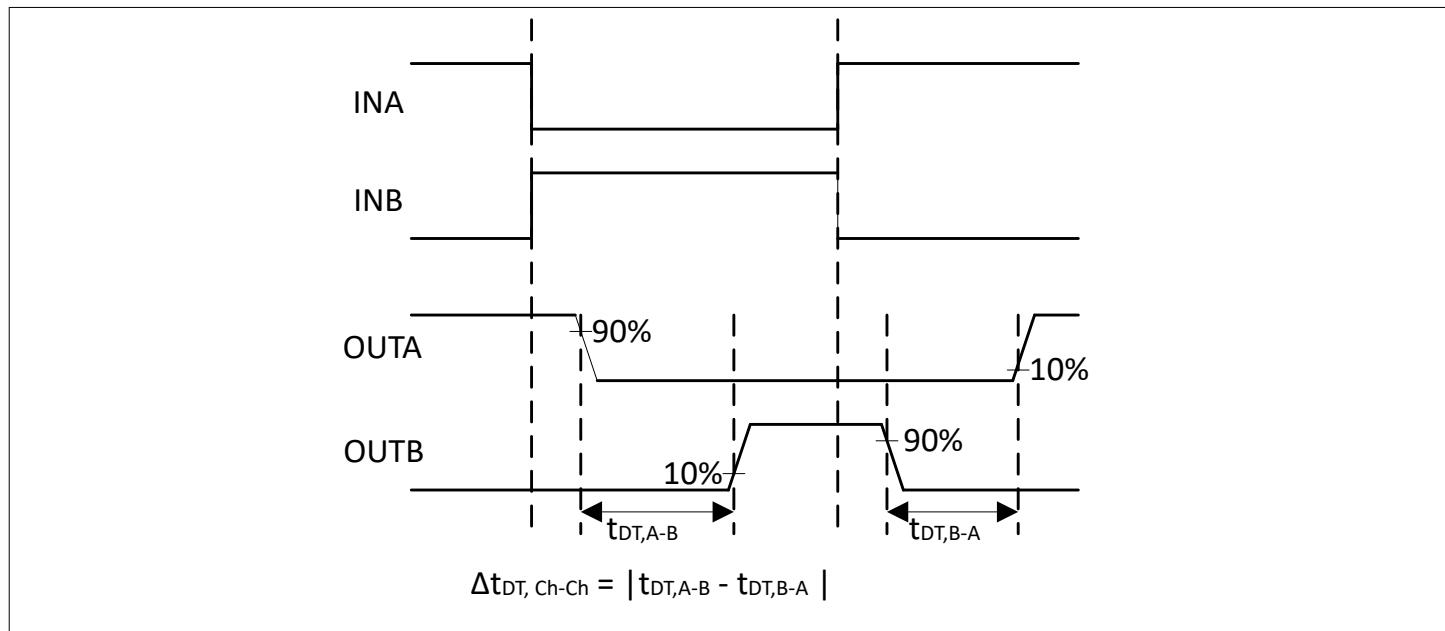


Figure 32 Channel-to-channel deadtime matching

The next figure illustrates the deadtime distortion t_{DTD} . Here a deadtime is applied from the microcontroller side to the *INA* and *INB* pins. Ideally, the deadtime at the outputs *OUTA* and *OUTB* should be the same. However, the driver introduces a distortion to this value, given by the OFF propagation delay of one channel and the ON propagation delay of the other channel.

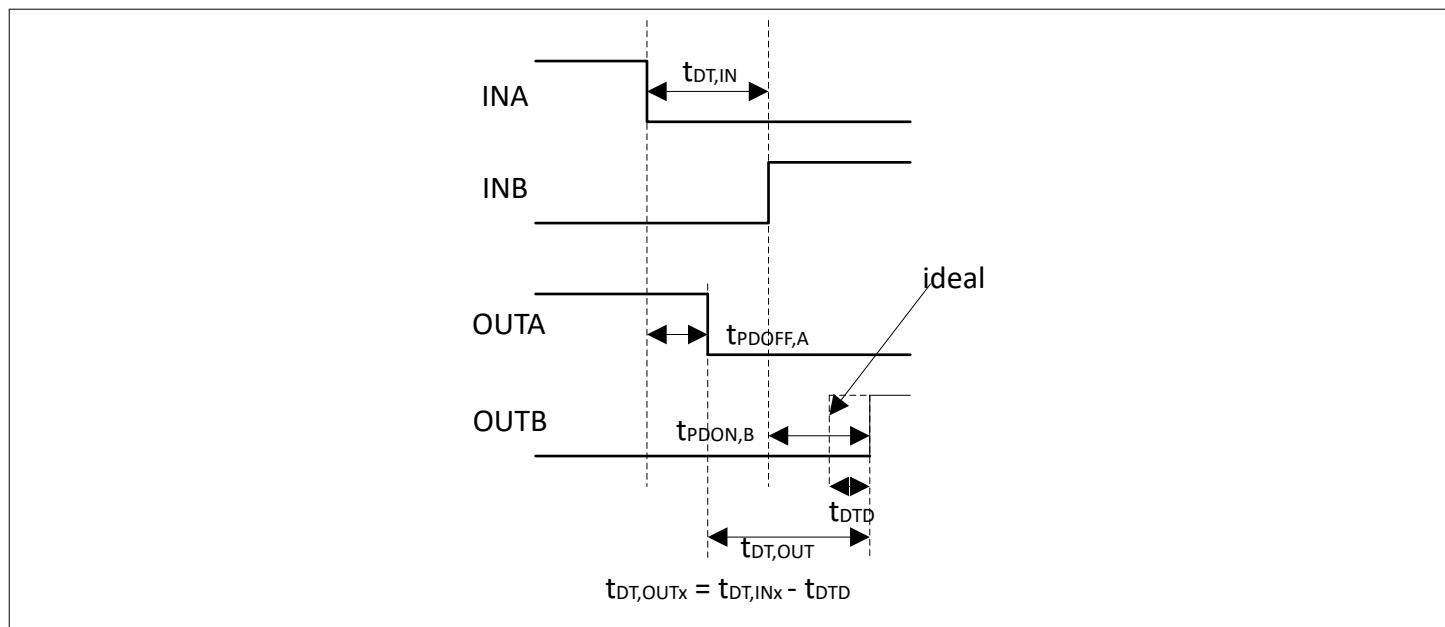


Figure 33

Deadtime distortion

7 Functional description

7.1 Input side functional blocks

The input side of the gate driver contains several blocks, which ensure the interfacing to the microcontroller, as well as the data transmission across the isolation barrier.

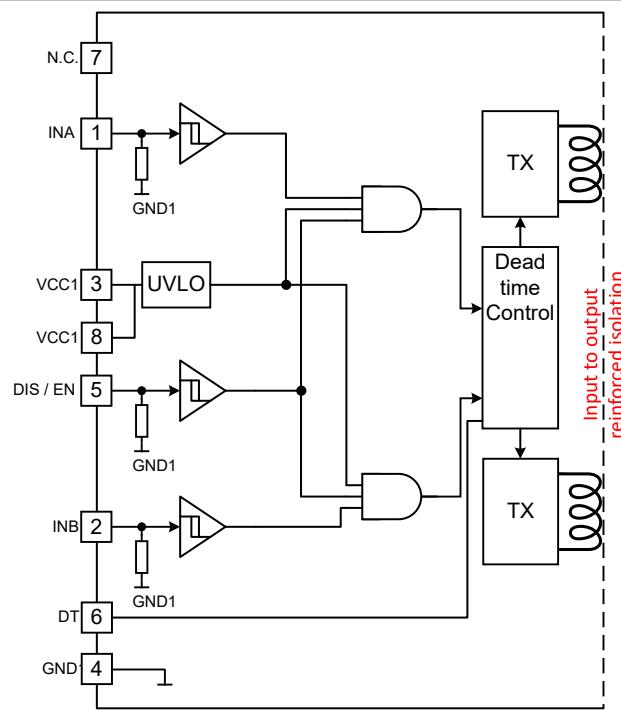


Figure 34 Input side block diagram

The following blocks are available:

- Input supply undervoltage lockout
- Input signal filters
- Pulldown resistors
- Deadtime control

7.1.1 Input supply undervoltage lockout (UVLO)

The UVLO block on the input chip monitors the voltage between the $VCC1$ and the $GND1$ pins and ensures that there is enough voltage between these pins for the internal circuitry to operate correctly.

As long as the voltage between these two pins is below V_{UVLOL1} , no turn-on signals coming on the INA or INB pins are sent across the isolation barrier, and the channels are by default turned off.

In order to allow turn-on signals to cross the isolation barrier, the voltage between the $VCC1$ and the $GND1$ pins must exceed the V_{UVLOH1} threshold and stay above V_{UVLOL1} , otherwise the communication across the isolation barrier is disabled and the channels are turned off.

It must be noted that the communication across the isolation barrier is also dependent on the DIS/EN pins.

Although the UVLO ensures that the voltage between the pins is large enough, it does not provide protection against dynamic disturbances coming across the supply lines, which can propagate to the internal circuits of the device.

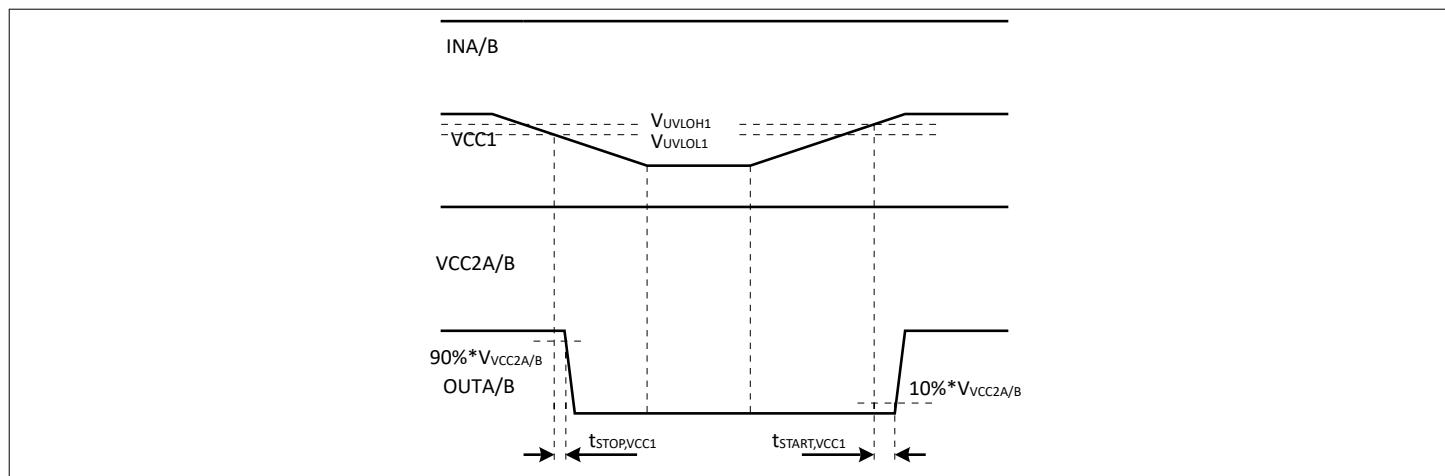


Figure 35 Input side UVLO behavior

7.1.2 Input signal filters

Every pulse at *INA*, *INB* or *DIS/EN*, shorter than the input pulse suppression time t_{INFLT} , will be filtered and will not be transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay t_{PDON} and t_{PDOFF} . This aids the design and an external RC filter for noise suppression will not be needed in most cases.

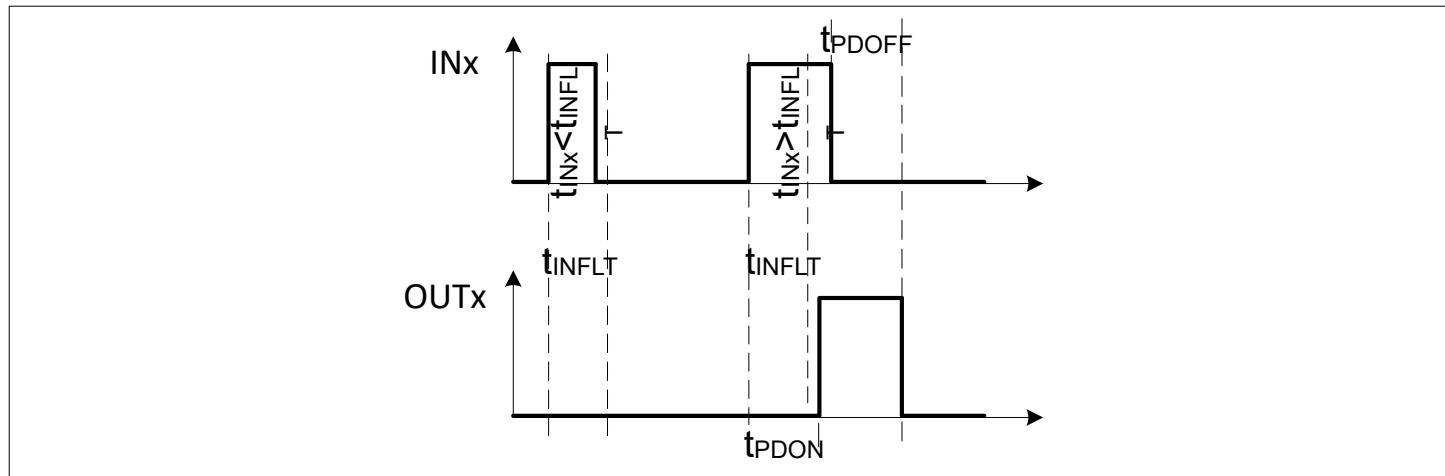


Figure 36 Input filter behavior

7.1.3 Pulldown resistors

Each of the digital input pins has a pulldown resistor attached to it. This ensures that in case the pin is desoldered from the board, it is pulled to a safe state, with the channels disabled. This is valid for *INA*, *INB*, as well as the variants with *EN* pins. The variants with *DIS* pins allow a simpler driving, as well as lower current consumption, since by default the driver is active. But it is highly recommended not to leave this pin floating, and if not actively driven by the microcontroller, it should be soldered to *GND1*.

7.1.4 Deadtime control

The Deadtime control block implements the non-overlapping between the two channels, depending on the state of the *DT* pin. The following states and behaviors are defined:

- *DT* ^connected to *GND1*: A minimal (<10 ns) shoot-through protection between the channels is implemented

7 Functional description

- DT connected to $VCC1$ or left floating: The two channels behave as independent drivers
- DT is connected through a resistor to $GND1$: A deadtime is implemented between the falling edge of a channel and the rising edge of the other channel, according to the equation:

$$t_{DT} = K_{DT_R} \times R_{DT_R} + M_{DT_R}$$

Note that in case of DT pin disconnection operation, the device will not transition automatically to independent driver mode.

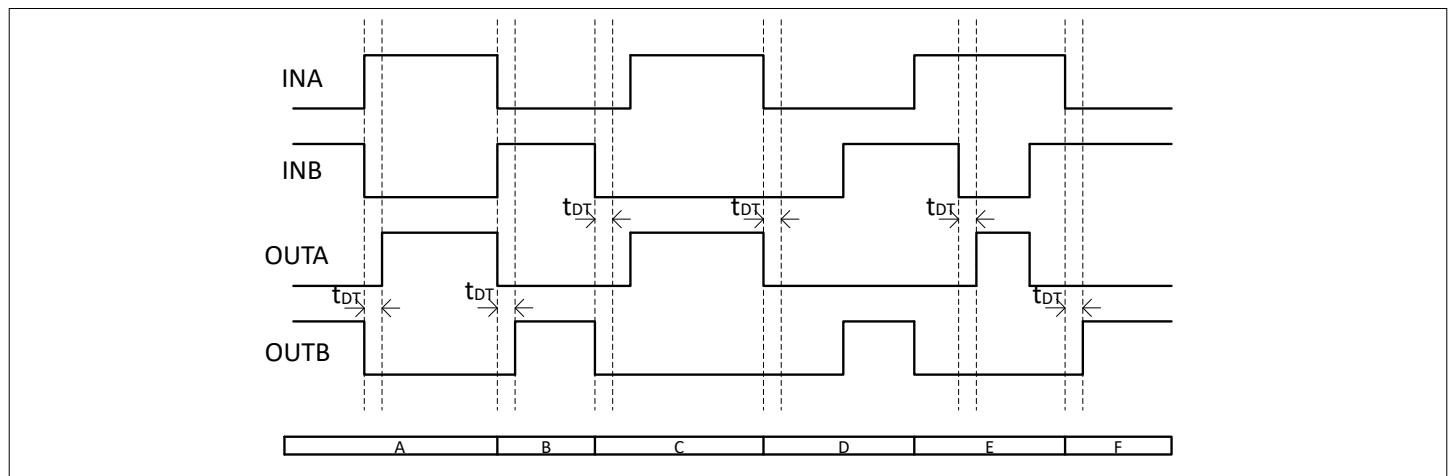


Figure 37 Deadtime special pulses

When a resistor is connected to the DT pin, the following behaviors are defined:

- A & B: when complementary signals appear at the input pins at the same time, the deadtime will be generated at the falling edge of the turned off channel, and only after it has expired, the turn-on of the other channel will be triggered
- C: if the turn-on signal on one channel has appeared after a time greater than t_{DT} from the turn-off of the other channel, the deadtime is not visible at the output of the two channels
- D: if a channel receives a turn-on command when the other channel is already on, both channels are turned immediately off, until the condition at the input disappears
- E & F: when exiting condition D, a deadtime will be generated from the turn-off command of one channel, until the other channel is turned on

It is not recommended to connect capacitors to the DT pin.

7.2 Output side functional blocks

The output side of the device contains 2 identical ICs, each driving one of the output channels. Each IC has the following blocks:

- Output side undervoltage lockout (UVLO)
- Short-circuit clamping
- Active shutdown
- Overtemperature protection (OTP)

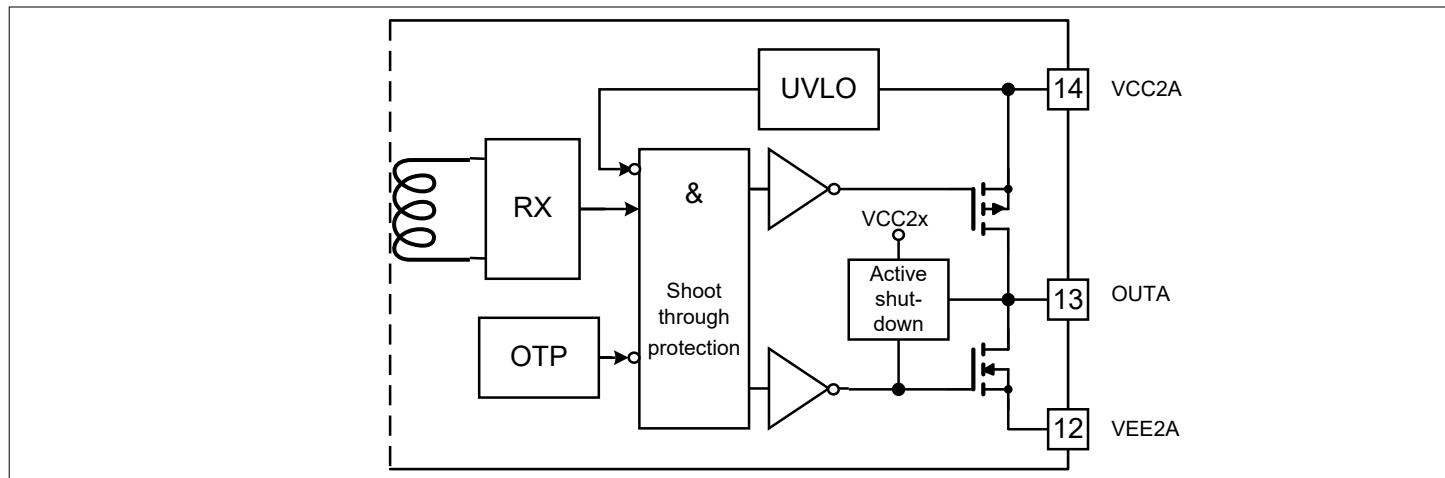


Figure 38 Output side block diagram

7.2.1 Output side undervoltage lockout (UVLO)

The UVLO block on the output chip monitors the voltage between the $VCC2A/B$ and the $VEE2A/B$ pins and ensures that there is sufficient voltage between these pins to drive the connected switch properly.

As long as the voltage between these two pins is below V_{UVLOL2} , no turn on signals coming across the isolation barrier will change the output state, and the channels are by default turned off.

In order to allow the turn-on of the channels, the voltage between the $VCC2A/B$ and the $VEE2A/B$ pins must exceed the V_{UVLOH2} threshold and stay above V_{UVLOL2} , otherwise the channels will automatically be turned off, regardless of the state of the input pins.

Since the charge required to turn-on the power switch connected to the channel is provided by the buffer capacitor connected between the $VCC2A/B$ and $VEE2A/B$, this capacitor must be dimensioned so that during or after the turn-on event, the voltage between these two pins does not drop below V_{UVLOL2} , as this will automatically trigger the turn off of the driver.

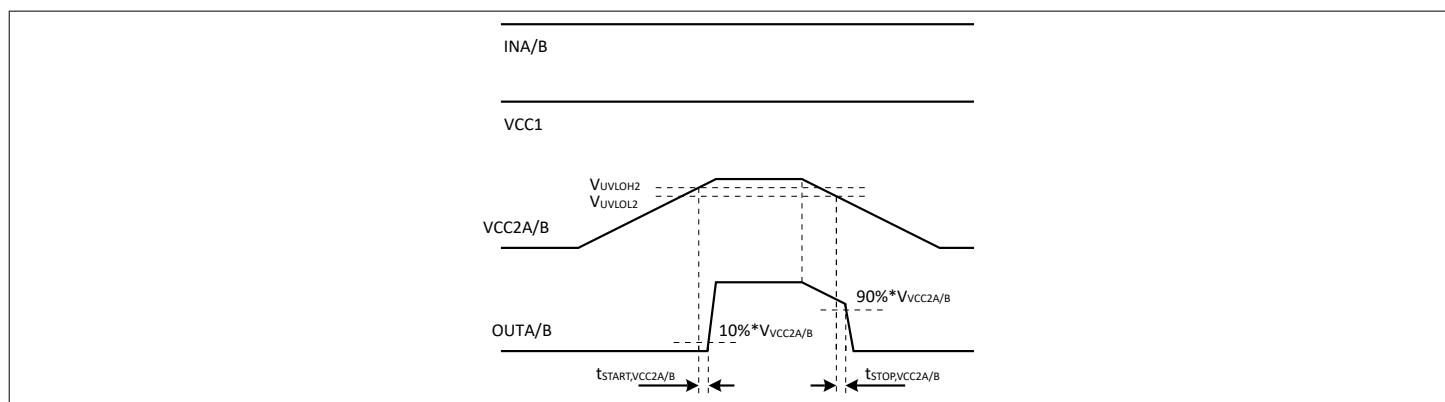


Figure 39 Output side UVLO behavior

7.2.2 Short-circuit clamping

During short circuit, the gate voltage of the power transistor tends to rise because of the feedback via the Miller capacitance. In this situation, the IC internally clamps the voltage on the OUTA/B pins and limits the voltage to a value slightly higher than the supply voltage $V_{VCC2A/B}$. A maximum current of 500 mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired, external Schottky diodes should be added between the OUTA/B and VCC2A/B pins.

7.2.3 Active Shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a turn-on of the power switch due to a floating gate.

The active shut-down feature ensures a safe IGBT, Si or SiC MOSFET off-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT, Si or SiC MOSFET gate is clamped via the OUTA/B-pin to VEE2A/B.

In case of a missing or collapsing power supply at the VCC2A/B pin, the output section of the driver operates in the active shutdown mode. In this case, the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is by far stronger than using the external resistor placed between the gate and the source pins of the power switch. At the same time, in case of fast dV/dt events on the switch that would generate miller current that could bias the gate, even when the gate driver is not powered on, the active shutdown circuit will use the voltage to self power and actively pull the gate low. The active shut-down feature functions in a similar manner across all the variants.

7.2.4 Overtemperature protection

The overtemperature protection shuts down the output of the gate driver IC and protects the application when the junction temperature of the IC exceeds the threshold temperature, $T_{OTP OFF}$. The output is then kept off until the temperature reaches the safe level of $T_{OTP REL}$. At this moment, the output is turned on again, if the turn-on command is again sent.

It must be noted that, although the overtemperature protection feature attempts to protect the device, operating the driver above T_J may potentially damage the driver permanently.

8 Application information

Note: Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical application

This section describes how the gate drivers can be used in the application.

The figures below show examples of application implementations.

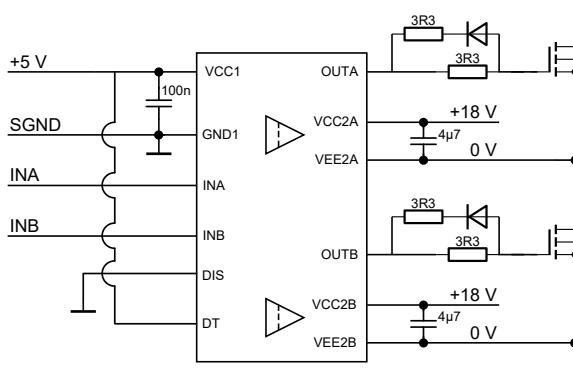


Figure 40 Independent dual channel operation with unipolar biasing using SiC switches

In order to operate the driver as two independent channels, the DT pin needs to be connected to the input supply pin $VCC1$. This way, the driver does not impose any restriction on the signals which are transmitted to the input channels. This operating mode can be used when dealing with space restrictions or in very cost-sensitive applications. Also shown in the figure above is the usage of unipolar power supplies, where $VEE2A/B$ pin should be connected directly to the source or emitter of the power transistor. This biasing strategy can be used when switches without parasitic turn-on are used, or at lower dV/dt of the switching node. For asymmetrical switching, a diode and an additional series resistor can be added in parallel to the main gate resistor. In the picture, the equivalent discharging resistor is roughly half of the charging resistor. A fast diode should be used for such an implementation and its voltage drop must be taken into consideration.

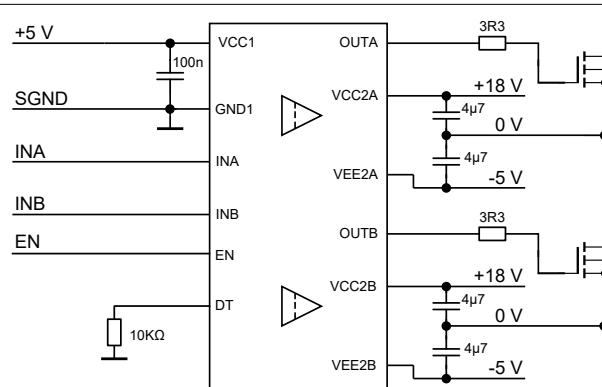


Figure 41 Half-bridge operation with bipolar biasing using SiC switches

The device can also be operated in half-bridge mode, by connecting a resistor between the *DT* and the *GND1* pins. When this is done, the driver implements a dead-time between the falling edge of one channel and the rising edge of the other channel. Note that also the dead-time distortion $|t_{DTD}|$ must be taken into account. Also shown in the picture is the usage of a bipolar driving supply. In this case a virtual ground is realized using two capacitors connected in series from *VCC2A/B* to *VEE2A/B*, with the middle point connected to the source or emitter of the driven switch.

8.2 Power supply recommendations

The 2ED314xMC12L gate drivers support a wide range of voltages on the input and the output side. The devices can operate with unipolar as well as bipolar power supply voltages on the output side for reliable and safe operation in the application.

To ensure that the gate driver operates correctly, it is necessary to place appropriate decoupling capacitors on the power supply pins. On the input side, it is recommended to place a low ESR, surface mount, multilayer ceramic capacitor of 100 nF between the *VCC1* pin and *GND1* pin. This capacitor should be placed as close as possible to the pins.

The decoupling capacitors on the output side, in addition to decoupling any disturbance on the power supply, also store the necessary energy to deliver the peak currents required for turning on and off the power transistor. Therefore, these capacitors should be dimensioned appropriately to limit the voltage drop during the power transistor turn-on and off. When using a unipolar power supply, a low ESR, surface mount, multilayer ceramic capacitor of at least 4.7 μ F should be placed between the *VCC2A/B* pin and the *VEE2A/B* pin in the close proximity of the pins. In case of a bipolar power supply, it is recommended to use at least 4.7 μ F ceramic capacitors between *VCC2A/B* and virtual ground(source or emitter potential of power transistor) and also between *VEE2A/B* pin and virtual ground. Depending on the gate charge of the power transistor and the peak source and sink gate currents, a higher capacitance may be necessary to limit the voltage drop during power transistor turn-on and turn-off. Finally, a 100 nF decoupling capacitor is recommended between *VCC2A/B* and *VEE2A/B* pins ensuring a short path between them to decouple any high frequency noise.

When selecting the capacitors, it is important to take into account the capacitance drop of ceramic capacitors in relation to the applied DC voltage.

8.3 Gate resistor selection

The gate resistor is a key component in the gate drive circuit. The gate resistor limits the source and the sink current of the gate driver thereby exercising control over the switching speed of the associated power transistor during both turn-on and turn-off operations. As such, the careful selection of an appropriate gate resistor represents a vital consideration in the design process. Some important considerations for selection of the gate resistance are:

- Optimize the switching losses
- Limit the overshoots and oscillations of the drain source voltage of the collector emitter voltage of the power transistor during turn-off
- Limit the overshoot and oscillations of the drain current or collector current during turn-on
- Damp the oscillations of the gate source or gate emitter voltage due to parasitic inductances and capacitances in the gate loop

As a starting point the gate driver selection, the gate resistor used in the datasheet of the power transistor for the characterization of the turn-on and turn-off losses can be used. The power supply conditions are rarely the same as the supply conditions that are used in power transistor data sheets. Therefore, an adaptation of the power transistor datasheet values is required to obtain a starting point for the optimization of the final gate resistor. The method which is proposed here uses the same peak gate current value for both the actual application and the power transistor datasheet.

The peak gate current as per power transistor datasheet equals to:

$$I_{G, \text{pk}} = \frac{\Delta V_{GS}}{R_{G, \text{datasheet}} + R_{G, \text{int}}} = \frac{\Delta V_{GS}}{R_{G, \text{application}} + R_{G, \text{int}}} \quad (1)$$

with $\Delta V_{GS} = V_{VCC2} - V_{VEE2}$

Solving this equation for R_G leads to:

$$R_G = \frac{\Delta V_{GS}}{I_{G, pk}} - R_{G, int} \quad (2)$$

This method results in a starting point for the gate resistor selection. Further evaluations, such as EMI measurements, are required for the final dimensioning of the gate resistors as they have to be adjusted to work with the circuitry inductance, margins and allowed dV/dt transients.

While dimensioning the components for gate resistances, it is necessary to take into account the average power dissipation in these resistors due to the switching of the power transistor as explained in the losses-based external gate resistor selection, as well as the pulse power capability of the component.

8.4 Deadtime resistor selection

The choice of the deadtime resistor must take into account the minimum pulse width which can occur during the operation. If the minimum pulse width has values similar to the deadtime, excessive diode conduction can occur, with loss of efficiency and potential device damage in the case of SiC switches. Therefore it is recommended to keep the deadtime reasonably smaller than the minimum pulse width, taking into account of course rise and fall time, as well as channel propagation delay.

8.5 Power dissipation estimation

8.5.1 Gate driver

The gate driver input side losses are dominated by the quiescent losses, which are calculated by:

$$P_{Q1} = V_{VCC1} \cdot I_{Q1} \quad (3)$$

The gate driver output side losses for each channel consist of the quiescent current losses $P_{Q2A/B}$ at nominal switching frequency and no load, the sourcing losses $P_{source,A/B}$ and the sinking losses $P_{sink,A/B}$

$$P_{OUT, A/B} = P_{Q2, A/B} + P_{source, A/B} + P_{sink, A/B} \quad (4)$$

The quiescent losses on the output side $P_{Q2,A/B}$ can be calculated as:

$$P_{Q2, A/B} = (V_{VCC2A/B} - V_{VEE2A/B}) \cdot I_{Q2} \quad (5)$$

The turn-on, $P_{source,A/B}$, and turn-off, $P_{sink,A/B}$, losses can be estimated using the resistive voltage divider between the internal resistance of the gate driver output stage, $R_{DSON,H}$ or $R_{DSON,L}$, and external gate resistor, $R_{G,ext}$, with the application related gate charge, Q_G , the total gate driving voltage, $V_{VCC2A/B} - V_{VEE2A/B}$, and switching frequency, f_{sw} :

$$P_{source, A/B} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2A/B} - V_{VEE2A/B}) \cdot \frac{R_{DSON,H}}{R_{DSON,H} + R_{G,ext, ON} + R_{G,int}} \quad (6)$$

$$P_{sink, A/B} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2A/B} - V_{VEE2A/B}) \cdot \frac{R_{DSON,L}}{R_{DSON,L} + R_{G,ext, OFF} + R_{G,int}}$$

Additionally, external components that surround the gate driver can heat up the IC. The mere calculation of losses and the theoretical junction temperature alone are not sufficient for a proven gate driver circuit design. A verification

by measurement is needed to avoid unexpected effects in the application. The identification of hotspots is possible, for example, by using an infrared camera.

8.5.2 External gate resistor

The losses in the gate resistor for turn-on, $R_{G,ext,ON}$ and the gate resistor for turn-off, $R_{G,ext,OFF}$ can be estimated using the same resistive voltage divider formed by the resistances in the source and the sink path of the gate current as:

$$P_{source,ext} = \frac{1}{2}Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{G,ext,ON}}{R_{DSON,H} + R_{G,ext,ON} + R_{G,int}} \quad (7)$$

$$P_{sink,ext} = \frac{1}{2}Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{DSON,L}}{R_{DSON,L} + R_{G,ext,OFF} + R_{G,int}}$$

8.6 Layout guidelines

Having a well-designed PCB layout is crucial to achieve optimal performance of the gate driver. Subsequently, this will ensure that the entire power electronic converter is operating at its best. Creating a well-designed PCB layout requires a certain level of attention and consideration to specific key factors. The following key points should be considered while designing the PCB layout using 2ED314xMC12L gate drivers:

- The low ESR, low ESL type decoupling capacitor on the input side, must be placed close to the *VCC1* and *GND1* pins and then connected to the pins such that the decoupling loop is as short as possible. Similarly, the decoupling capacitors on the output side should be placed close to the *VCC2A/B* and *VEE2A/B* pins and connected to the pins with a short connection
- It is crucial to minimize the physical area of the gate current loop that carries the current for charging and discharging the gate of the power transistor. The gate loop contain traces with high dv/dt and di/dt and having a short loop minimizes noise from the turn-on and off of the gates. Furthermore, a short loop also minimizes the stray inductance of the gate loop which improves the switching performance. To accomplish a short gate loop, the gate driver should be positioned near the power transistor, and the decoupling capacitors that store the energy for high peak currents should be located in close proximity to the gate driver
- In order to reduce the stray inductance of the gate loop even further, wide traces can be used for the traces in the gate loop. Furthermore, the forward path and the return path of the currents can be routed parallel to each other on the same PCB layer or overlapping each other on adjacent PCB layer to achieve the least amount of stray inductance
- In case of a unipolar power supply, the *VEE2A/B* pin of the gate driver should be connected to the Kelvin source/ emitter pin of the power transistor, if available. If the Kelvin pin is not available then the connection to the source/emitter should be as short as possible, starting from the device pin, in order to avoid the high current from the power transistor flowing in the gate loop
- The area below the body of the gate driver package should be kept free of any traces to ensure the integrity of the safety isolation between the input and output side
- It is recommended that the input signals of the gate driver connected to the *INA* and *INB* pins are kept away from any noisy traces. Although the 2ED314xMC12L comes with an integrated input filter that can filter high frequency noise on the input signal, an external RC filter with a small time constant can be placed close to these pins for enhanced filtering. Additionally, a ground plane is recommended below the input signal traces for shielding the signals from noise
- The gate driver IC experiences power dissipation during system operation as explained in the previous chapters. This heat generated in the device will be dissipated mostly via the PCB. It is recommended to maximize the copper area connected to the *VEE2A/B* pins, in order to effectively dissipate the heat from the gate driver on to the PCB

9 Related products

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKWH40N65WR6	650 V, 40 A IGBT with anti-parallel diode in TO-247-3-HCC
	IHW30N160R5	1600 V, 30 A IGBT Discrete with anti-parallel diode in TO-247
	IKW15N120CS7	1200 V IGBT7 S7, 15 A IGBT with anti-parallel diode in TO247
	IKQ75N120CS7	1200 V IGBT7 S7, 75 A IGBT with anti-parallel diode in TO247-3
CoolSiC™ SiC MOSFET Discrete	IMBF170R1K0M1	1700 V, 1000 mΩ SiC MOSFET in TO-263-7 with extended creepage
	IMZA120R040M1H	1200 V, 40 mΩ SiC MOSFET in TO247-4 package
	IMZA120R014M1H	1200 V, 14 mΩ SiC MOSFET in TO247-4 package
	IMBG120R030M1H	1200 V, 30 mΩ SiC MOSFET in TO-263-7 package
	IMYH200R012M1H	2000 V, 12 mΩ SiC MOSFET in TO-247-PLUS with high creepage and clearance
CoolSiC™ SiC MOSFET Module	FS33MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 33 mΩ sixpack module
	FF17MR12W1M1H_B11	EasyDUAL™ 1B 1200 V, 17 mΩ half-bridge module
	FF4MR12W2M1H_B11	EasyDUAL™ 2B 1200 V, 4 mΩ half-bridge module
	F4-17MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 17 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

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Package dimensions

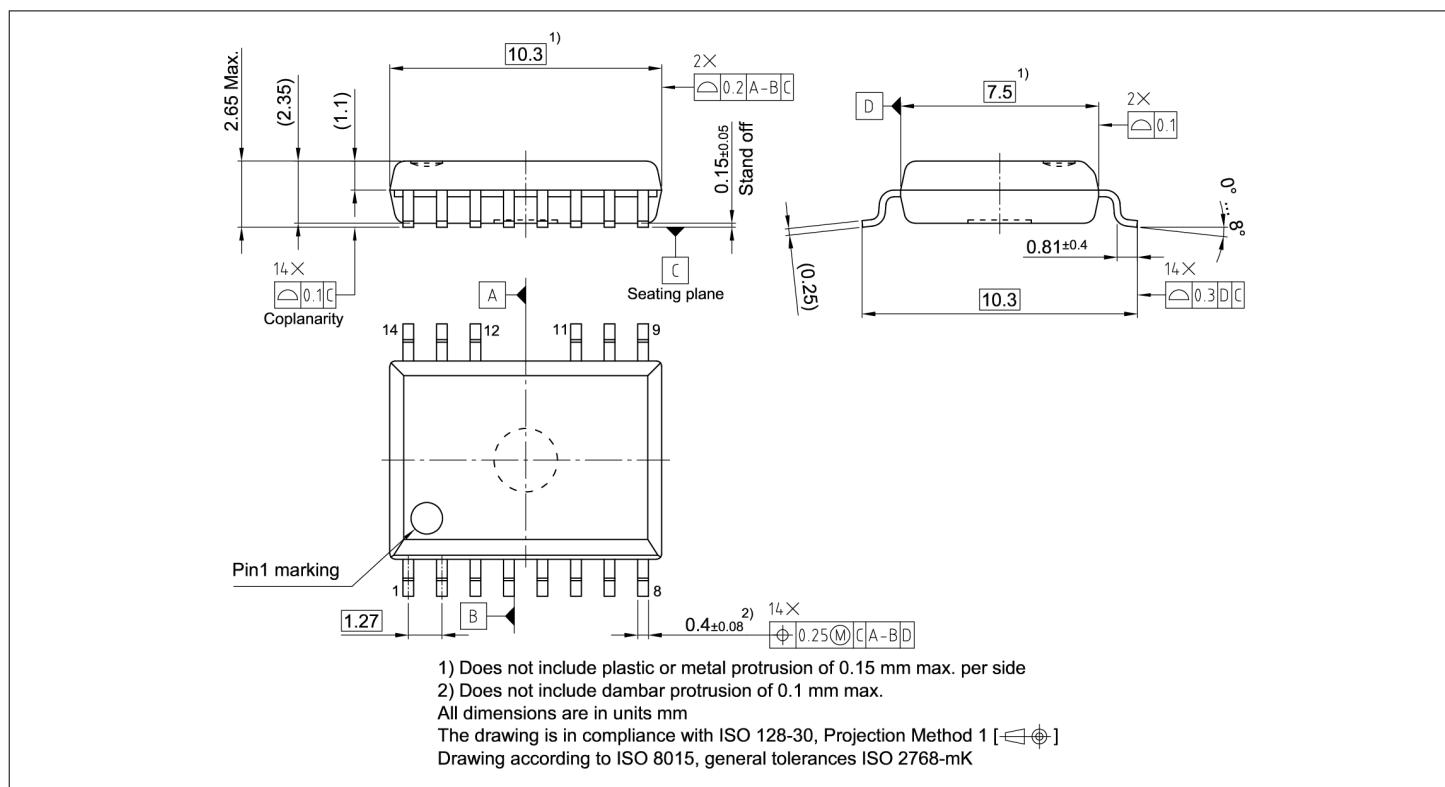


Figure 42 PG-DSO-14-71 (300 mil) outline

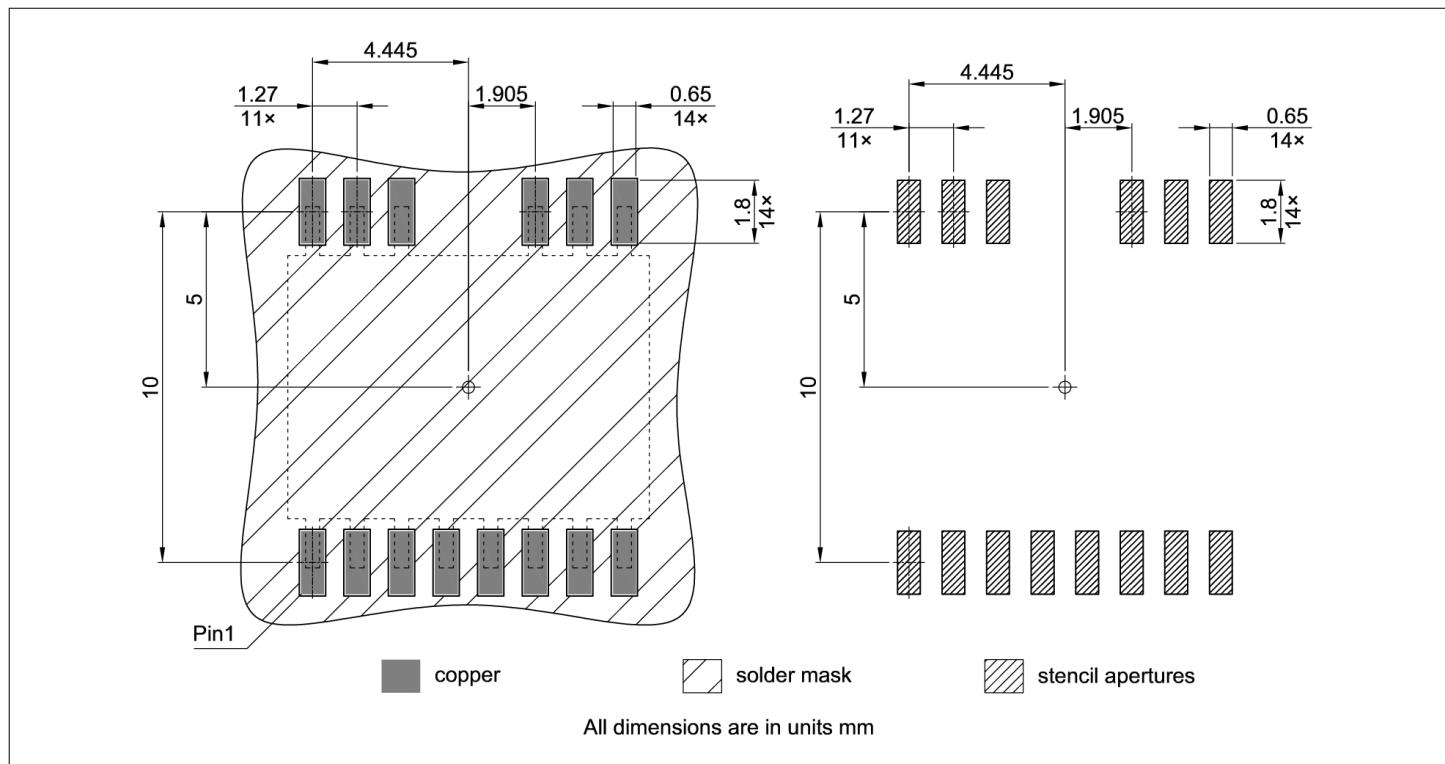


Figure 43

PG-DSO-14-71 (300 mil) recommended footprint

Revision history

Document version	Date of release	Description of changes
v1.00	2024-05-16	<ul style="list-style-type: none">Initial official release

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