

Description

The 6P40368 is a small form factor clock generator with integrated crystal that is intended for low-power, consumer, wearable and smart devices.

The device is designed to support a single 1.8V LVC MOS clock output and a dynamic frequency control for two frequency options. The frequency can be selected by one output pin. The 6P40368 has an embedded crystal to offer a more reliable clock source with small board space requirements.

Features

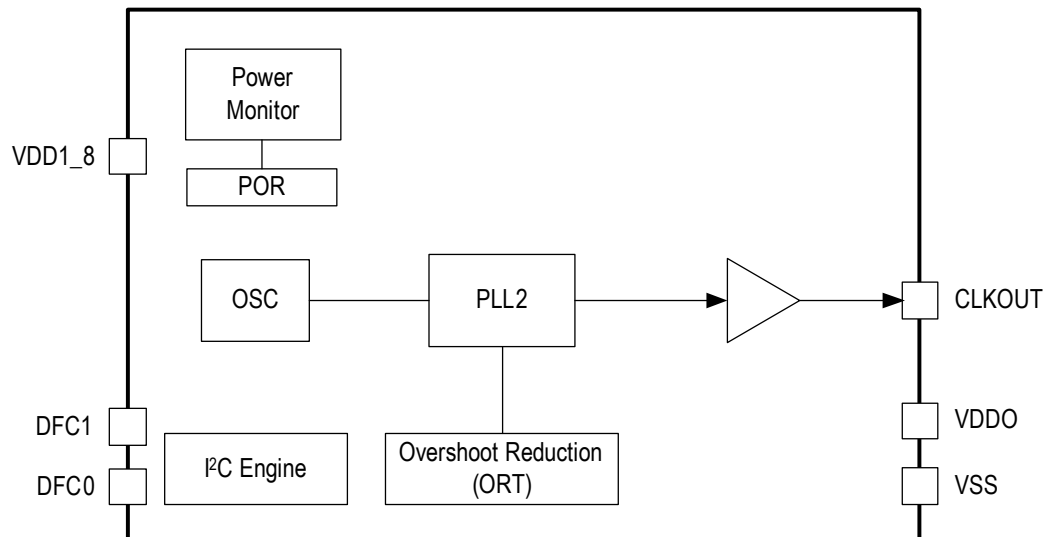
- No input clock source requirement
- Dynamic Frequency Control (DFC) is used for output frequency selection
- 1.8V operating voltage
- I²C interface
- 2.5 × 2.5 mm 12-DFN package, small form factor

Typical Applications

- Wireless charge module

Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2.5 × 2.5 mm 12-DFN Package

DFC0	1	12	V _{SS}
SEL_DFC/DFC1	2	11	NC
V _{SS}	3	10	V _{DDOUT2}
V _{SS}	4	9	NC
V _{DD1_8}	5	8	NC
V _{DDOUT1}	6	7	CLKOUT

2.5 × 2.5 mm 12-DFN

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	DFC0	Input	Dynamic frequency control pin.
2	SEL_DFC/DFC1	Input	Dynamic frequency control pin selected by SEL_DFC at power-on default.
3	V _{SS}	Power	Ground pin.
4	V _{SS}	Power	Ground pin.
5	V _{DD1_8}	Power	1.8V power rail.
6	V _{DDOUT1}	Power	Power supply pin for OUT1 output (1.8V).
7	CLKOUT	Output	1.8V LVCMOS clock output.
8	NC	—	No connect.
9	NC	—	No connect.
10	V _{DDOUT2}	Power	Output clock power supply pin 1.8V.
11	NC	—	No connect.
12	V _{SS}	Power	Ground pin.

Frequency Selection

Table 2: Frequency Selection

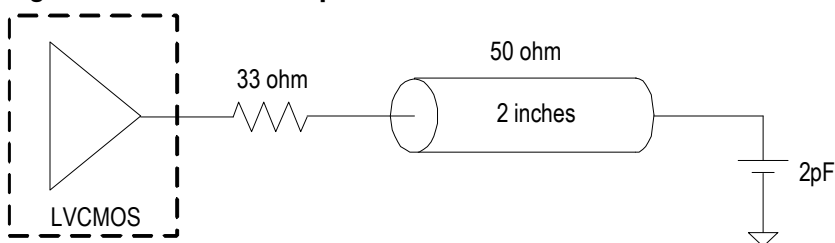
SEL_DFC	DFC1	DFC0	CLKOUT (MHz)
0	0	0	6.16791
0	0	1	6.1298496
0	1	0	N/A
0	1	1	N/A
1	x	x	x

ORT – VCO Overshoot Reduction Technology

The 6P40368 supports the VCO overshoot reduction technology to prevent an output clock frequency spike when the device is changing frequency on-the-fly or doing DFC (Dynamic Frequency Control) function. The VCO frequency changes are controlled instead of free-run to targeted frequency.

Output Clock Test Conditions

Figure 3. LVCMOS Output Clock Test Condition



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 6P40368. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings¹

Item	Rating
Supply Voltage, V_{DD1_8} , V_{DDOUTx}	-0.5V to 2.2V
Inputs	
Other inputs	-0.5V to V_{DD1_8} / V_{DDOUTx}
Outputs, V_{DDOUTx} (LVCMOS)	-0.5V to $V_{DDOUTx} + 0.5V$
Outputs, IO (SDA)	10mA
Package Thermal Impedance, θ_{JA}	42°C/W (0mps)
Package Thermal Impedance, θ_{JC}	41.8°C/W (0mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

¹ Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DDOUT1}	Power Supply Voltage for supporting OUT1	1	—	1.89	V
V_{DDOUT2}	Power Supply Voltage for supporting OUT2	1.71	1.8	1.89	
V_{DD1_8}	Power Supply Voltage for Core Logic functions	1.71	1.8	1.89	V
T_A	Ambient Operating Temperature	-40	—	85	°C
C_{LOAD_OUT}	Maximum Load Capacitance (1.8V LVCMOS only)	—	5	—	pF
t_{PU}	Power-up Time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic)	0.05	—	3	ms

Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance ($T_A = +25\text{ }^\circ\text{C}$)

Table 5. Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance

Symbol	Parameter	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance (OE, SDA, SCL)	—	3	7	pF
Pull-down Resistor	OE	—	150	—	k Ω
R_{OUT}	LVCMOS Output Driver Impedance ($V_{DDOUTx} = 1.8\text{V}$)	—	50	—	Ω

Integrated Crystal Characteristics

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation	—	Fundamental			
Frequency	—	—	26	—	MHz
Frequency Tolerance ¹	—	—	—	± 20	ppm
Equivalent Series Resistance (ESR)	—	—	10	100	Ω
Shunt Capacitance	—	—	2	7	pF
Load Capacitance (C_L)	—	6	8	10	pF
Maximum Crystal Drive Level	—	—	—	100	μW

¹ Frequency tolerance includes initial frequency, over-temperature range and aging data.

Electrical Characteristics

Table 7. DC Electrical Characteristics ^{1,2}

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Operation Supply Current	$V_{DD} = V_{DDOUTx} = V_{DD1_8} = 1.8\text{V}$; OUT = 6.1679100MHz with load.	—	2.5	—	mA
		$V_{DD} = V_{DDOUTx} = V_{DD1_8} = 1.8\text{V}$; OUT = 6.1298496MHz with load.	—	2.5	—	mA
I_{DDPD}	Power Down Current	PD asserted with V_{DD1_8} and V_{DDOUTx} on.	—	390	—	μA

¹ Single CMOS driver active.

² OUT current measured with 2-inch transmission line and 2pF load.

Table 8. Input Parameters ¹

Supply Voltage $V_{DD1_8} = 1.8V \pm 5\%$, $V_{DDOUTx} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{IL}	Input Leakage Low Current for OE1	$V_{IN} = GND$ at OE1 pin.	150	—	5	μA
I_{IH}	Input Leakage High Current for OE1	$V_{IN} = 1.89V$.	—	—	20	μA
I_{OE1}	Input Leakage Current	$V_{IN} = 1.89V$ at OE1 pin.	—	—	120	μA

¹ Guaranteed by design and characterization, not 100% tested in production.

Table 9. DC Electrical Characteristics for 1.8V LVCMOS

$V_{DDOUTx} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	$I_{OH} = -8mA$.	$0.7 \times V_{DDOUTx}$	—	V_{DDOUTx}	V
V_{OL}	Output Low Voltage	$I_{OL} = 8mA$.	0.1	—	0.15	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, $V_{DDOUTx} = 1.89V$.	—	—	3	μA
V_{IH}	Input High Voltage	Single-ended inputs – OE, SDA, SCL.	$0.65 \times V_{DDOUTx}$	—	$V_{DDOUTx} + 0.3$	V
V_{IL}	Input Low Voltage	Single-ended inputs – OE, SDA, SCL.	$GND - 0.3$	—	$0.35 \times V_{DDOUTx}$	V

AC Electrical Characteristics

Table 10. AC Timing Electrical Characteristics

$V_{DD1_8} = 1.8V \pm 5\%$, $V_{DDOUTx} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$; spread spectrum = off.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{OUT}^1	Output Frequency	SEL_DFC = 0, DFC[1:0] = 01.	—	6.16791	—	MHz
		SEL_DFC = 0, DFC[1:0] = 00.	—	6.1298496	—	MHz
t_0	Accuracy ⁴	Average.	—	—	50	ppm
t_1	Output Duty Cycle	LVCMOS clock < 120MHz.	45	—	55	%
t_2	Rise/Fall, SLEW[0] = 1	Single-ended LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDOUT} 1.8V$.	—	2.5	—	ns
t_3	Clock Jitter	Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage).	—	50	150	ps
t_4^2	Lock Time	PLL lock time from power-up.	—	—	20	ms
t_5^3	Lock Time	PLL lock time from shutdown mode.	—	0.1	2	ms

¹ Practical lower frequency is determined by loop filter settings.

² Includes loading the configuration bits from OTP to PLL registers. It does not include OTP programming/write time.

³ Actual PLL lock time depends on the loop configuration.

⁴ Includes initial frequency, over-temperature range and aging data.

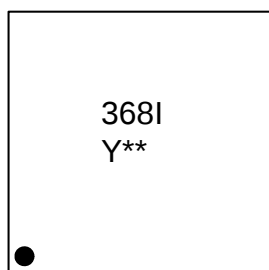
Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available.

Ordering Information

Orderable Part Number	Package	Shipping Packaging	Temperature
6P40368NDGI	2.5 × 2.5 mm, 0.4mm pitch 12-DFN	Cut Tape	-40° to +85°C
6P40368NDGI8	2.5 × 2.5 mm, 0.4mm pitch 12-DFN	Reel	-40° to +85°C

Marking Diagram



1. Line 1 is the truncated part number.
2. "Y" is the last digit of the year the part was assembled.
3. "***" denotes sequential lot number.

Revision History

Revision Date	Description of Change
August 16, 2018	▪ Updated Absolute Maximum Ratings table. ▪ Updated Package Outline Drawings section.
October 30, 2017	Initial release.



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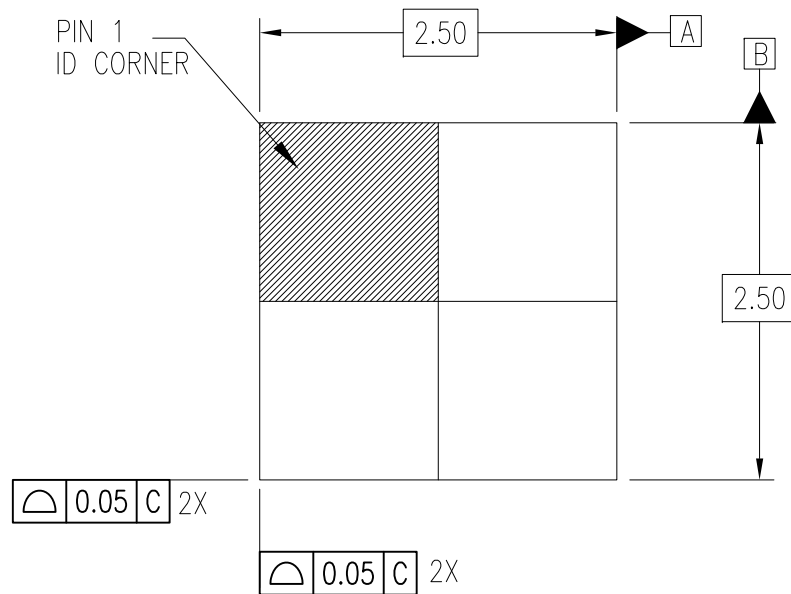
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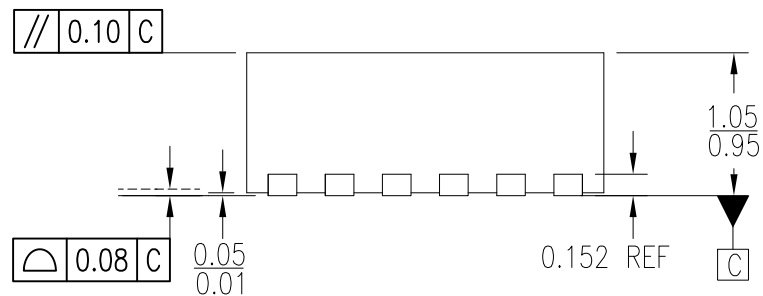
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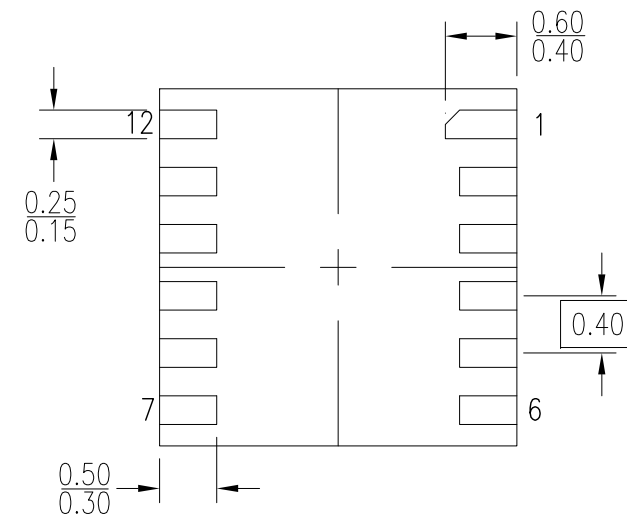
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	REV	DESCRIPTION		
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12/08/17	01	CORRECT DIMENSION		JH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE				



TOP VIEW



SIDE VIEW (ROTATE 90 DEG.)



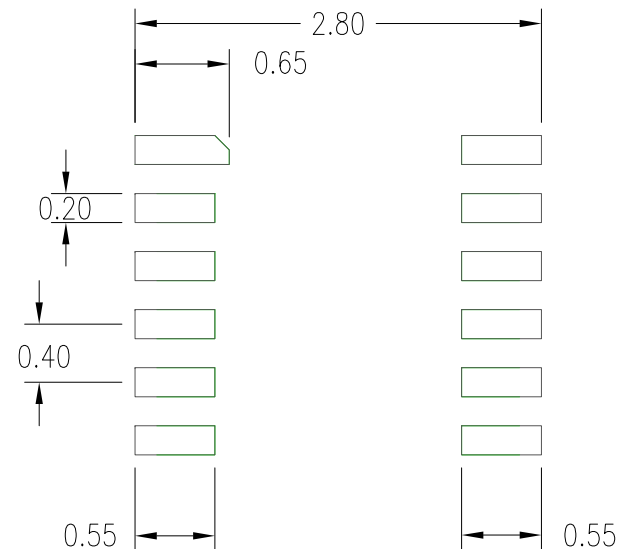
BOTTOM VIEW

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASMEY14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED		 IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
DECIMAL	ANGULAR		TITLE ND/NDG12 Package Outline Drawing 2.50 x 2.50 x 1.00 mm Body 0.40mm Pitch DFN	
X± .1	±1°			
XX± .05				
XXX± .030				
		SIZE C	DRAWING No. PSC-4665	REV 01
DO NOT SCALE DRAWING			SHEET 1 OF 2	

DATE CREATED	REVISIONS			
	REV	DESCRIPTION		AUTHOR
06/21/16	00	INITIAL RELEASE		JH
12/08/17	01	CORRECT DIMENSION		JH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE				



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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X± .1	±1°	TITLE ND/NDG12 Package Outline Drawing 2.50 x 2.50 x 1.00 mm Body 0.40mm Pitch DFN			
XX± .05					
XXX± .030					
		SIZE	DRAWING No.	REV	
		C	PSC-4665	01	
DO NOT SCALE DRAWING				SHEET 2 OF 2	