

## High-Performance Dual-Channel DC-DC Converter

### General Description

DA9220 is a power management unit (PMU) suitable for supplying CPUs, GPUs, DDR memory rails in single in-line pin package (SIPP) modules, smartphones, tablets, and other handheld applications.

DA9220 integrates two single-phase buck converters, each phase requiring a small external 0.10  $\mu$ H inductor. Each buck is capable of delivering up to 3 A output current at a 0.3 V to 1.9 V output voltage range. The 2.5 V to 5.5 V input voltage range is suitable for a wide variety of low-voltage systems, including, but not limited to, all Li-Ion battery supplied applications.

With remote sensing, the DA9220 guarantees the highest accuracy and supports multiple PCB routing scenarios without loss of performance.

The pass devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope-controlled rail activation.

The dynamic voltage control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via either a direct register write using the communication interface (I<sup>2</sup>C-compatible) or with a programmable input pin.

A configurable GPI allows multiple I<sup>2</sup>C address selection for multiple instances of DA9220 in the same application.

DA9220 has integrated over-temperature and over-current protection for increased system reliability, without the need for external sensing components.

### Key Features

- 2.5 V to 5.5 V input voltage
- 0.3 V to 1.9 V output voltage
- 4 MHz nominal switching frequency
- $\pm 1\%$  accuracy (static)
- $\pm 5\%$  accuracy (dynamic)
- I<sup>2</sup>C-compatible interface (FM+)
- Programmable GPIOs
- Programmable soft-start
- Voltage, current, and temperature supervision
- -40 °C to +85 °C ambient temperature range
- Package: 24WLCSP 2.5 mm x 1.7 mm (0.4 mm pitch)

### Applications

- SIPP modules (SoC, DRAM)
- Smartphones
- Tablet PCs
- Infotainment
- Ultrabooks™
- Wi-Fi Modules
- Game Consoles

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## System Diagrams

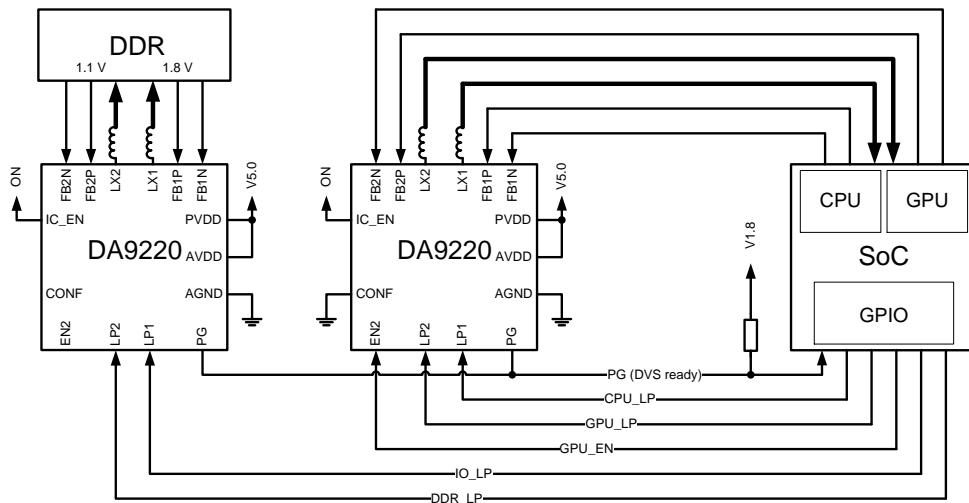


Figure 1: Typical Application Diagram (Port Control)

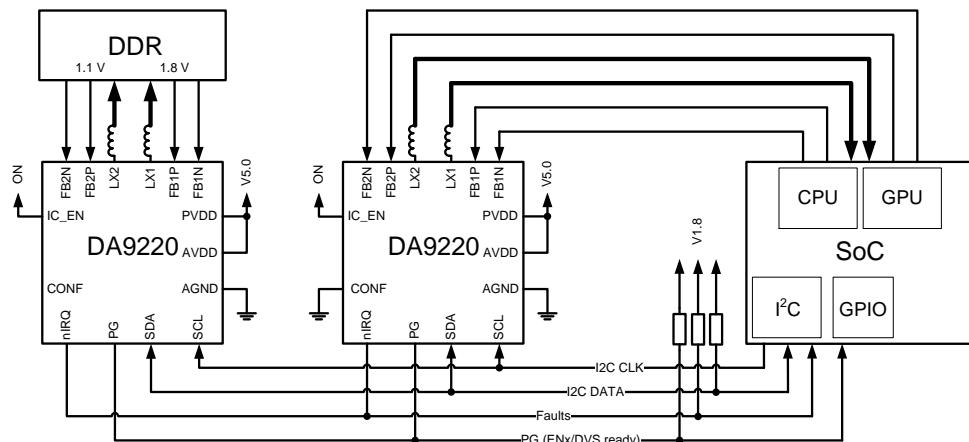
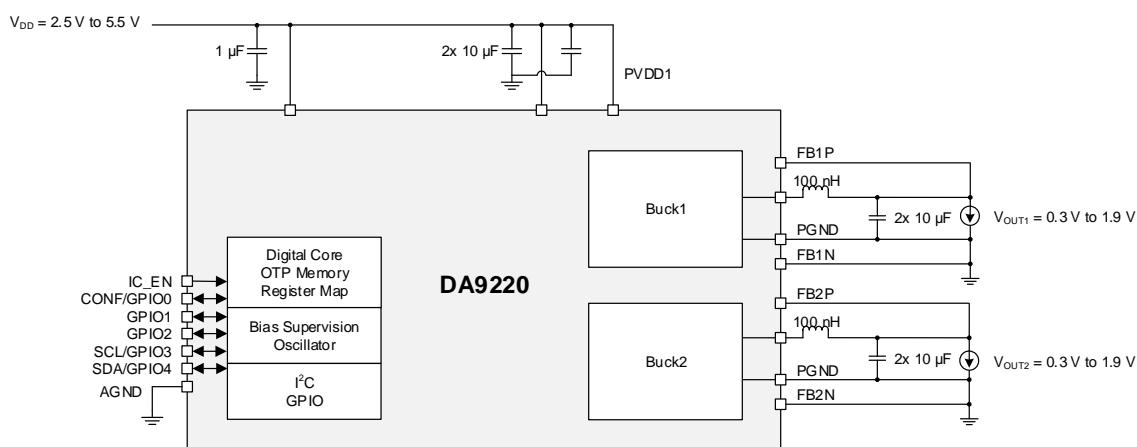
Figure 2: Typical Application Diagram (I<sup>2</sup>C Control)

Figure 3: Simplified Schematic Diagram

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## 1 Terms and Definitions

|        |  |
|--------|--|
| ATE    | Automated test equipment                           |
| CPU    | Central processing unit                            |
| DDR    | Dual data rate                                     |
| DVC    | Dynamic voltage control                            |
| FET    | Field effect transistor                            |
| FM+    | Fast mode plus                                     |
| GBD    | Guaranteed by design                               |
| GBQ    | Guaranteed by qualification                        |
| GBSPC  | Guaranteed by statistical process characterization |
| GPI    | General purpose input                              |
| GPIO   | General purpose input/output                       |
| GPU    | Graphics processing unit                           |
| IC     | Integrated circuit                                 |
| HW     | Hardware   |
| Li-Ion | Lithium-ion  |
| OTP    | One time programmable                              |
| PCB    | Printed circuit board                              |
| PRS    | Product requirements specification                 |
| SCL    | Serial clock                                       |
| SDA    | Serial data  |
| SIPP   | Single in-line pin package                         |
| SW     | Software   |

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## 2 Pinout

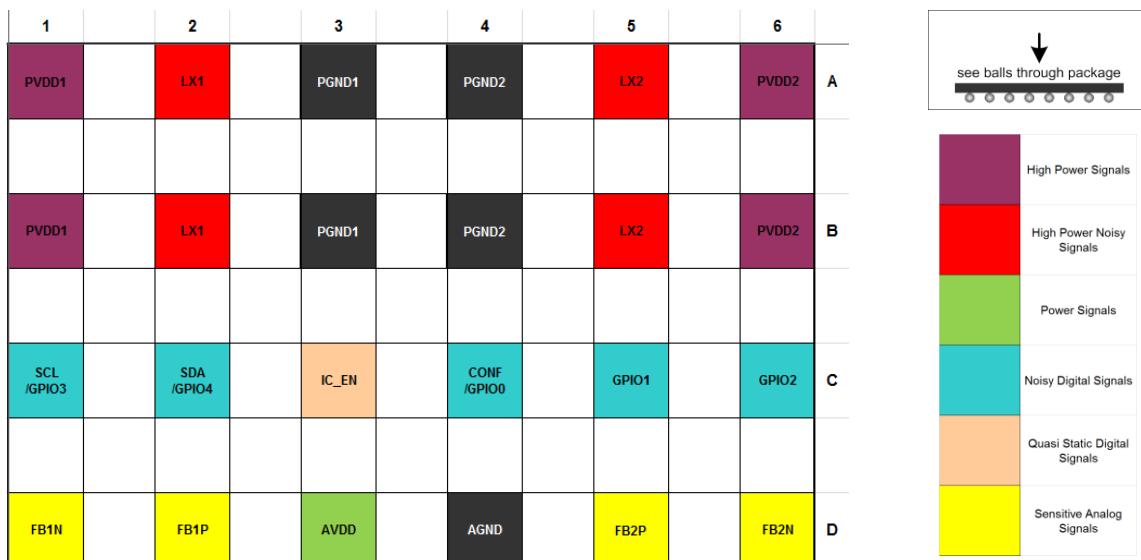


Figure 4: DA9220 Pinout Diagram (Top View)

Table 1: Pin Description

| Pin No. | Pin Name   | Type (Table 2) | Drive (mA) | Reset State | Description  |
|---------|------------|----------------|------------|-------------|--|
| A1, B1  | PVDD1      | PWR            | 5000       |             | Supply voltage for Buck1 power stage, decouple with 10 $\mu$ F and connect to same source as AVDD          |
| A2, B2  | LX1        | AIO            | 5000       |             | Switch node of Buck1, connect a 100 nH inductor between LX1 and output capacitor                           |
| A3, B3  | PGND1      | GND            | 5000       |             | Buck1 power stage VSS rail   |
| A4, B4  | PGND2      | GND            | 5000       |             | Buck2 power stage VSS rail   |
| A5, B5  | LX2        | AIO            | 5000       |             | Switch node of Buck2, connect a 100 nH inductor between LX2 and output capacitor                           |
| A6, B6  | PVDD2      | PWR            | 5000       |             | Supply voltage for Buck2 power stage, decouple with 10 $\mu$ F and connect to same source as AVDD          |
| C1      | SCL/GPIO3  | DIO            | 15         |             | I <sup>2</sup> C clock or general purpose I/O  |
| C2      | SDA/GPIO4  | DIO            | 15         |             | I <sup>2</sup> C data or general purpose I/O   |
| C3      | IC_EN      | AI             | 10         |             | Powers up SW control interface and auxiliary circuitry (for example, bandgap, oscillator, and references). |
| C4      | CONF/GPIO0 | AI/DIO         | 10         |             | Chip configuration or general purpose I/O  |
| C5      | GPIO1      | DIO            | 10         |             | General purpose I/O  |
| C6      | GPIO2      | DIO            | 10         |             | General purpose I/O  |
| D1      | FB1N       | AI             | 10         |             | Buck1 negative node of differential voltage feedback, connect to VSS at point of load                      |
| D2      | FB1P       | AI             | 10         |             | Buck1 positive node of differential voltage feedback, connect to VOUT1 at point of load                    |

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| Pin No. | Pin Name | Type<br>(Table 2) | Drive<br>(mA) | Reset<br>State | Description  |
|---------|----------|-------------------|---------------|----------------|--|
| D3      | AVDD     | PWR               | 10            |                | Supply rail for analog control circuitry, decouple with 1 $\mu$ F and connect to same source as PVDD |
| D4      | AGND     | GND               | 10            |                | Analog control and auxiliary circuitry VSS   |
| D5      | FB2P     | AI                | 10            |                | Buck2 positive node of differential voltage feedback, connect to VOUT2 at point of load              |
| D6      | FB2N     | AI                | 10            |                | Buck2 negative node of differential voltage feedback, connect to VSS at point of load                |

**Table 2: Pin Type Definition**

| Pin Type | Description          | Pin Type | Description         |
|----------|----------------------|----------|---------------------|
| DI       | Digital input        | AI       | Analog input        |
| DO       | Digital output       | AO       | Analog output       |
| DIO      | Digital input/output | AIO      | Analog input/output |
| PWR      | Power                | GND      | Ground              |

## High-Performance Dual-Channel DC-DC Converter

### 3 Characteristics

#### 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 3: Absolute Maximum Ratings**

| Parameter        | Description           | Conditions | Min  | Max | Unit |
|------------------|-----------------------|------------|------|-----|------|
| T <sub>STG</sub> | Storage temperature   |            | -65  | 150 | °C   |
| T <sub>J</sub>   | Junction temperature  |            | -40  | 150 | °C   |
| V <sub>SYS</sub> | System supply voltage |            | -0.3 | 6.0 | V    |
| V <sub>PIN</sub> | Voltage on pins       |            | -0.3 | 6.0 | V    |

#### 3.2 Recommended Operating Conditions

**Table 4: Recommended Operating Conditions**

| Parameter        | Description           | Conditions (Note 1) | Min  | Typ | Max                    | Unit |
|------------------|-----------------------|---------------------|------|-----|------------------------|------|
| V <sub>SYS</sub> | System supply voltage |                     | 2.5  |     | 5.5                    | V    |
| V <sub>PIN</sub> | Voltage on pins       |                     | -0.3 |     | V <sub>SYS</sub> + 0.3 | V    |
| T <sub>J</sub>   | Junction temperature  |                     | -40  |     | 125                    | °C   |
| T <sub>A</sub>   | Ambient temperature   |                     | -40  |     | 85                     | °C   |

**Note 1** Within the specified limits, a lifetime of 10 years is guaranteed. If operating outside of these recommended conditions, please consult with Dialog Semiconductor.

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## 3.3 Thermal Characteristics

## 3.3.1 Thermal Ratings

Table 5: Package Ratings

| Parameter     | Description                          | Conditions | Min | Typ  | Max | Unit |
|---------------|--------------------------------------|------------|-----|------|-----|------|
| $\theta_{JA}$ | Package thermal resistance<br>Note 1 |            |     | 32.7 |     | °C/W |

**Note 1** Obtained from package thermal simulation, 2S2P4L board (JEDEC), influenced by PCB technology and layout.

## 3.3.2 Power Dissipation

Table 6: Power Dissipation

| Parameter | Description       | Conditions  | Min | Typ  | Max | Unit |
|-----------|-------------------|---|-----|------|-----|------|
| $P_D$     | Power dissipation | Derating factor above $T_A = 70^\circ\text{C}$ : 30.6 mW/°C (1/ $\theta_{JA}$ ) |     | 2140 |     | mW   |

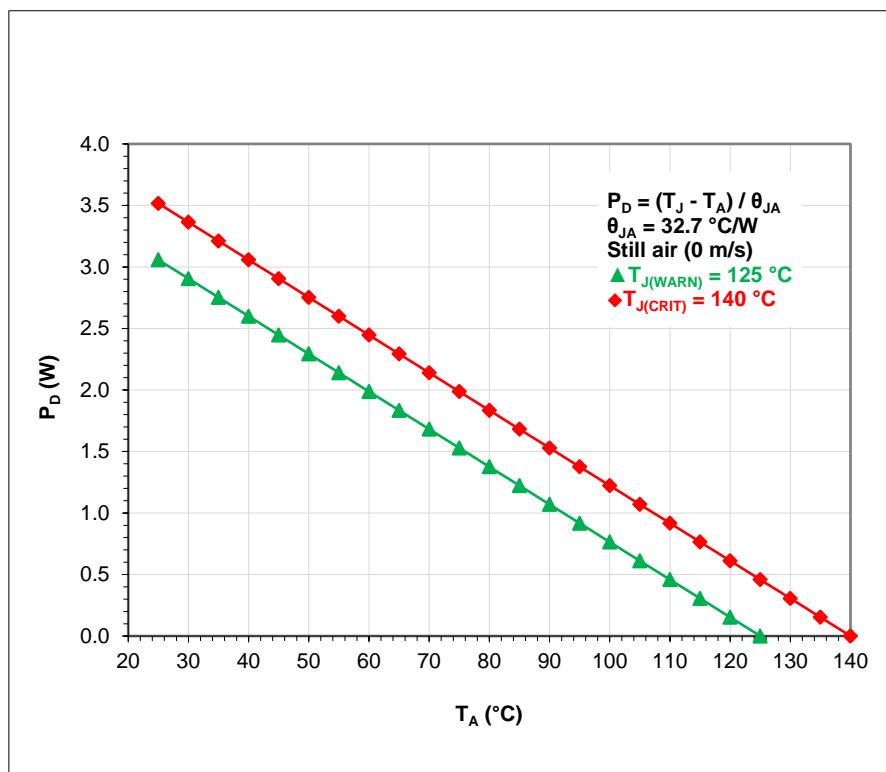


Figure 5: 24WLCSP Power Derating Curve

## 3.4 ESD Characteristics

Table 7: ESD Characteristics

| Parameter      | Description                            | Conditions | Min | Typ | Max | Unit |
|----------------|--|------------|-----|-----|-----|------|
| $V_{ESD\_HBM}$ | ESD protection, human body model (HBM) |            |     |     | 2   | kV   |

**High-Performance Dual-Channel DC-DC Converter****3.5 Buck Characteristics**

Unless otherwise noted, the following is valid for  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{\text{SYS}} = 2.5\text{ V}$  to  $5.5\text{ V}$

**Table 8: Buck Electrical Characteristics**

| Parameter                             | Description  | Conditions  | Min   | Typ           | Max   | Unit             |
|---------------------------------------|--|---|-------|---------------|-------|------------------|
| <b>External Electrical Conditions</b> |  |   |       |               |       |                  |
| $V_{\text{IN}}$                       | Input voltage  | $V_{\text{IN}} = V_{\text{SYS}}$  | 2.5   |               | 5.5   | V                |
| $C_{\text{OUT}}$                      | Output capacitance, per phase, including voltage and temperature coefficient |   | -40 % | $2 \times 10$ | +30 % | $\mu\text{F}$    |
| $\text{ESR}_{\text{COUT}}$            | Output capacitor series resistance, per phase                                | $f > 100\text{ kHz}$  |       | 2             |       | $\text{m}\Omega$ |
| $L$                                   | Inductor value, per phase, including current and temperature dependence      |   | -50 % | 0.1           | +20 % | $\mu\text{H}$    |
| $\text{DCR}_L$                        | Inductor DC resistance   |   |       | 30            | 50    | $\text{m}\Omega$ |
| <b>Electrical Performance</b>         |  |   |       |               |       |                  |
| $V_{\text{OUT}}$                      | Output voltage, programmable in 10 mV steps                                  | $I_{\text{OUT}} = 0\text{ mA}$ to $I_{\text{MAX}}$<br>$V_{\text{IN}} = 2.5\text{ V}$ to $5.5\text{ V}$                    | 0.3   |               | 1.57  | V                |
| $V_{\text{OUT\_LIM}}$                 | Output voltage, programmable in 10 mV steps                                  | $I_{\text{OUT}} = 0\text{ mA}$ to $I_{\text{MAX}}$<br>$V_{\text{IN}} = 3.0\text{ V}$ to $5.5\text{ V}$                    | 0.3   |               | 1.9   | V                |
| $I_{\text{LIM}}$                      | Current limit, programmable per phase<br><b>Note 1</b>                       | $\text{CHx\_ILIM} = 1010$   | -20 % | 8             | +20 % | A                |
| $V_{\text{OUT\_ACC}}$                 | Output voltage accuracy, including static line and load regulation           | $V_{\text{OUT}} \geq 1\text{ V}$  | -1    |               | 1     | %                |
| $V_{\text{OUT\_ACC}}$                 | Output voltage accuracy, including static line and load regulation           | $V_{\text{OUT}} < 1\text{ V}$   | -10   |               | 10    | mV               |
| $V_{\text{THR\_PG\_RISE}}$            | Power good voltage threshold for rising                                      | Referred to $V_{\text{OUT}}$  | -80   | -50           | -20   | mV               |
| $V_{\text{THR\_PG\_DWN}}$             | Power good voltage threshold for falling                                     | Referred to $V_{\text{OUT}}$  | -160  | -130          | -100  | mV               |
| $V_{\text{THR\_HV}}$                  | High $V_{\text{OUT}}$ voltage threshold                                      | Referred to $V_{\text{OUT}}$  | 100   | 150           | 200   | mV               |
| $V_{\text{OUT\_TR\_LINE}}$            | Line transient response  | $V_{\text{IN}} = 3\text{ V}$ to $3.6\text{ V}$<br>$I_{\text{OUT}} = 0.5 * I_{\text{MAX}}$<br>$dt = 10\text{ }\mu\text{s}$ |       | 15            |       | mV               |
| $f_{\text{sw}}$                       | Switching frequency, post-trim   |   |       | 4             |       | MHz              |

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| Parameter                  | Description   | Conditions  | Min | Typ     | Max | Unit             |
|----------------------------|---|---|-----|---------|-----|------------------|
| $t_{ON\_MIN}$              | Minimum turn-on pulse<br>0 % duty is also supported                                 |   |     | 20      |     | ns               |
| $t_{BUCK\_EN}$             | Turn-on time  | $CHx\_EN = \text{high}$   |     |         | 20  | $\mu\text{s}$    |
| $R_{PD}$                   | Output pull-down resistance<br>for each phase at the LX<br>node, see $CHx\_PD\_DIS$ | $V_{IN} = 3.7 \text{ V}$<br>$V_{OUT} = 0.5 \text{ V}$   | 100 | 150     | 200 | $\Omega$         |
| $R_{ON\_PMOS}$             | On resistance of switching<br>PMOS, per phase                                       | $V_{IN} = 3.7 \text{ V}$  |     | 36      |     | $\text{m}\Omega$ |
| $R_{ON\_NMOS}$             | On resistance of switching<br>NMOS, per phase                                       | $V_{IN} = 3.7 \text{ V}$  |     | 17      |     | $\text{m}\Omega$ |
| <b>AUTO Mode</b>           |   |   |     |         |     |                  |
| $V_{OUT\_TR\_LD\_1}$<br>PH | Load transient response   | 1-phase<br>$V_{OUT} = 1 \text{ V}$<br>$I_{OUT} = 0 \text{ A to } 5 \text{ A}$<br>$di/dt = 10 \text{ A}/\mu\text{s}$ |     | $\pm 5$ |     | %                |
| <b>PFM Mode</b>            |   |   |     |         |     |                  |
| $I_{Q\_PFM\_1PH}$          | Quiescent current in PFM  | 1-phase<br>$V_{IN} = 3.7 \text{ V}$<br>No load<br>No switching  |     | 88      |     | $\mu\text{A}$    |

**Note 1**  $t_{ON} > 40 \text{ ns}$

### 3.6 Performance and Supervision Characteristics

**Table 9: Electrical Characteristics**

| Parameter                     | Description                               | Conditions   | Min | Typ | Max  | Unit               |
|-------------------------------|---|--|-----|-----|------|--------------------|
| <b>Electrical Performance</b> |   |  |     |     |      |                    |
| $V_{THR\_POR}$                | Power-on-reset threshold                  | Threshold for AVDD falling                                       |     | 2.1 | 2.25 | V                  |
| $V_{THR\_POR\_HY}$<br>S       | Power-on-reset hysteresis                 |  |     | 200 |      | $\text{mV}$        |
| $T_{WARN}$                    | Thermal warning<br>temperature threshold  |  | 115 | 125 | 135  | $^{\circ}\text{C}$ |
| $T_{CRIT}$                    | Thermal shutdown<br>temperature threshold |  | 130 | 140 | 150  | $^{\circ}\text{C}$ |
| $I_{IN\_OFF}$                 | Supply current                            | OFF state<br>$T_A = 27 \text{ }^{\circ}\text{C}$<br>$IC\_EN = 0$ |     | 0.1 | 1    | $\mu\text{A}$      |

**High-Performance Dual-Channel DC-DC Converter**

| Parameter          | Description    | Conditions  | Min | Typ | Max | Unit |
|--------------------|----------------|---|-----|-----|-----|------|
| I <sub>IN_ON</sub> | Supply current | ON state<br>T <sub>A</sub> = 27 °C<br>IC_EN = 1<br>Buck off | 5   | 10  | 20  | µA   |

**3.7 Digital I/O Characteristics****Table 10: Digital I/O Electrical Characteristics**

| Parameter                     | Description                          | Conditions                                | Min       | Typ  | Max       | Unit |
|-------------------------------|--------------------------------------|---|-----------|------|-----------|------|
| <b>Electrical Performance</b> |                                      |   |           |      |           |      |
| V <sub>IH_EN</sub>            | Input high voltage, IC enable        |   | 1.2       |      | AVDD      | V    |
| V <sub>IL_EN</sub>            | Input low voltage, IC enable         |   |           |      | 0.4       | V    |
| t <sub>IC_EN</sub>            | IC enable time                       |   |           |      | 1000      | µs   |
| V <sub>IH_GPIO_SCL_SDA</sub>  | Input high voltage<br>GPIO, SCL, SDA |   | 1.2       |      | AVDD      | V    |
| V <sub>IL_GPIO_SCL_SDA</sub>  | Input low voltage<br>GPIO, SCL, SDA  |   |           |      | 0.4       | V    |
| V <sub>OH_GPIO</sub>          | Output high voltage<br>GPIO          | Push-pull mode<br>I <sub>OUT</sub> = 1 mA | 0.8*AV DD |      | AVDD      | V    |
| V <sub>OL_GPIO</sub>          | Output low voltage<br>GPIO           | Push-pull mode<br>I <sub>OUT</sub> = 1 mA |           |      | 0.2*AV DD | V    |
| V <sub>OL_SDA</sub>           | Output low voltage<br>SDA            | I <sub>OUT</sub> = 3 mA                   |           | 0.24 |           | V    |
| R <sub>PD</sub>               | GPIO pull-down resistor              |   | 2         | 10   | 120       | kΩ   |
| R <sub>PU</sub>               | GPIO pull-up resistor                |   | 2         | 10   | 120       | kΩ   |

**High-Performance Dual-Channel DC-DC Converter****3.8 Timing Characteristics****Table 11: I2C Electrical Characteristics**

| Parameter                     | Description                                      | Conditions            | Min          | Typ | Max  | Unit |
|-------------------------------|--|-----------------------|--------------|-----|------|------|
| <b>Electrical Performance</b> |  |                       |              |     |      |      |
| t <sub>BUS</sub>              | Bus free time between a STOP and START condition |                       | 0.5          |     |      | μs   |
| C <sub>BUS</sub>              | Bus line capacitive load                         |                       |              |     | 150  | pF   |
| f <sub>SCL</sub>              | SCL clock frequency                              |                       | 20<br>Note 1 |     | 1000 | kHz  |
| t <sub>LO_SCL</sub>           | SCL low time                                     |                       | 0.5          |     |      | μs   |
| t <sub>HI_SCL</sub>           | SCL high time                                    |                       | 0.26         |     |      | μs   |
| t <sub>RISE</sub>             | SCL and SDA rise time                            | Requirement for input |              |     | 1000 | ns   |
| t <sub>FALL</sub>             | SCL and SDA fall time                            | Requirement for input |              |     | 300  | ns   |
| t <sub>SETUP_START</sub>      | Start condition setup time                       |                       | 0.26         |     |      | μs   |
| t <sub>HOLD_START</sub>       | Start condition hold time                        |                       | 0.26         |     |      | μs   |
| t <sub>SETUP_STOP</sub>       | Stop condition setup time                        |                       | 0.26         |     |      | μs   |
| t <sub>DATA</sub>             | Data valid time                                  |                       |              |     | 0.45 | μs   |
| t <sub>DATA_ACK</sub>         | Data valid acknowledge time                      |                       |              |     | 0.45 | μs   |
| t <sub>SETUP_DATA</sub>       | Data setup time                                  |                       | 50           |     |      | ns   |
| t <sub>HOLD_DATA</sub>        | Data hold time                                   |                       | 0            |     |      | ns   |

**Note 1** Minimum clock frequency is limited to 20 kHz if I2C\_TIMEOUT is enabled

## High-Performance Dual-Channel DC-DC Converter

## 3.9 Typical Performance

Unless otherwise noted,  $V_{IN} = 3.7\text{ V}$ ,  $V_{OUT} = 1.0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , 2.0 mm x 1.6 mm 0.1  $\mu\text{H}$  output inductor (DCR = typ. 11.5 m $\Omega$ ) and 2 x 10  $\mu\text{F}$  output capacitors per-channel.

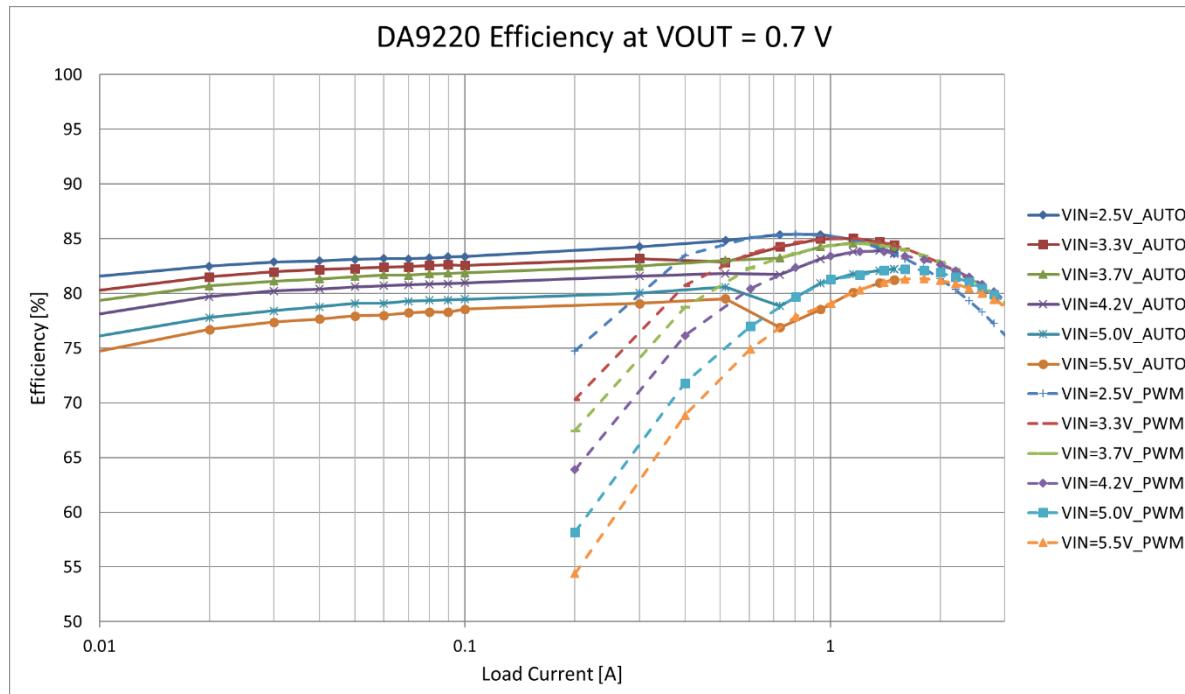


Figure 6: Efficiency vs Load,  $V_{OUT} = 0.7\text{ V}$

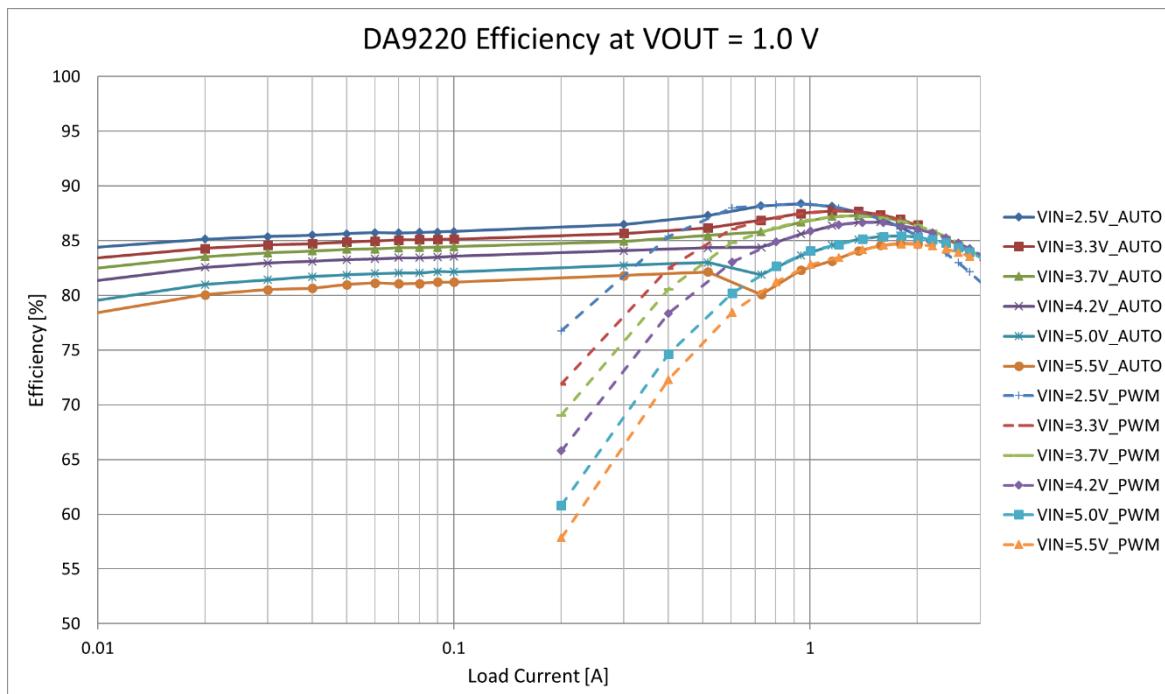


Figure 7: Efficiency vs Load,  $V_{OUT} = 1.0\text{ V}$

## High-Performance Dual-Channel DC-DC Converter

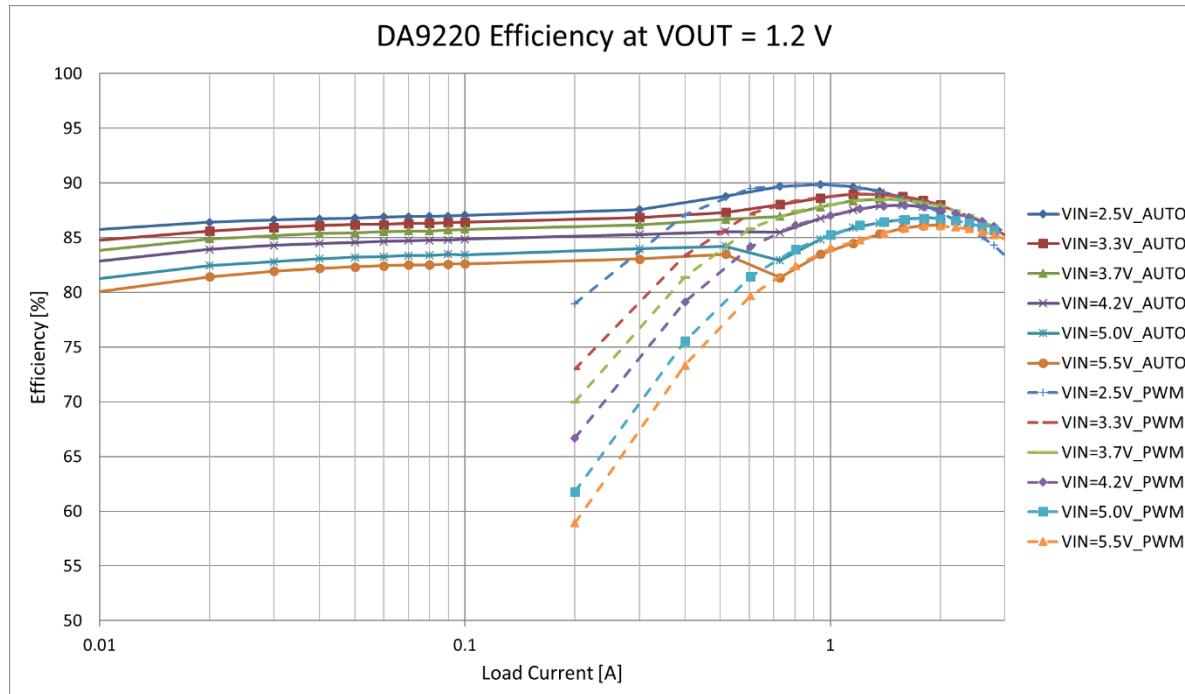


Figure 8: Efficiency vs Load, VOUT = 1.2 V

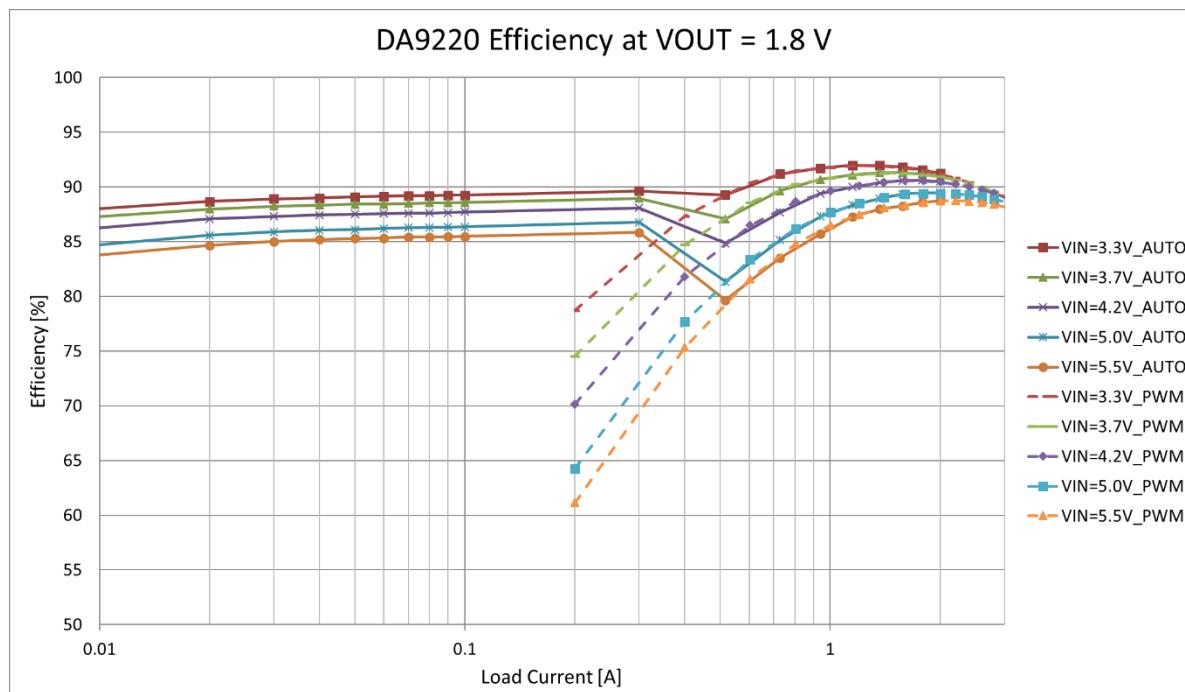


Figure 9: Efficiency vs Load, VOUT = 1.8 V

## High-Performance Dual-Channel DC-DC Converter

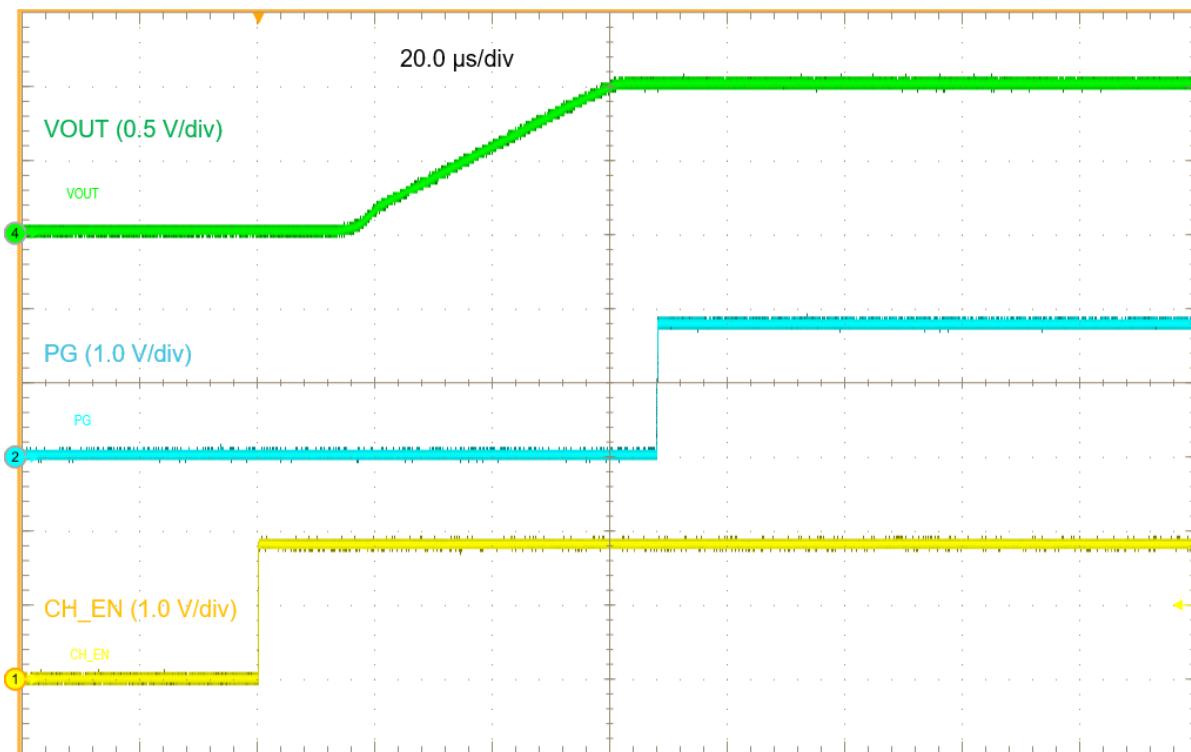


Figure 10: Buck Soft Start-up at 20 mV/μs Slew Rate

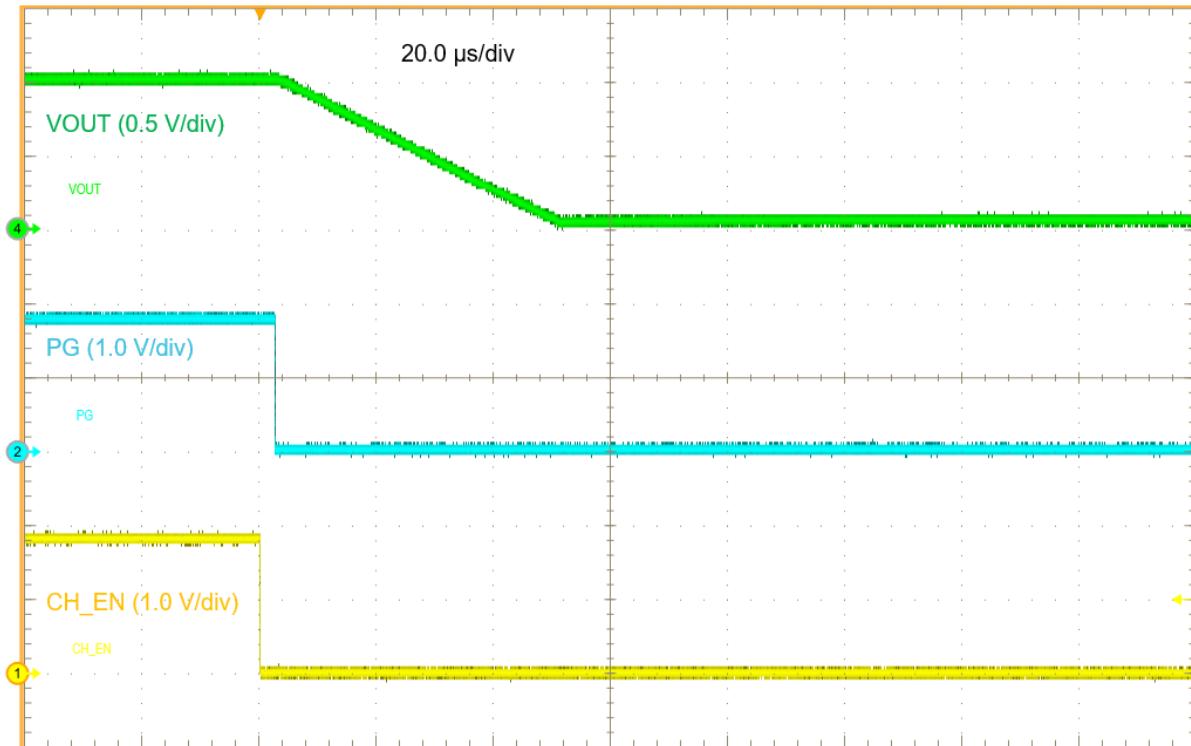


Figure 11: Buck Active Shutdown at 20 mV/μs Slew Rate

## High-Performance Dual-Channel DC-DC Converter

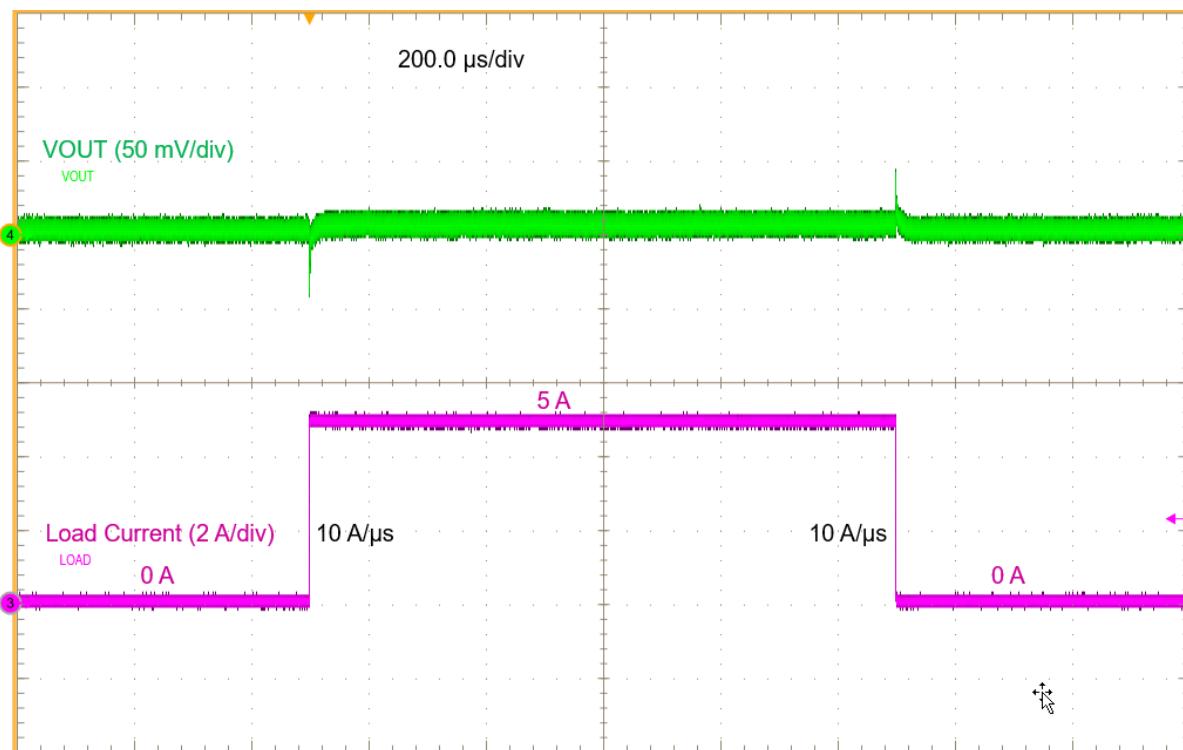


Figure 12: Buck Load Transient Response in PWM Mode, 0 A to 5 A at 10 A/μs

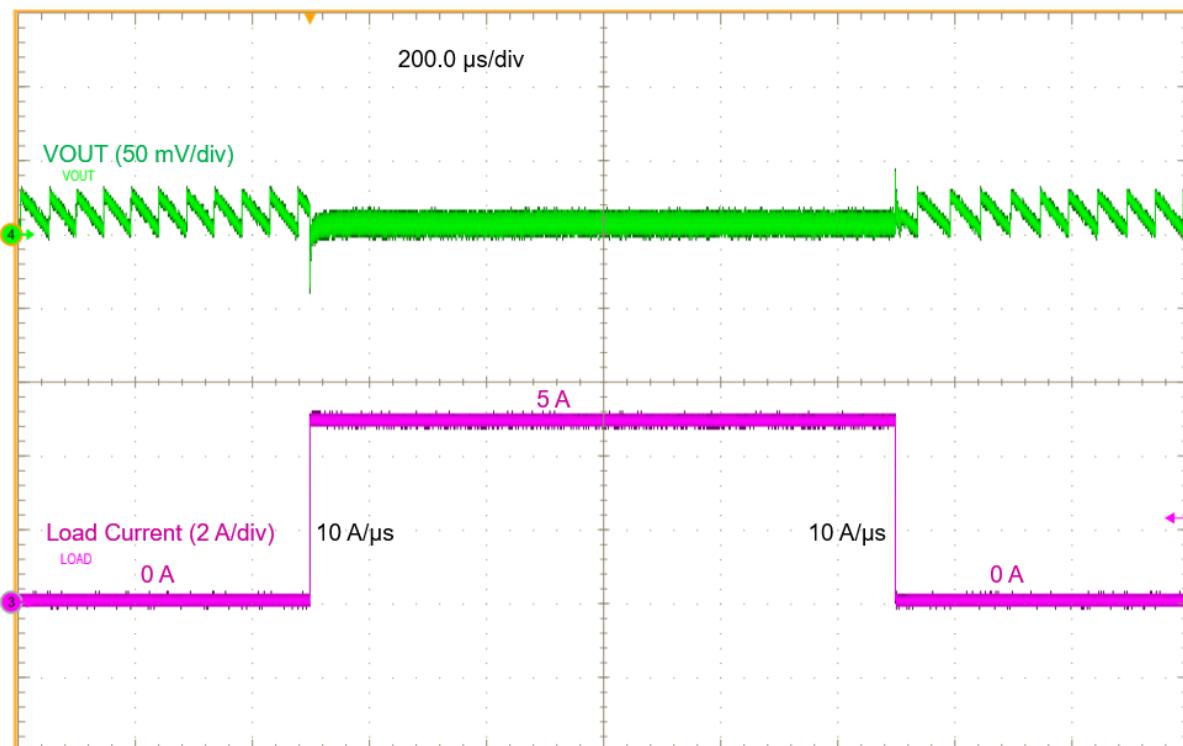


Figure 13: Buck Load Transient Response in AUTO Mode, 0 A to 5 A at 10 A/μs

## 4 Functional Description

### 4.1 DC-DC Buck Converter

DA9220 contains two buck converters, Buck1 and Buck2, each capable of delivering up to 3 A output current at a 0.3 V to 1.9 V output voltage range.

Buck1 and Buck2 have two voltage registers each. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way, different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored and a power good signal indicates that the buck output voltage has reached a level higher than the  $V_{THR\_PG\_RISE}$  threshold. The power good status is lost when the voltage drops below  $V_{THR\_PG\_DWN}$  or increases above  $V_{THR\_HV}$ . For each of the buck converters the status of the power good indicator can be read back via I<sup>2</sup>C from the PG1 and PG2 status bits. It can be also individually assigned to any of the GPIOs by setting the GPIO mode registers to either PG1 or PG2 output.

The buck converters are capable of supporting DVC transitions that occur:

- When the active and selected A- or B-voltage is updated to a new target value.
- When the voltage selection is changed from the A- to B-voltage (or B- to A-voltage) using CH<x>\_VSEL.

The DVC controller operates in pulse width modulation (PWM) mode with synchronous rectification.

The slew rate of the DVC transition is individually programmed for each buck converter at 10 mV per 8  $\mu$ s, 4  $\mu$ s, 2  $\mu$ s, 1  $\mu$ s, or 0.5  $\mu$ s in register bits CH1\_SR\_DVC and CH2\_SR\_DVC.

A pull-down resistor (typically 150  $\Omega$ ) for each phase is always activated unless it is disabled by setting register bits CH<x>\_PD\_DIS to 1.

#### 4.1.1 Switching Frequency

The buck switching frequency can be tuned using register bit OSC\_TUNE. The internal 8 MHz oscillator frequency is tuned in  $\pm 160$  kHz steps. This impacts the buck converter frequency in steps of 80 kHz and helps to mitigate possible disturbances to other high frequency systems in the application.

#### 4.1.2 Operation Modes and Phase Selection

The buck converters can operate in PWM and PFM modes. The operating mode is selected using register bits CH1\_<A or B>\_MODE and CH2\_<A or B>\_MODE.

If the automatic operation mode is selected on CH1\_<A or B>\_MODE or CH2\_<A or B>\_MODE, the buck converters automatically change between synchronous PWM mode and PFM depending on the load current. This improves the efficiency across the whole range of output load currents.

## High-Performance Dual-Channel DC-DC Converter

### 4.1.3 Output Voltage Selection

The switching converter can be configured using the I<sup>2</sup>C interface.

For each buck converter two output voltages can be pre-configured in registers CH<x>\_<A or B>\_VOUT. The output voltage can be selected by either toggling register bit CH<x>\_VSEL or by re-programming the selected voltage control register. Both changes will result in ramped voltage transitions. After being enabled, the buck converter will, by default, use the register settings in CH<x>\_A\_VOUT unless the output voltage selection is configured via the GPIO port.

Registers CH<1 and 2>\_VMAX limit the output voltage that can be set for each of the respective buck converters.

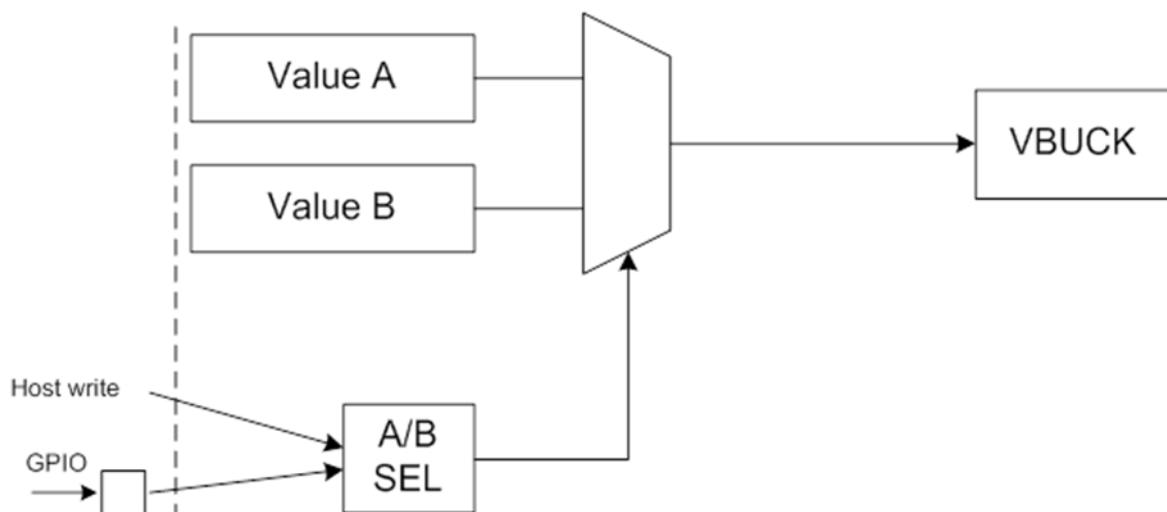


Figure 14: Buck Output Voltage Control Concept

### 4.1.4 Soft Start-Up and Shutdown

To limit in-rush current from VSYS, the buck converters can perform a soft-start after being enabled. The start-up behavior is a compromise between acceptable inrush current from the battery and turn-on time. Individual ramp times can be configured for each buck converter in registers CH<1 and 2>\_SR\_STARTUP respectively. Rates higher than 20 mV/μs may produce overshoot during the start-up phase, so they should be considered carefully.

A ramped power down can be selected in register bits CH<1 and 2>\_SR\_SHDN. When no ramp is selected (immediate power down), the output node will be discharged only by the pull-down resistor, if enabled in registers CH<1 and 2>\_PD\_DIS.

### 4.1.5 Current Limit

The integrated current limit protects the power stages and external coil from excessive current. The buck current limit should be configured to at least 40 % higher than the required maximum output current.

When the current limit is reached, each buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using register M\_OC<x> in SYS\_MASK\_1. Register bits OC\_DVC\_MASK is used to mask over-current events during DVC transitions.

## High-Performance Dual-Channel DC-DC Converter

## 4.1.6 Thermal Protection

DA9220 is protected from internal overheating by thermal shutdown.

There are two kinds of flags concerning thermal protection, thermal warning and thermal critical. The warning flag is asserted when  $T_J > T_{WARM}$  and the critical flag is asserted when  $T_J > T_{CRIT}$ . When the critical flag is asserted, Buck1 and 2 are shut down immediately.

Table 12: Thermal Protection Control Registers

| Category  | Register name | Description   |
|-----------|---------------|---|
| Status    | TEMP_WARN     | Asserted as long as the thermal warning threshold is reached  |
|           | TEMP_CRIT     | Asserted as long as the thermal shutdown threshold is reached |
| IRQ event | E_TEMP_WARN   | TEMP_WARN caused event  |
|           | E_TEMP_CRIT   | TEMP_CRIT caused event  |
| IRQ mask  | M_TEMP_WARN   | TEMP_WARN event IRQ mask                                      |
|           | M_TEMP_CRIT   | TEMP_CRIT event IRQ mask                                      |
|           | M_VR_HOT      | TEMP_WARN status IRQ mask                                     |

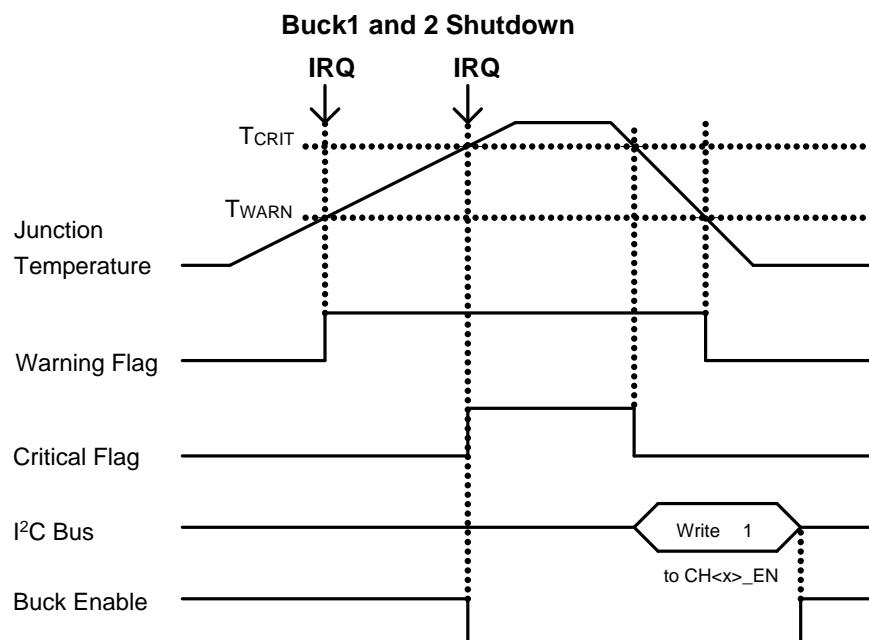


Figure 15: Thermal Protection Operation

## High-Performance Dual-Channel DC-DC Converter

## 4.2 Internal Circuits

## 4.2.1 IC\_EN/Chip Enable/Disable

IC\_EN is chip enable/disable control input. When IC\_EN = 0, all blocks except for low  $I_Q$  POR are powered-down and buck output is pulled-down.

## 4.2.2 nIRQ/Interrupt

The interrupt triggers events. Trigger conditions and control registers for each interrupt event are listed in [Table 13](#).

Some of these events are categorized as fault events and affect device operation (for example, buck disable), see Section [4.1.6](#).

**Table 13: Interrupt List**

| Name                        | Polarity<br>( <a href="#">Note 1</a> ) | Trigger  | IRQ Status<br>Register | IRQ Mask<br>Register | Deglitch<br>Period               |
|-----------------------------|--|--|------------------------|----------------------|----------------------------------|
| Thermal warning (event)     | N                                      | $T_J$ rising above $T_{WARN}$  | E_TEMP_WARN            | M_TEMP_WARN          | 0 s                              |
| Thermal critical (event)    | N                                      | $T_J$ rising above $T_{CRIT}$  | E_TEMP_CRIT            | M_TEMP_CRIT          | 0 s                              |
| System good (event)         | P                                      |  | E_SG                   | M_SG                 | 0 s                              |
| Buck1 power-good (event)    | P                                      | Buck1 $V_{OUT}$ is in power-good voltage range (not under- or over-voltage)            | E_PG1                  | M_PG1                | 0 s                              |
| Buck2 power-good (event)    | P                                      | Buck2 $V_{OUT}$ is in power-good voltage range (not under- or over-voltage)            | E_PG2                  | M_PG2                | 0 s                              |
| Buck1 over-voltage (event)  | N                                      | Buck1 $V_{OUT}$ rising above over-voltage threshold (target voltage + 150 mV)          | E_OV1                  | M_OV1                | Rise:8 $\mu$ s<br>Fall:8 $\mu$ s |
| Buck2 over-voltage (event)  | N                                      | Buck2 $V_{OUT}$ rising above over-voltage threshold (target voltage + 150 mV)          | E_OV2                  | M_OV2                | Rise:8 $\mu$ s<br>Fall:8 $\mu$ s |
| Buck1 under-voltage (event) | N                                      | Buck1 $V_{OUT}$ falling below under-voltage threshold (target voltage - $V_{TH\_PG}$ ) | E_UV1                  | M_UV1                | 0 s                              |
| Buck2 under-voltage (event) | N                                      | Buck2 $V_{OUT}$ falling below under-voltage threshold (target voltage - $V_{TH\_PG}$ ) | E_UV2                  | M_UV2                | 0 s                              |
| Buck1 over-current (event)  | N                                      | Buck1 current rising above over-current threshold                                      | E_OC1                  | M_OC1                | 0 s                              |

**High-Performance Dual-Channel DC-DC Converter**

| Name                               | Polarity<br>(Note 1) | Trigger  | IRQ Status<br>Register | IRQ Mask<br>Register | Deglitch<br>Period                   |
|------------------------------------|----------------------|--|------------------------|----------------------|--------------------------------------|
| Buck2 over-current (event)         | N                    | Buck2 current rising above over-current threshold                                  | E_OC2                  | M_OC2                | 0 s                                  |
| Buck1 power-good (status) (Note 2) | P                    | Buck1 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage) | PG1                    | M_PG1_STAT (Note 3)  | 0 s                                  |
| Buck2 power-good (status) (Note 2) | P                    | Buck2 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage) | PG2                    | M_PG2_STAT (Note 3)  | 0 s                                  |
| System good (status) (Note 2)      | P                    |  | SG                     | M_SG_STAT (Note 3)   | 0 s                                  |
| Thermal warning (status) (Note 2)  | N                    | T <sub>J</sub> rising above T <sub>WARN</sub>                                      | TEMP_WARN              | M_VR_HOT (Note 3)    | 0 s                                  |
| GPIO0 change (event)               | N                    | Detect GPIO0 change for active trigger selected GPIO0_TRIG register                | E_GPIO0                | M_GPIO0              | 100 µs/<br>1 ms/<br>10 ms/<br>100 ms |
| GPIO1 change (event)               | N                    | Detect GPIO1 change for active trigger selected GPIO1_TRIG register                | E_GPIO1                | M_GPIO1              |                                      |
| GPIO2 change (event)               | N                    | Detect GPIO2 change for active trigger selected GPIO2_TRIG register                | E_GPIO2                | M_GPIO2              |                                      |

**Note 1** Polarity at the source of the flag: P = active-high, N = active-low.

General rule is: normal system state is high, and abnormal system state is low (for example, PG = high means power-good, TEMP\_CRIT = low when TEMP critical state).

**Note 2** Interrupt outputs the status as is. I<sup>2</sup>C write is not required for interrupt clear.

**Note 3** OTP load value defined by CONF pin setting if CONF\_EN = 1.

**High-Performance Dual-Channel DC-DC Converter****Table 14: Interrupt Registers Except for Power Good Status**

| Register | Description   |
|----------|---|
| E_<name> | Read-only interrupt event register<br>0: No interrupt<br>1: Interrupt occurred<br><b>Cleared after being written to I<sup>2</sup>C.</b> Set until IRQ is removed. |
| M_<name> | Interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Event register (E_<name>) is updated.  |

**Table 15: Interrupt Registers for Power Good, System Good, and Temp Warning Status**

| Register     | Description  |
|--------------|--|
| PG<x>        | Buck<x> power good status. Asserted as long as the buck<x> output voltage is in range (under-voltage threshold < buck output voltage < over-voltage threshold)<br>0: Not power good<br>1: Power good |
| M_PG<x>_STAT | Power good status interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Power good status register (PG<x>) is updated   |
| SG           | System good status<br>0: Not system good<br>1: System good   |
| M_SG_STAT    | System good status (SG) interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. System good status register (SG) is updated   |
| TEMP_WARN    | Asserted as long as the thermal warning threshold (T <sub>WARN</sub> ) is reached<br>0: Junction temperature is below T <sub>WARN</sub><br>1: Junction temperature is above T <sub>WARN</sub>        |
| M_VR_HOT     | Temperature warning status (TEMP_WARN) interrupt mask register<br>0: Not masked<br>1: Masked. No IRQ signal sent. Temperature warning status register (TEMP_WARN) is updated                         |

## High-Performance Dual-Channel DC-DC Converter

Condition

- GPIO is configured as nIRQ
- M\_TEMP\_WARN = 0
- M\_PG#\_STAT = 0

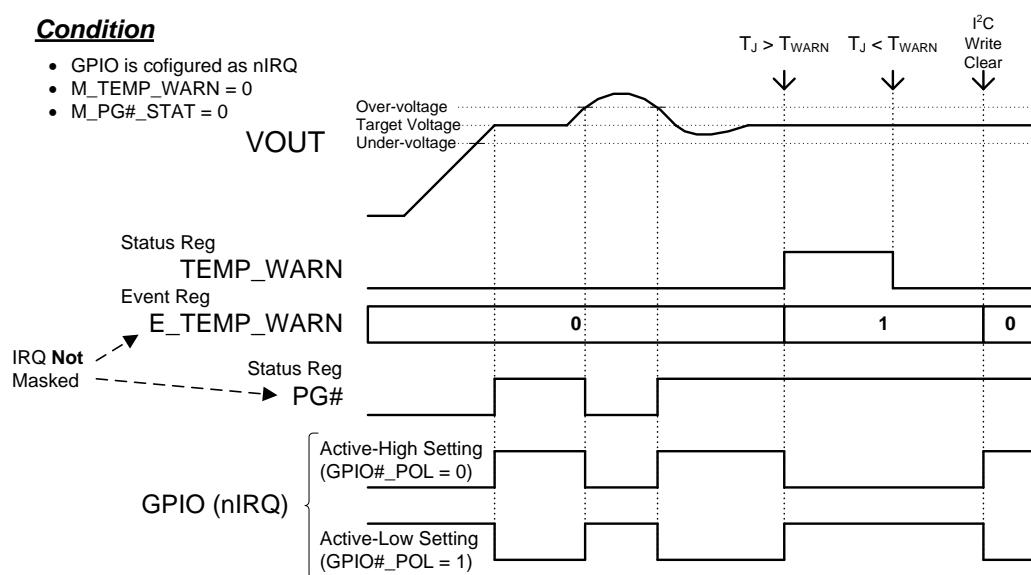


Figure 16: Interrupt Operation Example 1

Condition

- GPIO is configured as nIRQ
- M\_VR\_HOT = 0
- M\_PG1\_STAT = 0
- M\_PG2\_STAT = 0

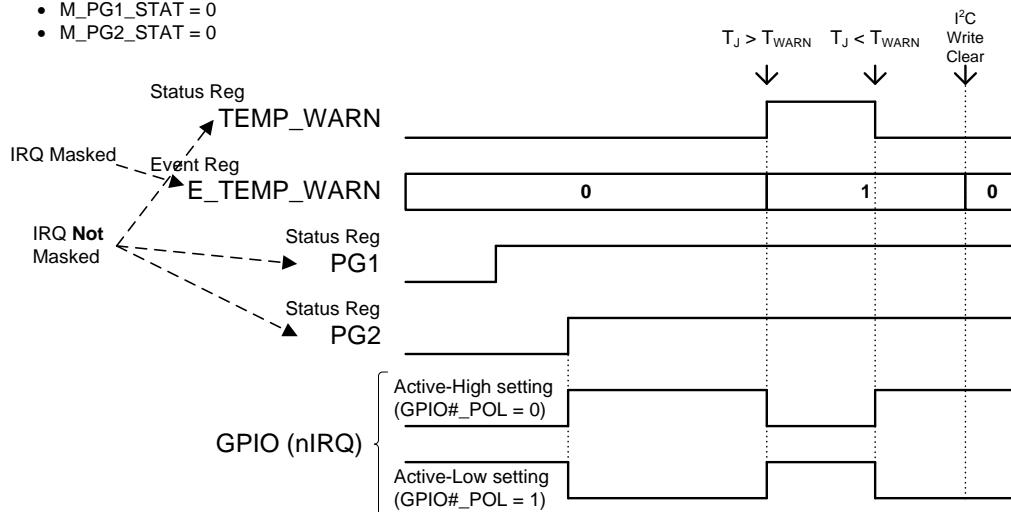


Figure 17: Interrupt Operation Example 2

## High-Performance Dual-Channel DC-DC Converter

Condition

- GPIO is configured as nIRQ
- **M\_SG = 0**

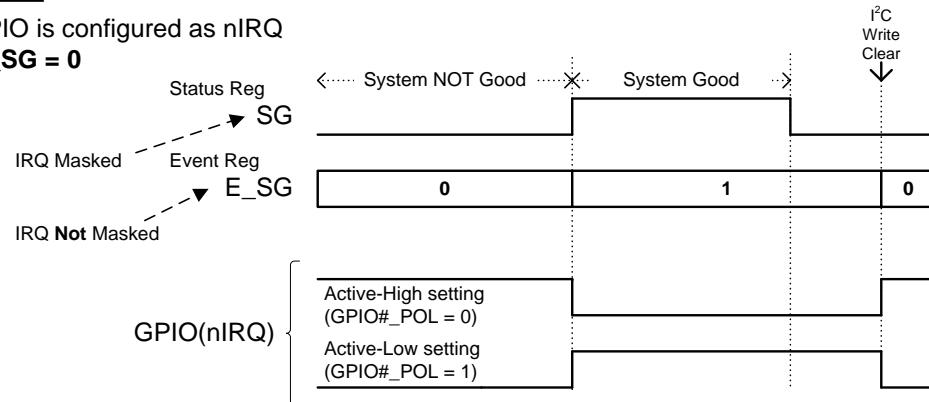


Figure 18: Interrupt Operation Example 3

Condition

- GPIO is configured as nIRQ
- **M\_SG\_STAT = 0**

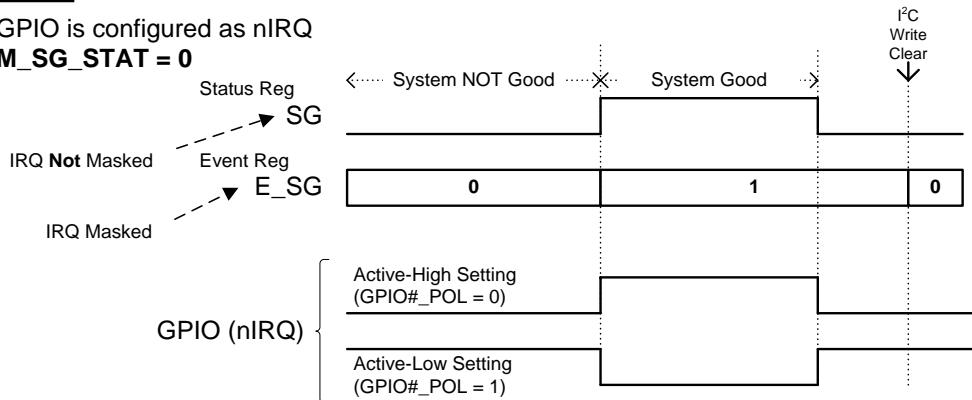


Figure 19: Interrupt Operation Example 4

**High-Performance Dual-Channel DC-DC Converter****4.2.3 GPIO****4.2.3.1 GPIO Pin Assignment**

The DA9220 provides up to five GPIO pins, three if the I<sup>2</sup>C is enabled, see [Table 16](#). These registers are OTP programmable. When CONF\_EN = 1 GPIO0 can be used for chip configuration.

Any register settings for GPIO3 and GPIO4 are ignored and GPIO3 and GPIO4 function as SCL and SDA respectively if I2C\_EN = 1.

**Table 16: GPIO Pin Assignment**

| OTP Option |         | GPIO Pin       |       |       |               |               | Available<br>GPIOs |
|------------|---------|----------------|-------|-------|---------------|---------------|--------------------|
| I2C_EN     | CONF_EN | CONF/<br>GPIO0 | GPIO1 | GPIO2 | SCL/<br>GPIO3 | SDA/<br>GPIO4 |                    |
| 1'b0       | 1'b0    | GPIO0          | GPIO1 | GPIO2 | GPIO3         | GPIO4         | 5                  |
|            | 1'b1    | CONF           | GPIO1 | GPIO2 | GPIO3         | GPIO4         | 4                  |
| 1'b1       | 1'b0    | GPIO0          | GPIO1 | GPIO2 | SCL           | SDA           | 3                  |
|            | 1'b1    | CONF           | GPIO1 | GPIO2 | SCL           | SDA           | 2                  |

**4.2.3.2 GPIO Function**

The GPIOs pins are configurable as the following functions in register GPIO<x>\_MODE (x = 0 to 4):

- Buck1 enable input (EN1)
- Buck2 enable input (EN2)
- Buck1 and Buck2 enable input (EN1 & EN2)
- Buck1 DVC control input (DVC1)
- Buck2 DVC control input (DVC2)
- Buck1 and Buck2 DVC control input (DVC1 & DVC2)
- Buck1 and Buck2 OTP setting reload input (RELOAD)
- Buck1 power good output (PG1)
- Buck2 power good output (PG2)
- Buck1 power good and Buck2 power good output (PG1 & PG2)
- System good output (SG)
- Interrupt output (nIRQ)

**Table 17: GPIO Function Configuration**

| GPIO<x>_MODE[3:0] | Function     | IO Condition |
|-------------------|--------------|--------------|
| 4'h0              | GPIO disable | HiZ          |
| 4'h1              | EN1          | In           |
| 4'h2              | EN2          | In           |
| 4'h3              | EN1 & EN2    | In           |
| 4'h4              | DVC1         | In           |
| 4'h5              | DVC2         | In           |
| 4'h6              | DVC1 & DVC2  | In           |
| 4'h7              | RELOAD       | In           |
| 4'h8              | PG1          | Out          |

## High-Performance Dual-Channel DC-DC Converter

| GPIO<x>_MODE[3:0] | Function   | IO Condition |
|-------------------|------------|--------------|
| 4'h9              | PG2        | Out          |
| 4'hA              | PG1 & PG2  | Out          |
| 4'hB              | SG         | Out          |
| 4'hC              | nIRQ       | Out          |
| 4'hD              | Reserved   | HiZ          |
| 4'hE              | Low level  | Out          |
| 4'hF              | High level | Out          |

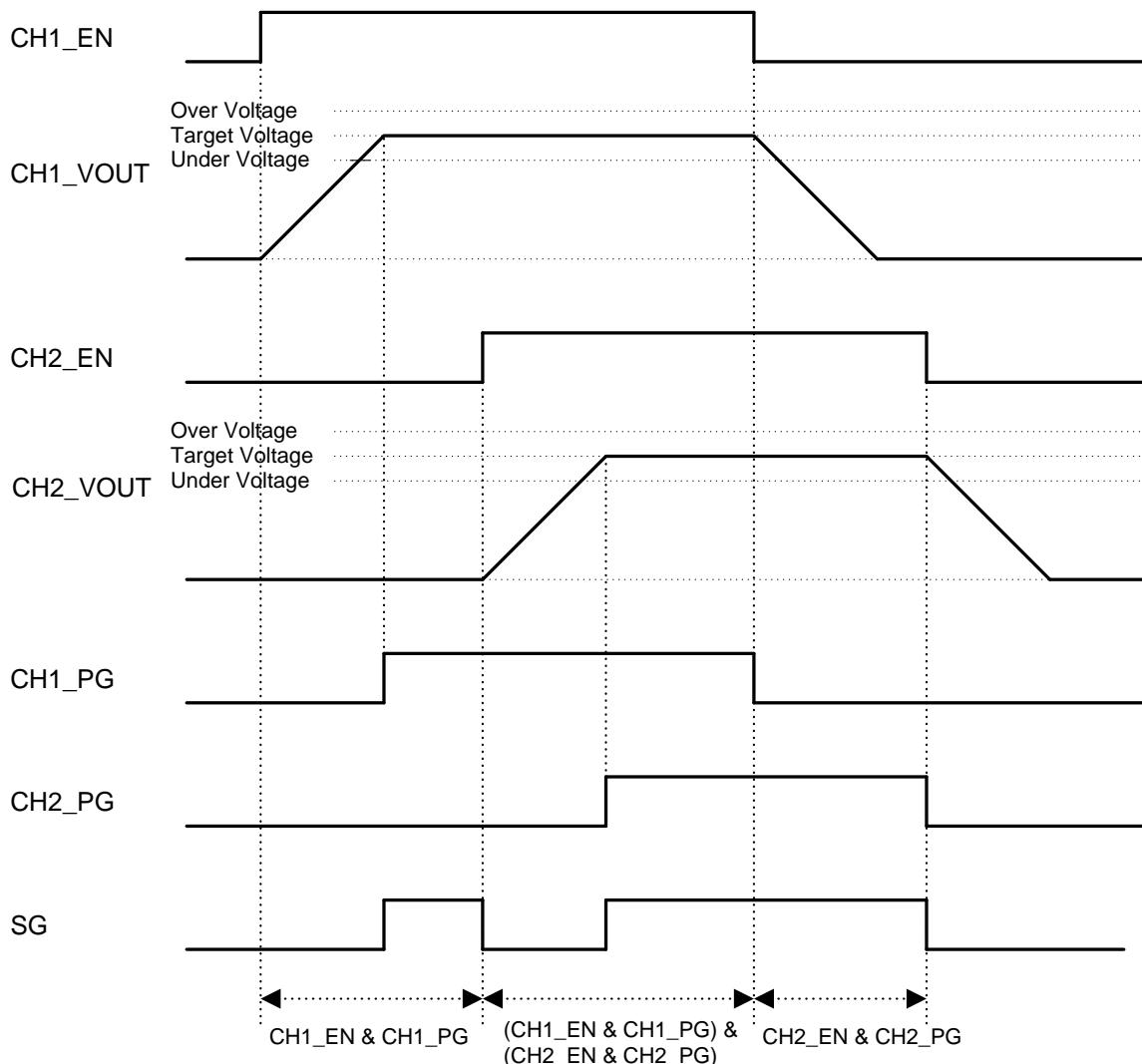


Figure 20: Power Good (PG) and System Good (SG)

## High-Performance Dual-Channel DC-DC Converter

## 4.2.3.3 Chip Configuration Select (CONF)

GPIO0 functions as chip configuration select (CONF) input when CONF\_EN = 1.

Three different chip configurations can be selected according to the CONF pin level, whether it is HIGH, LOW, or Hi-Z.

**Table 18: GPIO0-Configurable Registers when CONF\_EN = 1**

| Register Name      | Description                                |
|--------------------|--|
| IF_SLAVE_ADDR[6:0] | I2C slave address                          |
| CH1_A_MODE[1:0]    | CH1_A Operation mode select                |
| CH1_B_MODE[1:0]    | CH1_B Operation mode select                |
| CH1_VSEL           | CH1 output voltage and operation selection |
| CH1_EN             | CH1 enable                                 |
| CH1_A_VOUT[7:0]    | CH1 output voltage setting A               |
| CH1_B_VOUT[7:0]    | CH1 output voltage setting B               |
| CH2_A_MODE[1:0]    | CH2_A Operation mode select                |
| CH2_B_MODE[1:0]    | CH2_B Operation mode select                |
| CH2_VSEL           | CH2 output voltage and operation selection |
| CH2_EN             | CH2 enable                                 |
| CH2_A_VOUT[7:0]    | CH2 output voltage setting A               |
| CH2_B_VOUT[7:0]    | CH2 output voltage setting B               |
| M_PG1_STAT         | IRQ mask setting for CH1 power good status |
| M_PG2_STAT         | IRQ mask setting for CH2 power good status |
| M_SG_STAT          | IRQ mask setting for system good status    |
| M_VR_HOT           | IRQ mask setting for temp warning status   |
| CH1_EN_DLY[3:0]    | Delay setting for CH1 enable               |
| CH1_DIS_DLY[3:0]   | Delay setting for CH1 disable              |
| CH2_EN_DLY[3:0]    | Delay setting for CH2 enable               |
| CH2_DIS_DLY[3:0]   | Delay setting for CH2 disable              |
| GPIO1_MODE[3:0]    | GPIO1 mode setting                         |
| GPIO2_MODE[3:0]    | GPIO2 mode setting                         |
| GPIO1_OBUF         | GPIO1 output buffer select                 |
| GPIO2_OBUF         | GPIO2 output buffer select                 |
| GPIO1_TRIG[1:0]    | GPIO1 input trigger select                 |
| GPIO1_POL          | GPIO1 polarity select                      |
| GPIO1_PUPD         | GPIO1 pull-up/pull-down enable             |
| GPIO1_DEB[1:0]     | GPIO1 input debounce time setting          |
| GPIO1_DEB_RISE     | GPIO1 input debounce rising edge enable    |
| GPIO1_DEB_FALL     | GPIO1 input debounce falling edge enable   |
| GPIO2_TRIG[1:0]    | GPIO2 input trigger select                 |
| GPIO2_POL          | GPIO2 polarity select                      |

## High-Performance Dual-Channel DC-DC Converter

| Register Name  | Description                              |
|----------------|--|
| GPIO2_PUPD     | GPIO2 pull-up/pull-down enable           |
| GPIO2_DEB[1:0] | GPIO2 input debounce time setting        |
| GPIO2_DEB_RISE | GPIO2 input debounce rising edge enable  |
| GPIO2_DEB_FALL | GPIO2 input debounce falling edge enable |

### 4.2.3.4 OTP Reload (RELOAD)

Buck settings listed in **Error! Reference source not found.** are reloaded from CONF registers by triggering GPIO configured as RELOAD input.

The OTP reload happens at the same time for Buck1 and Buck2 settings. During reloading, Buck1/2 keep operating as configured without shut-down.

**Table 19: OTP Reload Registers**

| Register Name   | Description   |
|-----------------|---|
| CH#_VSEL        | CH# output voltage and operation selection.<br>0: A, 1: B   |
| CH#_A_VOUT[7:0] | CH# output voltage setting A : CH#_A_VOUT * 10 mV<br>Setting under 0.3V is clamped to 0.3V, and setting over 1.9V is clamped to 1.9 V   |
| CH#_B_VOUT[7:0] | CH# output voltage setting B : CH#_A_VOUT * 10 mV<br>Setting under 0.3 V is clamped to 0.3 V, and setting over 1.9V is clamped to 1.9 V |
| CH#_A_MODE[1:0] | Operation mode selection<br>0: Force PFM<br>1: Force PWM. full phase<br>2: Force PWM with phase shedding<br>3: Auto mode                |
| CH#_B_MODE[1:0] | Operation mode selection<br>0: Force PFM<br>1: Force PWM. full phase<br>2: Force PWM with phase shedding<br>3: Auto mode                |

## 4.3 Operating Modes

### 4.3.1 ON

DA9220 is ON when the IC\_EN port is higher than  $V_{IH\_EN}$  and the supply voltage is higher than  $V_{THR\_POR}$ . Once enabled, the host processor can start communicating with DA9220 using the control interface, after the  $t_{IC\_EN}$  delay.

### 4.3.2 OFF

DA9220 is OFF when the IC\_EN port is lower than  $V_{IL\_EN}$ . In OFF, the bucks are always disabled and LX nodes are pulled down by (typically 150  $\Omega$ ) internal pull-down resistors.

## 4.4 I<sup>2</sup>C Communication

All features of DA9220 can be controlled with the I<sup>2</sup>C interface which is enabled or disabled in register I2C\_EN.

## High-Performance Dual-Channel DC-DC Converter

| I <sup>2</sup> C_EN | Description  |
|---------------------|--|
| 0                   | I <sup>2</sup> C disable: SCL/GPIO3 and SDA/GPIO4 pins can be used as GPIO   |
| 1                   | I <sup>2</sup> C enable: SCL/GPIO3 and SDA/GPIO4 pins are used as I <sup>2</sup> C clock input and I <sup>2</sup> C data input/output. |

GPIO3 functions as the I<sup>2</sup>C clock and GPIO4 carries all the power manager bidirectional I<sup>2</sup>C data. The I<sup>2</sup>C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The standard frequency of the I<sup>2</sup>C bus is 1 MHz in fast-mode plus (FM+), 400 kHz in fast-mode, or 100 kHz in standard mode.

### 4.4.1 I<sup>2</sup>C Protocol

All data is transmitted across the I<sup>2</sup>C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).



Figure 21: I<sup>2</sup>C START and STOP Condition Timing

The I<sup>2</sup>C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 22 and Figure 23).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9220 responds to all bytes with acknowledgement (A), see Figure 22.

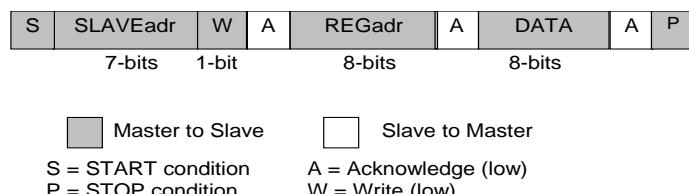
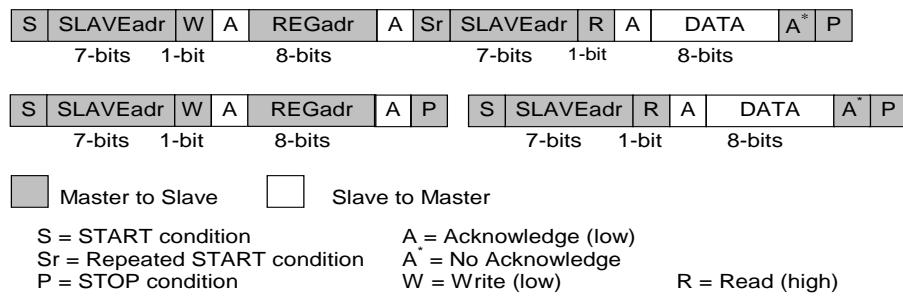


Figure 22: I<sup>2</sup>C Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9220 with the target register address and then read from DA9220 with a repeated START, or alternatively a second START, condition. After receiving the data, the host sends no acknowledgement (A\*) and terminates the transmission with a STOP condition, see Figure 23.

**High-Performance Dual-Channel DC-DC Converter****Figure 23: I<sup>2</sup>C Byte Read (SDA Line) Examples**

**High-Performance Dual-Channel DC-DC Converter****5 Register Definitions****5.1 Register Map****Table 20: Register Map**

| Addr                 | Register     | 7                | 6                | 5              | 4                | 3               | 2         | 1               | 0           |
|----------------------|--------------|------------------|------------------|----------------|------------------|-----------------|-----------|-----------------|-------------|
| <b>System Module</b> |              |                  |                  |                |                  |                 |           |                 |             |
| <b>System</b>        |              |                  |                  |                |                  |                 |           |                 |             |
| 0x0001               | SYS_STATUS_0 | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | SG        | TEMP_CRIT       | TEMP_WARN   |
| 0x0002               | SYS_STATUS_1 | PG2              | OV2              | UV2            | OC2              | PG1             | OV1       | UV1             | OC1         |
| 0x0003               | SYS_STATUS_2 | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | GPIO2     | GPIO1           | GPIO0       |
| 0x0004               | SYS_EVENT_0  | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | E_SG      | E_TEMP_C_RIT    | E_TEMP_WARN |
| 0x0005               | SYS_EVENT_1  | E_PG2            | E_OV2            | E_UV2          | E_OC2            | E_PG1           | E_OV1     | E_UV1           | E_OC1       |
| 0x0006               | SYS_EVENT_2  | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | E_GPIO2   | E_GPIO1         | E_GPIO0     |
| 0x0007               | SYS_MASK_0   | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | M_SG      | M_TEMP_C_RIT    | M_TEMP_WARN |
| 0x0008               | SYS_MASK_1   | M_PG2            | M_OV2            | M_UV2          | M_OC2            | M_PG1           | M_OV1     | M_UV1           | M_OC1       |
| 0x0009               | SYS_MASK_2   | Reserved         | Reserved         | Reserved       | Reserved         | Reserved        | M_GPIO2   | M_GPIO1         | M_GPIO0     |
| 0x000A               | SYS_MASK_3   | Reserved         | Reserved         | Reserved       | Reserved         | M_VR_HO_T       | M_SG_STAT | M_PG2_STAT      | M_PG1_STAT  |
| 0x000B               | SYS_CONFIG_0 | CH1_DIS_DLY<3:0> |                  |                |                  | CH1_EN_DLY<3:0> |           |                 |             |
| 0x000C               | SYS_CONFIG_1 | CH2_DIS_DLY<3:0> |                  |                |                  | CH2_EN_DLY<3:0> |           |                 |             |
| 0x000D               | SYS_CONFIG_2 | Reserved         | OC_LATCHOFF<1:0> | OC_DVC_MASK    | PG_DVC_MASK<1:0> |                 | Reserved  | Reserved        | Reserved    |
| 0x000E               | SYS_CONFIG_3 | Reserved         | OSC_TUNE<2:0>    |                |                  | Reserved        | Reserved  | I2C_TIMEO_UT    | Reserved    |
| 0x0010               | SYS_GPIO0_0  | Reserved         | Reserved         | Reserved       | GPIO0_MODE<3:0>  |                 |           |                 | GPIO0_O_BUF |
| 0x0011               | SYS_GPIO0_1  | GPIO0_D_EB_FALL  | GPIO0_D_EB_RISE  | GPIO0_DEB<1:0> |                  | GPIO0_P_UPD     | GPIO0_POL | GPIO0_TRIG<1:0> |             |
| 0x0012               | SYS_GPIO1_0  | Reserved         | Reserved         | Reserved       | GPIO1_MODE<3:0>  |                 |           |                 | GPIO1_O_BUF |
| 0x0013               | SYS_GPIO1_1  | GPIO1_D_EB_FALL  | GPIO1_D_EB_RISE  | GPIO1_DEB<1:0> |                  | GPIO1_P_UPD     | GPIO1_POL | GPIO1_TRIG<1:0> |             |
| 0x0014               | SYS_GPIO2_0  | Reserved         | Reserved         | Reserved       | GPIO2_MODE<3:0>  |                 |           |                 | GPIO2_O_BUF |
| 0x0015               | SYS_GPIO2_1  | GPIO2_D_EB_FALL  | GPIO2_D_EB_RISE  | GPIO2_DEB<1:0> |                  | GPIO2_P_UPD     | GPIO2_POL | GPIO2_TRIG<1:0> |             |

**High-Performance Dual-Channel DC-DC Converter**

| Addr                 | Register        | 7               | 6                   | 5        | 4        | 3                   | 2               | 1                      | 0 |  |  |  |  |  |  |
|----------------------|-----------------|-----------------|---------------------|----------|----------|---------------------|-----------------|------------------------|---|--|--|--|--|--|--|
| <b>Buck Control</b>  |                 |                 |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| <b>Buck1</b>         |                 |                 |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0020               | BUCK_BUCK1_0    | Reserved        | CH1_SR_DVC_DWN<2:0> |          |          | CH1_SR_DVC_UP<2:0>  |                 | CH1_EN                 |   |  |  |  |  |  |  |
| 0x0021               | BUCK_BUCK1_1    | Reserved        | CH1_SR_SHDN<2:0>    |          |          | CH1_SR_STARTUP<2:0> |                 | CH1_PD_DIS             |   |  |  |  |  |  |  |
| 0x0022               | BUCK_BUCK1_2    | Reserved        | Reserved            | Reserved | Reserved | CH1_ILIM<3:0>       |                 |                        |   |  |  |  |  |  |  |
| 0x0023               | BUCK_BUCK1_3    | CH1_VMAX<7:0>   |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0024               | BUCK_BUCK1_4    | Reserved        | Reserved            | Reserved | CH1_VSEL | CH1_B_MODE<1:0>     | CH1_A_MODE<1:0> |                        |   |  |  |  |  |  |  |
| 0x0025               | BUCK_BUCK1_5    | CH1_A_VOUT<7:0> |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0026               | BUCK_BUCK1_6    | CH1_B_VOUT<7:0> |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0027               | BUCK_BUCK1_7    | Reserved        | Reserved            | Reserved | Reserved | Reserved            | Reserved        | CH1_RIPPLE_CANCEL<1:0> |   |  |  |  |  |  |  |
| <b>Buck2</b>         |                 |                 |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0028               | BUCK_BUCK2_0    | Reserved        | CH2_SR_DVC_DWN<2:0> |          |          | CH2_SR_DVC_UP<2:0>  |                 | CH2_EN                 |   |  |  |  |  |  |  |
| 0x0029               | BUCK_BUCK2_1    | Reserved        | CH2_SR_SHDN<2:0>    |          |          | CH2_SR_STARTUP<2:0> |                 | CH2_PD_DIS             |   |  |  |  |  |  |  |
| 0x002A               | BUCK_BUCK2_2    | Reserved        | Reserved            | Reserved | Reserved | CH2_ILIM<3:0>       |                 |                        |   |  |  |  |  |  |  |
| 0x002B               | BUCK_BUCK2_3    | CH2_VMAX<7:0>   |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x002C               | BUCK_BUCK2_4    | Reserved        | Reserved            | Reserved | CH2_VSEL | CH2_B_MODE<1:0>     | CH2_A_MODE<1:0> |                        |   |  |  |  |  |  |  |
| 0x002D               | BUCK_BUCK2_5    | CH2_A_VOUT<7:0> |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x002E               | BUCK_BUCK2_6    | CH2_B_VOUT<7:0> |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x002F               | BUCK_BUCK2_7    | Reserved        | Reserved            | Reserved | Reserved | Reserved            | Reserved        | CH2_RIPPLE_CANCEL<1:0> |   |  |  |  |  |  |  |
| <b>Serialization</b> |                 |                 |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0048               | OTP_DEVICE_ID   | DEV_ID<7:0>     |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x0049               | OTP_VARIANT_ID  | MRC<3:0>        |                     |          |          | VRC<3:0>            |                 |                        |   |  |  |  |  |  |  |
| 0x004A               | OTP_CUSTOMER_ID | CUST_ID<7:0>    |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |
| 0x004B               | OTP_CONFIG_ID   | CONFIG_REV<7:0> |                     |          |          |                     |                 |                        |   |  |  |  |  |  |  |

**High-Performance Dual-Channel DC-DC Converter****5.1.1 System****Table 21: SYS\_STATUS\_0 (0x0001)**

| Bit | Symbol    | Description   |
|-----|-----------|---|
| [2] | SG        | Asserted as long as the enabled buck output voltage is in range |
| [1] | TEMP_CRIT | Asserted as long as the thermal shutdown threshold is reached   |
| [0] | TEMP_WARN | Asserted as long as the thermal warning threshold is reached    |

**Table 22: SYS\_STATUS\_1 (0x0002)**

| Bit | Symbol | Description  |
|-----|--------|--|
| [7] | PG2    | Asserted as long as the Buck2 output voltage is in range |
| [6] | OV2    | Asserted as long as Buck2 hitting over-voltage           |
| [5] | UV2    | Asserted as long as Buck2 hitting under-voltage          |
| [4] | OC2    | Asserted as long as Buck2 hitting over-current           |
| [3] | PG1    | Asserted as long as the Buck1 output voltage is in range |
| [2] | OV1    | Asserted as long as Buck1 hitting over-voltage           |
| [1] | UV1    | Asserted as long as Buck1 hitting under-voltage          |
| [0] | OC1    | Asserted as long as Buck1 hitting over-current           |

**Table 23: SYS\_STATUS\_2 (0x0003)**

| Bit | Symbol | Description  |
|-----|--------|--------------|
| [2] | GPIO2  | GPIO2 status |
| [1] | GPIO1  | GPIO1 status |
| [0] | GPIO0  | GPIO0 status |

**Table 24: SYS\_EVENT\_0 (0x0004)**

| Bit | Symbol      | Description   |
|-----|-------------|---|
| [2] | E_SG        | SG caused event. Writing 1 action clear this bit into 0 if event source has been released.        |
| [1] | E_TEMP_CRIT | TEMP_CRIT caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [0] | E_TEMP_WARN | TEMP_WARN caused event. Writing 1 action clear this bit into 0 if event source has been released. |

**High-Performance Dual-Channel DC-DC Converter****Table 25: SYS\_EVENT\_1 (0x0005)**

| Bit | Symbol | Description   |
|-----|--------|---|
| [7] | E_PG2  | PG2 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [6] | E_OV2  | OV2 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [5] | E_UV2  | UV2 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [4] | E_OC2  | OC2 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [3] | E_PG1  | PG1 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [2] | E_OV1  | OV1 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [1] | E_UV1  | UV1 caused event. Writing 1 action clear this bit into 0 if event source has been released. |
| [0] | E_OC1  | OC1 caused event. Writing 1 action clear this bit into 0 if event source has been released. |

**Table 26: SYS\_EVENT\_2 (0x0006)**

| Bit | Symbol  | Description  |
|-----|---------|--|
| [2] | E_GPIO2 | GPIO2 event. Writing 1 action clear this bit into 0 if event source has been released. |
| [1] | E_GPIO1 | GPIO1 event. Writing 1 action clear this bit into 0 if event source has been released. |
| [0] | E_GPIO0 | GPIO0 event. Writing 1 action clear this bit into 0 if event source has been released. |

**Table 27: SYS\_MASK\_0 (0x0007)**

| Bit | Symbol      | Description        |
|-----|-------------|--------------------|
| [2] | M_SG        | SG IRQ mask        |
| [1] | M_TEMP_CRIT | TEMP_CRIT IRQ mask |
| [0] | M_TEMP_WARN | TEMP_WARN IRQ mask |

**Table 28: SYS\_MASK\_1 (0x0008)**

| Bit | Symbol | Description        |
|-----|--------|--------------------|
| [7] | M_PG2  | PG2 event IRQ mask |
| [6] | M_OV2  | OV2 event IRQ mask |
| [5] | M_UV2  | UV2 event IRQ mask |
| [4] | M_OC2  | OC2 event IRQ mask |
| [3] | M_PG1  | PG1 event IRQ mask |
| [2] | M_OV1  | OV1 event IRQ mask |
| [1] | M_UV1  | UV1 event IRQ mask |
| [0] | M_OC1  | OC1 event IRQ mask |

**High-Performance Dual-Channel DC-DC Converter****Table 29: SYS\_MASK\_2 (0x0009)**

| Bit | Symbol  | Description    |
|-----|---------|----------------|
| [2] | M_GPIO2 | GPIO2 IRQ mask |
| [1] | M_GPIO1 | GPIO1 IRQ mask |
| [0] | M_GPIO0 | GPIO0 IRQ mask |

**Table 30: SYS\_MASK\_3 (0x000A)**

| Bit | Symbol     | Description  |
|-----|------------|--|
| [3] | M_VR_HOT   | Temp warning status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |
| [2] | M_SG_STAT  | SG status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1           |
| [1] | M_PG2_STAT | PG2 status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1          |
| [0] | M_PG1_STAT | PG1 status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1          |

**Table 31: SYS\_CONFIG\_0 (0x000B)**

| Bit   | Symbol      | Description   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
|-------|-------------|---|-------|-------------|-----|---|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|-----|---------|
| [7:4] | CH1_DIS_DLY | <p>Delay for CH1 disable. Active with GPIO configured as EN1&amp;EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0</td> </tr> <tr> <td>0x1</td> <td>1.0 ms</td> </tr> <tr> <td>0x2</td> <td>2.0 ms</td> </tr> <tr> <td>0x3</td> <td>3.0 ms</td> </tr> <tr> <td>0x4</td> <td>4.0 ms</td> </tr> <tr> <td>0x5</td> <td>5.0 ms</td> </tr> <tr> <td>0x6</td> <td>6.0 ms</td> </tr> <tr> <td>0x7</td> <td>7.0 ms</td> </tr> <tr> <td>0x8</td> <td>8.0 ms</td> </tr> <tr> <td>0x9</td> <td>9.0 ms</td> </tr> <tr> <td>0xA</td> <td>10.0 ms</td> </tr> <tr> <td>0xB</td> <td>11.0 ms</td> </tr> <tr> <td>0xC</td> <td>12.0 ms</td> </tr> <tr> <td>0xD</td> <td>13.0 ms</td> </tr> <tr> <td>0xE</td> <td>14.0 ms</td> </tr> <tr> <td>0xF</td> <td>15.0 ms</td> </tr> </tbody> </table> | Value | Description | 0x0 | 0 | 0x1 | 1.0 ms | 0x2 | 2.0 ms | 0x3 | 3.0 ms | 0x4 | 4.0 ms | 0x5 | 5.0 ms | 0x6 | 6.0 ms | 0x7 | 7.0 ms | 0x8 | 8.0 ms | 0x9 | 9.0 ms | 0xA | 10.0 ms | 0xB | 11.0 ms | 0xC | 12.0 ms | 0xD | 13.0 ms | 0xE | 14.0 ms | 0xF | 15.0 ms |
| Value | Description |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x0   | 0           |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x1   | 1.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x2   | 2.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x3   | 3.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x4   | 4.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x5   | 5.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x6   | 6.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x7   | 7.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x8   | 8.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0x9   | 9.0 ms      |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xA   | 10.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xB   | 11.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xC   | 12.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xD   | 13.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xE   | 14.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| 0xF   | 15.0 ms     |   |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |
| [3:0] | CH1_EN_DLY  | Delay for CH1 enable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1  |       |             |     |   |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |         |     |         |     |         |     |         |     |         |     |         |

**High-Performance Dual-Channel DC-DC Converter**

| Bit | Symbol | Description |             |
|-----|--------|-------------|-------------|
|     |        | Value       | Description |
|     |        | 0x0         | 0           |
|     |        | 0x1         | 0.5 ms      |
|     |        | 0x2         | 1.0 ms      |
|     |        | 0x3         | 1.5 ms      |
|     |        | 0x4         | 2.0 ms      |
|     |        | 0x5         | 2.5 ms      |
|     |        | 0x6         | 3.0 ms      |
|     |        | 0x7         | 3.5 ms      |
|     |        | 0x8         | 4.0 ms      |
|     |        | 0x9         | 4.5 ms      |
|     |        | 0xA         | 5.0 ms      |
|     |        | 0xB         | 5.5 ms      |
|     |        | 0xC         | 6.0 ms      |
|     |        | 0xD         | 6.5 ms      |
|     |        | 0xE         | 7.0 ms      |
|     |        | 0xF         | 7.5 ms      |

**Table 32: SYS\_CONFIG\_1 (0x000C)**

| Bit   | Symbol      | Description   |             |
|-------|-------------|---|-------------|
| [7:4] | CH2_DIS_DLY | Delay for CH2 disable. Active with GPIO configured as EN1&EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |             |
|       |             | Value   | Description |
|       |             | 0x0   | 0           |
|       |             | 0x1   | 1.0 ms      |
|       |             | 0x2   | 2.0 ms      |
|       |             | 0x3   | 3.0 ms      |
|       |             | 0x4   | 4.0 ms      |
|       |             | 0x5   | 5.0 ms      |
|       |             | 0x6   | 6.0 ms      |
|       |             | 0x7   | 7.0 ms      |
|       |             | 0x8   | 8.0 ms      |
|       |             | 0x9   | 9.0 ms      |
|       |             | 0xA   | 10.0 ms     |
|       |             | 0xB   | 11.0 ms     |
|       |             | 0xC   | 12.0 ms     |
|       |             | 0xD   | 13.0 ms     |

**High-Performance Dual-Channel DC-DC Converter**

| Bit        | Symbol      | Description  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
|------------|-------------|--|-------|-------------|------------|----------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|--------|
|            |             | 0xE      14.0 ms<br>0xF      15.0 ms   |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| [3:0]      | CH2_EN_DLY  | <p>Delay for CH2 enable. Active with GPIO configured as EN1&amp;EN2 control and IC_EN control. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td><b>0x0</b></td><td><b>0</b></td></tr> <tr> <td>0x1</td><td>0.5 ms</td></tr> <tr> <td>0x2</td><td>1.0 ms</td></tr> <tr> <td>0x3</td><td>1.5 ms</td></tr> <tr> <td>0x4</td><td>2.0 ms</td></tr> <tr> <td>0x5</td><td>2.5 ms</td></tr> <tr> <td>0x6</td><td>3.0 ms</td></tr> <tr> <td>0x7</td><td>3.5 ms</td></tr> <tr> <td>0x8</td><td>4.0 ms</td></tr> <tr> <td>0x9</td><td>4.5 ms</td></tr> <tr> <td>0xA</td><td>5.0 ms</td></tr> <tr> <td>0xB</td><td>5.5 ms</td></tr> <tr> <td>0xC</td><td>6.0 ms</td></tr> <tr> <td>0xD</td><td>6.5 ms</td></tr> <tr> <td>0xE</td><td>7.0 ms</td></tr> <tr> <td>0xF</td><td>7.5 ms</td></tr> </tbody> </table> | Value | Description | <b>0x0</b> | <b>0</b> | 0x1 | 0.5 ms | 0x2 | 1.0 ms | 0x3 | 1.5 ms | 0x4 | 2.0 ms | 0x5 | 2.5 ms | 0x6 | 3.0 ms | 0x7 | 3.5 ms | 0x8 | 4.0 ms | 0x9 | 4.5 ms | 0xA | 5.0 ms | 0xB | 5.5 ms | 0xC | 6.0 ms | 0xD | 6.5 ms | 0xE | 7.0 ms | 0xF | 7.5 ms |
| Value      | Description |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| <b>0x0</b> | <b>0</b>    |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x1        | 0.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x2        | 1.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x3        | 1.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x4        | 2.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x5        | 2.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x6        | 3.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x7        | 3.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x8        | 4.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0x9        | 4.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xA        | 5.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xB        | 5.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xC        | 6.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xD        | 6.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xE        | 7.0 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |
| 0xF        | 7.5 ms      |  |       |             |            |          |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |     |        |

**High-Performance Dual-Channel DC-DC Converter****Table 33: SYS\_CONFIG\_2 (0x000D)**

| Bit        | Symbol                             | Description  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
|------------|------------------------------------|--|-------|-------------|------------|--------------------------|-----|------------------------------------|-----|------------------------------------|-----|------------------------------------|
| [6:5]      | OC_LATCHOFF                        | <p>Over-current latch-off setting. BUCK shut-down after OCP for 8 µs/1 ms/3 ms unless disable setting. IRQ is generated unless IRQ is masked.</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td><b>0x0</b></td><td><b>Latch off disable</b></td></tr> <tr> <td>0x1</td><td>Latch off after 8 µs of OCP signal</td></tr> <tr> <td>0x2</td><td>Latch off after 1 ms of OCP signal</td></tr> <tr> <td>0x3</td><td>Latch off after 3 ms of OCP signal</td></tr> </tbody> </table> | Value | Description | <b>0x0</b> | <b>Latch off disable</b> | 0x1 | Latch off after 8 µs of OCP signal | 0x2 | Latch off after 1 ms of OCP signal | 0x3 | Latch off after 3 ms of OCP signal |
| Value      | Description                        |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| <b>0x0</b> | <b>Latch off disable</b>           |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x1        | Latch off after 8 µs of OCP signal |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x2        | Latch off after 1 ms of OCP signal |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x3        | Latch off after 3 ms of OCP signal |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| [4]        | OC_DVC_MASK                        | Over-current event (IRQ and latch-off feature) mask during DVC ramp-up and ramp-down for both CH1 and CH2  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| [3:2]      | PG_DVC_MASK                        | <p>Power-good mask during DVC for both CH1 and CH 2</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td><b>0x0</b></td><td><b>No mask</b></td></tr> <tr> <td>0x1</td><td>Mask as not power good during DVC</td></tr> <tr> <td>0x2</td><td>Mask as power good during DVC</td></tr> <tr> <td>0x3</td><td>Reserved</td></tr> </tbody> </table>   | Value | Description | <b>0x0</b> | <b>No mask</b>           | 0x1 | Mask as not power good during DVC  | 0x2 | Mask as power good during DVC      | 0x3 | Reserved                           |
| Value      | Description                        |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| <b>0x0</b> | <b>No mask</b>                     |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x1        | Mask as not power good during DVC  |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x2        | Mask as power good during DVC      |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |
| 0x3        | Reserved                           |  |       |             |            |                          |     |                                    |     |                                    |     |                                    |

**Table 34: SYS\_CONFIG\_3 (0x000E)**

| Bit        | Symbol      | Description  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
|------------|-------------|--|-------|-------------|-----|---|-----|---|-----|---|------------|----------|-----|----|-----|----|-----|----|-----|----|
| [6:4]      | OSC_TUNE    | <p>Tune oscillator frequency, tuned frequency = Current + OSC_TUNE * 160 kHz</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x3</td><td>3</td></tr> <tr> <td>0x2</td><td>2</td></tr> <tr> <td>0x1</td><td>1</td></tr> <tr> <td><b>0x0</b></td><td><b>0</b></td></tr> <tr> <td>0x7</td><td>-1</td></tr> <tr> <td>0x6</td><td>-2</td></tr> <tr> <td>0x5</td><td>-3</td></tr> <tr> <td>0x4</td><td>-4</td></tr> </tbody> </table> | Value | Description | 0x3 | 3 | 0x2 | 2 | 0x1 | 1 | <b>0x0</b> | <b>0</b> | 0x7 | -1 | 0x6 | -2 | 0x5 | -3 | 0x4 | -4 |
| Value      | Description |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x3        | 3           |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x2        | 2           |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x1        | 1           |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| <b>0x0</b> | <b>0</b>    |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x7        | -1          |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x6        | -2          |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x5        | -3          |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| 0x4        | -4          |  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |
| [1]        | I2C_TIMEOUT | Enable automatic reset of 2-wire interface (if SDA stays low for >50 ms).  |       |             |     |   |     |   |     |   |            |          |     |    |     |    |     |    |     |    |

**High-Performance Dual-Channel DC-DC Converter****Table 35: SYS\_GPIO0\_0 (0x0010)**

| Bit   | Symbol                   | Description  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
|-------|--------------------------|--|-------|-------------|-----|--------------------------|-----|------------------|-----|-----------|-----|-----------------|-----|------------|-----|------------|-----|-------------------|-----|--------------|-----|------------|-----|------------|-----|------------------|-----|-----------|-----|-------------|-----|----------|-----|------------|-----|-------------|
| [4:1] | GPIO0_MODE               | <p>GPIO function mode select</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td><b>GPIO disable</b></td></tr> <tr><td>0x1</td><td>EN1 input</td></tr> <tr><td>0x2</td><td>EN2 input</td></tr> <tr><td>0x3</td><td>EN1 &amp; EN2 input</td></tr> <tr><td>0x4</td><td>DVC1 input</td></tr> <tr><td>0x5</td><td>DVC2 input</td></tr> <tr><td>0x6</td><td>DVC1 &amp; DVC2 input</td></tr> <tr><td>0x7</td><td>RELOAD input</td></tr> <tr><td>0x8</td><td>PG1 output</td></tr> <tr><td>0x9</td><td>PG2 output</td></tr> <tr><td>0xA</td><td>PG1 &amp; PG2 output</td></tr> <tr><td>0xB</td><td>SG output</td></tr> <tr><td>0xC</td><td>nIRQ output</td></tr> <tr><td>0xD</td><td>Reserved</td></tr> <tr><td>0xE</td><td>Low output</td></tr> <tr><td>0xF</td><td>High output</td></tr> </tbody> </table> | Value | Description | 0x0 | <b>GPIO disable</b>      | 0x1 | EN1 input        | 0x2 | EN2 input | 0x3 | EN1 & EN2 input | 0x4 | DVC1 input | 0x5 | DVC2 input | 0x6 | DVC1 & DVC2 input | 0x7 | RELOAD input | 0x8 | PG1 output | 0x9 | PG2 output | 0xA | PG1 & PG2 output | 0xB | SG output | 0xC | nIRQ output | 0xD | Reserved | 0xE | Low output | 0xF | High output |
| Value | Description              |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x0   | <b>GPIO disable</b>      |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x1   | EN1 input                |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x2   | EN2 input                |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x3   | EN1 & EN2 input          |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x4   | DVC1 input               |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x5   | DVC2 input               |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x6   | DVC1 & DVC2 input        |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x7   | RELOAD input             |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x8   | PG1 output               |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x9   | PG2 output               |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xA   | PG1 & PG2 output         |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xB   | SG output                |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xC   | nIRQ output              |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xD   | Reserved                 |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xE   | Low output               |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0xF   | High output              |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| [0]   | GPIO0_OBUF               | <p>GPIO output buffer select</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td><b>open-drain output</b></td></tr> <tr><td>0x1</td><td>push-pull output</td></tr> </tbody> </table>   | Value | Description | 0x0 | <b>open-drain output</b> | 0x1 | push-pull output |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| Value | Description              |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x0   | <b>open-drain output</b> |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |
| 0x1   | push-pull output         |  |       |             |     |                          |     |                  |     |           |     |                 |     |            |     |            |     |                   |     |              |     |            |     |            |     |                  |     |           |     |             |     |          |     |            |     |             |

## High-Performance Dual-Channel DC-DC Converter

Table 36: SYS\_GPIO0\_1 (0x0011)

| Bit   | Symbol         | Description   |
|-------|----------------|---|
| [7]   | GPIO0_DEB_FALL | GPI debounce falling edge   |
| [6]   | GPIO0_DEB_RISE | GPI debounce rising edge  |
| [5:4] | GPIO0_DEB      | GPI debounce time<br><b>Value</b> <b>Description</b><br><b>0x0</b> <b>100 µs debounce</b><br>0x1      1 ms debounce<br>0x2      10 ms debounce<br>0x3      100 ms debounce                                    |
| [3]   | GPIO0_PUPD     | GPIO pull-up/pull-down enable<br><b>Value</b> <b>Description</b><br><b>0x0</b> <b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b><br>0x1      GPI: pull-down enabled, GPO: pull-up to AVDD enabled |
| [2]   | GPIO0_POL      | GPIO polarity<br><b>Value</b> <b>Description</b><br><b>0x0</b> <b>GPIO is active-high</b><br>0x1      GPIO is active-low  |
| [1:0] | GPIO0_TRIG     | GPI trigger type<br><b>Value</b> <b>Description</b><br><b>0x0</b> <b>Dual-edge triggered</b><br>0x1      Pos-edge triggered<br>0x2      Neg-edge triggered<br>0x3      Reserved (No trigger)                  |

Table 37: SYS\_GPIO1\_0 (0x0012)

| Bit   | Symbol     | Description  |
|-------|------------|--|
| [4:1] | GPIO1_MODE | GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><b>Value</b> <b>Description</b><br><b>0x0</b> <b>GPIO disable</b><br>0x1      EN1 input<br>0x2      EN2 input<br>0x3      EN1 & EN2 input<br>0x4      DVC1 input<br>0x5      DVC2 input<br>0x6      DVC1 & DVC2 input |

**High-Performance Dual-Channel DC-DC Converter**

| Bit   | Symbol            | Description   |       |             |     |                   |     |                  |
|-------|-------------------|---|-------|-------------|-----|-------------------|-----|------------------|
|       |                   | 0x7 RELOAD input<br>0x8 PG1 output<br>0x9 PG2 output<br>0xA PG1 & PG2 output<br>0xB SG output<br>0xC nIRQ output<br>0xD Reserved<br>0xE Low output<br>0xF High output   |       |             |     |                   |     |                  |
| [0]   | GPIO1_OBUF        | GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>open-drain output</td></tr> <tr> <td>0x1</td><td>push-pull output</td></tr> </tbody> </table> | Value | Description | 0x0 | open-drain output | 0x1 | push-pull output |
| Value | Description       |   |       |             |     |                   |     |                  |
| 0x0   | open-drain output |   |       |             |     |                   |     |                  |
| 0x1   | push-pull output  |   |       |             |     |                   |     |                  |

## High-Performance Dual-Channel DC-DC Converter

Table 38: SYS\_GPIO1\_1 (0x0013)

| Bit   | Symbol  | Description  |       |             |     |   |     |  |     |                    |     |                       |
|-------|---|--|-------|-------------|-----|---|-----|--|-----|--------------------|-----|-----------------------|
| [7]   | GPIO1_DEB_FALL  | GPI debounce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1  |       |             |     |   |     |  |     |                    |     |                       |
| [6]   | GPIO1_DEB_RISE  | GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1   |       |             |     |   |     |  |     |                    |     |                       |
| [5:4] | GPIO1_DEB   | GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>100 µs debounce</b></td></tr> <tr> <td>0x1</td><td>1 ms debounce</td></tr> <tr> <td>0x2</td><td>10 ms debounce</td></tr> <tr> <td>0x3</td><td>100 ms debounce</td></tr> </tbody> </table>                   | Value | Description | 0x0 | <b>100 µs debounce</b>  | 0x1 | 1 ms debounce  | 0x2 | 10 ms debounce     | 0x3 | 100 ms debounce       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>100 µs debounce</b>  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | 1 ms debounce   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x2   | 10 ms debounce  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x3   | 100 ms debounce   |  |       |             |     |   |     |  |     |                    |     |                       |
| [3]   | GPIO1_PUPD  | GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b></td></tr> <tr> <td>0x1</td><td>GPI: pull-down enabled, GPO: pull-up to AVDD enabled</td></tr> </tbody> </table>                      | Value | Description | 0x0 | <b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b> | 0x1 | GPI: pull-down enabled, GPO: pull-up to AVDD enabled |     |                    |     |                       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b> |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | GPI: pull-down enabled, GPO: pull-up to AVDD enabled          |  |       |             |     |   |     |  |     |                    |     |                       |
| [2]   | GPIO1_POL   | GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>GPIO is active-high</b></td></tr> <tr> <td>0x1</td><td>GPIO is active-low</td></tr> </tbody> </table>   | Value | Description | 0x0 | <b>GPIO is active-high</b>                                    | 0x1 | GPIO is active-low                                   |     |                    |     |                       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>GPIO is active-high</b>                                    |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | GPIO is active-low  |  |       |             |     |   |     |  |     |                    |     |                       |
| [1:0] | GPIO1_TRIG  | GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>Dual-edge triggered</b></td></tr> <tr> <td>0x1</td><td>Pos-edge triggered</td></tr> <tr> <td>0x2</td><td>Neg-edge triggered</td></tr> <tr> <td>0x3</td><td>Reserved (No trigger)</td></tr> </tbody> </table> | Value | Description | 0x0 | <b>Dual-edge triggered</b>                                    | 0x1 | Pos-edge triggered                                   | 0x2 | Neg-edge triggered | 0x3 | Reserved (No trigger) |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>Dual-edge triggered</b>                                    |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | Pos-edge triggered  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x2   | Neg-edge triggered  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x3   | Reserved (No trigger)   |  |       |             |     |   |     |  |     |                    |     |                       |

Table 39: SYS\_GPIO2\_0 (0x0014)

| Bit   | Symbol              | Description  |       |             |     |                     |     |           |     |           |     |                 |
|-------|---------------------|--|-------|-------------|-----|---------------------|-----|-----------|-----|-----------|-----|-----------------|
| [4:1] | GPIO2_MODE          | GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>GPIO disable</b></td></tr> <tr> <td>0x1</td><td>EN1 input</td></tr> <tr> <td>0x2</td><td>EN2 input</td></tr> <tr> <td>0x3</td><td>EN1 &amp; EN2 input</td></tr> </tbody> </table> | Value | Description | 0x0 | <b>GPIO disable</b> | 0x1 | EN1 input | 0x2 | EN2 input | 0x3 | EN1 & EN2 input |
| Value | Description         |  |       |             |     |                     |     |           |     |           |     |                 |
| 0x0   | <b>GPIO disable</b> |  |       |             |     |                     |     |           |     |           |     |                 |
| 0x1   | EN1 input           |  |       |             |     |                     |     |           |     |           |     |                 |
| 0x2   | EN2 input           |  |       |             |     |                     |     |           |     |           |     |                 |
| 0x3   | EN1 & EN2 input     |  |       |             |     |                     |     |           |     |           |     |                 |

**High-Performance Dual-Channel DC-DC Converter**

| Bit   | Symbol                   | Description  |       |             |     |                          |     |                  |
|-------|--------------------------|--|-------|-------------|-----|--------------------------|-----|------------------|
|       |                          | 0x4 DVC1 input<br>0x5 DVC2 input<br>0x6 DVC1 & DVC2 input<br>0x7 RELOAD input<br>0x8 PG1 output<br>0x9 PG2 output<br>0xA PG1 & PG2 output<br>0xB SG output<br>0xC nIRQ output<br>0xD Reserved<br>0xE Low output<br>0xF High output   |       |             |     |                          |     |                  |
| [0]   | GPIO2_OBUF               | GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>open-drain output</b></td></tr> <tr> <td>0x1</td><td>push-pull output</td></tr> </tbody> </table> | Value | Description | 0x0 | <b>open-drain output</b> | 0x1 | push-pull output |
| Value | Description              |  |       |             |     |                          |     |                  |
| 0x0   | <b>open-drain output</b> |  |       |             |     |                          |     |                  |
| 0x1   | push-pull output         |  |       |             |     |                          |     |                  |

**High-Performance Dual-Channel DC-DC Converter****Table 40: SYS\_GPIO2\_1 (0x0015)**

| Bit   | Symbol  | Description  |       |             |     |   |     |  |     |                    |     |                       |
|-------|---|--|-------|-------------|-----|---|-----|--|-----|--------------------|-----|-----------------------|
| [7]   | GPIO2_DEB_FALL  | GPI debounce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1  |       |             |     |   |     |  |     |                    |     |                       |
| [6]   | GPIO2_DEB_RISE  | GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1   |       |             |     |   |     |  |     |                    |     |                       |
| [5:4] | GPIO2_DEB   | GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>100 µs debounce</b></td></tr> <tr> <td>0x1</td><td>1 ms debounce</td></tr> <tr> <td>0x2</td><td>10 ms debounce</td></tr> <tr> <td>0x3</td><td>100 ms debounce</td></tr> </tbody> </table>                   | Value | Description | 0x0 | <b>100 µs debounce</b>  | 0x1 | 1 ms debounce  | 0x2 | 10 ms debounce     | 0x3 | 100 ms debounce       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>100 µs debounce</b>  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | 1 ms debounce   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x2   | 10 ms debounce  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x3   | 100 ms debounce   |  |       |             |     |   |     |  |     |                    |     |                       |
| [3]   | GPIO2_PUPD  | GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b></td></tr> <tr> <td>0x1</td><td>GPI: pull-down enabled, GPO: pull-up to AVDD enabled</td></tr> </tbody> </table>                      | Value | Description | 0x0 | <b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b> | 0x1 | GPI: pull-down enabled, GPO: pull-up to AVDD enabled |     |                    |     |                       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</b> |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | GPI: pull-down enabled, GPO: pull-up to AVDD enabled          |  |       |             |     |   |     |  |     |                    |     |                       |
| [2]   | GPIO2_POL   | GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>GPIO is active-high</b></td></tr> <tr> <td>0x1</td><td>GPIO is active-low</td></tr> </tbody> </table>   | Value | Description | 0x0 | <b>GPIO is active-high</b>                                    | 0x1 | GPIO is active-low                                   |     |                    |     |                       |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>GPIO is active-high</b>                                    |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | GPIO is active-low  |  |       |             |     |   |     |  |     |                    |     |                       |
| [1:0] | GPIO2_TRIG  | GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br><table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td><b>Dual-edge triggered</b></td></tr> <tr> <td>0x1</td><td>Pos-edge triggered</td></tr> <tr> <td>0x2</td><td>Neg-edge triggered</td></tr> <tr> <td>0x3</td><td>Reserved (No trigger)</td></tr> </tbody> </table> | Value | Description | 0x0 | <b>Dual-edge triggered</b>                                    | 0x1 | Pos-edge triggered                                   | 0x2 | Neg-edge triggered | 0x3 | Reserved (No trigger) |
| Value | Description   |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x0   | <b>Dual-edge triggered</b>                                    |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x1   | Pos-edge triggered  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x2   | Neg-edge triggered  |  |       |             |     |   |     |  |     |                    |     |                       |
| 0x3   | Reserved (No trigger)   |  |       |             |     |   |     |  |     |                    |     |                       |

**High-Performance Dual-Channel DC-DC Converter****5.1.2 Buck1****Table 41: BUCK\_BUCK1\_0 (0x0020)**

| Bit        | Symbol                         | Description  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
|------------|--------------------------------|--|-------|-------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|----------------|------------|--------------------------------|-----|----------------|-----|----------|-----|----------|
| [6:4]      | CH1_SR_DVC_DWN                 | <p>Voltage slew-rate for DVC ramp-down</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr> <td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr> <td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr> <td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr> <td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr> <td>0x5</td><td>Reserved</td></tr> <tr> <td>0x6</td><td>Reserved</td></tr> <tr> <td>0x7</td><td>Reserved</td></tr> </tbody> </table>              | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | Reserved       | 0x6 | Reserved | 0x7 | Reserved |
| Value      | Description                    |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x0        | 10 mV/8 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x1        | 10 mV/4 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x2        | 10 mV/2 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x3        | 10 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x5        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x6        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x7        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| [3:1]      | CH1_SR_DVC_UP                  | <p>Voltage slew-rate for DVC ramp-up</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr> <td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr> <td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr> <td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr> <td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr> <td>0x5</td><td>40 mV/<math>\mu</math>s</td></tr> <tr> <td>0x6</td><td>Reserved</td></tr> <tr> <td>0x7</td><td>Reserved</td></tr> </tbody> </table> | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | 40 mV/ $\mu$ s | 0x6 | Reserved | 0x7 | Reserved |
| Value      | Description                    |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x0        | 10 mV/8 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x1        | 10 mV/4 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x2        | 10 mV/2 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x3        | 10 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x5        | 40 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x6        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x7        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| [0]        | CH1_EN                         | Channel enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |

**High-Performance Dual-Channel DC-DC Converter****Table 42: BUCK\_BUCK1\_1 (0x0021)**

| Bit        | Symbol                         | Description   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
|------------|--------------------------------|---|-------|-------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|----------------|------------|--------------------------------|-----|----------------|-----|----------|-----|----------------------|
| [6:4]      | CH1_SR_SHDN                    | <p>Voltage slew-rate during shut-down</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr><td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr><td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr><td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr><td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr><td>0x5</td><td>Reserved</td></tr> <tr><td>0x6</td><td>Reserved</td></tr> <tr><td>0x7</td><td>Immediate power-down</td></tr> </tbody> </table>  | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | Reserved       | 0x6 | Reserved | 0x7 | Immediate power-down |
| Value      | Description                    |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x0        | 10 mV/8 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x1        | 10 mV/4 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x2        | 10 mV/2 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x3        | 10 mV/ $\mu$ s                 |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x5        | Reserved                       |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x6        | Reserved                       |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x7        | Immediate power-down           |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| [3:1]      | CH1_SR_STARTUP                 | <p>Voltage slew-rate during startup</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr><td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr><td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr><td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr><td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr><td>0x5</td><td>40 mV/<math>\mu</math>s</td></tr> <tr><td>0x6</td><td>Reserved</td></tr> <tr><td>0x7</td><td>Reserved</td></tr> </tbody> </table> | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | 40 mV/ $\mu$ s | 0x6 | Reserved | 0x7 | Reserved             |
| Value      | Description                    |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x0        | 10 mV/8 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x1        | 10 mV/4 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x2        | 10 mV/2 $\mu$ s                |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x3        | 10 mV/ $\mu$ s                 |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x5        | 40 mV/ $\mu$ s                 |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x6        | Reserved                       |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| 0x7        | Reserved                       |   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |
| [0]        | CH1_PD_DIS                     | Pull-down while buck is disabled. 0: enable, 1: disable   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |                      |

**Table 43: BUCK\_BUCK1\_2 (0x0022)**

| Bit        | Symbol      | Description  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
|------------|-------------|--|-------|-------------|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| [3:0]      | CH1_ILIM    | <p>Select OCP threshold (A)</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>Reserved</td></tr> <tr><td>0x1</td><td>3.5</td></tr> <tr><td>0x2</td><td>4.0</td></tr> <tr><td>0x3</td><td>4.5</td></tr> <tr><td>0x4</td><td>5.0</td></tr> <tr><td><b>0x5</b></td><td><b>5.5</b></td></tr> <tr><td>0x6</td><td>6.0</td></tr> <tr><td>0x7</td><td>6.5</td></tr> <tr><td>0x8</td><td>7.0</td></tr> <tr><td>0x9</td><td>7.5</td></tr> </tbody> </table> | Value | Description | 0x0 | Reserved | 0x1 | 3.5 | 0x2 | 4.0 | 0x3 | 4.5 | 0x4 | 5.0 | <b>0x5</b> | <b>5.5</b> | 0x6 | 6.0 | 0x7 | 6.5 | 0x8 | 7.0 | 0x9 | 7.5 |
| Value      | Description |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x0        | Reserved    |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x1        | 3.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x2        | 4.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x3        | 4.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x4        | 5.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| <b>0x5</b> | <b>5.5</b>  |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x6        | 6.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x7        | 6.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x8        | 7.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x9        | 7.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |

**High-Performance Dual-Channel DC-DC Converter**

| Bit | Symbol | Description |         |
|-----|--------|-------------|---------|
|     |        | 0xA         | 8.0     |
|     |        | 0xB         | 8.5     |
|     |        | 0xC         | 9.0     |
|     |        | 0xD         | 9.5     |
|     |        | 0xE         | 10.0    |
|     |        | 0xF         | Disable |

**Table 44: BUCK\_BUCK1\_3 (0x0023)**

| Bit   | Symbol   | Description   |                    |
|-------|----------|---|--------------------|
| [7:0] | CH1_VMAX | VOUT max setting (V):<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in 10 mV steps.<br>This is a read-only register. |                    |
|       |          | <b>Value</b>  | <b>Description</b> |
|       |          | 0x1E  | 0.3                |
|       |          | 0x1F  | 0.31               |
|       |          | 0x20  | 0.32               |
|       |          | Continuing through...   |                    |
|       |          | 0x99  | 1.53               |
|       |          | To...   |                    |
|       |          | 0xBD  | 1.89               |
|       |          | <b>0xBE</b>   | <b>1.9</b>         |

**Table 45: BUCK\_BUCK1\_4 (0x0024)**

| Bit   | Symbol     | Description   |                     |
|-------|------------|---|---------------------|
| [4]   | CH1_VSEL   | Output voltage and operation selection: 0: A, 1: B.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |                     |
| [3:2] | CH1_B_MODE | Operation mode selection.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |                     |
|       |            | <b>Value</b>  | <b>Description</b>  |
|       |            | 0x0   | Force PFM operation |
|       |            | 0x1   | Force PWM operation |
|       |            | 0x2   | Force PWM operation |
|       |            | <b>0x3</b>  | <b>Auto mode</b>    |
| [1:0] | CH1_A_MODE | Operation mode selection.<br>Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |                     |
|       |            | <b>Value</b>  | <b>Description</b>  |
|       |            | 0x0   | Force PFM operation |
|       |            | 0x1   | Force PWM operation |

## High-Performance Dual-Channel DC-DC Converter

| Bit | Symbol | Description             |
|-----|--------|-------------------------|
|     |        | 0x2 Force PWM operation |
|     |        | 0x3 Auto mode           |

Table 46: BUCK\_BUCK1\_5 (0x0025)

| Bit                   | Symbol      | Description  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
|-----------------------|-------------|--|-------|-------------|------|-----|------|------|------|------|-----------------------|--|-------------|----------|-------|--|------|------|------|------|------|-----|
| [7:0]                 | CH1_A_VOUT  | <p>Output voltage setting A: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br/>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br/>Write-protected when value is written below 0.30 V or above 1.90 V</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1E</td> <td>0.3</td> </tr> <tr> <td>0x1F</td> <td>0.31</td> </tr> <tr> <td>0x20</td> <td>0.32</td> </tr> <tr> <td colspan="2">Continuing through...</td></tr> <tr> <td><b>0x64</b></td> <td><b>1</b></td> </tr> <tr> <td colspan="2">To...</td></tr> <tr> <td>0xBC</td> <td>1.88</td> </tr> <tr> <td>0xBD</td> <td>1.89</td> </tr> <tr> <td>0xBE</td> <td>1.9</td> </tr> </tbody> </table> | Value | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | <b>0x64</b> | <b>1</b> | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
| Value                 | Description |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1E                  | 0.3         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1F                  | 0.31        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x20                  | 0.32        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| Continuing through... |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| <b>0x64</b>           | <b>1</b>    |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| To...                 |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBC                  | 1.88        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBD                  | 1.89        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBE                  | 1.9         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |

Table 47: BUCK\_BUCK1\_6 (0x0026)

| Bit                   | Symbol      | Description  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
|-----------------------|-------------|--|-------|-------------|------|-----|------|------|------|------|-----------------------|--|-------------|----------|-------|--|------|------|------|------|------|-----|
| [7:0]                 | CH1_B_VOUT  | <p>Output voltage setting B: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br/>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br/>Write-protected when value is written below 0.30 V or above 1.90 V</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1E</td> <td>0.3</td> </tr> <tr> <td>0x1F</td> <td>0.31</td> </tr> <tr> <td>0x20</td> <td>0.32</td> </tr> <tr> <td colspan="2">Continuing through...</td></tr> <tr> <td><b>0x64</b></td> <td><b>1</b></td> </tr> <tr> <td colspan="2">To...</td></tr> <tr> <td>0xBC</td> <td>1.88</td> </tr> <tr> <td>0xBD</td> <td>1.89</td> </tr> <tr> <td>0xBE</td> <td>1.9</td> </tr> </tbody> </table> | Value | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | <b>0x64</b> | <b>1</b> | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
| Value                 | Description |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1E                  | 0.3         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1F                  | 0.31        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x20                  | 0.32        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| Continuing through... |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| <b>0x64</b>           | <b>1</b>    |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| To...                 |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBC                  | 1.88        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBD                  | 1.89        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBE                  | 1.9         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |

## High-Performance Dual-Channel DC-DC Converter

Table 48: BUCK\_BUCK1\_7 (0x0027)

| Bit   | Symbol                  | Description   |       |             |     |                         |     |                     |     |                   |     |                     |
|-------|-------------------------|---|-------|-------------|-----|-------------------------|-----|---------------------|-----|-------------------|-----|---------------------|
| [3]   | Reserved                | Reserved  |       |             |     |                         |     |                     |     |                   |     |                     |
| [2]   | Reserved                | Reserved  |       |             |     |                         |     |                     |     |                   |     |                     |
| [1:0] | CH1_RIPPLE_CANCEL       | <p>Ripple cancel control (can be used to improve output overshoot at heavy to light load transient).</p> <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x0</td><td><b>No ripple cancel</b></td></tr><tr><td>0x1</td><td>Small ripple cancel</td></tr><tr><td>0x2</td><td>Mid ripple cancel</td></tr><tr><td>0x3</td><td>Large ripple cancel</td></tr></tbody></table> | Value | Description | 0x0 | <b>No ripple cancel</b> | 0x1 | Small ripple cancel | 0x2 | Mid ripple cancel | 0x3 | Large ripple cancel |
| Value | Description             |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x0   | <b>No ripple cancel</b> |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x1   | Small ripple cancel     |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x2   | Mid ripple cancel       |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x3   | Large ripple cancel     |   |       |             |     |                         |     |                     |     |                   |     |                     |

**High-Performance Dual-Channel DC-DC Converter****5.1.3 Buck2****Table 49: BUCK\_BUCK2\_0 (0x0028)**

| Bit        | Symbol                         | Description  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
|------------|--------------------------------|--|-------|-------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|----------------|------------|--------------------------------|-----|----------------|-----|----------|-----|----------|
| [6:4]      | CH2_SR_DVC_DWN                 | <p>Voltage slew-rate for DVC ramp-down</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr> <td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr> <td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr> <td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr> <td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr> <td>0x5</td><td>Reserved</td></tr> <tr> <td>0x6</td><td>Reserved</td></tr> <tr> <td>0x7</td><td>Reserved</td></tr> </tbody> </table>              | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | Reserved       | 0x6 | Reserved | 0x7 | Reserved |
| Value      | Description                    |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x0        | 10 mV/8 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x1        | 10 mV/4 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x2        | 10 mV/2 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x3        | 10 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x5        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x6        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x7        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| [3:1]      | CH2_SR_DVC_UP                  | <p>Voltage slew-rate for DVC ramp-up</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0x0</td><td>10 mV/8 <math>\mu</math>s</td></tr> <tr> <td>0x1</td><td>10 mV/4 <math>\mu</math>s</td></tr> <tr> <td>0x2</td><td>10 mV/2 <math>\mu</math>s</td></tr> <tr> <td>0x3</td><td>10 mV/<math>\mu</math>s</td></tr> <tr> <td><b>0x4</b></td><td><b>20 mV/<math>\mu</math>s</b></td></tr> <tr> <td>0x5</td><td>40 mV/<math>\mu</math>s</td></tr> <tr> <td>0x6</td><td>Reserved</td></tr> <tr> <td>0x7</td><td>Reserved</td></tr> </tbody> </table> | Value | Description | 0x0 | 10 mV/8 $\mu$ s | 0x1 | 10 mV/4 $\mu$ s | 0x2 | 10 mV/2 $\mu$ s | 0x3 | 10 mV/ $\mu$ s | <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> | 0x5 | 40 mV/ $\mu$ s | 0x6 | Reserved | 0x7 | Reserved |
| Value      | Description                    |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x0        | 10 mV/8 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x1        | 10 mV/4 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x2        | 10 mV/2 $\mu$ s                |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x3        | 10 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| <b>0x4</b> | <b>20 mV/<math>\mu</math>s</b> |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x5        | 40 mV/ $\mu$ s                 |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x6        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| 0x7        | Reserved                       |  |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |
| [0]        | CH2_EN                         | Channel enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1   |       |             |     |                 |     |                 |     |                 |     |                |            |                                |     |                |     |          |     |          |

**High-Performance Dual-Channel DC-DC Converter****Table 50: BUCK\_BUCK2\_1 (0x0029)**

| Bit        | Symbol               | Description  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
|------------|----------------------|--|-------|-------------|-----|------------|-----|------------|-----|------------|-----|----------|------------|-----------------|-----|----------|-----|----------|-----|----------------------|
| [6:4]      | CH2_SR_SHDN          | <p>Voltage slew-rate during power-down</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>10 mV/8 µs</td></tr> <tr><td>0x1</td><td>10 mV/4 µs</td></tr> <tr><td>0x2</td><td>10 mV/2 µs</td></tr> <tr><td>0x3</td><td>10 mV/µs</td></tr> <tr><td><b>0x4</b></td><td><b>20 mV/µs</b></td></tr> <tr><td>0x5</td><td>Reserved</td></tr> <tr><td>0x6</td><td>Reserved</td></tr> <tr><td>0x7</td><td>Immediate power-down</td></tr> </tbody> </table> | Value | Description | 0x0 | 10 mV/8 µs | 0x1 | 10 mV/4 µs | 0x2 | 10 mV/2 µs | 0x3 | 10 mV/µs | <b>0x4</b> | <b>20 mV/µs</b> | 0x5 | Reserved | 0x6 | Reserved | 0x7 | Immediate power-down |
| Value      | Description          |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x0        | 10 mV/8 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x1        | 10 mV/4 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x2        | 10 mV/2 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x3        | 10 mV/µs             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| <b>0x4</b> | <b>20 mV/µs</b>      |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x5        | Reserved             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x6        | Reserved             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x7        | Immediate power-down |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| [3:1]      | CH2_SR_STARTUP       | <p>Voltage slew-rate during startup</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>10 mV/8 µs</td></tr> <tr><td>0x1</td><td>10 mV/4 µs</td></tr> <tr><td>0x2</td><td>10 mV/2 µs</td></tr> <tr><td>0x3</td><td>10 mV/µs</td></tr> <tr><td><b>0x4</b></td><td><b>20 mV/µs</b></td></tr> <tr><td>0x5</td><td>40 mV/µs</td></tr> <tr><td>0x6</td><td>Reserved</td></tr> <tr><td>0x7</td><td>Reserved</td></tr> </tbody> </table>                | Value | Description | 0x0 | 10 mV/8 µs | 0x1 | 10 mV/4 µs | 0x2 | 10 mV/2 µs | 0x3 | 10 mV/µs | <b>0x4</b> | <b>20 mV/µs</b> | 0x5 | 40 mV/µs | 0x6 | Reserved | 0x7 | Reserved             |
| Value      | Description          |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x0        | 10 mV/8 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x1        | 10 mV/4 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x2        | 10 mV/2 µs           |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x3        | 10 mV/µs             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| <b>0x4</b> | <b>20 mV/µs</b>      |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x5        | 40 mV/µs             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x6        | Reserved             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| 0x7        | Reserved             |  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |
| [0]        | CH2_PD_DIS           | Pull-down while BUCK is disabled. 0: enable, 1: disable  |       |             |     |            |     |            |     |            |     |          |            |                 |     |          |     |          |     |                      |

**Table 51: BUCK\_BUCK2\_2 (0x002A)**

| Bit        | Symbol      | Description  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
|------------|-------------|--|-------|-------------|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| [3:0]      | CH2_ILIM    | <p>Select OCP threshold</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0x0</td><td>Reserved</td></tr> <tr><td>0x1</td><td>3.5</td></tr> <tr><td>0x2</td><td>4.0</td></tr> <tr><td>0x3</td><td>4.5</td></tr> <tr><td>0x4</td><td>5.0</td></tr> <tr><td><b>0x5</b></td><td><b>5.5</b></td></tr> <tr><td>0x6</td><td>6.0</td></tr> <tr><td>0x7</td><td>6.5</td></tr> <tr><td>0x8</td><td>7.0</td></tr> <tr><td>0x9</td><td>7.5</td></tr> </tbody> </table> | Value | Description | 0x0 | Reserved | 0x1 | 3.5 | 0x2 | 4.0 | 0x3 | 4.5 | 0x4 | 5.0 | <b>0x5</b> | <b>5.5</b> | 0x6 | 6.0 | 0x7 | 6.5 | 0x8 | 7.0 | 0x9 | 7.5 |
| Value      | Description |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x0        | Reserved    |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x1        | 3.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x2        | 4.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x3        | 4.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x4        | 5.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| <b>0x5</b> | <b>5.5</b>  |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x6        | 6.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x7        | 6.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x8        | 7.0         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |
| 0x9        | 7.5         |  |       |             |     |          |     |     |     |     |     |     |     |     |            |            |     |     |     |     |     |     |     |     |

## High-Performance Dual-Channel DC-DC Converter

| Bit | Symbol | Description |         |
|-----|--------|-------------|---------|
|     |        | 0xA         | 8.0     |
|     |        | 0xB         | 8.5     |
|     |        | 0xC         | 9.0     |
|     |        | 0xD         | 9.5     |
|     |        | 0xE         | 10.0    |
|     |        | 0xF         | Disable |

Table 52: BUCK\_BUCK2\_3 (0x002B)

| Bit   | Symbol   | Description   |                    |
|-------|----------|---|--------------------|
| [7:0] | CH2_VMAX | VOUT max setting (V):<br>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV<br>This is a read-only register. |                    |
|       |          | <b>Value</b>  | <b>Description</b> |
|       |          | 0x1E  | 0.3                |
|       |          | 0x1F  | 0.31               |
|       |          | 0x20  | 0.32               |
|       |          | Continuing through...   |                    |
|       |          | 0x64  | 1                  |
|       |          | To...   |                    |
|       |          | 0xBC  | 1.88               |
|       |          | 0xBD  | 1.89               |
|       |          | 0xBE  | 1.9                |

Table 53: BUCK\_BUCK2\_4 (0x002C)

| Bit   | Symbol     | Description  |                     |
|-------|------------|--|---------------------|
| [4]   | CH2_VSEL   | Output voltage and operation selection: 0: A, 1: B. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 |                     |
| [3:2] | CH2_B_MODE | Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |                     |
|       |            | <b>Value</b>   | <b>Description</b>  |
|       |            | 0x0  | Force PFM operation |
|       |            | 0x1  | Force PWM operation |
|       |            | 0x2  | Force PWM operation |
|       |            | 0x3  | Auto mode           |
| [1:0] | CH2_A_MODE | Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1                           |                     |
|       |            | <b>Value</b>   | <b>Description</b>  |
|       |            | 0x0  | Force PFM operation |
|       |            | 0x1  | Force PWM operation |

**High-Performance Dual-Channel DC-DC Converter**

| Bit | Symbol | Description             |
|-----|--------|-------------------------|
|     |        | 0x2 Force PWM operation |
|     |        | 0x3 Auto mode           |

**Table 54: BUCK\_BUCK2\_5 (0x002D)**

| Bit                   | Symbol      | Description  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
|-----------------------|-------------|--|-------|-------------|------|-----|------|------|------|------|-----------------------|--|-------------|----------|-------|--|------|------|------|------|------|-----|
| [7:0]                 | CH2_A_VOUT  | <p>Output voltage setting A: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br/>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br/>Write-protected when value is written below 0.30 V or above 1.90 V</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1E</td> <td>0.3</td> </tr> <tr> <td>0x1F</td> <td>0.31</td> </tr> <tr> <td>0x20</td> <td>0.32</td> </tr> <tr> <td colspan="2">Continuing through...</td></tr> <tr> <td><b>0x64</b></td> <td><b>1</b></td> </tr> <tr> <td colspan="2">To...</td></tr> <tr> <td>0xBC</td> <td>1.88</td> </tr> <tr> <td>0xBD</td> <td>1.89</td> </tr> <tr> <td>0xBE</td> <td>1.9</td> </tr> </tbody> </table> | Value | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | <b>0x64</b> | <b>1</b> | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
| Value                 | Description |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1E                  | 0.3         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1F                  | 0.31        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x20                  | 0.32        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| Continuing through... |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| <b>0x64</b>           | <b>1</b>    |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| To...                 |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBC                  | 1.88        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBD                  | 1.89        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBE                  | 1.9         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |

**Table 55: BUCK\_BUCK2\_6 (0x002E)**

| Bit                   | Symbol      | Description  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
|-----------------------|-------------|--|-------|-------------|------|-----|------|------|------|------|-----------------------|--|-------------|----------|-------|--|------|------|------|------|------|-----|
| [7:0]                 | CH2_B_VOUT  | <p>Output voltage setting B: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1<br/>From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V)<br/>Write-protected when value is written below 0.30 V or above 1.90 V</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1E</td> <td>0.3</td> </tr> <tr> <td>0x1F</td> <td>0.31</td> </tr> <tr> <td>0x20</td> <td>0.32</td> </tr> <tr> <td colspan="2">Continuing through...</td></tr> <tr> <td><b>0x64</b></td> <td><b>1</b></td> </tr> <tr> <td colspan="2">To...</td></tr> <tr> <td>0xBC</td> <td>1.88</td> </tr> <tr> <td>0xBD</td> <td>1.89</td> </tr> <tr> <td>0xBE</td> <td>1.9</td> </tr> </tbody> </table> | Value | Description | 0x1E | 0.3 | 0x1F | 0.31 | 0x20 | 0.32 | Continuing through... |  | <b>0x64</b> | <b>1</b> | To... |  | 0xBC | 1.88 | 0xBD | 1.89 | 0xBE | 1.9 |
| Value                 | Description |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1E                  | 0.3         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x1F                  | 0.31        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0x20                  | 0.32        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| Continuing through... |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| <b>0x64</b>           | <b>1</b>    |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| To...                 |             |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBC                  | 1.88        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBD                  | 1.89        |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |
| 0xBE                  | 1.9         |  |       |             |      |     |      |      |      |      |                       |  |             |          |       |  |      |      |      |      |      |     |

## High-Performance Dual-Channel DC-DC Converter

**Table 56: BUCK\_BUCK2\_7 (0x002F)**

| Bit   | Symbol                  | Description   |       |             |     |                         |     |                     |     |                   |     |                     |
|-------|-------------------------|---|-------|-------------|-----|-------------------------|-----|---------------------|-----|-------------------|-----|---------------------|
| [3]   | Reserved                | Reserved  |       |             |     |                         |     |                     |     |                   |     |                     |
| [2]   | Reserved                | Reserved  |       |             |     |                         |     |                     |     |                   |     |                     |
| [1:0] | CH2_RIPPLE_CANCEL       | <p>Ripple cancel control (can be used to improve output overshoot at heavy to light load transient).</p> <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x0</td><td><b>No ripple cancel</b></td></tr><tr><td>0x1</td><td>Small ripple cancel</td></tr><tr><td>0x2</td><td>Mid ripple cancel</td></tr><tr><td>0x3</td><td>Large ripple cancel</td></tr></tbody></table> | Value | Description | 0x0 | <b>No ripple cancel</b> | 0x1 | Small ripple cancel | 0x2 | Mid ripple cancel | 0x3 | Large ripple cancel |
| Value | Description             |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x0   | <b>No ripple cancel</b> |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x1   | Small ripple cancel     |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x2   | Mid ripple cancel       |   |       |             |     |                         |     |                     |     |                   |     |                     |
| 0x3   | Large ripple cancel     |   |       |             |     |                         |     |                     |     |                   |     |                     |

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## High-Performance Dual-Channel DC-DC Converter

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### 5.1.4     Serialization

**Table 57: OTP\_DEVICE\_ID (0x0048)**

| Bit   | Symbol | Description |
|-------|--------|-------------|
| [7:0] | DEV_ID | Device ID   |

**Table 58: OTP\_VARIANT\_ID (0x0049)**

| Bit   | Symbol | Description        |
|-------|--------|--------------------|
| [7:4] | MRC    | Mask Revision Code |
| [3:0] | VRC    | Chip Variant Code  |

**Table 59: OTP\_CUSTOMER\_ID (0x004A)**

| Bit   | Symbol  | Description |
|-------|---------|-------------|
| [7:0] | CUST_ID | Customer ID |

**Table 60: OTP\_CONFIG\_ID (0x004B)**

| Bit   | Symbol     | Description |
|-------|------------|-------------|
| [7:0] | CONFIG_REV | OTP Variant |

## 6 Package Information

### 6.1 Package Outlines

## High-Performance Dual-Channel DC-DC Converter

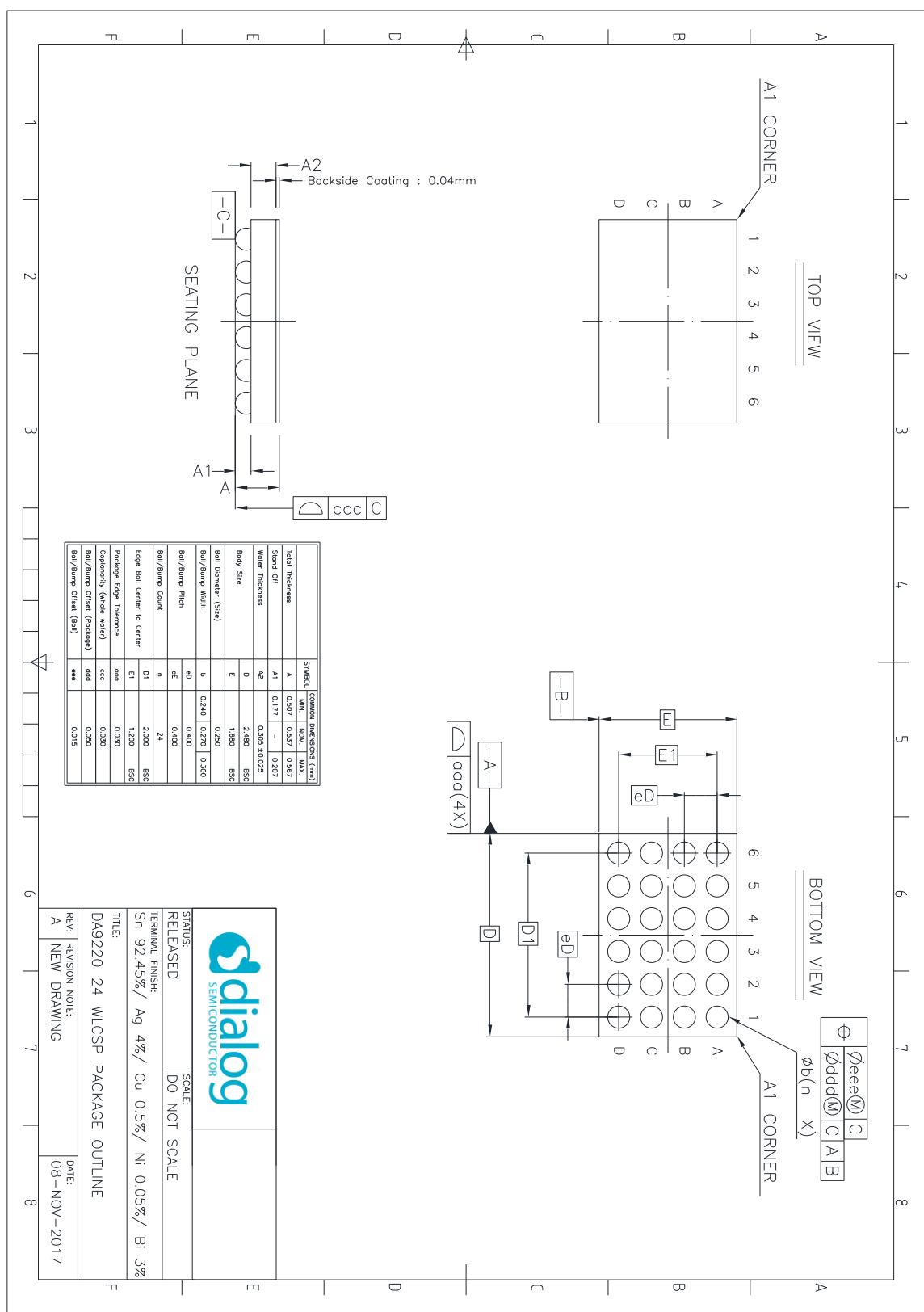


Figure 24: Package Outline Drawing

## High-Performance Dual-Channel DC-DC Converter

### 6.2 Moisture Sensitivity Level

The moisture sensitivity level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 61](#).

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The DA9220 package is qualified for MSL1.

**Table 61: MSL Classification**

| MSL Level | Floor Lifetime | Conditions       |
|-----------|----------------|------------------|
| MSL 1     | Unlimited      | ≤30 °C / 85 % RH |

### 6.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

### 6.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

## High-Performance Dual-Channel DC-DC Converter

## 7 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's [customer support portal](#) or your local sales representative.

**Table 62: Ordering Information**

| Part Number  | Package  | Size (mm) | Shipment Form | Pack Quantity |
|--|----------|-----------|---------------|---------------|
| DA9220-xxV72   | 24 WLCSP | 2.5 x 1.7 | T&R           | 4500          |
| DA9220-xxV76   | 24 WLCSP | 2.5 x 1.7 | Waffle Tray   | 140           |
| DA9220-70V72<br>Standard OTP Variant<br>V <sub>OUT1</sub> = 1.2 V, V <sub>OUT2</sub> = 1.8 V | 24 WLCSP | 2.5 x 1.7 | T&R           | 4500          |
| DA9220-70V76<br>Standard OTP Variant<br>V <sub>OUT1</sub> = 1.2 V, V <sub>OUT2</sub> = 1.8 V | 24 WLCSP | 2.5 x 1.7 | Waffle Tray   | 140           |
| DA9220-71V72<br>Standard OTP Variant<br>V <sub>OUT1</sub> = 1.0 V, V <sub>OUT2</sub> = 1.0 V | 24 WLCSP | 2.5 x 1.7 | T&R           | 4500          |
| DA9220-71V76<br>Standard OTP Variant<br>V <sub>OUT1</sub> = 1.0 V, V <sub>OUT2</sub> = 1.0 V | 24 WLCSP | 2.5 x 1.7 | Waffle Tray   | 140           |

## 8 Application Information

The following recommended components are examples selected from requirements of a typical application.

### 8.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

**Table 63: Recommended Capacitor Types**

| Application                    | Value      | Size | Temp. Char.    | Tol. (%) | V-Rate | Type                        |
|--------------------------------|------------|------|----------------|----------|--------|-----------------------------|
| V <sub>OUT</sub> output bypass | 10 $\mu$ F | 0402 | X5R $\pm$ 15 % | $\pm$ 20 | 6.3 V  | Murata<br>GRM155R60J106ME15 |
| PVDDx bypass                   | 10 $\mu$ F | 0603 | X5R $\pm$ 15 % | $\pm$ 20 | 25 V   | Murata<br>GRM188R61E106MA73 |
| AVDD bypass                    | 1 $\mu$ F  | 0402 | X5R $\pm$ 15 % | $\pm$ 10 | 10 V   | Murata<br>GRM155R61A105KE15 |

**High-Performance Dual-Channel DC-DC Converter****8.2 Inductor Selection**

Inductors should be selected based on the following parameters:

- Rated maximum current

Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.

- DC resistance

Critical for the converter efficiency and should therefore be minimized.

**Table 64: Recommended Inductor Types**

| Value<br>( $\mu$ H) | Size (mm)        | IMAX (DC)<br>(A) | ISAT (A) | Tol. (%) | DC<br>Resistance<br>(m $\Omega$ ) | Type                                       |
|---------------------|------------------|------------------|----------|----------|-----------------------------------|--|
| 0.1                 | 2.0 x 1.6 x 1.0  | 6.5              | 9.0      | $\pm 20$ | 11.5                              | Cyntec<br>HTEN20161T-R10MDR                |
| 0.1                 | 1.6 x 0.8 x 1.0  | 5.2              | 6.5      | $\pm 20$ | 17                                | Taiyo Yuden<br>MEKK1608TR10M               |
| 0.1                 | 1.6 x 0.8 x 0.8  | 4.1              | 9.4      | $\pm 20$ | 19                                | Taiyo Yuden<br>MCHK1608TR10MJN             |
| 0.11                | 2.0 x 1.25 x 0.8 | 5.8              | 6.9      | $\pm 20$ | 9.1                               | Taiyo Yuden<br>MCHK2012TR11MKG             |
| 0.1                 | 1.0 x 0.5 x 0.55 | 2.3              | 2.2      | $\pm 20$ | 41                                | Taiyo Yuden<br>MCEE1005TR10MHN             |
| 0.1                 | 2.5 x 2.0 x 1.2  | 12               | 13       | $\pm 20$ | 4                                 | TDK<br>TFM252012ALMAR10MT                  |
| 0.1                 | 1.6 x 0.8 x 0.95 | 3.8              | 4.3      | $\pm 20$ | 15                                | Tokyo Coil Engineering<br>TFP160810M-R10N  |
| 0.11                | 2.0 x 1.6 x 0.6  | 3.0              | 6.0      | $\pm 20$ | 24                                | Wurth Elektronik<br>WE-PMMI 744 799 771 11 |

**High-Performance Dual-Channel DC-DC Converter****Revision History**

| Revision | Date        | Description   |
|----------|-------------|---|
| 2.2      | 15-Feb-2022 | <p>Modification:</p> <ul style="list-style-type: none"> <li>Rebranded to Renesas</li> </ul>   |
| 2.1      | 17-Sep-2020 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 4.2.3.4: Added new section</li> <li>Section 8.2: Updated <a href="#">Table 64</a></li> </ul>   |
| 2.0      | 18-Jul-2019 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 3.5: Updated <math>R_{PD}</math> condition</li> <li>Section 3.9: Added typical performance graphs</li> <li>Section 7: Updated <a href="#">Table 62: Ordering Information</a></li> <li>Section 8.2: Updated <a href="#">Table 64: Recommended Inductor Types</a></li> </ul>   |
| 1.1      | 01-Mar-2019 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 3.5: Updated Buck <math>t_{BUCK\_EN}</math> parameter condition and value, <math>RPD</math> parameter description</li> <li>Section 3.7 Updated <math>R_{PD}</math> and <math>R_{PU}</math> parameter values</li> <li>Section 8.2: Updated <a href="#">Table 64: Recommended Inductor Types</a></li> <li>Removed watermark</li> </ul>   |
| 1.0      | 02-Oct-2018 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 3.5: Updated Buck <math>V_{OUT\_TR\_LINE}</math>, <math>V_{OUT\_TR\_LD\_1PH}</math>, and <math>I_{Q\_PFM\_1PH}</math> parameter descriptions</li> <li>Section 5.1.2: Updated BUCK_BUCK1_4 register description</li> <li>Section 5.1.3: Updated BUCK_BUCK2_4 register description</li> </ul>  |
| 0.3      | 28-Sep-2018 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 3.5: Updated Buck <math>R_{ON\_PMOS}</math> and <math>R_{ON\_NMOS}</math> parameter values</li> <li>Section 0: Updated <math>V_{THR\_POR}</math> parameter and added <math>V_{THR\_POR\_HYS}</math> parameter</li> </ul>   |
| 0.2      | 10-Jul-2018 | <p>Modifications:</p> <ul style="list-style-type: none"> <li>Section 3.1: Updated <math>V_{SYS}</math> and <math>V_{PIN}</math> Max values and moved note to Section 3.3.1</li> <li>Section 3.2: Added <math>V_{PIN}</math> and updated note</li> <li>Section 3.3.1: Updated thermal ratings</li> <li>Section 3.3.2: Updated power dissipation and added <a href="#">Figure 5: 24WLCSP Power Derating Curve</a></li> <li>Section <b>Error! Reference source not found.</b>: Updated Buck electrical characteristics</li> <li>Section 0: Added <math>I_{IN\_OFF}</math> and <math>I_{IN\_ON}</math> parameters</li> <li>Section 4.1: Updated DC-DC buck converter description</li> <li>Section 4.1.2: Removed mention of phase shedding</li> <li>Section 4.1.4: Renamed section to Soft Start-Up and Shutdown</li> <li>Section 4.2.3.2: Added <a href="#">Figure 20: Power Good (PG) and System Good (SG)</a></li> <li>Section 5.1: Updated Register map</li> <li>Section 5.1.2: Updated BUCK_BUCK1_2 register description and added BUCK_BUCK1_7</li> <li>Section 5.1.3: Updated BUCK_BUCK2_2 register description and added BUCK_BUCK2_7</li> <li>Section 5.1.4: Updated MRC bit (register <math>OTP\_VARIANT\_ID</math>) reset value</li> </ul> |

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## High-Performance Dual-Channel DC-DC Converter

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| Revision | Date        | Description   |
|----------|-------------|---|
|          |             | <ul style="list-style-type: none"><li>Section 7: Added part numbers</li><li>Section 8.2: Updated Table 64: Recommended Inductor Types</li></ul> |
| 0.1      | 12-Apr-2018 | Initial version.  |

## High-Performance Dual-Channel DC-DC Converter

### Status Definitions

| Revision | Datasheet Status | Product Status | Definition   |
|----------|------------------|----------------|--|
| 1.<n>    | Target           | Development    | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.   |
| 2.<n>    | Preliminary      | Qualification  | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.  |
| 3.<n>    | Final            | Production     | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via <a href="http://www.dialog-semiconductor.com">www.dialog-semiconductor.com</a> . |
| 4.<n>    | Obsolete         | Archived       | This datasheet contains the specifications for discontinued products. The information is provided for reference only.  |

### RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

## High-Performance Dual-Channel DC-DC Converter

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