InnoSwitch3-Pro Family

Digitally Controllable Off-Line CV/CC QR Flyback Switcher IC with Integrated High-Voltage Switch, Synchronous Rectification and FluxLink Feedback

Product Highlights

Digitally Controlled via I²C Interface

- Dynamic adjustment of power supply voltage and current
- Telemetry for power supply status and fault monitoring
- Comprehensive set of configurable protection features
- PowiGaN™ technology – up to 100 W without heatsinks (INN3378C, INN3379C and INN3370C)

Highly Integrated, Compact Footprint

- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

EcoSmart™ – Energy Efficient

- Less than 30 mW no-load including line sense and MCU
- Enables power supply designs that easily comply with all global energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Input voltage monitoring with accurate brown-in/brown-out and overvoltage protection
- Output OV/UV fault detection with independently configured responses
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Programmable watchdog timer for system faults

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 and TUV (EN60950 and EN62368) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- High efficiency USB PD 3.0 + PPS/QC adapters
- Multi protocol adapters including QuickCharge, AFC, FCP, SCP
- Direct-charge mobile device chargers
- Multi-chemistry tool and general purpose battery chargers
- Adjustable CV and CC LED ballast

Description

The InnoSwitch™3-Pro series family of ICs dramatically simplifies the development and manufacturing of fully programmable, highly efficient power supplies, particularly those in compact enclosures. The universal I²C interface enables dynamic control of output voltage and current along with many configurable features. Telemetry provides reporting of programmed features and fault modes.

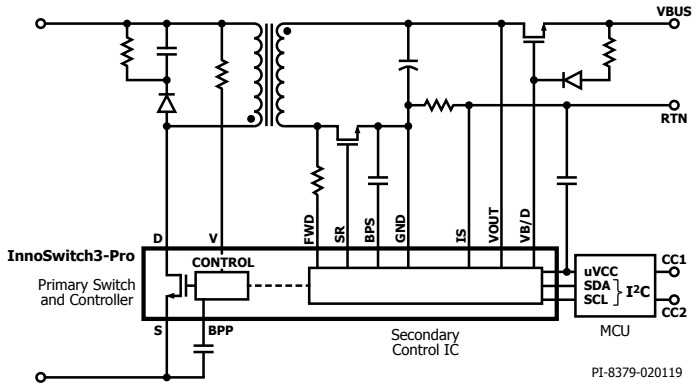


Figure 1. Typical Application.

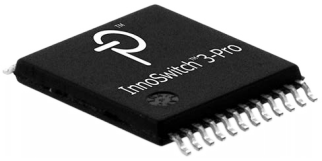


Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table[1]

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN3365C/3375C	25 W	30 W	22 W	25 W
INN3366C/3376C	35 W	40 W	27 W	36 W
INN3377C	40 W	45 W	36 W	40 W
INN3367C	45 W	50 W	40 W	45 W
INN3368C	55 W	65 W	50 W	55 W
INN3378C	70 W	75 W	55 W	65 W
INN3379C	80 W	85 W	65 W	75 W
INN3370C	90 W	100 W	75 W	85 W

Table 1. Output Power Table.

Notes:

1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. C Package: InSOP-24D.
5. INN336xC – 650 V MOSFET, INN337xC – 725 V MOSFET, INN3378C, INN3379C and INN3370C – 750 V PowiGaN switch.

InnoSwitch3-Pro devices are ideal for AC/DC power supply applications where fine (10 mV, 50 mA) output voltage and current adjustment are necessary. Typical implementations comprise a system microprocessor or dedicated microcontroller with an I²C port that is used to configure, control and supervise operation of the power sub-system. The uVCC pin provides a bias supply for the microprocessor in stand-alone implementations such as USB PD adapters and chargers.

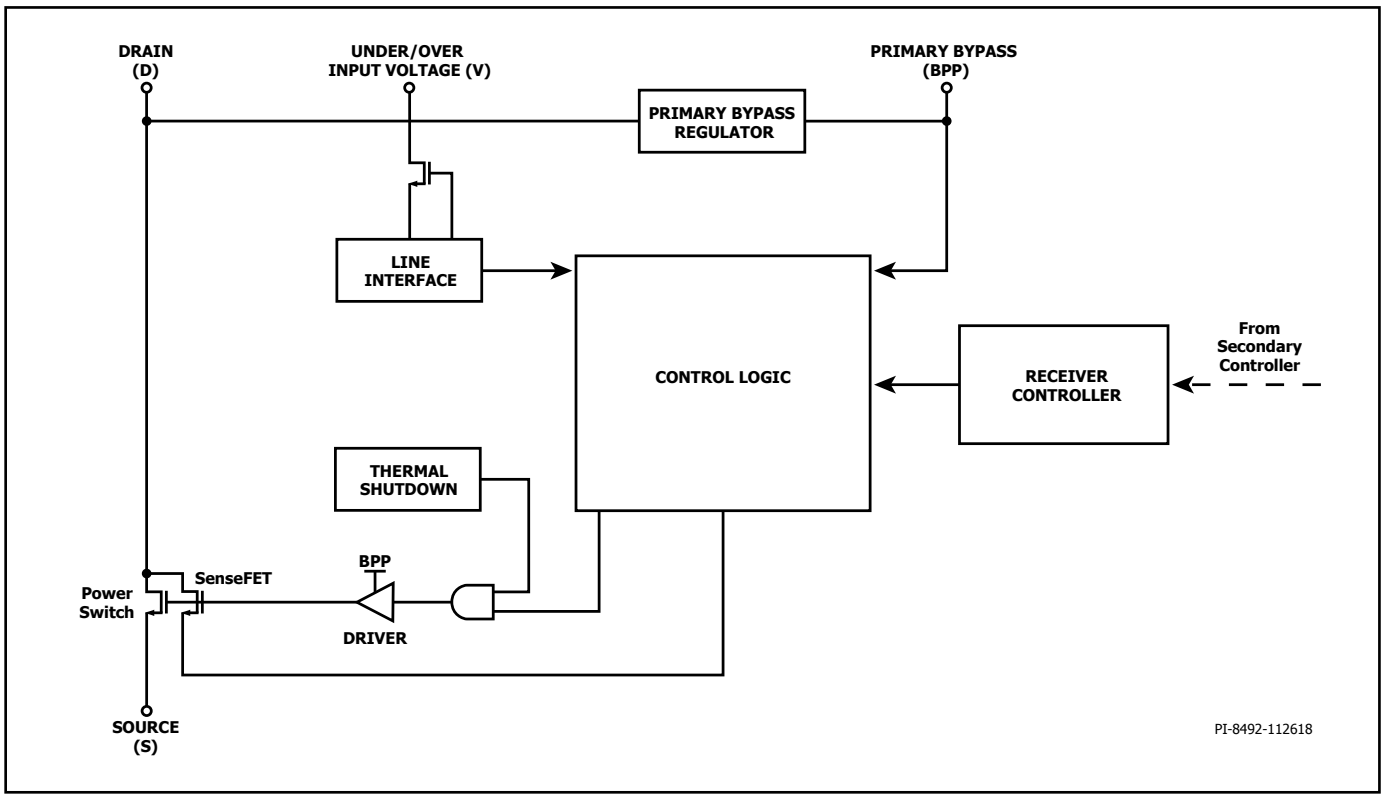


Figure 3. Primary Controller Block Diagram.

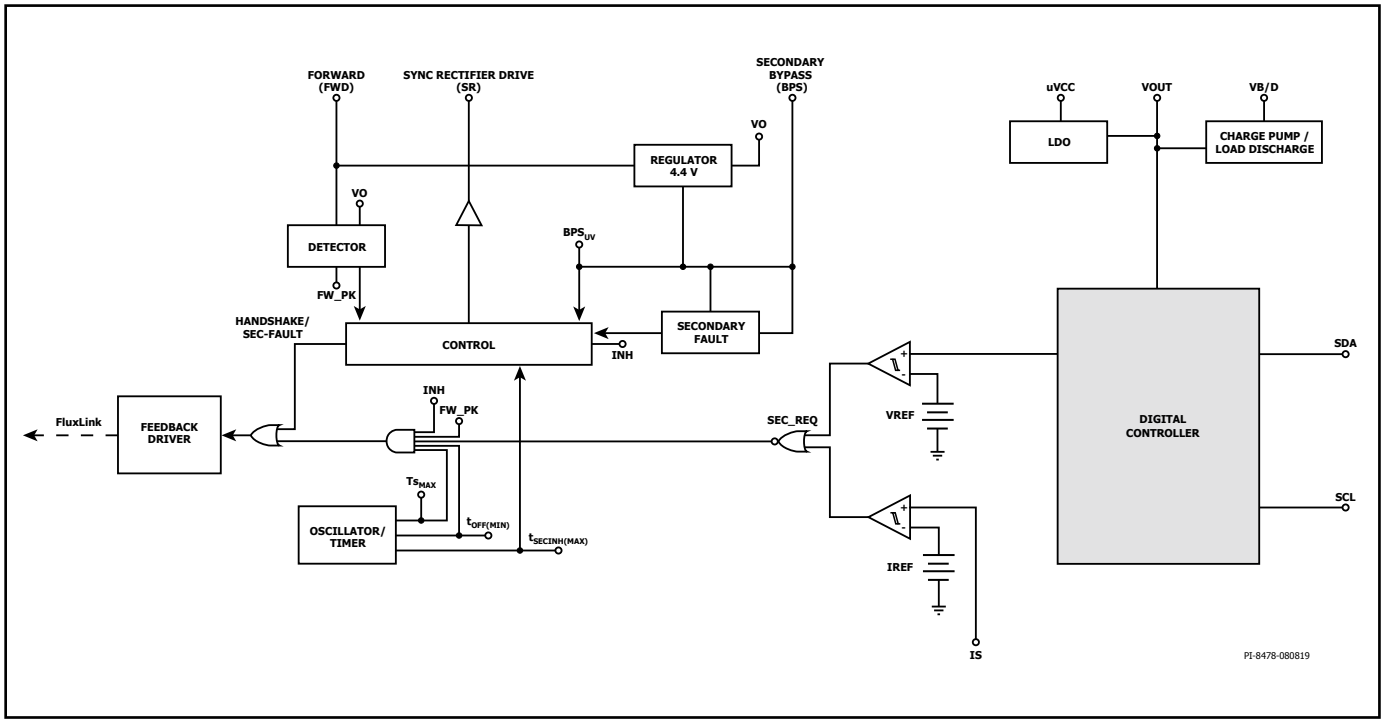


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

NC Pin (Pin 3)
Leave open. Should not be connected to any other pins.

SECONDARY BYPASS (BPS) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the secondary IC supply.

I²C Clock (SCL) Pin (Pin 5)
I²C serial communication protocol clock line sourced by the Bus master (max 700 kHz).

I²C Serial Data (SDA) Pin (Pin 6)
I²C serial communication protocol data line sourced by the Bus master (max 700 kHz).

External VCC Supply (uVCC) Pin (Pin 7)
This is a 3.6 V supply for an external controller.

VBUS Series Switch Drive and Load Discharge (VB/D) Pin (Pin 8)
VBUS enable and driver for NMOS gate for VOUT to VBUS pass FETs. This pin can also be used to discharge output load voltage.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver output and connection to external SR FET gate terminal.

OUTPUT VOLTAGE (VOUT) Pin (Pin 10)
Connected directly to the output voltage providing current for the secondary IC and sense for output voltage regulation. Also active pull-down current source for minimum load.

FORWARD (FWD) Pin (Pin 11)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing plus providing power for the secondary IC when V_{OUT} is below a threshold value.

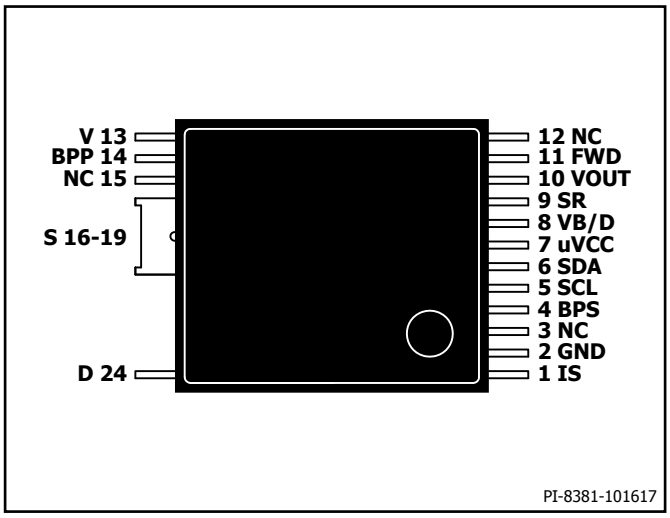


Figure 5. Pin Configuration.

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting under and overvoltage conditions at the power supply input. When connected to the AC side of the bridge, a high-voltage switch is opened when not sensing to reduce power consumption. This pin should be tied to GND to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
It is the connection point for an external bypass capacitor for the primary IC supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
This pin is the power switch drain connection.

InnoSwitch3-Pro Functional Description

The InnoSwitch3-Pro combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to communicate accurate direct sensing of the output voltage and output current on the secondary IC to the primary IC.

The primary controller on InnoSwitch3-Pro is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection and leading edge blanking.

The InnoSwitch3-Pro secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, an I^2C interface to control power supply parameters and telemetry functions, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, QR mode circuit, oscillator and timing functions, and a host of integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

InnoSwitch3-Pro has variable frequency QR controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-Pro to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass ILIM Programming

InnoSwitch3-Pro ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes - 0.47 µF and 4.7 µF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{BP} to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has a OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds ISD, the device will latch-off or auto-restart depending on the H-code.

VOUT OV protection is also included as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response depending on the H-code.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

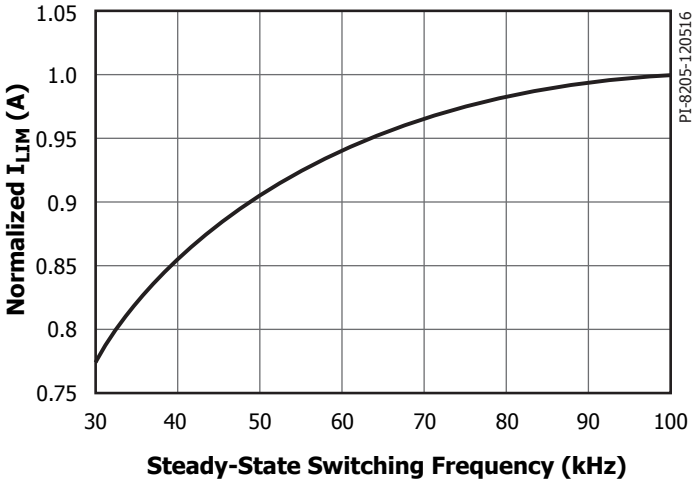


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter
The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart
In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-Pro enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~ 3 V or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection
In the event that there are two consecutive cycles where the drain current is reached 110% of I_{LIM} within ~500 ns (the blanking time + current limit delay time) (including leading edge current spike), the controller will skip 2.5 cycles or ~25 μs (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring
The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage (V_V) switch on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. The controller samples the input line at light load conditions when the time between switching cycles is 50 μsec or more. At <50 μsec between switching cycles, the high-voltage switch will remain on making sensing continuous.

Primary-Secondary Handshake
At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

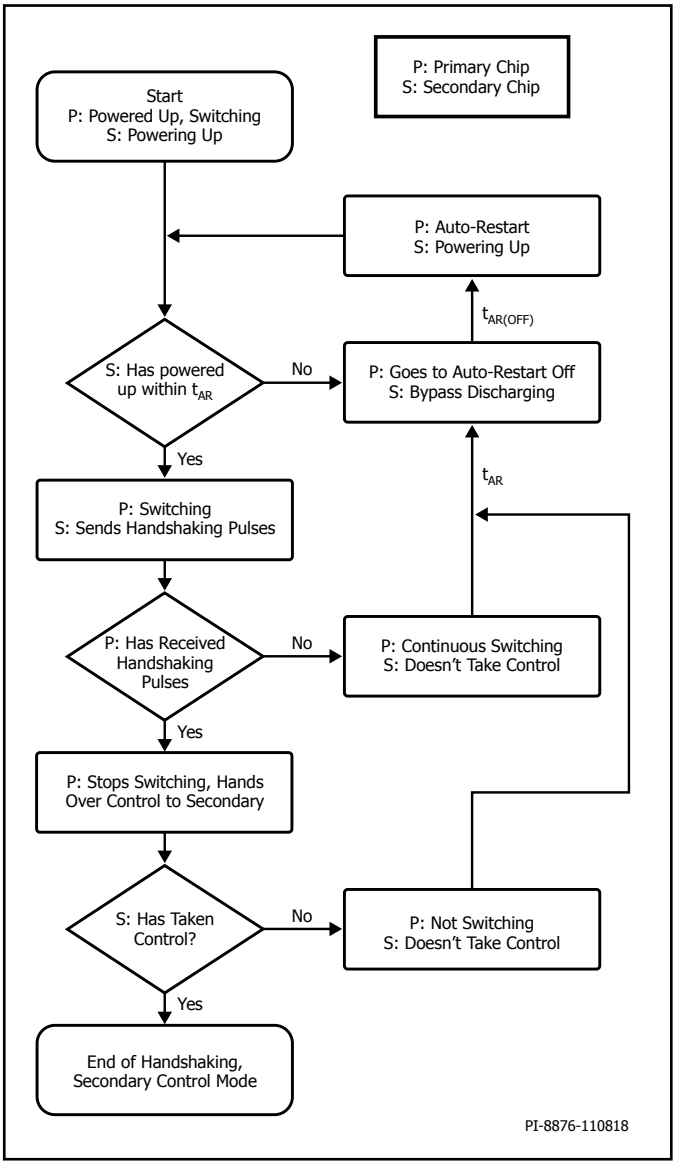


Figure 7. Primary-Secondary Handshake Flow Chart.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoSwitch3-Pro features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 5 kHz and 12 kHz - 200 µs and 83 µs period respectively. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered through regulator 4.4 V block by either VOUT or FW connections to the SECONDARY BYPASS pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below the $V_{SR(TH)}$ threshold.

In continuous conduction mode (CCM) operation of the SR FET is turned off when the feedback pulse is sent to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off while operating in continuous mode.

The output voltage is regulated on the VOUT pin and defaults to 5 V at start-up.

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins regulates the output current in constant current regulator mode.

Programmable Voltage and Current

The operating voltage and current set points are set fully programmable through I^2C interface. The output voltage is fully user programmable with a range from 3 V to 24 V. The fast response feedback loop of the IC features 10 mV (ΔV_{OUT}) voltage change resolution. The programmable current set point features 20% to 100% operating range, with a programming step size of 0.8% of full scale current. Below 5 V and for load current less than 50 mA, voltage command step size of 10 mV may result in non-montonicity since operating frequency is very low.

Internal uVCC Generation, Bus Switch Driver and Discharge
The internal LDO generates 3.6 V uVCC for MCU which simplifies the system design. InnoSwitch3-Pro also has an internal driver that guarantees turn-on of an n-channel FET series bus switch with source voltage as high as 24 V. The VB/D pin which enables the bus switch is also configurable as the discharge path for the load.

Programmable Protections
User programmable protection features include output undervoltage (UV) and overvoltage (OV) protection and over-temperature protection. The UV/OV thresholds are dynamically programmable. Users can program three responses to these protections, including auto-restart, latch-off and no-response. An auto-restart (AR) or latch-off (LO) response does not inherently open the series bus switch. The I²C master must send a command to open it if this is the desired behavior.

The secondary controller also features generation of an interrupt signal if one or more of the faults is detected. The SCL pin is pulled down for ~55 µs to generate an interrupt for MCU.

In the case when the MCU loses communication with the secondary controller, a watchdog timer triggers a reset to reassert a safe 5 V condition and opens the series bus switch.

Telemetry Feature
The controller communicates to the MCU to report back the status of the power supply. Output voltage and current is measured by internal ADC and available to MCU through I²C. The telemetry features also covers CV, CC and constant power set points, OV/UV thresholds, all protection settings, interrupt status, and complete fault status.

Minimum Off-Time
The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 70% of the maximum programmed current limit (at f_{SREQ} operation).

After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

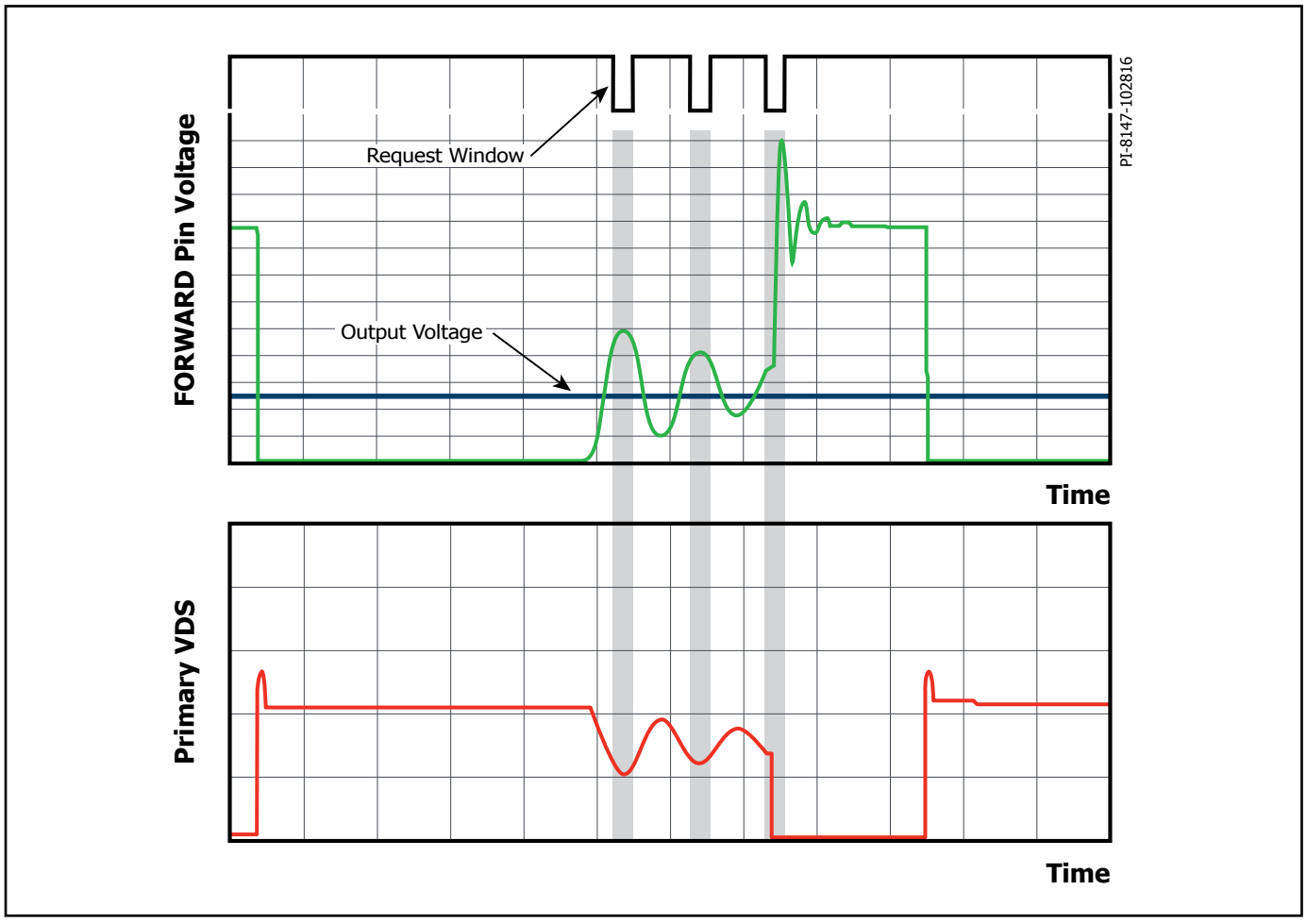


Figure 8. Intelligent Quasi-Resonant Mode Switching.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the 3.6 V before the expiration of the soft start timer ($t_{SS(RAMP)}$) after handshake has occurred.

If the output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period

Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Output Voltage Weak Bleeder

In the event that the sensed voltage on the OUTPUT VOLTAGE pin is slightly higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

SECONDARY BYPASS Pin Overvoltage Protection

The InnoSwitch3-Pro secondary controller features a SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ the secondary will initiate a fault response dictated by sec-fault response.

SR Disable Protection

In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down

To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection

In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. At start-up the controller will apply a current to the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF the resulting voltage is above the reference voltage, and the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF (the resulting voltage is below the reference voltage), the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching

In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-Pro features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous-conduction mode (CCM). See Figure 8.

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-Resonant (QR) mode is enabled for 20 µsec after DCM is detected. QR switching is disabled after 20 µsec, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

Register Definition

I²C Slave Address

The InnoSwitch3-Pro 7-bit slave address is 0x18 (7'b001 1000).

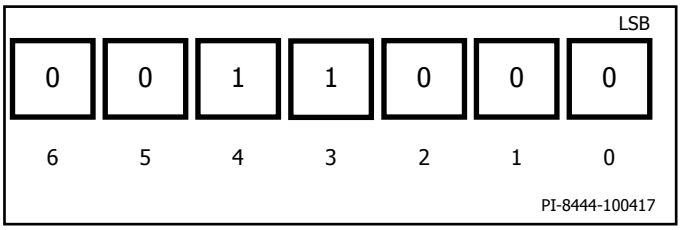


Figure 9. PI Slave Address.

I²C Protocol Format is 3-Byte Write Command

Write commands:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Byte][A] or
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Low Byte][A][High Byte][A]

Write and Read Command I²C Protocol

[A] denotes a Slave Acknowledgement
[a] denotes a Master Acknowledgement
[na] denotes a Master nack
[W] denotes Write (1'b0)
[r] denotes Read (1'b1)
[PI_SLAVE_ADDRESS] = 0x18 (7'b001 1000)
[PI_COMMAND] (see PI COMMAND Register Address Assignments, Description and Control Range Section)
[TELEMETRY_REGISTER_ADDRESS] (see Telemetry (Read-Back) Registers Address Assignment and Description Section)

Every I²C transaction should have a minimum of 150 µsec delay between commands. If this delay is not provided commands may be ignored. The InnoSwitch3-Pro does not support clock stretching.

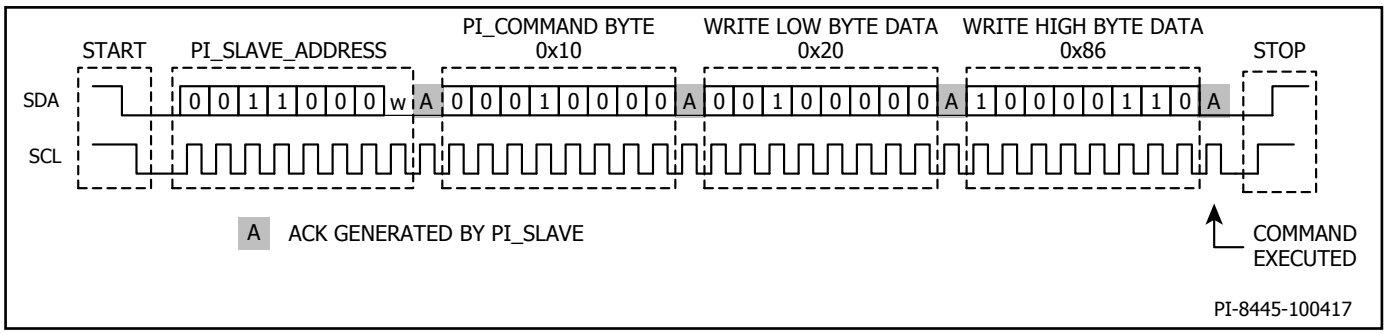


Figure 10. Example Register Write Command Sequence (CV set to 8 V).

I²C Protocol Format is 2-Byte Read Command

Word Read transaction:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][START_TELEMETRY_REGISTER_ADDRESS]
[A][END_TELEMETRY_REGISTER_ADDRESS [A]
[PI_SLAVE_ADDRESS] [r][A]{PI Slave responds Low Byte}[a]{PI Slave responds High Byte}[na]

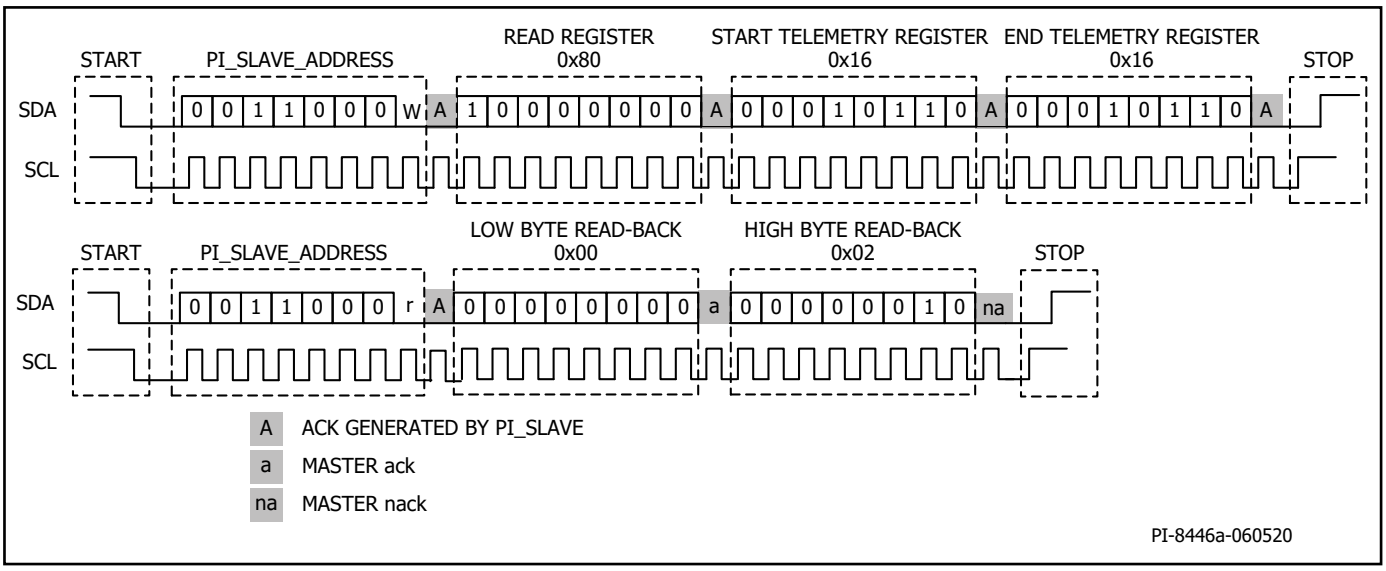


Figure 11. Example Read Register Sequence (Read Fault Register READ11). Note: START and END TELEMETRY Register Addresses Does Not Have to Point to Same Register to Read multiple Registers in Single Command.

PI COMMAND Register Address Assignments, Description and Control Range

All command register addresses in InnoSwitch3-Pro are odd-parity addressing. Some select registers (some highlighted below) also employ odd parity error bit to the high and low bytes of data.

Name	Function	Adjustment Range	Register Address		Type	Default	Description		
			Address	Address with Odd Parity					
VBEN	Series Bus Switch Control	Enable or Disabled?	0x04		WR_Byte	0x0	bit[7]	Parity	
							bit[1:0]	{11} Enable VBEN/Disable VDIS {00} Disable VBEN	
BLEEDER	Activate Bleeder (V_{OUT}) Function	Enable or Disabled?	0x06	0x86	WR_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled OTP clears this register	
VDIS	Load (VBUS) Discharge	Enable or Disabled?	0x08		W/R_Byte	0x0	bit[7]	Parity	
							bit[1:0]	{11} Enable Discharge/Disable VBEN	
							bit[3:2]	{11} Disable Discharge	
Turn-Off PSU	Latch-off Device	Enable or Disabled?	0x0A	0x8A	W/R_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled	
Fast VI Command	Speed of CV/CC Update	10 ms Update Limit or No Speed Limit?	0x0C	0x8C	W/R_Byte	0x0	bit[0]	{1}: Disable 10 msec update limit	
CVO	Constant-Voltage Only	Only CV Mode	0x0E		W/R_Byte	0x0	bit[0]	{1}: CV Only Mode/No CC Regulation	
CV	Output Voltage	3 V to 24 V (10 mV/step)	0x10		W/R_Word	500 (5 V)	bit[15]	High Byte Parity	Range {300 to 2400} 10 mV/LSB
							bit[12:8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
OVA	Overvoltage Threshold	6.2 V to 25 V (100 mV/step)	0x12	0x92	W/R_Word	62 (6.2 V)	bit[15]	High Byte Parity	Range {62 to 250} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
UVA	Undervoltage Threshold	3 V to 24 V (100 mV/step)	0x14	0x94	W/R_Word	36 (3.6 V)	bit[15]	High Byte Parity	Range {30 to 240} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
CDC	Cable Drop Compensation	0 mV to 600 mV (50 mV/step)	0x16		W/R_Word	0 (0 V)	bit[3:0]	Range {0 to 12} 50 mV/LSB	
CC	Constant Current Regulation	20% to 100% of CC, (0.25 mV/ step/Rs)	0x18	0x98	W/R_Word	128 (100%)	bit[15]	High Byte Parity	Range {25 (20%) to 128 (100%)}
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		

Table 2. Command Register Assignments.

Name	Function	Adjustment Range	Register Address		Type	Default	Description	
			Address	Address with Odd Parity				
V_{KP}	Constant Output Power Knee Voltage	5.3 V to 24 V (100 mV/step)	0x1A		W/R_Word	240 (24V)	bit[15]	High Byte Parity
							bit[8]	Range {53 to 240} 100 mV/LSB
							bit[7]	Low Byte Parity
							bit[6:0]	
OVL	Overvoltage Fault Response	Latch-off or AR or No Response?	0x1C		W/R_Byte	0x02	bit[1:0]	{00}: No Response {01}: Latch-off {10}: Auto-Restart
UVL	Undervoltage Fault Response	Latch-off or AR or No Response?	0x1E	0x9E	W/R_Byte	0x0	bit[1:0]	{00}: Auto-Restart {01}: Latch-off {10}: No Response
CCSC	Output Short-Circuit Fault Detection	AR or No-Response	0x20		W/R_Byte	0x02	bit[1:0]	{00}: No Response {10}: Auto-Restart
ISSC	IS-pin Short Fault Response and Detection Frequency	Latch-off or AR or No Response?	0x22	0xA2	W/R_Byte	0x00	bit[1:0]	{00}: No Response {01}: Latch-off {10}: Auto-Restart
		Frequency? (30kHz/40kHz/ 50kHz/60kHz)					bit[3:2]	Frequency Detection Threshold {00}: 50kHz {01}: 30kHz {10}: 40kHz {11}: 60kHz
UVL Timer	UVL Fault Timer	8/16/32/64 msec	0x24	0xA4	W/R_Byte	0x03 (64 msec)	bit[1:0]	{00}: 8 msec {01}: 16 msec {10}: 32 msec {11}: 64 msec
Watchdog Timer	Communication Rate Monitor	Disable/0.5 s/1 s/2 s	0x26		W/R_Byte	0x01 (0.5 sec)	bit[1:0]	{00}: No Watch-Dog {01}: 0.5 sec {10}: 1 sec {11}: 2 sec
CVOL	Constant Voltage Mode Fault Response	Latch-off or AR or No Response?	0x28	0xA8	W/R_Byte	0x00	bit[1:0]	{00}: No Response {01}: Auto-Restart {10}: Latch-off
CVOL Timer	Constant Voltage Fault Timer	8/16/32/64 msec	0x2A		W/R_Byte	0x00 (8 msec)	bit[1:0]	{00}: 8 msec {01}: 16 msec {10}: 32 msec {11}: 64 msec
Interrupt	Interrupt Mask	Writing a non-zero value enables interrupt	0x2C		W/R_Byte	0x00	bit[6]	Control Secondary
							bit[5]	BPS Current Latch-off
							bit[4]	CVO Mode Peak load timer
		Interrupt is automatically disabled after one interrupt pulse sent out					bit[3]	IS-pin Short
							bit[2]	Output Short-Circuit
							bit[1]	Vout(UV)
							bit[0]	Vout(OV)
OTP	Secondary Over-Temperature Fault Hysteresis	40°C/60°C	0x2E	0xAE	W/R_Byte	0x00	bit[0]	{0}: 40°C {1}: 60°C

Table 2. Command Register Assignments (cont).

Telemetry (Read-Back) Registers Address Assignment and Description

	Name	Register Name	Register Address		Type	Register Bit Assignments		
			Address	Address with Odd Parity				
	READ0	Rev ID	0x00	0x80	R_Word	bit[15:0]	[Rev ID]	
Command Register Read-Back	READ1	Output Voltage Set-Point	0x02		R_Word	bit[15]	High Byte Parity	{Reg_CV}
						bit[12:8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ2	Undervoltage Threshold	0x04		R_Word	bit[15]	High Byte Parity	{Reg_UVA}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ3	Overvoltage Threshold	0x06		R_Word	bit[15]	High Byte Parity	{Reg_OVA}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ4	VBUS Switch Enable	0x08		R_Word	bit[14]	{Reg_VBEN}	
		Minimum Load				bit[13]	{Reg_BLEEDER}	
		Turn PSU Off				bit[12]	{Reg_PSUOFF}	
		Fast VI Commands				bit[11]	{Reg_FSTVIC}	
		Constant-Voltage Mode Only				bit[10]	{Reg_CVO}	
		Over-Temperature Fault Hysteresis				bit[9]	{Reg_OTP_HYS}	
		Cable Drop Compensation				bit[3:0]	{Reg_CDC}	
	READ5	Constant Current Set-Point	0x0A		R_Word	bit[15:8]	{Reg_CC}	
		Constant Power Threshold				bit[7:0]	{Reg_VKP}	
Programmed Fault Respose	READ6	Overvoltage Fault	0x0C		R_Word	bit[15:14]	{Reg_OVL}	
		Undervoltage Fault				bit[13:12]	{Reg_UVL}	
		Output Short-Circuit				bit[11:10]	{Reg_CCSC}	
		IS-pin Short				bit[9:8]	{Reg_ISSC}	
		Undervoltage Time Out				bit[7:6]	{Reg_UVLTIMER}	
		Watchdog Time Out				bit[5:4]	{Reg_WD_TIMER}	
		CV Mode				bit[3:2]	{Reg_CVMODE}	
		CV Mode Timer				bit[1:0]	{Reg_CVTIMER}	
Measurement	READ7	Measured Output Current	0x0E		R_Word	bit[15]	High Byte Parity	{Reg_MEASURED_I}
						bit[8]		
						bit[7]	Low Byte Parity	
						bit[6:0]		
	READ9	Measured Output Voltage	0x12		R_Word	bit[15:12]	4'b0	
						bit[11:0]	{Reg_MEASURED_V}	
							Vout Range	Report-back resolution
							3 - 7.2 V	20 mV
							7.2 - 10 V	50 mV
							10 - 20 V	100 mV

Table 3. Telemetry (Read-Back) Register Assignments.

Name	Description	Register Address		Type	Register Name	
		Address	Address with Odd Parity			
READ10 (Instantaneous)	Interrupt Enable	0x14		R_Word	bit[15]	{Reg_INTERRUPT_EN}
	System Ready Signal				bit[14]	{Reg_CONTROL_S}
	Output Discharge				bit[13]	{Reg_VDIS}
	Switching Frequency High?				bit[12]	{Reg_HIGH_FSW}
	Over-Temperature Protection Fault?				bit[9]	{Reg_OTP}
	Weak Bleeder Enabled				bit[5]	{Reg_VOUTWK}
	VOUTADC > 1.1*Vout				bit[4]	{Reg_VOUT10PCT}
	IS-pin Short Circuit Detected				bit[3]	{Reg_ISSC}
	Output Short-Circuit Detected				bit[2]	{Reg_CCSC}
	Output Voltage UV Fault Comparator				bit[1]	{Reg_VOUT_UV}
	Output Voltage OV Fault Comparator				bit[0]	{Reg_VOUT_OV}
READ11 (Latched)	CVO Mode AR	0x16		R_Word	bit[15]	{Reg_ar _CV}
	IS-pin Short-Circuit AR				bit[12]	{Reg_ar_ISSC}
	Output Short-Circuit AR				bit[11]	{Reg_ar_CCSC}
	Output Voltage OV AR				bit[10]	{Reg_ar_VOUT_OV}
	Output Voltage UV AR				bit[9]	{Reg_ar_VOUT_UV}
	Latch-Off (LO) Occurred				bit[7]	{Reg_LO}
	CVO Mode LO				bit[6]	{Reg_Lo_CVO}
	PSU Turn-Off CMD Received				bit[5]	{Reg_PSUOFF}
	IS-pin Short-Circuit LO				bit[4]	{Reg_Lo_ISSC}
	Output Voltage OV LO				bit[2]	{Reg_Lo_VOUT_OV}
	Output Voltage UV LO				bit[1]	{Reg_Lo_VOUT_UV}
	BPS-pin LO				bit[0]	{Reg_BPS_OV}
READ12	Interrupts	0x18		R_Word	Mask	Status
					bit[14]	bit[6]	{Reg_CONTROL_S}
					bit[13]	bit[5]	{Reg_LO_Fault}
					bit[12]	bit[4]	{Reg_CCAR}
					bit[11]	bit[3]	{Reg_ISSC}
					bit[10]	bit[2]	{Reg_CCSC}
					bit[9]	bit[1]	{Reg_VOUT_UV}
					bit[8]	bit[0]	{Reg_VOUT_OV}
READ13	Average Output Current	0x1A		R_Word	bit[15:8]		8b'0
					bit[7:0]		16 sample average of READ 7
READ14	Average Output Voltage	0x1C		R_Word	bit[15:12]		4b'0
					bit[11:0]		16 sample average of READ 9
READ15	Voltage DAC	0x5C		R_Word	bit[15:8]		DAC_100mV
					bit[7:0]		DAC_10mV

Table 3. Telemetry (Read-Back) Register Assignments (cont.)

Command Registers

System Ready Status Register

The system ready bit {Reg_control_s} must be read prior to the start of any I²C transactions and after the InnoSwitch3-Pro has entered into a reset state resulting from auto-restart (AR), latch-off (LO) or initial power-up.

When the {Reg_control_s} bit is set to "1", it means InnoSwitch3-Pro is ready to receive I²C commands.

To read the {Reg_control_s} bit, write the READ10 sub address 0x14 into the 0x80 address. Then read High Byte data back from address 0x80. The bit 14 is {Reg_control_s}.

Constant current regulation is based on the average current measurement register (READ13).

For a 5 A CC threshold, the current sense resistor is 6.4 mΩ.
The current limit step size for this example is 39.1 mA/step.

Example: For a power supply with maximum CC of 5 A (Rs = 6.4mΩ), the following demonstrates changing the CC set point from 5 A to 2.5 A. This corresponds to change in CC from 100% (0x80) to 50% (0x40) – with odd parity this becomes 0x8040:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CC Register (0x98)
Low Byte:	0x40 (8'b0100 0000)
High Byte:	0x80 (8'b1000 0000)

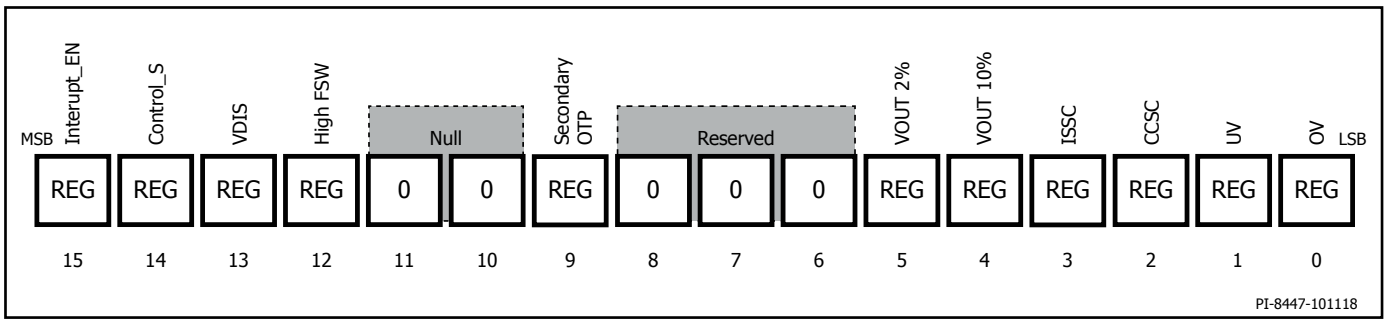


Figure 12. {Reg_Control_s} Telemetry Register (READ 10).

Example: Reading the {Reg_control_s} bit:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
PI_Command:	READ10 (0x14), READ10 (0x14)
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)

Programming Output Voltage (CV), Output Constant Current (CC), Constant Power Mode (CP), Cable Drop Compensation (CDC) and Constant Voltage Only Mode (CVO)

CV Register (0x10)
The output voltage of the power supply is regulated on the Vout-pin. The valid programming range is from 3 V to 24 V with 10 mV / lsb. The default CV register value is 5 V. Below 5 V and at light load below 50 mA, output monotonicity may not be visible with 10 mV / steps.

Example: to change CV from 5 V to 8 V
Convert 8 V to lsb representation: 8/(10mV/lsb) = 800
Convert to hex format (800 = 0x0320)
With odd parity bits added the hex data is 0x8620)
The bit I²C command for this is shown below:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CV Register (0x10)
Low Byte:	0x20 (8'b0010 0000)
High Byte:	0x86 (8'b1000 0110)

This sequence of commands is shown in Figure 10 and Figure 23.

CC Register (0x98)
The constant current regulation register address is 0x18 and with odd parity it is 0x98. The constant current regulation threshold is adjustable from 20% (d'25) CC up to 100% (d'128) of the full scale. The full-scale constant-current threshold is set with the sense resistor between the IS and GND pins. The typical value for the full-scale current voltage drop is 32 mV ($I_{SV(TH)}$). The resolution step size is (0.78%/step):

32 mV/128 = 0.25 mV/step/Rs

Constant Output Power Voltage Threshold V_{KP} (0x1A)
A constant output power characteristic is programmed via the "knee power voltage" in conjunction with the 100% constant current regulation threshold (full-scale current setting). If the full-scale CC is 2.5 A and the knee power voltage is set to 8 V, the constant power is 20 W. If the V_{KP} register were set to 12 V, the resultant constant power characteristic above the V_{KP} threshold would be 30 W.

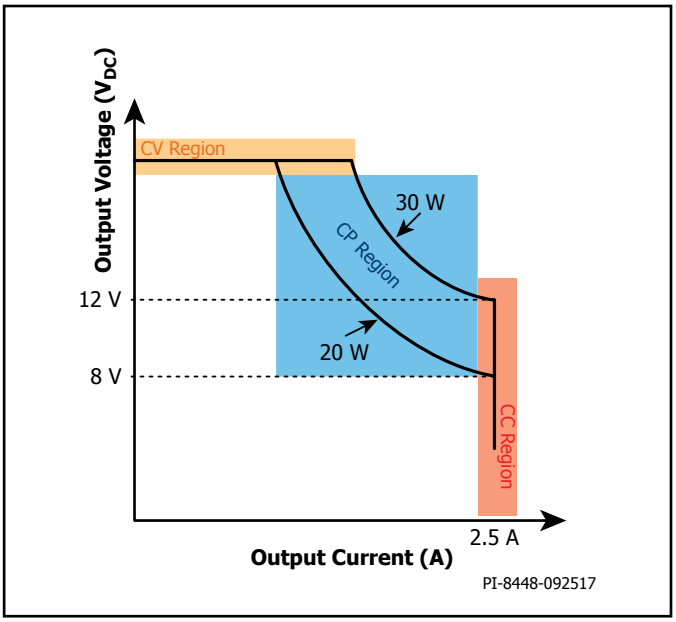


Figure 13. Constant Output Power Profile.

From no-load to heavy loading conditions, InnoSwitch3-Pro will operate in CV then transition into CP then into CC region below the V_{KP} threshold. Setting V_{KP} to maximum value (24 V) results in no Constant Output Power regulation region.

Example: To change V_{KP} from 24 V (d'240) (0xF0 = 0x0170 with odd parity) to 8 V (0x50 = 0x80D0):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VKP Register (0x1A)
Low Byte:	0xD0 (8'b1101 0000)
High Byte:	0x80 (8'b1000 0000)

Reducing the constant current regulation threshold does not modify the maximum programmed output power with a given V_{KP} setting. From the example shown above, setting CC regulation to 2 A (full-scale CC is still 2.5 A), with V_{KP} = 8 V, would result in output profile shown below with CP characteristic intercept of 10 V for the same 20 W constant power characteristic.

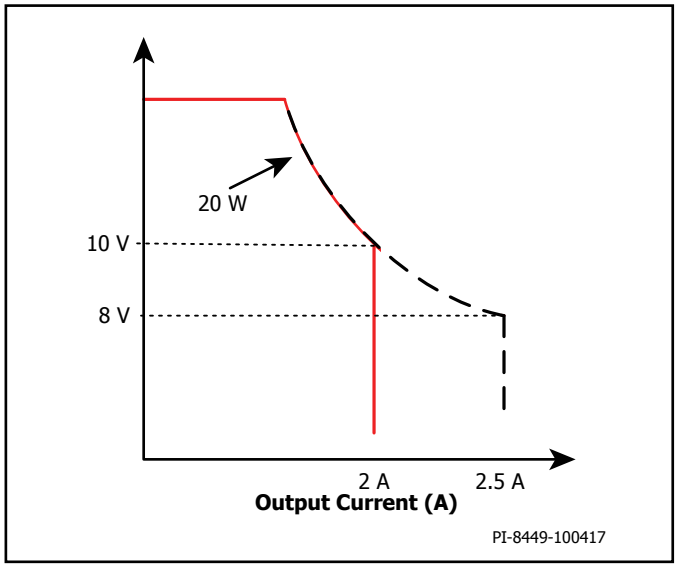


Figure 14. Constant Output Power Profile with Reduced CC Regulation Threshold.

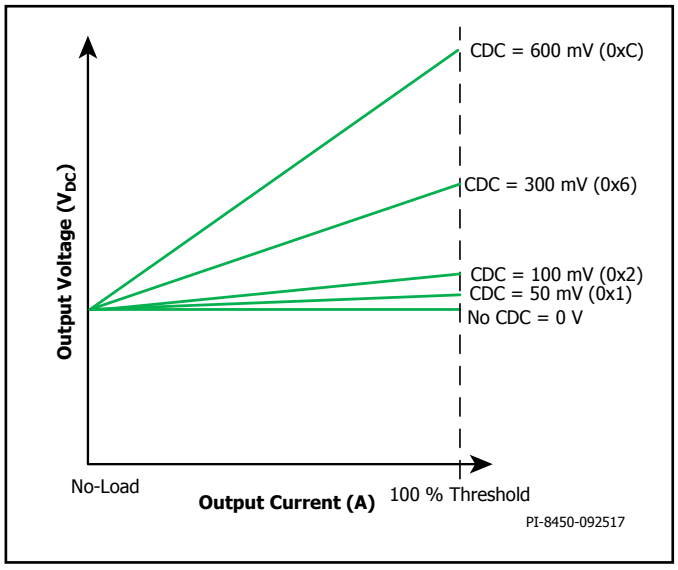


Figure 15. CDC as Function of Load Current.

Cable Drop Compensation (CDC) (0x16)

The amount of cable drop compensation has a controllable range of 0 V to 600 mV in 50 mV/steps. CDC is applied as a function of the current through the sense resistor (resistor between IS and GND pins) used to program the constant current regulation threshold. At no-load there is no CDC and the compensation is increased linearly as load increases and reaches the maximum programmed value at the onset of the 100% constant-current regulation threshold (full-scale voltage across the current sense resistor).

The table below shows the register values to program the desired CDC:

CDC (mV)	Hex Value	Binary
0	0x00	4'b0000
100	0x02	4'b0010
150	0x03	4'b0011
200	0x04	4'b0100
250	0x05	4'b0101
300	0x06	4'b0110
350	0x07	4'b0111
400	0x08	4'b1000
450	0x09	4'b1001
500	0x0A	4'b1010
550	0x0B	4'b1011
600	0x0C	4'b1100

Table 4. Cable Drop Compensation.

If the current sense resistor between IS pin to GND pin is shorted, there will be neither any cable drop compensation nor any constant current regulation.

Example: To change CDC from 0 V to 300 mV (0x06):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b1011 0000)
PI_Command:	CDC Register (0x16)
Byte:	0x06 (4'b0110)

Constant Voltage Only Mode (0x0E)

The InnoSwitch3-Pro can be programmed to operate with constant-voltage only and have no constant current regulation mode. The set output current register (0x98) sets the over-load threshold instead of regulating the constant current when the CVO mode is enabled. Once the load current exceeds the programmed current a peak load timer (t_{PLT}) is started. The options for the peak load timer (CVOL Timer Register 0x2A) are 8/16/32 and 64 ms. If the peak load exceeds the programmable timer, the InnoSwitch3-Pro can be programmed to respond to this fault as auto-restart, latch-off or no-response through the CVOL Register 0xA8. The default response for CVOL (CVO response) is no-response with 8 ms timer.

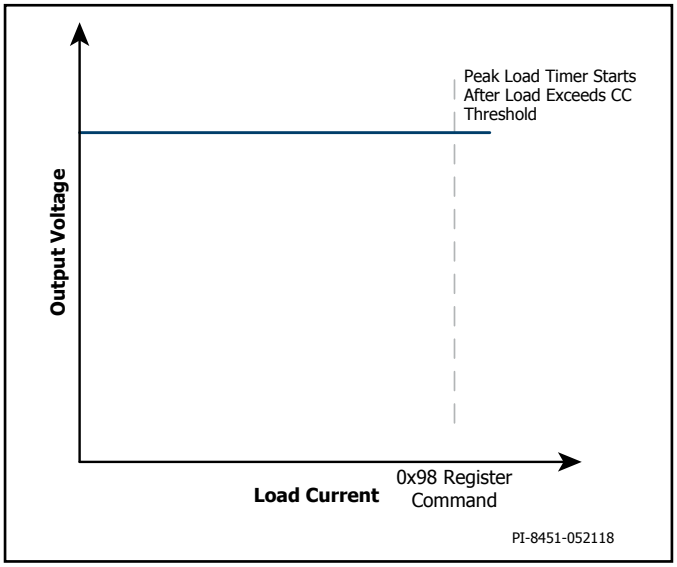


Figure 16. Constant Voltage Only (CVO) Mode.

Example: Enable CVO Mode, set t_{PLT} to 16 msec and fault response to latch-off (LO):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVO Register (0x0E)
Byte:	0x01 (1'b1)
PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVOL Timer Register (0x2A)
Byte:	0x01 (2'b01)
PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVOL Register (0xA8)
Byte:	0x02 (2'b10)

The output undervoltage protection mode discussed in Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior section is still active in the CVO mode of operation even if the individual UV fault response is set to 'No response'. The following control flow-chart shows the expected behavior of the device under the different potential programming scenarios.

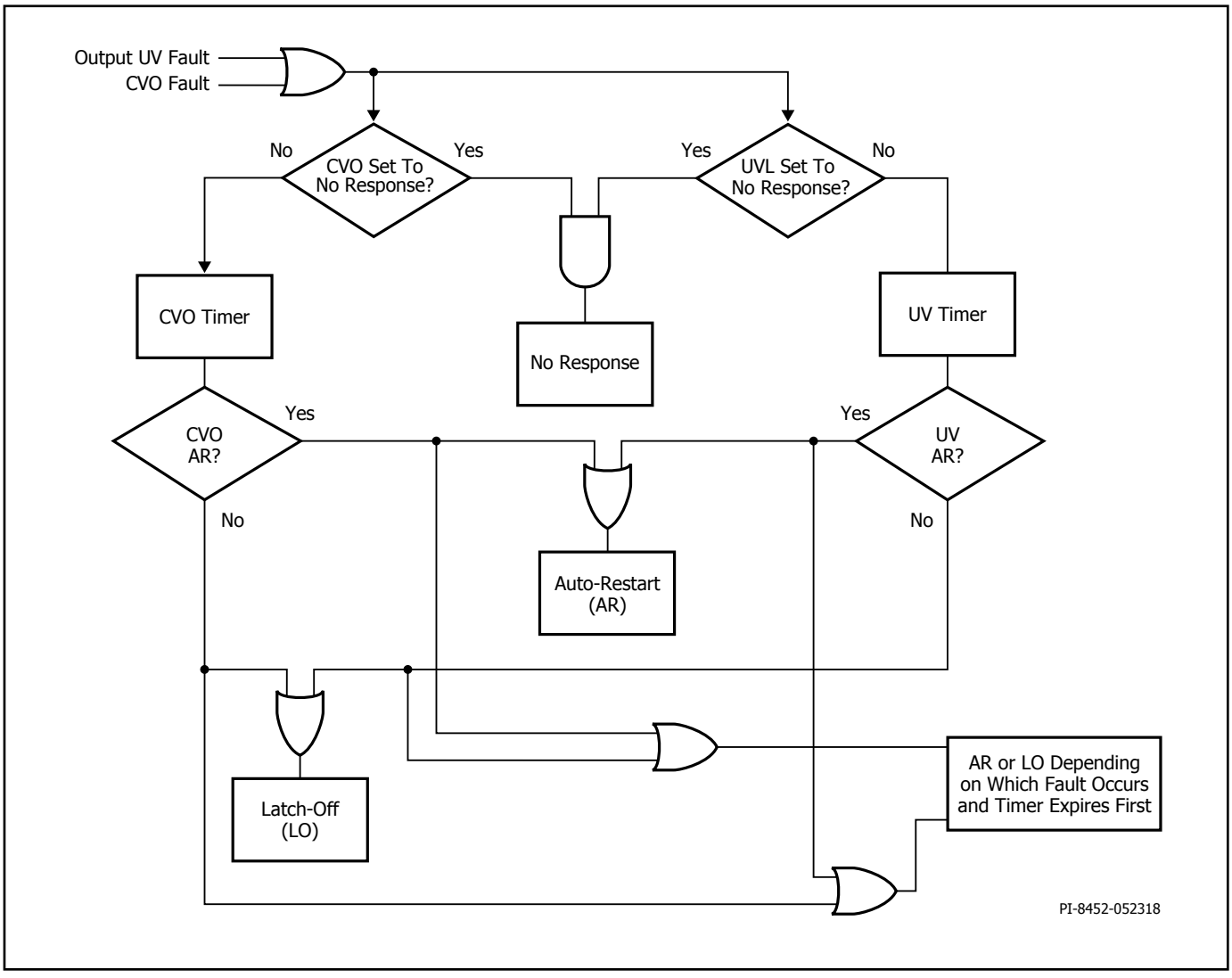


Figure 17. CVO and Output UV Control.

Programmable Protection Mechanisms

Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior

Besides the ability of programing the OV/UV thresholds on the fly as a function of the set CV, the behavior of the power supply once a fault occurs (a. No-Fault which just sets the fault register, b. Auto-restart (AR) or c. Latch-off (LO) the power supply) and timing for the UV fault detection (8 to 64 msec) is programmable as well. The output overvoltage delay is fixed at ~80 µs. All faults that are programmed to have no-fault respose will be logged into the telemetry read-back fault register. Since the minimum UV setting is 3 V, the response should be set to no-response for 3 V operation.

OVA(0x92) : write to this address to specify the overvoltage threshold
UVA(0x94) : write to this address to specify the undervoltage threshold
OVL(0x1C) : write to this address to specify the behavior to OV fault
UVL(0x9E) : write to this address to specify the behavior to UV fault
UVL Timer(0xA4) : write to this register specify the UV timer

Example: To change the absolute output undervoltage threshold 3 V (d'30) (0x809E with odd parity) fault response to latch-off (LO) (0x01) and configure fault timer to 64 msec (0x03):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVA Register (0x94)
Low Byte:	0x9E (8'b1001 1110)
High Byte:	0x80 (8'b1000 0000)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVL Register (0x9E)
Byte:	0x01 (2'b01)

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVL Timer Register (0xA4)
Byte:	0x03 (2'b11)

IS Pin and Output Short-Circuit Fault Protection

The InnoSwitch3-Pro can be configured to monitor whether a short-circuit fault occurs across the output current sense resistor or a short-circuit fault across the IS to GND pins.

A fault is annunciated in the event the IS pin voltage does not exceed approximately 50% of the full constant-current threshold ($IS_{V(TH)}$) with a switching frequency exceeding a programmed threshold. The switching frequency can be selected in a range from 30 to 60 kHz. This must be carefully selected to suit the expected operating conditions of the design.

An IS pin short (ISSC) can be programmed to have a response to be a. No-fault, b. Auto-restart (AR) or c. Latch-off (LO). In the event the behavior is a No-fault, the Telemetry Read-Back Fault Register is logged.

ISSC(0xA2) : write to this address to specify the behavior for an IS-GND short.

Example: To set the behavior of an IS pin short to AR for switching frequency exceeding 40 kHz. (4'b10 10 = 0x10):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	ISSC register (0xA2)
Byte:	0x10 (4'b1010)

The InnoSwitch3-Pro sets the CCSC fault register (READ 10 bit 2) once the voltage across the IS pin resistor exceeds more than ~3 times the $I_{S(VTH)}$. The CCSC register can be programmed to have response of a (a.) No Fault or (b.) Auto-Restart. The default response for this command register is Auto-restart. In applications where the output capacitance after the series bus-switch exceeds 100 µF, the response for CCSC should be set to No-Response for proper start-up and may be programmed back to Auto-restart during normal operation after the series bus-switch is closed.

CCSC (0xA0): write to this address to specify the behavior for an output short-circuit.

Example: Set behavior of output short-circuit to No-response.

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CCSC Register (0x20)
Byte:	0x00 (2'b00)

Note: Setting CCSC register to No-response and creating a short-circuit condition at output will result in Auto-restart.

Watchdog Timer (0x26)

The Watchdog timer supervises the communication on the I²C command lines and has an adjustable time-out. InnoSwitch3-Pro will go into a reset state if I²C commands are not received within the programmable time interval. The watchdog timer does not engage until the master issues the first I²C command (Read or Write). In the reset state the following occurs:

1. VBUS switch is Disabled (Series switch is open).
2. VOUT pin voltage regulates at the default 5 V threshold.
3. All command registers are cleared.

By writing 0x00 into register 0x26, the Watchdog timer is disabled. Disabling this feature can be useful in initial software debugging or checking functionality of the device on the bench.

Example: To disable the Watchdog timer:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Watchdog Timer Register (0x26)
Byte:	0x00 (2'b00)

Opening and Closing the Series VBUS Switch (0x04)

Enabling VBEN (closing the VBUS Series switch) speeds up the ADC sampling frequency in order to achieve high control accuracy. Write commands to CVC register (0x10) and CC register (0x98) cannot be accepted faster than 80 msec when the VBEN is disabled (Series VBUS switch open).

Write 0x03 (with odd parity this becomes 0x8083) into the VBEN register (0x04) to close the series VBUS switch and write 0x00 to this register to open the switch. When the VBUS switch is open (VBEN disabled), the system is reset to the default output voltage set point of 5 V. Disabling the series VBUS switch also resets all the programmable command registers to their default values. The InnoSwitch3-Pro controller is in a state of reset when VBEN is disabled or the VDIS register is enabled. For both these commands, since the controller is in reset, an ACK or Nack at the end of the command should not be expected.

Enabling the VBEN register automatically disables the VDIS register (0x08) described in Active VOUT Pin Bleeder and Output Load Discharge Functions section.

Example: Enabling (Closing) the Series VBUS switch (0x8083):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VBEN Register (0x04)
Byte:	0x83 (8'b1000 0011)

Prior to sending command to open the series bus switch, a command to set the output voltage (CV registor 0x10) to 5 V is recommended. In the event of an auto-restart or latch-off, the bus switch is not disabled.

Turn-Off the Power Supply (0x8A)

The I²C master has the ability to turn-off the power supply (through an I²C command), which will require AC power cycling to restart the power supply.

Example: Turn-off the power supply:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: Turn-Off PSU Register (0x8A)
Byte: 0x01 (1'b1)

Fast VI Command

By default, the maximum speed in which CV (0x10) and CC (0x98) commands can be sent to program output voltage/current respectively is 10 msec. However, the speed limit can be removed by setting 0x1 to the Fast VI Command Register (0x8C).

Example: To disable speed limit for V/I commands:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: Fast VI Speed Register (0x8C)
Byte: 0x01 (1'b1)

Active VOUT Pin Bleeder and Output Load Discharge Functions

There may be circumstances where the VOUT pin strong bleeder function must be activated to discharge the output voltage from a high to low regulation set point.

The VOUT bleeder can be activated by writing 0x01 into BLEEDER Register (0x86).

The BLEEDER register must not be enabled for extended period of time to prevent excessive power dissipation in the controller. When the BLEEDER function is being used to bleed the output voltage from high to low set point, the status of the V_{OUT}10PCT register (bit 4 in the READ10 0x14 read register) should be used to disable the function. The VOUT10PCT register is set once the output voltage is above 10% of the target regulation voltage. The weak Bleeder Enabled Register, READ10 (0X14) bit 5 can be used instead of the VOUT10PCT to determine when the BLEEDER register should be disabled for no-load transients from high to low output voltage transitions.

The InnoSwitch3-Pro automatically activates a weak current bleeder (<5 mA) on the VOUT pin until the output voltage settles within the set regulation threshold.

The InnoSwitch3-Pro can also discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. Load discharge function can be activated by writing 0x03 (0x8083 with odd parity) into VDIS register (0x08).

Enabling the VDIS register will automatically disable the VBEN register (0x04) and reset the device to the default state.

The I^2C master can use telemetry to monitor the VOUT pin voltage or a fixed timer to help determine when to disable both these functions.

Example: Activate the Vout Bleeder:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: BLEEDER Register (0x86)
Byte: 0x01 (1'b1)

Example: Discharge the VBUS Output:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: VDIS Register (0x08)
Byte: 0x83 (8'b1000 0011)

Secondary Over-Temperature Protection (0xAE)

As the secondary controller die temperature increases beyond ~125 °C, the active VOUT pin bleeder function described above will be turned off. The bleeder will not be permitted to be re-enabled until the controller temperature falls below the programmable hysteresis value.

Example: Set Secondary OTP Hysteresis to 60 °C:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: OTP Register (0xAE)
Byte: 0x01 (1'b1)

Transient Response

If faster transient response is required in the application the InnoSwitch3-Pro includes command registers to reduce the time for low to high output voltage transitions. The command register addresses and recommended settings are shown in the table below:

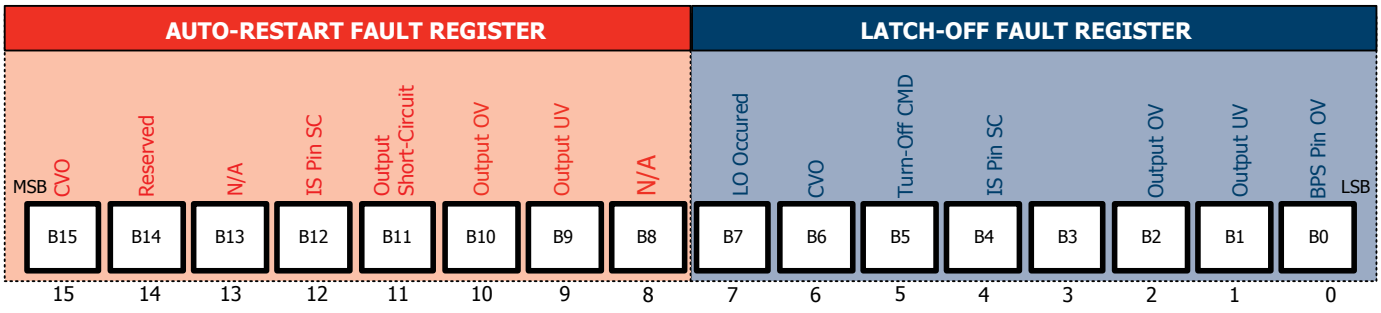
Command Register Address	Default		Recommended for Speed Up	
	MSB	LSB	MSB	LSB
0x32	0x28	0x1E	0x14	0x0A
0x34	0x08	0xC8	0x0F	0x84

Using values other than the default or recommended settings about could lead to oscillatory behavior.

Constant Voltage Load

The constant current regulation mode in the InnoSwitch3-Pro can be optimized for constant voltage (CV) type load if this is required by the end application. Enabling this command register reduces the output current ripple for CV load only. The command register and setting below should only be used if CV load must be supported.

Command Register		Default		Recommended for CV Load	
Address	Address with Odd Parity	MSB	LSB	MSB	LSB
0x30	0xB0		0x20		0x80



PI-8453-101118

Figure 18. READ11 Fault Telemetry Register Assignments.

Telemetry (Read-back) Registers

Telemetry read registers (READ1 to READ6) show the content of all the command registers in Table 2.

Fault Registers

All the command registers including set voltage, set current, constant-power knee voltage, control (Series VBUS switch, VOUT pin Bleeder, Load discharge etc.) and all fault status can be read-back using the Telemetry functionality of the InnoSwitch3-Pro through I²C.

The READ10 telemetry registers are instantaneous and are cleared whenever the condition is no longer valid.

The READ11 (0x16) Register contains fault register data for auto-restart and latch-off. This register is only cleared when the BPS pin falls below its undervoltage threshold or the series VBUS switch is opened.

Example: Read the Fault Telemetry Register to determine an auto-restart occurred due to an output undervoltage (UV) Fault:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
Telemetry Register:	0x16
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)
PI_Slave Response:	Low Byte 8'b0000 0000 (0x00) High Byte 8'b0000 0010 (0x02)

Refer to Figure 11 and Figure 24 that illustrates this read sequence.

Type of Fault	High-Byte	Low-Byte
Auto-Restart: CVO Mode	0x80	0x00
Auto-Restart: IS pin Short-Circuit	0x10	0x00
Auto-Restart: Output Short-Circuit	0x08	0x00
Auto-Restart: Output Voltage OV	0x04	0x00
Auto-Restart: Output Voltage UV	0x02	0x00

Table 5. Summary of Telemetry Fault Codes.

Main Regulation DAC Input

The READ15 telemetry register is the input into the main regulation loop that controls constant voltage, constant current and constant output power regulation. If this register is the same as the Set CV Register (0x10) the converter is operating in constant-voltage mode. If the READ15 is less than the Set CV Register (0x10) the converter is operating in constant-current (CC) or constant-power (CP) mode depending on the value of the Constant Power Knee Voltage Register (0x1A).

The output voltage from the READ15 register is computed as V_{OUT} = 5 V + (MSB × 100 mV) – (LSB x 10 mV).

Example: READ15 (0x5C): MSB = 0x00, LSB = 0x0E
LSB is d'14 so the computed V_{OUT} = 5 – (14 × 10 mV) = 4.86 V

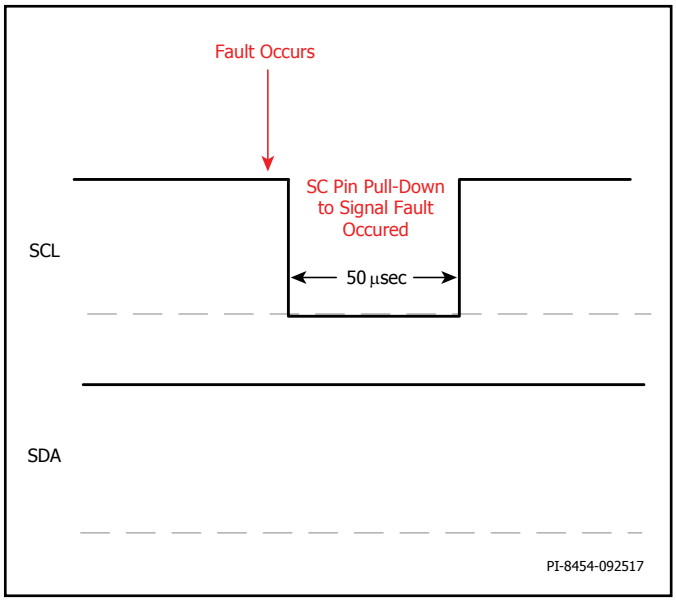


Figure 19. Interrupt Mask During Idle I²C.

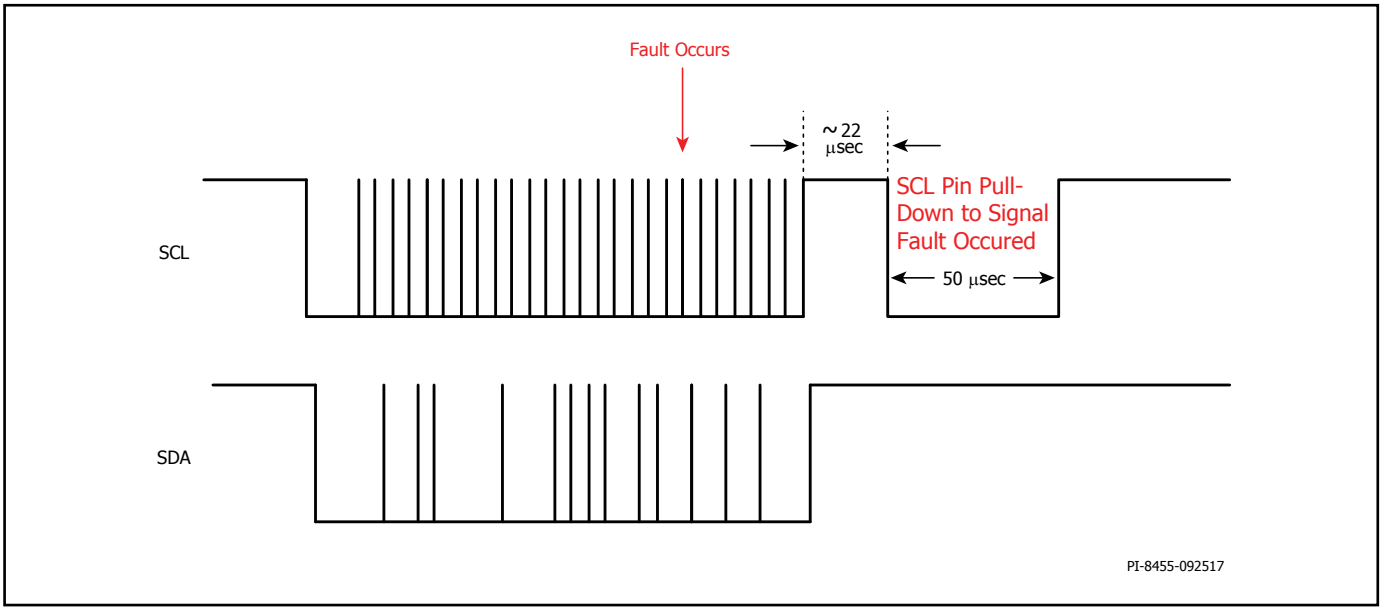


Figure 20. Interrupt Mask During Active I²C Transaction.

Fault Signaling Interrupt Through SCL Pin

In order to improve the fault reporting, an active interrupt reporting scheme is featured on the SCL pin during I²C idle state (when both SDA and SCL pins are pulled high).

When a fault occurs, the SCL pin will behave in one of the following two conditions:

1. When the SCL pin is in idle mode (see Figure 19), the fault interrupt will happen as soon as the fault is detected. The interrupt pulls down the SCL pin for 50 µsec then releases it back to HI State.
2. When the SCL pin is busy (active I²C transaction) (see Figure 20), the fault interrupt will wait for the I²C transaction to be completed, wait ~22 µsec and then pull down the SCL line for 50 µsec (minimum) then releases it back to HI State.

The Interrupt Mask Write Register (0x2C) must be enabled for each of the individual fault conditions shown below in order to activate this feature. Once a fault occurs, the Interrupt Mask is reset and the particular faults of interest must be re-enabled to activate the SCL reporting scheme. The Control Secondary Interrupt (Bit 6) is an indication that the secondary controller is waiting to handshake with primary. Several system faults could trigger this event such as primary-side thermal shutdown or an input line under or overvoltage condition.

Note: Any fault response configured as a "No Response" and Interrupt Mask enabled will result in an interrupt signal on the SCL pin.

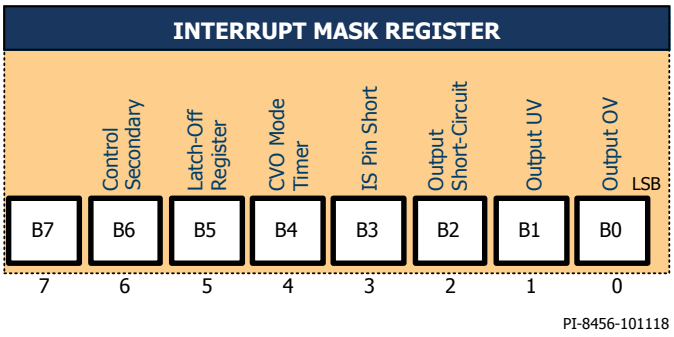


Figure 21. Interrupt Mask Register.

Example: Set the Interrupt Write Register to flag SCL pin fault for output OV, UV or short-circuit only:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	INTM Register (0x2C)
Byte:	0x07 (8'b0000 0111)

Output Voltage Measurement

The voltage on the VOUT pin is available on the Telemetry Register READ 9 (0x12). The tolerance of this telemetry register is ±3% over the entire regulation range of 3 to 24 V.

When the output voltage is below 5 V at loads below ~50 mA, the voltage may fluctuate due to very low switching frequency of the converter but within the specified tolerance. This is normal and expected behavior.

The output voltage report back is in 12-bit format but the resolution depends on the output voltage range as shown in Table 6. This telemetry register is for indication only, in steady-state operation the VOUT pin is very tightly regulated per the CV Write Register (0x10) discussed in CV Register (0x10) section.

The report back resolution step size depending on output voltage is tabulated below:

Output Voltage Range (V)		Resolution Step Size
3	7.2	20 mV
7.2	10	50 mV
10	24	100 mV

Table 6. Output Voltage Report Back Resolution.

If the actual output voltage is 5.11 V (CV Write Register 0x10 set to 0x837F.)

The READ9 register will be at 5.10 V or 5.12 V since the resolution step size is 20 mV in this range

Example: If the READ 9 read-back register value is 0xA801 recalling that low byte precedes the high byte, the proper hex to decimal conversion would be from 0x01A8 = 424 in decimal.

The full output voltage range the report back should be divided by 10 mV to convert into actual output voltage, which in this example results in an output voltage of 4.24 V.

Read-back of the output voltage set-point READ1 (0x02) as with all the read registers is formatted with low-byte preceding the high-byte.

Output Current Measurement

The load output current is also available on the Telemetry Register.

Telemetry Register READ7 (0x0E) contains the measured relative output load current data. The load current is available on a relative basis with respect to the full-scale constant current regulation threshold programmed by the sense resistor tied between the IS and GND pin of the InnoSwitch3-Pro.

The ADC full range is 128, which denotes 100% threshold across the current sense resistor.

The accuracy of the output current read-back is tightest at full scale and decreases as the voltage threshold across the current sense resistor decreases as shown in Figure 22.

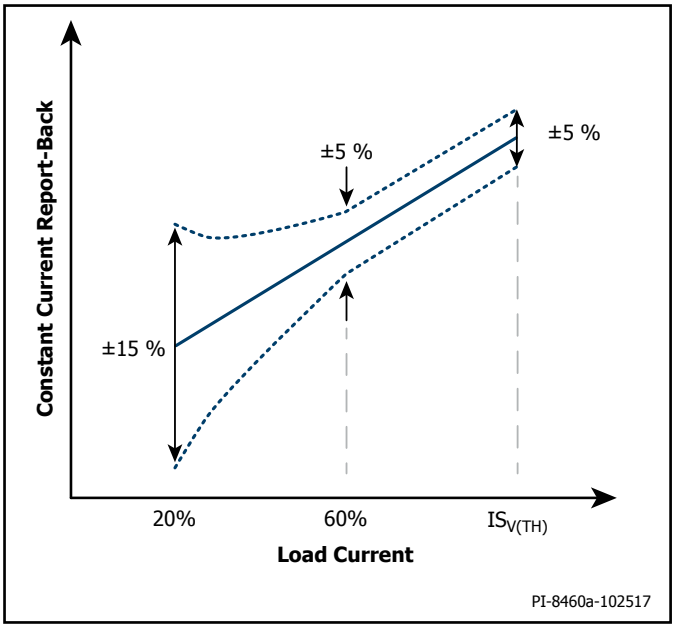


Figure 22. Constant-Current Report Back Tolerance.

Example: If a 16 mΩ sense resistor is used and the read-back register is 0x8040.

Removing the odd parity bit from high byte results in 0x40 = 64 in decimal.

Sensed current value = N (decimal) x 0.25/R_{SENSE}.
64 x 0.25/16 = 1A. This is the measured output current value:

(0.25 mV = 32 mV/128, where 32 mV ($I_{SV(TH)}$) is the full range R_{SENSE} voltage, 128 is the ADC full range).

The READ13 and READ14 are 16 sample rolling averages of the measured output current and output voltage respectively. The value of these average registers is more stable than the instantaneous registers (READ7 and READ9) but take slightly longer to stabilize. When the series BUS switch is opened these registers are cleared and values are reset to zero until the measurement start to accumulate. The resolution of READ 13 and READ 14 is the same as the READ7 and READ 9 respectively.

The output voltage and current measurement registers are updated every 100 µs.

I²C Connection

uVCC External Power Supply

The uVCC pin provides an accurately regulated 3.6 V supply to an external controller. The maximum load current capability of this supply is 45 mA (I_{uVCC})for 0.5 seconds when the VOUT pin is greater than or equal to 5 V. For steady-state operation, it is expected the current drawn from uVCC is less than 10 mA. The uVCC pin should be decoupled to the GND pin with at least a 2.2 µF ceramic capacitor. When the VOUT pin voltage is less than 3.9 V, the internal LDO will droop and follow VOUT pin voltage. Under these conditions, the uVCC pin voltage is dependent on load current and internal series impedance. At VOUT pin = 3 V and 6 mA load current on uVCC, the expected output on uVCC will be ~2.85 V (3 V – 24 Ω x 6 mA).

If the VOUT pin voltage falls sufficiently to cause the uVCC pin to go below the $uVCC_{RST}$ threshold, communication through I²C is no longer available.

SCL/SDA Pull-up Requirements

The SCL and SDA-pins should be pulled-up to the uVCC pin with a resistor. The maximum pull-up resistance is dependent on the capacitance of the SCL/SDA pins and I²C Master. The resultant voltage fall-time to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as function of SCL clock frequency in the table below.

The InnoSwitch3-Pro part can be used with I²C frequency above 535 kHz, however there are specific timing requirements that need to be met as describer in the data sheet parameter table and associated notes below the table. Meeting these requirements at frequencies above 535 kHz may require the interface IC to have the ability to produce asymmetrical I²C CLK signals. If such ability is not available in the interface IC (or micro-controller connected to the InnoSwitch3-Pro through the I²C bus), it is recommended that I²C frequency of 535 kHz or lower is used.

Max Frequency (kHz)	Max Pull-Up Resistance (kΩ)	t_F (ns)
400	13	300
500	10	240
600	8	200
700	7	178

Table 7. I²C Pull-Up Resistor Values.

I²C Example Waveforms

Setting The Output Voltage To 8 V

Same as Example shown in Figure 10.

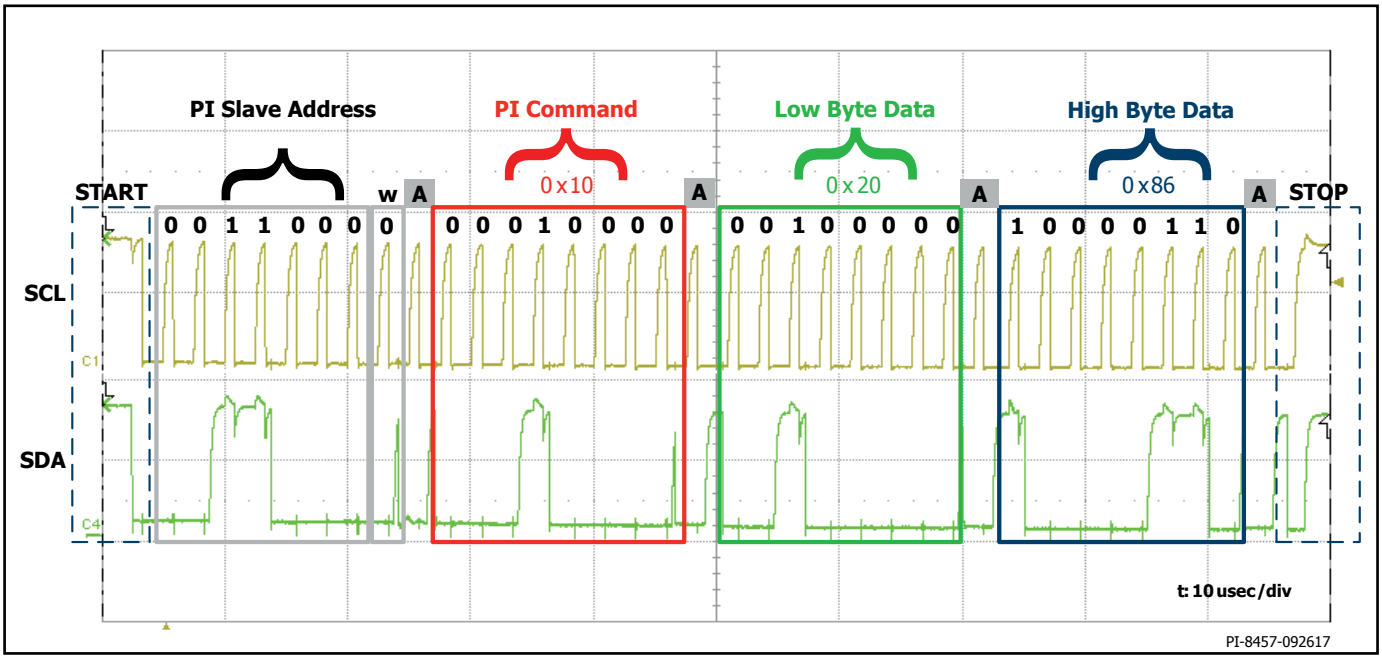


Figure 23. I²C Waveforms for Setting Output Voltage to 8 V.

Reading Telemetry Fault Register After AR Event Caused by Undervoltage

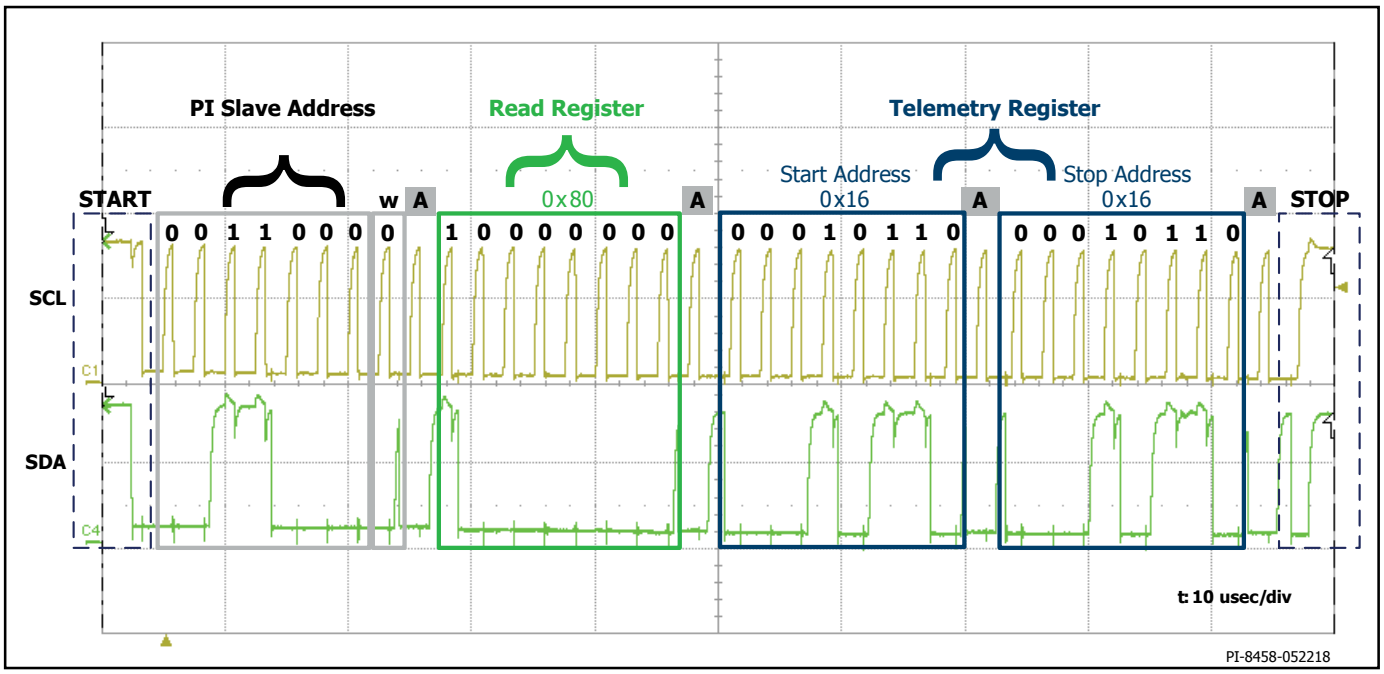


Figure 24. I²C Waveforms for Writing Address of Fault Register READ11 in Read Register (READ0) in Order to Read Back READ11.

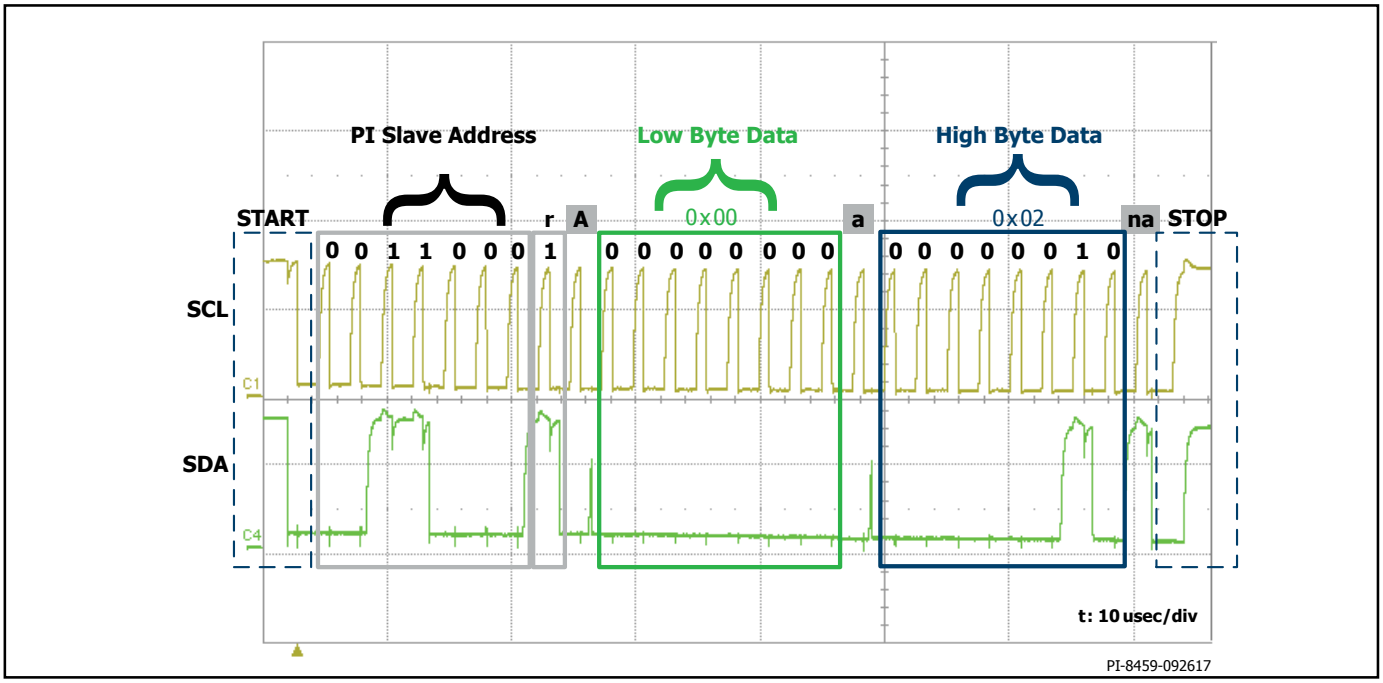


Figure 25. I²C Waveforms for Read Value From READ11 Register.

Applications Example

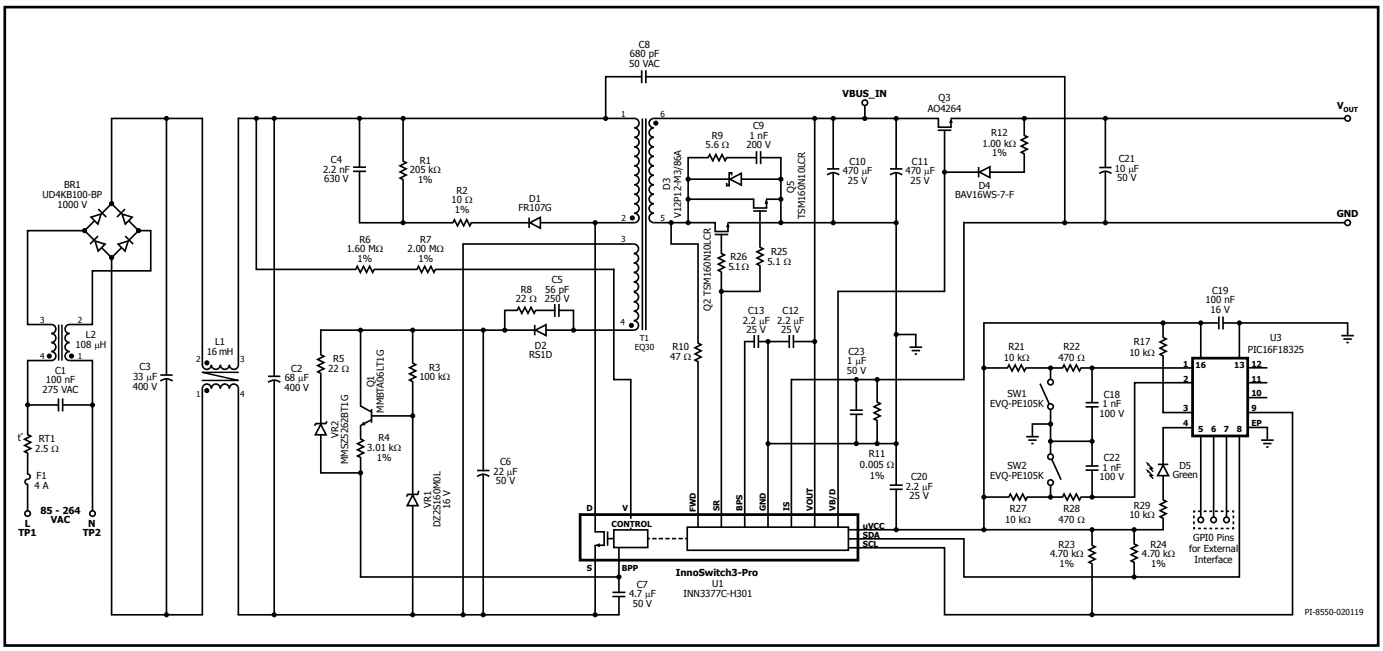


Figure 26. 3 V – 8 V, 5 A; 8 V – 20 V Constant Power 40 W Programmable Power Supply.

The circuit shown in Figure 26 is a 3 V – 8 V, 5 A; 8 V – 20 V constant power 40 W programmable power supply using the INN3377C IC. The power stage is controlled by a general purpose PIC16F18325 microcontroller. This design features DOE Level 6 and EC CoC 5 compliance.

Common mode choke L1 and L2 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection from component failure.

One end of the transformer primary is connected to the rectified DC bus; the other end is connected to the drain terminal of the integrated switch in the InnoSwitch3-Pro IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R1, R2 and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn-off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-Pro IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C7) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistors R3 and R4 along with Q1 and VR1 form a linear regulator circuit to limit the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC (U1) irrespective of the output voltage. The Zener diode VR2 along with resistor R5 provides latching OVP in the event of an output overvoltage condition.

In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2. This causes a current to flow into the PRIMARY BYPASS pin of InnoSwitch3-Pro IC (U1). If the current flowing into the PRIMARY BYPASS pin increases above the I_{SD} threshold, the InnoSwitch3-Pro IC controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and output current sensing along with drive to a FET providing synchronous rectification. The secondary output of the transformer is rectified by FETs Q2, Q5 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI, is reduced via a RC snubber, R9 and C9. Current sharing of the two FETs Q2 and Q5 are obtained by adding the resistors R25 and R26 in series with the gates of the respective FETs.

The gate of Q2 and Q5 are turned on by secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the FET is turned off just prior to the secondary-side requesting the start of a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power FET is turned off when the voltage drop across the FET falls below a threshold of $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switchs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13, connected to SECONDARY BYPASS pin of InnoSwitch3-Pro IC (U1) provides decoupling for the internal circuitry. Capacitor C12 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R10 and an internal

regulator. This allows output current regulation to be maintained down to the minimum auto-restart threshold set by the I²C interface. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R11 between the IS and SECONDARY GROUND pins. A threshold of approximately 32 mV reduces losses. A decoupling capacitor C23 is needed between the IS and SECONDARY GROUND pin to improve CC accuracy. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

When the output current is below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I²C interface.

The PIC microcontroller gets its supply through the μVCC pin of InnoSwitch3-Pro. Switch1 (SW1) increments output voltage while Switch2 (SW2) decrements output voltage. Such a design is used in a system where output voltage is required to be controlled through an external interface.

The PIC microcontroller communicates over its I²C lines to the SDA and SCL pins (which are both 3.3 V and 5 V compatible) of the InnoSwitch3-Pro IC. The SDA and SCL lines need pull-up resistors R24 and R23 respectively to the μVCC pin. The μVCC pin needs a decoupling capacitor C20.

N-chaneel FET Q3 forms the bus switch and is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R12 and diode D4 are needed from the Source of the FET to its gate for providing a voltage discharge path when the bus switch is opened. Capacitor C21 is needed at the output for ESD protection.

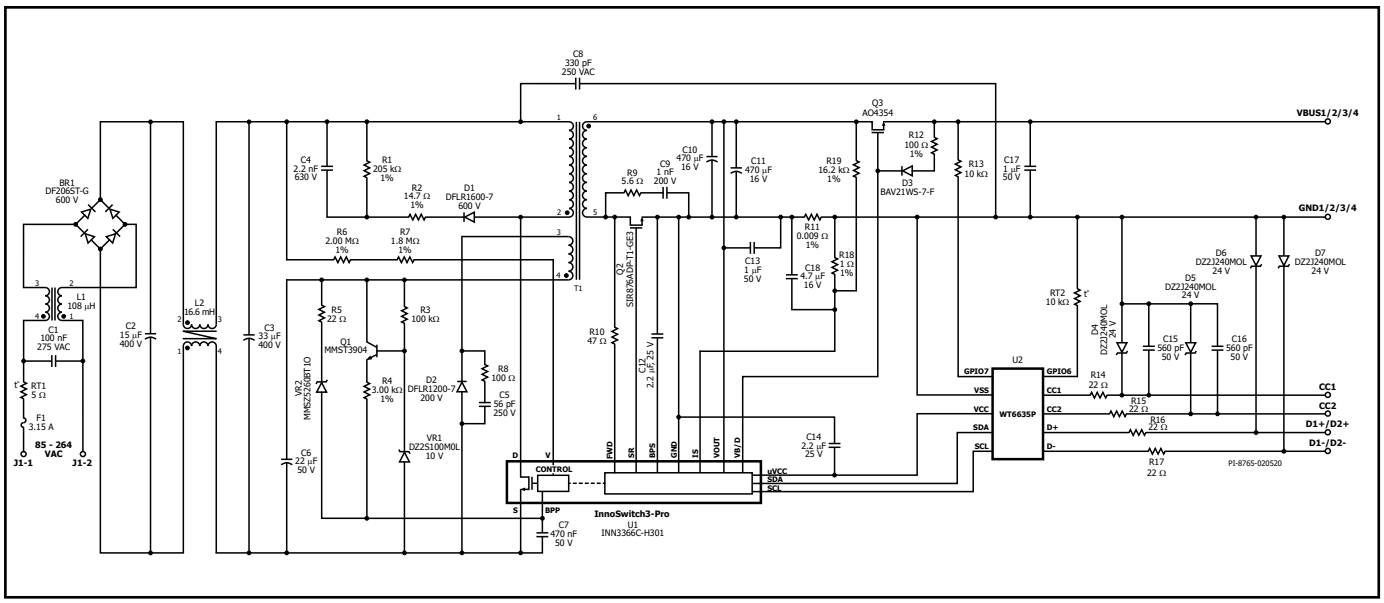


Figure 27. 5 V / 3 A; 9 V / 3 A; 3.3 V – 11 V PPS USB PD 3.0 Compliant Adapter.

The circuit shown in Figure 27 is a 5 V / 3 A; 9 V / 3 A; 3.3 V – 11 V PPS USB PD 3.0 compliant adapter using INN3366C IC. The power stage is controlled by a USB PD Controller. This design features DOE Level 6 and EC CoC 5 compliance.

Common mode choke L1 and L2 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection in case of catastrophic failure by any of the components. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

One end of the transformer primary is connected to the rectified DC bus; the other end is connected to the drain terminal of the integrated switch in the InnoSwitch3-Pro IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R1 and R2 and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn-off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-Pro IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS BPP pin capacitor (C7) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R3 and R4 along with Q1 and VR1 form a linear regulator circuit to limit the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC (U1) irrespective of the output voltage. The Zener VR2 along with resistor R5 provides latching OVP in the event of an output overvoltage condition.

In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2. This causes a current to flow into the PRIMARY BYPASS pin of InnoSwitch3-Pro IC (U1). If the current flowing into the PRIMARY BYPASS pin increases above the I_{SD} threshold, the InnoSwitch3-Pro IC controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and output current sensing along with drive to a FET providing synchronous rectification. The secondary output of the transformer is rectified by FET Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI, is reduced via a RC snubber, R9 and C9.

The gate of Q2 is turned on by secondary-side controller inside U1, based on the winding voltage sensed via resistor R10 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the FET is turned off just prior to the secondary-side requesting the start of a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power FET is turned off when the voltage drop across the FET falls below a threshold of $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switchs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C12, connected to the SECONDARY BYPASS BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry. Capacitor C13 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS decoupling capacitor C12 via resistor R10 and an internal regulator. This allows output current regulation to be maintained

down to the minimum auto-restart threshold set by the I²C interface. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R11 between the IS and SECONDARY GROUND pins. A threshold of approximately 32 mV reduces losses. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

Below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I²C interface.

In this design, (U2) is the USB PD controller. It gets its supply from the uVCC pin of the InnoSwitch3-Pro IC. Output voltage requests are sent by the IC (U2) to InnoSwitch3-Pro through the I²C communication lines (SDA and SCL) when sink requests for the same. The uVCC pin needs a decoupling capacitor C14.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected.

N-channel FETS Q3 and Q4 form the bus switch and make the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. Resistor R12 and diode D3 are needed from the Source of the FET to the gate for providing a voltage discharge path when the bus switch is opened. Capacitor C17 is needed at the output for ESD protection.

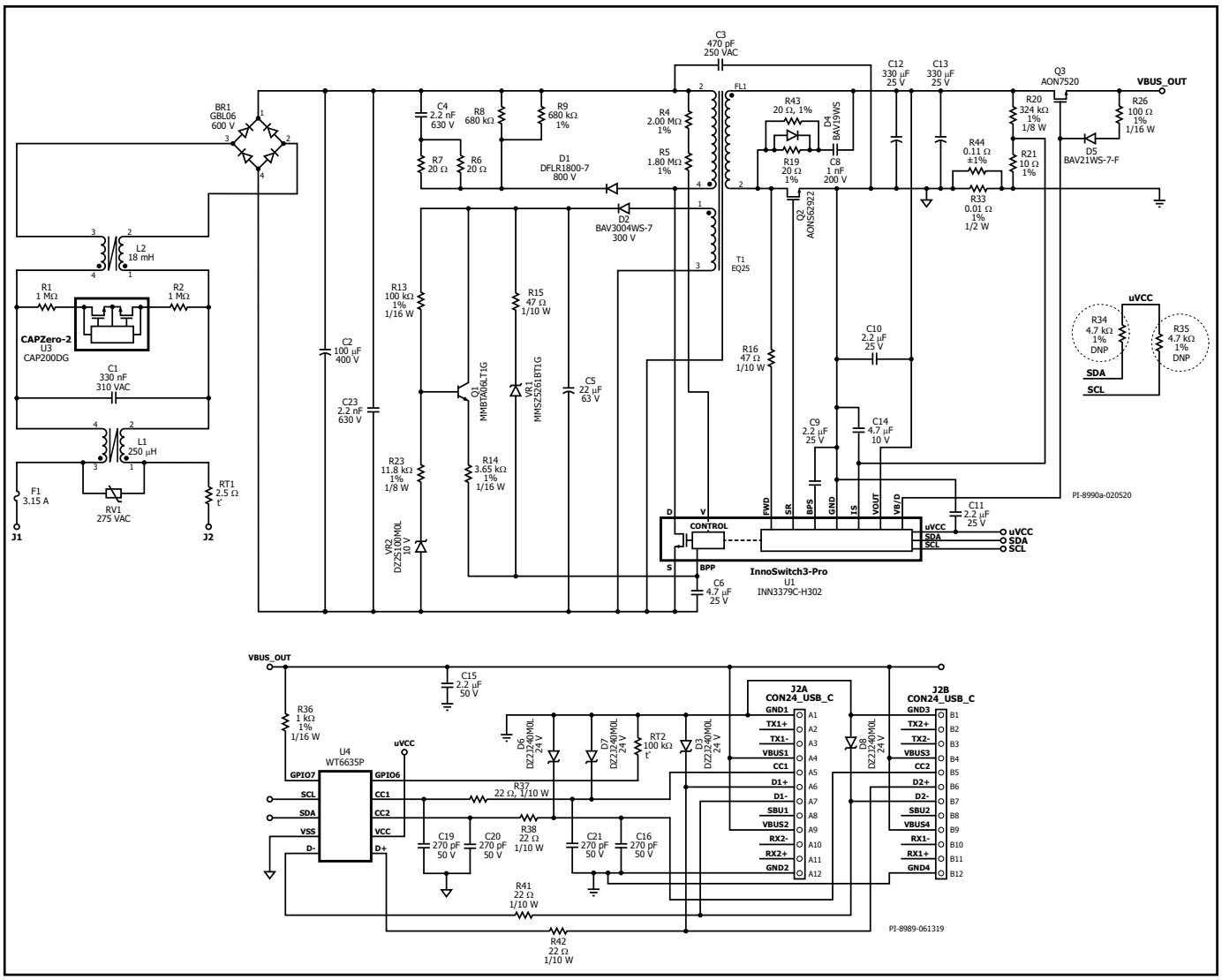


Figure 28. 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A; 3.3 V – 21 V PPS USB PD 3.0 Compliant Adapter.

The circuit shown in Figure 28 is a 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A; 3.3 V – 21 V PPS USB PD 3.0 compliant adapter using INN3379C IC. The power stage is controlled by a USB PD controller. This design features DOE Level 6 and EC CoC 5 compliance.

Fuse F1 isolates the circuit and provides protection from component failure, and thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Varistor RV1 provides safety during high-voltage transients in case of input line surge. Common mode chokes L1 and L2 with capacitors C1, C3, and C23 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across C2. Resistors R1 and R2 along with CAPZero-2 IC U3 discharges capacitor C1 when the power supply is disconnected from AC mains.

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC U1. Resistors R4 and R5 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost RCD clamp formed by diode D1, resistors R6, R7, R8, R9, R10, R11, and capacitor C4 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C6 when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R14 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U1. A linear regulator comprising resistor R13, R23, BJT Q1 and Zener diode VR2 ensures sufficient current flows through R14 such that the internal current source of U1 is not required to charge C6 during normal operation.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes excess current to flow into the

BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R15 limits the current injected to BPP pin.

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side FET (or SR FET) Q2 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber, R19, R43, C8, and D4. The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R16 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R33 and R44. Resistors R20 and R21 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C14 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I²C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary-side controller inside InnoSwitch3-Pro IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C9 via resistor R16 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the I²C interface and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C10 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-FET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. Q3 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R26, and diode D5 are connected across the Source and Gate terminals of the Q3 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitor C15 is needed at the output for ESD protection.

In this design, WT6635P (U4) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the uVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

WT6635P communicates with InnoSwitch3-Pro IC through the I²C interface using the SCL and SDA lines in which it sets the CV, CC, V_{KP}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the WT6635P IC from the telemetry registers also using the I²C interface.

Capacitor C11 provides decoupling to VCC of the WT6635P IC. Capacitors C19, C20, C21, C16, resistors R37, R38, R41, R42, and TVS D3, D6, D7, and D8 provide protection from ESD to pins CC1, CC2, D- and D+.

Thermistor RT2 is connected to pin GPIO6 of the WT6635P IC to provide temperature detection of the USB Type-C receptacle. Resistor R36 is used by the WT6635P IC to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus switch Q3. Resistor R36 is also used for discharging the capacitor C15 through the GPIO converted as sink after the bus switch Q3 is opened.

Key application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage-doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device assumes efficiency >84% and increases to efficiency >89% for the largest device.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (V_{OR}) is set to maintain K_P = 0.8 at minimum input voltage conditions for universal line and K_P = 1 for high input line conditions.
5. Maximum conduction losses for adapter ratings is limited to 0.6 W and 0.8 W for open frame.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink is used to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.

Primary-Side Overvoltage Protection
The primary-side output overvoltage protection provided by the InnoSwitch3-Pro IC triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5x or 2x the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current charging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during any output overvoltage.

Reducing No-Load Consumption
The InnoSwitch3-Pro IC can start in self-powered mode from the PRIMARY BYPASS pin capacitor charged through the internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-Pro IC has become operational. Auxiliary or bias winding provided on the transformer is required for this purpose. The addition of a bias winding that provides bias supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption down to <30 mW. Resistor R4 shown in Figure 26 should be adjusted to achieve current into BPP that is just slightly over I_{S1} which is also the condition when no-load power is the lowest.

If there is an external controller used to issue commands to InnoSwitch3-Pro then the controller should be put in sleep mode in order to reduce the power consumption and none of the GPIO pins should be put in a state that will result in additional power consumption.

Secondary-Side Overvoltage Protection (Auto-Restart Mode)
The secondary-side output overvoltage protection provided by the InnoSwitch3-Pro IC uses an internal auto-restart circuit that is triggered by a threshold current of ISD into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between the 1.25 times output voltage and 4.4 V SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor, R2 shown in series with the OVP Zener diode to limit the maximum current into SECONDARY BYPASS pin. The secondary-side OVP function is disabled during soft-start.

Under some conditions, the secondary OVP may take several switching cycles to initiate.

Selection of Components

Components for InnoSwitch3-Pro IC Primary-Side Circuit

BPP Capacitor
Capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC provides decoupling for the primary-side controller and also selects current limit. A 0.47 μF or 4.7 μF capacitor may be used as indicated in InnoSwitch3-Pro IC data sheet. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for design of compact switching power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit
The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin.

Turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest (or no-load) load condition. If the voltage is lower than this, the no-load input power will increase. Generally, in USB PD or rapid charge applications, the output voltage range is very wide. For example, a 45 W adapter would need to support 5 V, 9 V and 15 V whereas a 100 W adapter would have output voltages selectable from 5 V to 20 V. Such a wide output voltage variation results in a large change in bias winding output voltage as well. As shown in Figure 26, a linear regulator circuit is generally required to limit the current injected into the PRIMARY BYPASS pin of the InnoSwitch3-Pro IC.

The bias current from the external circuit should be set to $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at 230 VAC input voltage, (V_{BPP} > 5 V).

A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to prevent the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 μF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and rated load with the lowest input AC supply voltage. It is recommended to ground the bias winding capacitor to the negative of the input bulk capacitor than the SOURCE pin.

Line UV and OV Protection

Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage to provide line under-voltage and overvoltage protection. For a typical universal input application, a resistor value of approximately 3.8 MΩ is recommended. Figure 29 shows circuit configurations that enable selectively either the line UV or the line OV feature, disabling the other.

The InnoSwitch3-Pro IC features a primary sensed OV protection feature that can be used to latch-off/AR the power supply. Once the power supply is in latch-off/AR, it can be reset if the UNDER/OVER INPUT VOLTAGE pin current is reduced to zero. Once the power supply is latched off, even after input supply is turned off, it can take considerable amount of time to reset InnoSwitch3-Pro IC controller as the energy stored in the DC bus will continue to provide bias supply to the controller. In case of latch-off, a fast AC reset can be achieved using the modified circuit configuration shown in Figure 30. The voltage across capacitor CS reduces rapidly after input supply is disconnected reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch3-Pro IC and resetting the InnoSwitch3-Pro IC controller.

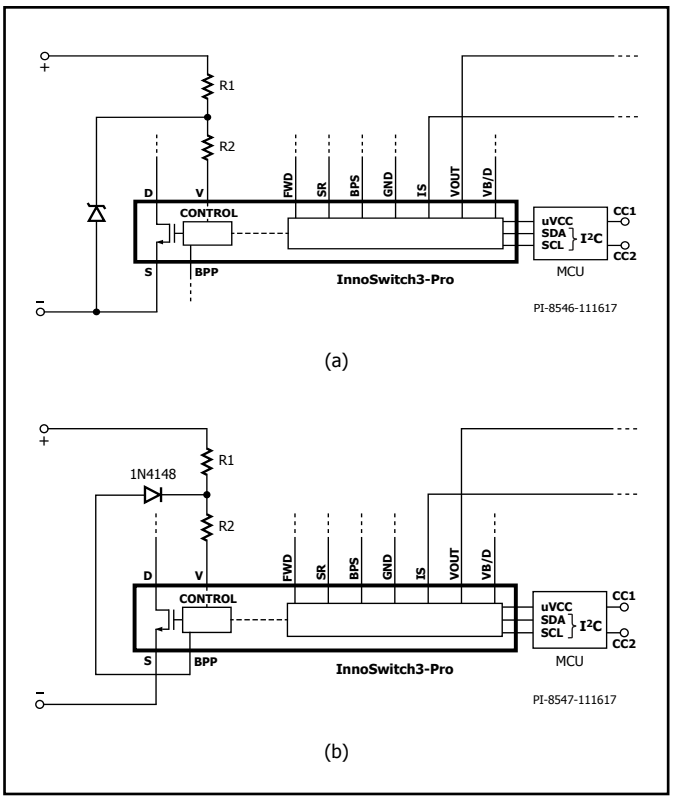


Figure 29. (a) Line UV Only; (b) Line OV Only.

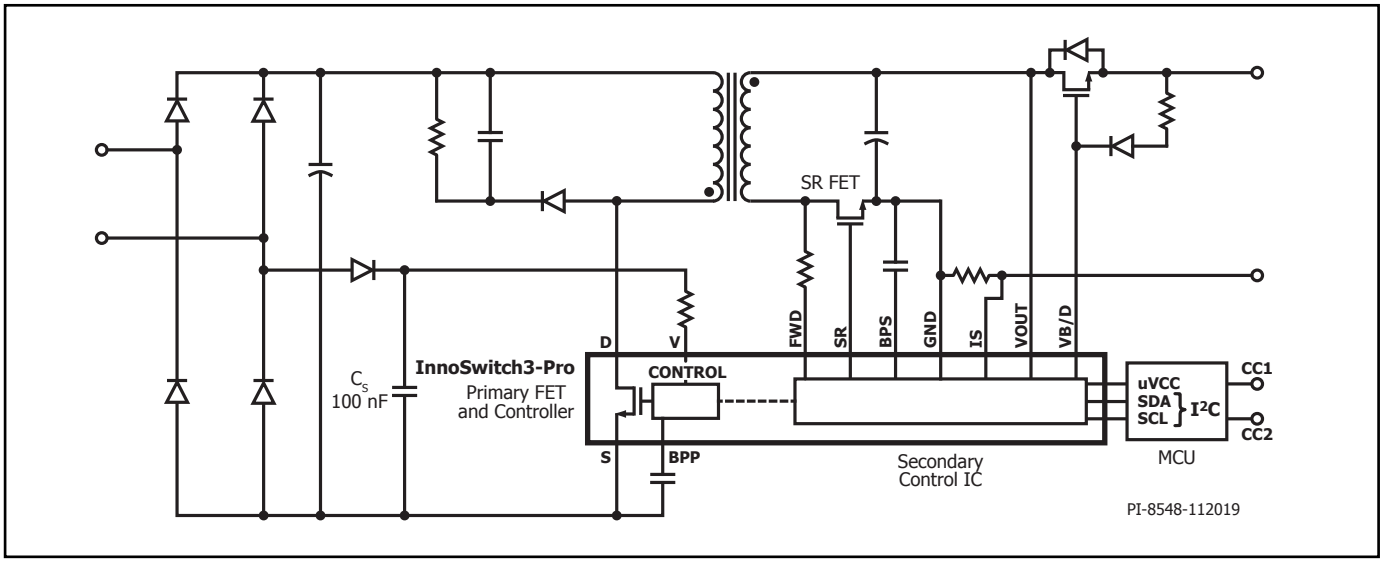


Figure 30. Fast AC Reset Configuration.

Primary Sensed OVP (Overvoltage Protection)
The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonably accurate detection of the amplitude of the output voltage can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and causes the primary-side controller to latch-off/AR. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions (at full rated load and lowest rated input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will not trigger under any normal operating conditions but will only operate in case of a fault condition.

Primary-Side Snubber Clamp
A snubber circuit should be used on the primary-side as shown in the example circuit in Figure 26. This prevents excess voltage spikes at the Drain of the switch at the instant of turn-off of the switch during each switching cycle. Though conventional RCD clamps can be used, RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 26 uses RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recover glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch3-PRO

Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor
A 2.2 μF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-Pro IC. Since the SECONDARY BYPASS pin voltage needs to be 4.4 V before the output voltage reaches to the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. The values lower than 1.5 μF may not offer enough capacitance, which can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

When the output voltage of the power supply is 5 V or higher, the supply current for the secondary-side controller is supplied by the OUTPUT VOLTAGE (VOUT) pin of the IC as the voltage at this pin is higher than the SECONDARY BYPASS pin voltage. During start-up and operating conditions where the output voltage of the power supply is below 5 V, the secondary-side controller is supplied current from an internal current source connected to the FORWARD pin. If the output voltage of the power supply is below 5 V and the load at the output of the power supply is very light, the operating frequency can drop considerably and the current supplied to the secondary-side controller from the FORWARD pin may not be sufficient to maintain the SECONDARY BYPASS pin voltage at 4.4 V. For such applications, InnoSwitch3-Pro IC has an internal charge pump to regulate the voltage of the SECONDARY BYPASS pin at 4.4 V.

FORWARD Pin Resistor
A 47 Ω 5% resistor is recommended to ensure sufficient IC supply current. A lower resistor value should not be used as it can affect device operation such as the synchronous rectifier drive timing. In some cases a higher value should be used if pulse grouping is observed. However this number should not exceed 150 Ω.

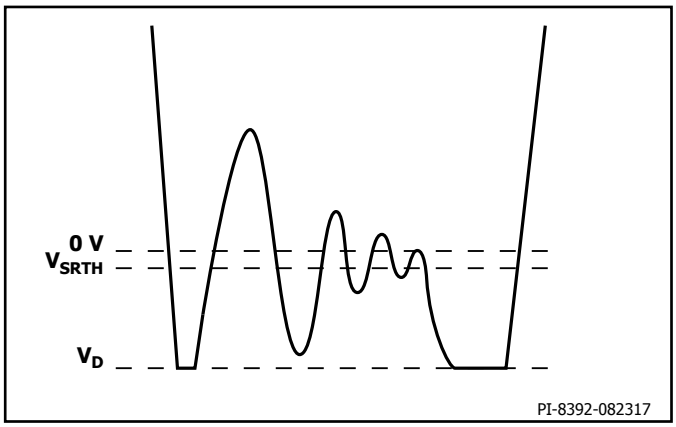


Figure 31. Unacceptable FORWARD Pin Waveform After Handshake With SR FET Conduction During Flyback Cycle.

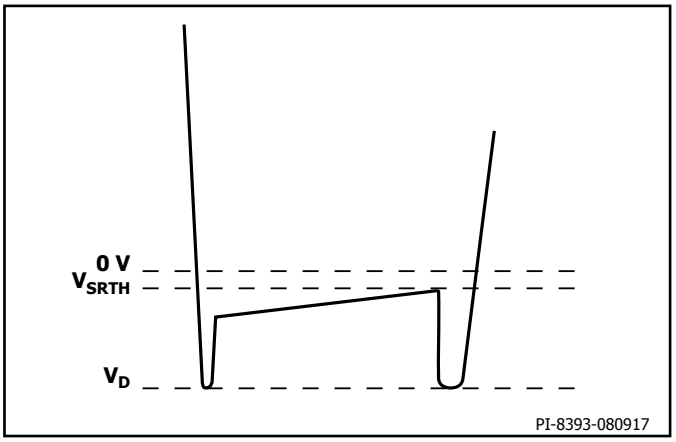


Figure 32. Acceptable FORWARD Pin Waveform After Handshake With SR FET Conduction During Flyback Cycle.

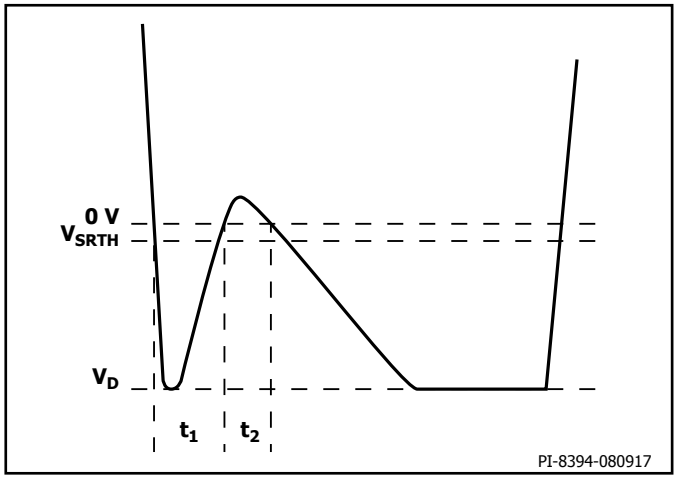


Figure 33. Unacceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/AR.

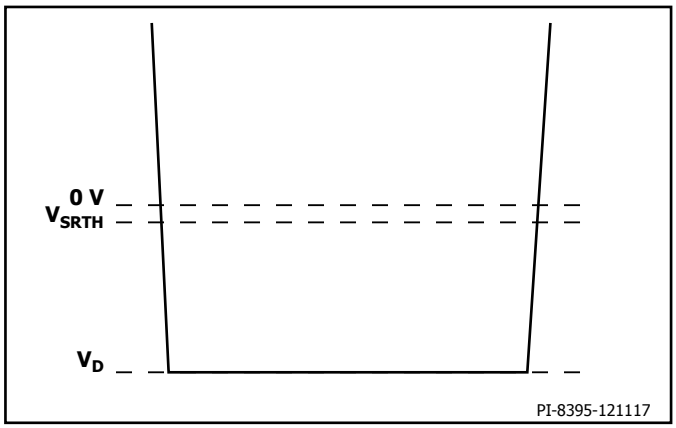


Figure 34. Acceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

SR FET Operation and Selection

Although a simple diode rectifier and filter works for the output, use of a SR FET enables significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-Pro IC (with no additional resistors connected to the gate circuit of the SR FET if a single SR FET is used). The SR FET is turned off once the Drain voltage of the SR FET drops below 0 V.

A FET with 18 mΩ $R_{DS(ON)}$ is good for 5 V, 2 A output, and a FET with 8 mΩ $R_{DS(ON)}$ is suitable for designs rated for 12 V, 3 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with too high a threshold voltage is therefore not suitable, and FETs with a low threshold voltage of 1.5 V to 2.5 V are ideal although FETs with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets clearly specify $R_{DS(ON)}$ over-temperature range for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-Pro IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ drops below $V_{SR(TH)}$, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. A Schottky diode parallel to the SR FET may be added to provide higher efficiency and typically a 1 A surface mount Schottky diode is often adequate. However, the gains are modest; for a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.3 to 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} < 60 V, and 100 V rated FETs and diodes are suitable for 12 V design.

The interaction between the leakage reactance of the secondary and the SR FET capacitance (COSS) leads to ringing on the voltage waveforms at the instance of voltage reversal at the winding due to the primary switch turn-on. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (a higher resistance value leads to noticeable drop in efficiency). A capacitance of 1 nF to 2.2 nF is adequate for most designs.

In designs where the SR FET drain waveform is not as shown in Figure 31 during voltage transitions, and looks similar to Figure 30 it is recommended that voltage transitions be made in small increments of 200 mV.

Output Capacitor
Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable design of ultra-compact chargers and adapters. Typically, 200 µF to 300 µF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Care should be taken to ensure that capacitors have a voltage rating higher than the highest output voltage with sufficient margin (>20%).

Output Overload Protection
The maximum power which can be delivered by the power supply is obtained by the product of the programmed V_{KP} and the full scale current limit. For output voltage below the programmed V_{KP} threshold, the InnoSwitch3-Pro IC will limit the output current once the programmed current limit is reached (if it is less than the full scale current limit) or voltage across the IS and GND pins exceeds the $I_{SV(TH)}$ threshold and provides current limited or constant current operation. The full scale current limit is set by the resistor between the IS and GND pins. A lower value of current limit can be programmed over I²C. For any output voltage above the programmed V_{KP} threshold, InnoSwitch3-Pro IC will provide a constant power characteristic. An increase in load current within the programmed current limit will result in a drop in output voltage such that the product of output voltage and current equals the maximum power set by the product of V_{KP} and set current limit.

Decoupling Capacitor at µVCC Pin
It is recommended that at least a 2.2 µF ceramic capacitor be placed between the uVCC and GND pins.

Pull-Up Resistors for SDA and SCL Pins
A 4.7 kΩ pull-up resistor from each of the SDA and SCL pin to the uVCC pin is recommended for communication at a frequency of 400 kHz. Maximum value of the pull-up resistor is dependent on the capacitance presented by the SDA/SCL lines and the I²C master. The resultant voltage rise to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as a function of SCL clock frequency in Table 7.

Decoupling Capacitor at V_O Pin
It is recommended that a 1-2.2 µF ceramic capacitor be placed close to the V_O pin.

IS to GND Pin Current Sense Resistor
This sense resistor is chosen such that the required full scale current produces a 32 mV drop across IS and GND pins. A 1% or lower tolerance resistor is recommended. This sense resistor needs to be placed as close to the InnoSwitch3-Pro IC pins as possible for accurate current measurement and CC regulation.

Output Decoupling Capacitor
A ceramic output decoupling capacitor up to 10 µF is required to pass 18 kV ESD air discharge.

Bus Switch
A low $R_{DS(ON)}$ N-channel FET bus switch is recommended to reduce impact of efficiency at high load currents. The FET need not be a logic level FET. It should be sufficiently enhanced at a gate threshold of 4 V.

Bus Discharge
The resistor value for bus discharge is chosen as per the discharge time requirements for high-voltage to low-voltage transitions. A 100 Ω resistor value is recommended to meet the USB PD discharge time specification. A general purpose diode in series is recommended for unidirectional current flow.

External Controller
An external controller is needed to send the I²C commands to the InnoSwitch3-Pro IC over the SDA and SCL lines. For standalone applications, the external controller can get its supply from the uVCC pin of the InnoSwitch3-Pro IC. It should be able to sustain operation for a supply voltage as low as 2.8 V.

Recommendations for Circuit Board Layout

See Figure 35 for a recommended circuit board layout for a switching power supply using InnoSwitch3-Pro IC.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

IS to GND Pin Capacitor
A 1 µF or higher ceramic capacitor is recommended to be used between the IS and GND pins of the InnoSwitch3-Pro IC for accurate constant current regulation.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area should be maximized for good heat sinking. Similarly for output SR FET, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR FET.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to

keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage. Further de-rating can be applied depending on any additional specific requirements.

Y Capacitor

The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. Such a placement will route high amplitude common mode surge currents away from the IC. Note – if an input π (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR FET

For best performance, the area of the loop connecting the secondary winding, the output SR FET and the output filter capacitor, should be minimized. The Source pin connection of the SR FET should be connected to the output capacitor negative terminal and the GND pin of the InnoSwitch3-Pro IC in a short connection to reduce the trace impedance drop as this is critical for FWD pin sensing wrt IC GND pin in order to turn OFF the SR FET during Discontinuous mode of operation. The connection between the Drain of the SR FET and the FWD pin resistor should also be made short. In addition, sufficient copper area should be provided at the terminals of the SR FET for heat sinking.

IS-GND Pin, Sense Resistor Traces

It is recommended to have the traces from the current sense resistor to the IS-GND pins to be in a star connection at the respective two nodes of the current sense resistor in order to have an accurate CC set-point. The IS-GND sense traces should be at the innermost of the solder pads of the current sense resistor to avoid measuring any drop across the solder pads of the resistor or the load traces coming in and out of the sense resistor.

uVCC, SDA and SCL Pins

The traces to SDA and SCL pins should be kept away from any noise node or trace. If possible a shield trace should be made in parallel to the SDA and SCL traces.

ESD

Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / hi-pot requirements.

The spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration a 6.4 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input. To further improve ESD performance, spark gaps can be added under common mode chokes.

If there is a controller used for USB PD communication then the Ground of the controller should be connected to the GND pin of the InnoSwitch3-Pro IC and not the GND pin of the type C connector, this helps for ESD performance. However, if there is a separate daughter board connected with the controller IC on it and the Ground path becomes long then the Ground of the controller IC can be connected closer to the USB connector GND pins to help in the eye diagram during USB PD compliance tests.

Drain Node

The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and associated circuit trace lengths should be minimized.

The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example

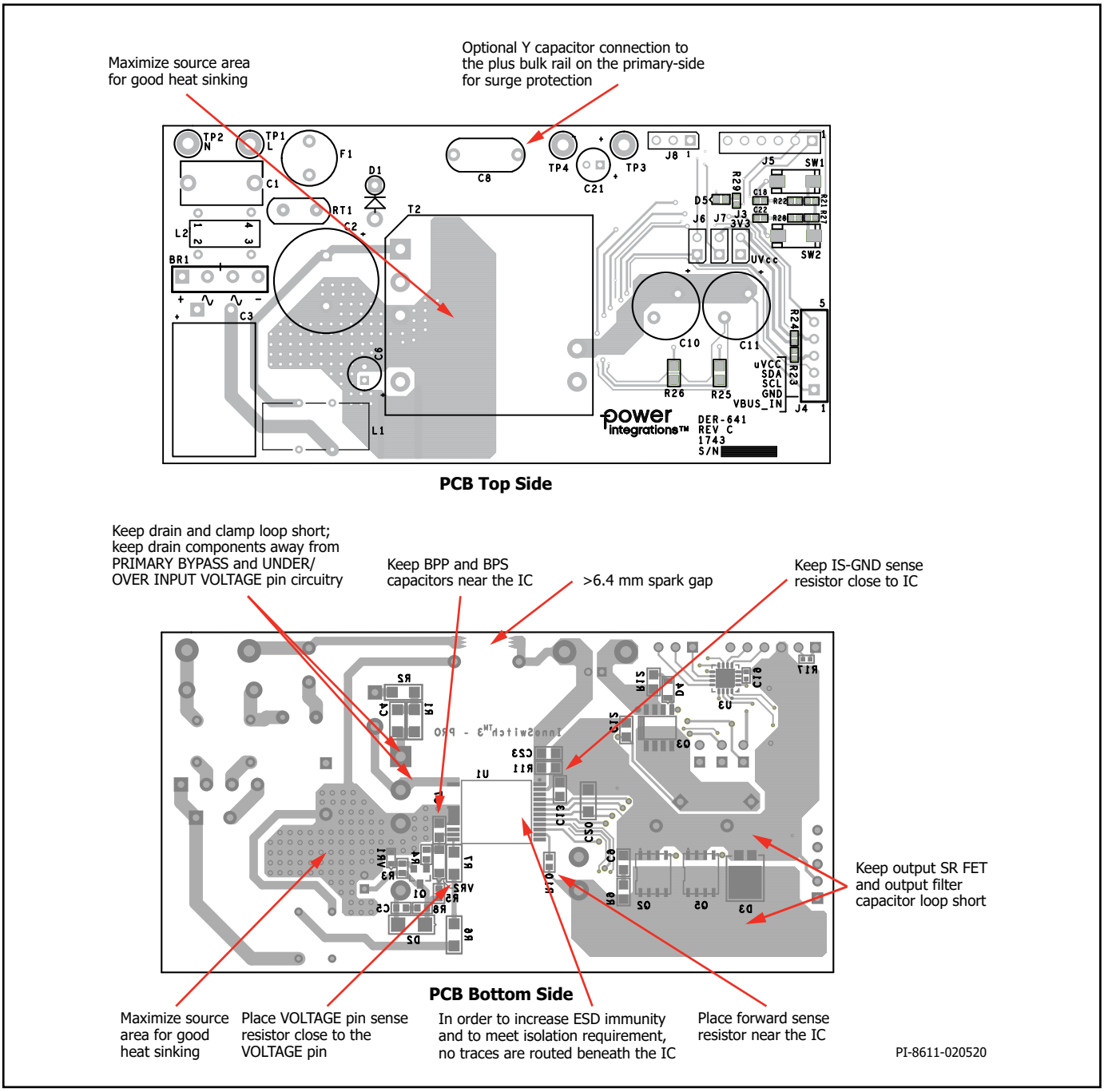


Figure 35. PCB Layout Recommendation.

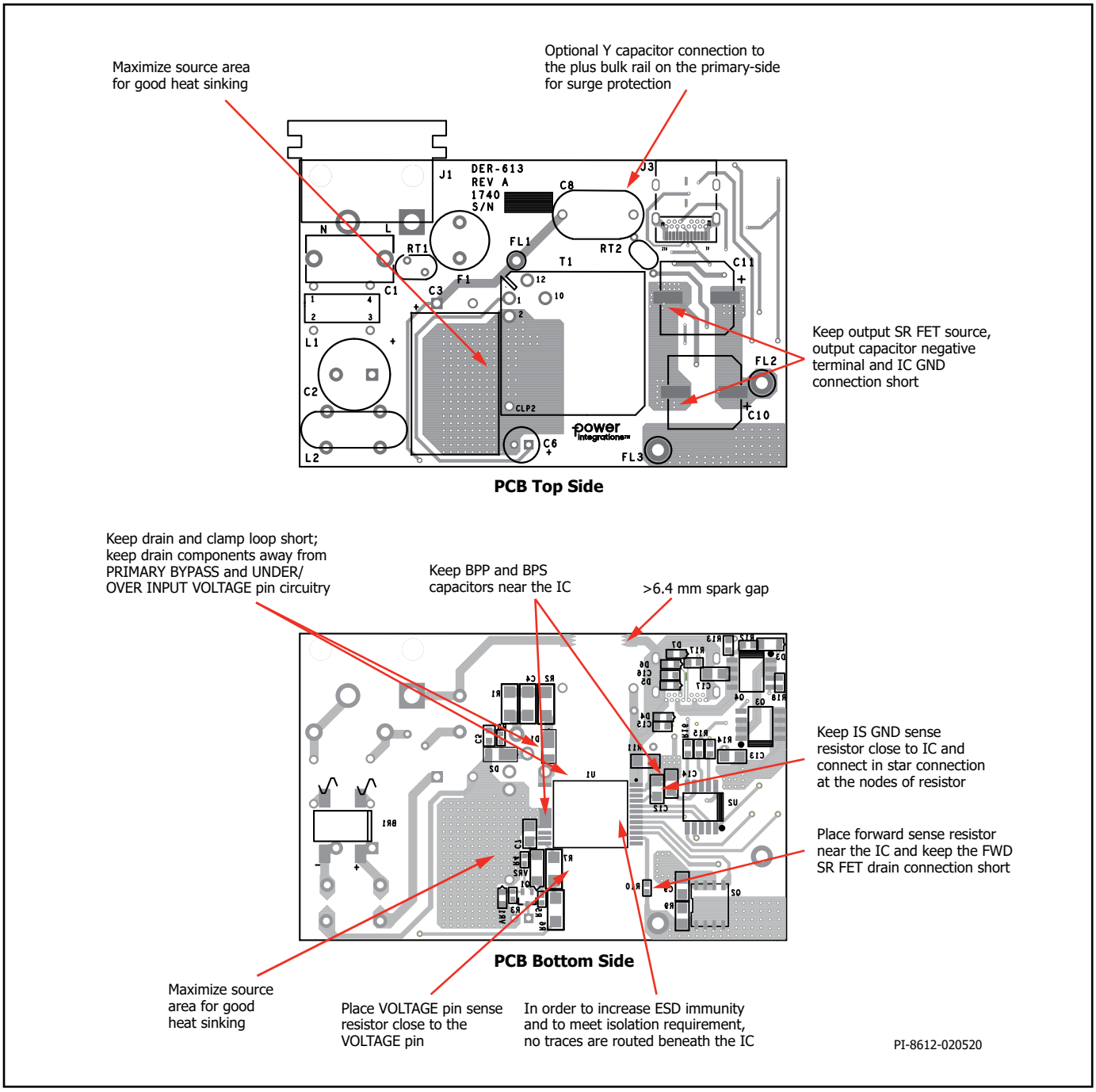


Figure 36. PCB Layout Recommendation.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area and keeping the switching nodes/traces away from the quiet nodes/traces.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduced radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. The same can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to achieve improved conducted and radiated EMI margins.
5. Values of components of the RC snubber connected across the output SR FET can help reduce high frequency radiated and conducted EMI.
6. A π filter comprising of differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 μF or higher ceramic capacitor when connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply is able to deliver the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus of the power supply depends on the capacitance of the filter capacitor used. At least 2 µF / W is recommended to keep the DC bus voltage always above 70 V, though 3 µF / W provides sufficient margin. The ripple on the DC bus should be measured and care should be taken to verify this voltage to confirm the design calculations for transformer primary-winding inductance selection.

Switching Frequency (F_{SW})

It is a unique feature in InnoSwitch3-Pro ICs that a designer can set the switching frequency at full load between 25 kHz to 95 kHz depending on the design specification. To have lower device temperature, the switching frequency can be set to around 60 kHz. To have smaller size transformer, the switching frequency needs to be set to a value closer to a maximum of 95 kHz. When setting the full load switching frequency, it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection. The following table provides a guide for frequency selection based on the device size. This represents the best compromise between the overall device losses (conduction and switching losses) based on size of the internal high-voltage switch.

INN3365C / INN3375C	80 kHz
INN3366C / INN3376C	75 kHz
INN3377C	70 kHz
INN3367C / INN3368C	65 kHz
PowiGaN device INN3378C	70 kHz
PowiGaN device INN3379C	65 kHz
PowiGaN device INN3370C	60 kHz

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary switch Drain voltage of the secondary-winding voltage during the diode / SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of QR capability and ensure flattest efficiency over line / load, it is better to set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage conditions for universal line input and K_P = 1 for high-line input only conditions.

The following should be kept in mind for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-Pro device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance that reduces efficiency of the power supply.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents where the V_{OR} should be reduced to get highest efficiency, and higher output voltages above 15 V, V_{OR} should be higher to maintain a reasonable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, K_P

A K_P below 1, indicates continuous conduction mode, K_P is the ratio of ripple-current to peak-primary-current (Figure 38).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode. In this case, K_P is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T / t = V_{OR} \times (1 - D_{MAX}) / (V_{MIN} - V_{DS}) \times D_{MAX}$$

It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-Pro IC designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-Pro IC temperature. The benefits of quasi-resonant switching start to diminish for a further reduction in K_P.

For typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. PIXls spreadsheet from Power Integrations can be used to effectively optimize selection of K_P, inductance of the primary winding, turns ratio of the transformer and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of suitable core is dependent on the physical design constraints of the power supply enclosure. It is recommended that only cores with low loss be used as power supply designs are often thermally challenged due to the small enclosure requirement.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs, a total margin of 6.2 mm is typically required, and a value of 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical. However if a total margin of 6.2 mm is required then the physical margin can be placed only on one side of the bobbin. For designs using triple insulated wire it may still be necessary to use a small margin in order to meet the required safety creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required. As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. It is recommended that for compact power supply designs using an InnoSwitch3-Pro IC, triple insulated wire should be used for secondary which then eliminates need for margins.

Primary Layers, L

Primary layers should be in the range of 1 < L < 3 and in general it should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs though higher values may be required based on thermal design constraints. Designs with more than 3 layers are possible but the increased leakage inductance and physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance

is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)

A maximum value of 3800 gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density under start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-Pro IC provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

Transformer Primary Inductance, (LP)

Once the lowest operating input voltage, switching frequency at full load, and the required V_{OR} are determined, transformer primary inductance can be calculated. The PIXls design spreadsheet which is part of the free PI Expert suite can be used to assist in designing the transformer.

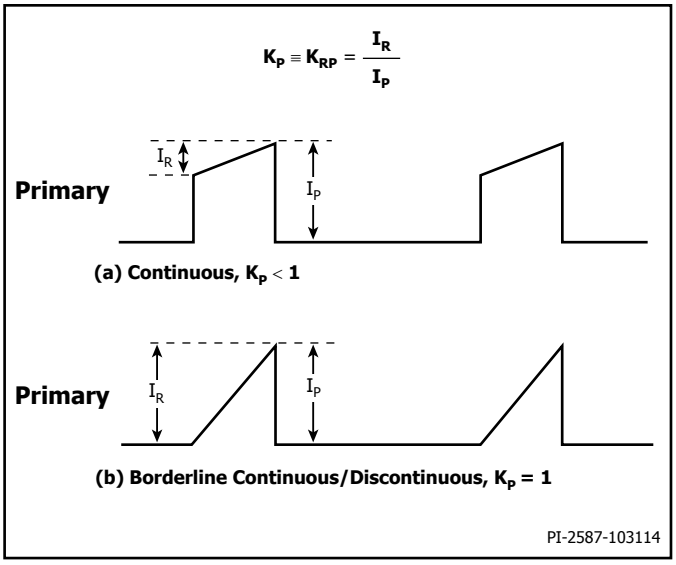


Figure 38. Continuous Mode Current Waveform, $K_p \leq 1$.

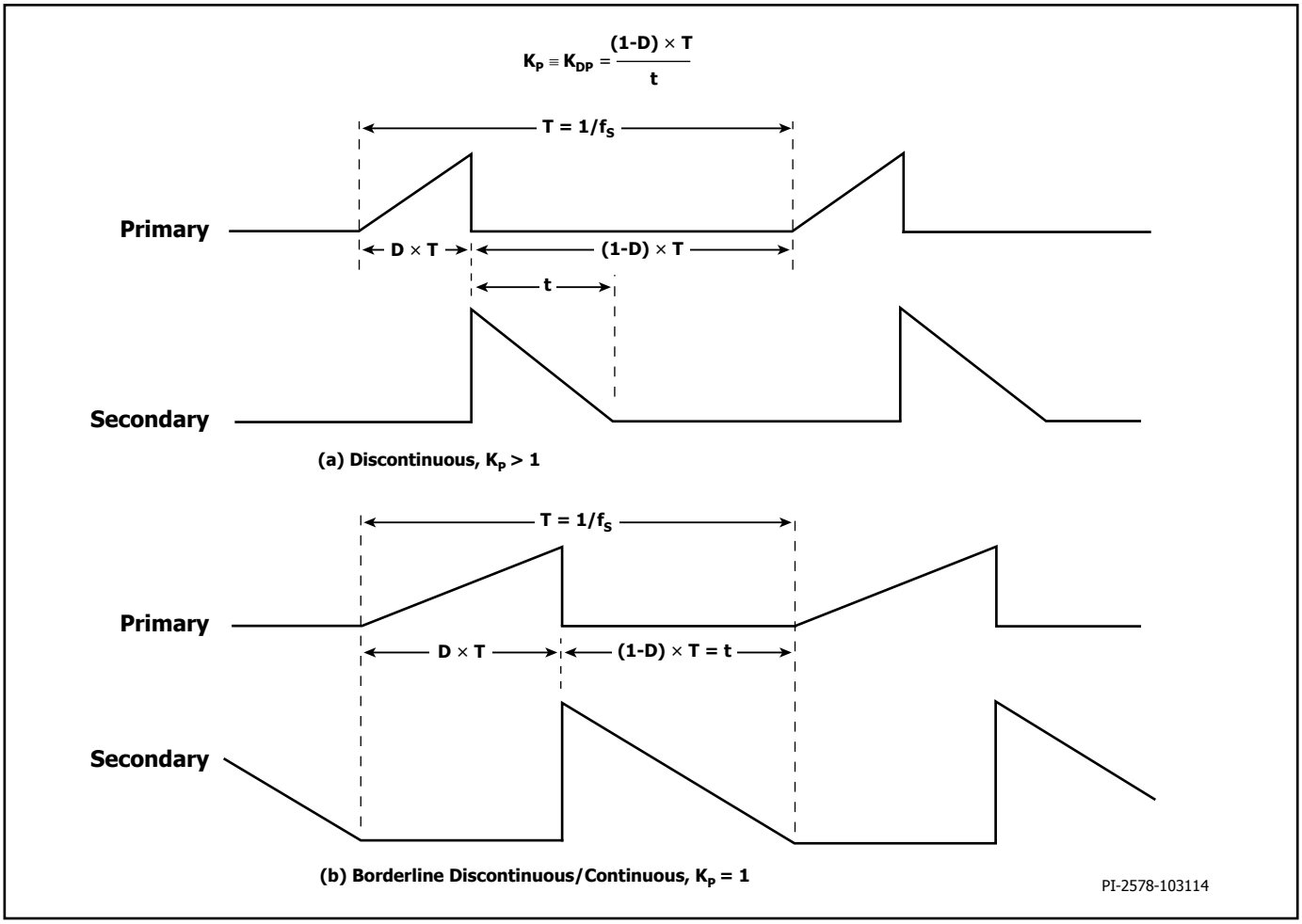


Figure 37. Discontinuous Mode Current Waveform, $K_p \geq 1$.

Transformer Construction for Mitigation of Audible Noise
Although InnoSwitch3-Pro features audible noise reduction engine which prevents operation in the predominant audible range, application of the thixotropic epoxy glue in the transformer air gap is recommended. This helps to damp any audible noise when the power supply operates at light load which results in the low frequency operation.

Design Considerations When Using PowiGaN Devices (INN3378C, INN3379C and INN3370C)

For a flyback converter configuration, typical voltage waveform at the drain pin of the IC is shown in Figure 39.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 39 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

V_{OR} choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for VOR
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 150
24 V	135 - 180

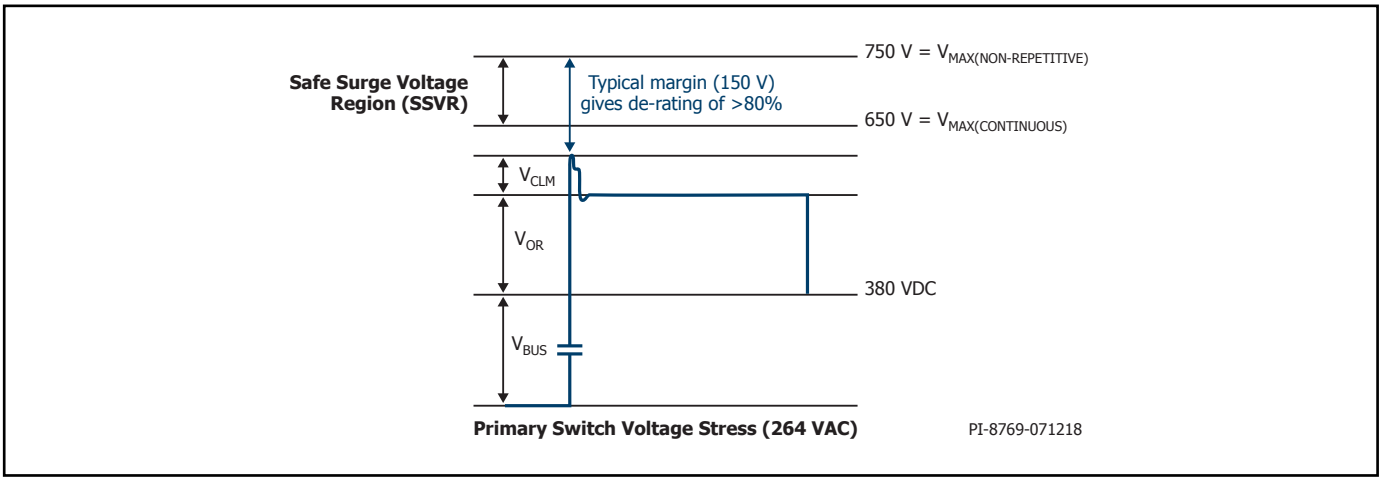


Figure 39. Peak Drain Voltage for 264 VAC Input Voltage.

Quick Design Checklist

As with any power supply design, all InnoSwitch3-Pro designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch3-Pro and SR FET do not exceed 90% of breakdown voltages at highest input voltage and peak (overload) output power in normal operating and start-up conditions.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady-state conditions and verify that the leading edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.

Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specification limits are not exceeded for InnoSwitch3-Pro IC, transformer, output SR FET, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of InnoSwitch3-Pro IC as specified in the data sheet.

Under low-line, maximum power, a maximum InnoSwitch3-Pro IC SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Thermal Resistance Test Conditions for PowiGaN Devices (INN3378C, INN3379C and INN3370C)

Thermal resistance value is for primary power device junction to ambient only.

Testing performed on custom thermal test PCB as shown in Figure 40. The test board consists of 2 layers of 2 oz. Cu with the InSOP package mounted to the top surface and connected to a bottom layer Cu heat sinking area of 550 mm^2.

Connection between the two layers was made by 82 vias in a 5 x 17 matrix outside the package mounting area. Vias are spaced at 40 mils, with 12 mil diameter and plated through holes are not filled.

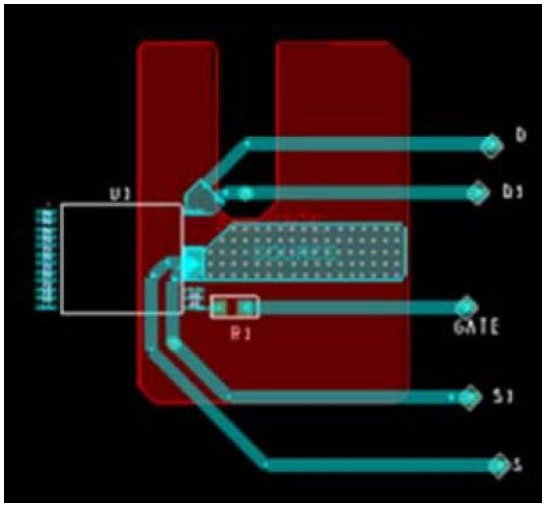


Figure 40. Thermal Resistance Test Conditions for PowiGaN Devices (INN3378C, INN3379C and INN3370C.)

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: INN33x5C–INN33x8C ..... -0.3 V to 650 V / 725 V
DRAIN Pin Voltage[6]: INN3378C–INN3370C..... -0.3 V to 750 V
DRAIN Pin Peak Current: INN3365C.....3.87 A[7]
INN3375C.....4.11 A[7]
INN3366C.....4.88 A[7]
INN3376C.....5.19 A[7]
INN3367C.....5.57 A[7]
INN3377C.....5.92 A[7]
INN3368C.....6.24 A[7]
PowiGaN device INN3378C .....6.5 A[7]
PowiGaN device INN3379C .....10 A[7]
PowiGaN device INN3370C .....14 A[7]
BPP/BPS Pin Voltage .....-0.3 to 6 V
BPP/BPS Current ..... 100 mA
SCL, SDA, uVCC Pin Voltage .....-0.3 to 6 V
uVCC Current[5] ..... 12 mA
FWD Pin Voltage ..... -1.5 V to 150 V
SR Pin Voltage .....-0.3 V to 6 V
V Pin Voltage .....-0.3 V to 650 V
VOUT Pin Voltage .....-0.3 V to 27 V
VB/D Pin Voltage .....-0.3 V to 35 V
IS Pin Voltage .....-0.3 V to 0.3 V[8]
Storage Temperature .....-65 to 150 °C
Operating Junction Temperature[3].....-40 to 150 °C
Ambient Temperature .....-40 to 105 °C
Lead Temperature[4] .....260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Only at 5 V output, the uVCC pin can supply 48 mA maximum current for 0.5 seconds.
6. PowiGaN devices:
   Maximum drain voltage (non-repetitive pulse) .....-0.3 V to 750 V
   Maximum continuous drain voltage.....-0.3 V to 650 V
7. Please refer to Figures 42, 48 and 56 for maximum allowable voltage and current combinations.
8. Absolute maximum voltage for less than 500 µs is 3 V.

Thermal Resistance

Thermal Resistance:
INN33x5C to INN33x8C
(θ_{JA}).....76 °C/W[1], 65 °C/W[2]
(θ_{JC}).....8 °C/W[3]
PowiGaN devices INN3378C to INN3370C
(θ_{JA}).....50 °C/W[4]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.
4. Please see Figure 40.

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W
Package Characteristics			
Clearance		12.1	mm (typ)
Creepage		11.7	mm (typ)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		600	-

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Startup Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz		0.80	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C	INN33x5C – INN33x8C	145	200	425	µA
			INN3378C – INN3370C	145	266	425	
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz) T_J = 25 °C	INN3365C	0.49	0.65	1.03	mA
			INN3366C	0.64	0.86	1.21	
			INN3367C	0.77	1.03	1.38	
			INN3368C	0.90	1.20	1.75	
			INN3375C	0.59	0.79	1.10	
			INN3376C	0.77	1.02	1.38	
			INN3377C	0.90	1.20	1.73	
			INN3378C	0.93	1.24	1.79	
			INN3379C INN3370	1.46	1.95	2.81	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	INN33x5C – INN33x8C	-1.73	-1.35	-0.88	mA
			INN3378C – INN3370C	-1.75	-1.35	-0.88	
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.65	4.90	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C		0.22	0.39	0.55	V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.80	3.15	3.50	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	INN33x5C – INN33x8C	23.9	26.1	28.2	µA
			INN3378C – INN3370C	22.4	24.4	26.7	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	INN33x5C – INN33x8C	21.0	23.7	25.5	µA
			INN3378C – INN3370C	19.0	21.6	23.5	
Brown-Out Delay Time	t_{UV-}				35		ms

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	INN33x5C – INN33x8C	106	115	118	µA
			INN3378C – INN3370C	106	112	118	
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C	INN33x5C – INN33x8C		7		µA
			INN3378C – INN3370C		8		
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100			µA
Line Fault Protection							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C			3		µs
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF See Note D	I_{LIMIT}	di/dt = 213 mA/µs T_J = 25 °C	INN33x5C	883	950	1017	mA
		di/dt = 238 mA/µs T_J = 25 °C	INN33x6C	1162	1250	1338	
		di/dt = 300 mA/µs T_J = 25 °C	INN3377C	1255	1350	1445	
			INN3367C	1348	1450	1552	
		di/dt = 375 mA/µs T_J = 25 °C	INN3368C	1534	1650	1766	
		di/dt = 375 mA/µs T_J = 25 °C	INN3378C	1581	1700	1819	
		di/dt = 425 mA/µs T_J = 25 °C	INN3379C	1767	1900	2033	
		di/dt = 525 mA/µs T_J = 25 °C	INN3370C	2139	2300	2461	
Increased Current Limit (BPP) Capacitor = 4.7 µF See Note D	$I_{LIMIT+1}$	di/dt = 213 mA/µs T_J = 25 °C	INN33x5C	1046	1150	1254	mA
		di/dt = 238 mA/µs T_J = 25 °C	INN33x6C	1319	1450	1581	
		di/dt = 300 mA/µs T_J = 25 °C	INN3377C	1410	1550	1689	
			INN3367C	1501	1650	1799	
		di/dt = 375 mA/µs T_J = 25 °C	INN3368C	1683	1850	2017	
		di/dt = 375 mA/µs T_J = 25 °C	INN3378C	1767	1900	2033	
		di/dt = 425 mA/µs T_J = 25 °C	INN3379C	1980	2130	2279	
		di/dt = 525 mA/µs T_J = 25 °C	INN3370C	2395	2576	2756	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		102	110	118	kHz

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
BYPASS Pin Fault Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5	11.3	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C		0.17	0.20	0.23	sec
Output							
ON-State Resistance	$R_{DS(ON)}$	INN3365C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	Ω
			T_J = 100 °C		3.02	3.47	
		INN3375C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		INN3366C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.30	1.50	
			T_J = 100 °C		2.02	2.32	
		INN3376C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.34	1.54	
			T_J = 100 °C		2.08	2.39	
		INN3367C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.02	1.17	
			T_J = 100 °C		1.58	1.82	
		INN3377C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
		INN3368C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.86	0.99	
			T_J = 100 °C		1.33	1.53	
		INN3378C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		INN3379C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN3370C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	118	132	145	kHz
Minimum Off-time	$t_{OFF(MIN)}$		2.48	3.38	4.37	µs
BPS Pin Latch Command Shutdown Threshold Current	$I_{BPS(SD)}$		5.2	8.9	12	mA
Start-up VOUT Pin Regulation Voltage	$VOUT_{REG}$	T_J = 25 °C	4.85	5	5.15	V
Output Voltage Programming Range	$V_{OUT(R)}$	Default = 5 V	3.00		24.00	V
	TOL_{VOUT}	Tolerance T_J = 25 °C	-3		+3	%
Output Voltage Step Size	ΔV_{OUT}	T_J = 25 °C		10		mV
Report-Back Output Voltage Tolerance	$V_{OUT(T)}$	T_J = 25 °C	-3		+3	%
Normalized Output Current	I_{OUT}	0.6 - 1.0 T_J = 25 °C, See Note C	-5		+5	%
		0.2 T_J = 25 °C, See Note C	-15		+15	
Normalized Output Current Step Size	ΔI_{OUT}	T_J = 25 °C		0.78		%
Maximum V/I Update Rate	t_{VI}	See Note B		10		ms
Minimum Time Delay Between I²C Commands	t_{DELAY}	See Note B	150			µs
Internal Current Limit Voltage Threshold	$I_{SV(TH)}$	T_J = 25 °C Across External IS to GND Pin Resistor See Note F		32		mV
Cable Drop Compensation (CDC) Programming Range	$\Delta\phi_{CD}$	T_J = 25 °C Default = 0 V	0		600	mV
CDC Tolerance	$TOL\phi_{CD}$	CDC ≥ 100 mV T_J = 25 °C	-25		25	mV
CDC Programming Step Size	$\Delta\phi_{CD}$			50		mV
Output Overvoltage Programming Range	V_{OVA}	Default = 6.2 V	6.2		25	V
Output Overvoltage Tolerance	TOL_{OVA}	T_J = 25 °C	-3		3	%
Output Overvoltage Programming Step Size	ΔV_{OVA}			100		mV
Output Undervoltage Programming Range	V_{UVA}	Default = 3.6 V	3		24	V
Output Undervoltage Tolerance	TOL_{UVA}	T_J = 25 °C	-3		3	%

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary (cont.)							
Output Undervoltage Programming Step Size	ΔV_{UVA}				100		mV
Output Undervoltage Timer Programming Options	t_{UVL}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Programming Option 4		64		
Constant Output Power Onset Threshold Programming Range	V_{KP}	Default = 24 V		5.3		24	V
Constant Output Power Tolerance	$TOLP_{OUT}$	At 85% of Full Scale Current		-10		+10	%
Constant Output Power Onset Threshold Programming Step Size	ΔV_{KP}				100		mV
Constant Voltage Mode Timer Programming Options	t_{CVO}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Programming Option 4		64		
Watchdog Timer	t_{WDT}	Default Programming Option 1 See Note B			0.5		sec
		Programming Option 2, See Note B			1		
		Programming Option 3, See Note B			2		
VB/D Drive Voltage	$V_{VB/D}$	With Respect to VOUT Pin		4		10	V
VB/D Turn-On Time	$t_{R(VB/D)}$	T_J = 25 °C C_{LOAD} = 10 nF			4	10	ms
VB/D Turn-Off Time	$t_{F(VB/D)}$	T_J = 25 °C C_{LOAD} = 10 nF			4	10	µs
VB/D Pin Load Discharge Internal On-State Resistance	$R_{B/D(ON)}$			20	35	70	Ω
VB/D Pin Load Discharge Internal Off-State Resistance	$R_{B/D(OFF)}$			80			kΩ
Secondary Over-Temperature Hysteresis	$T_{SEC(HYS)}$	Programming Option 1 See Note B			40		°C
		Programming Option 2 See Note B			60		
VOUT Pin Bleeder Current	IVO_{BLD}	VOUT = 5 V		170	270	380	mA
uVCC Supply Voltage	uVCC	I_{uVCC} = 0 A V_{OUT} = 5 V		3.42	3.60	3.78	V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary (cont.)						
Maximum uVCC Supply Current	I_{uVCC}	uVCC > 3.3 V, V_{OUT} = 5 V T_J = 25 °C, See Note 5 in Absolute Maximum Ratings Table	48			mA
		uVCC > 3.3 V 3.9 V ≤ V_{OUT} T_J = 25 °C	10			
uVCC Pin Output Resistance	R_{uVCC}	T_J = 25 °C	18	21	24	Ω
uVCC Reset Voltage Threshold	$uVCC_{RST}$	See Note B			2.65	V
BPS Pin Voltage	V_{BPS}		4.2	4.4	4.6	V
BPS Pin Current	I_{SNL}	T_J = 25 °C VBUS Switch Open		0.67	0.85	mA
		T_J = 25 °C VBUS Switch Closed		1.03	1.3	
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)TH}$		3.6	3.8	4.0	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)TH}$			0.65		V
Soft Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C	7.5	11.8	19	ms
FORWARD Pin Breakdown Voltage	BV_{FWD}		150			V
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}		4.2	4.4	4.6	V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-2.5	0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF f_S = 100 kHz	125	165	195	mA
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF f_S = 100 kHz	238	265	314	mA
Rise Time	$t_{R(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 10-90%		50		ns
Fall Time	$t_{F(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 90-10%		30		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} + 0.1 V I_{SR} = 30 mA	7.2	8.9	12	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} + 0.2 V I_{SR} = 30 mA	3.5	4.7	5.5	Ω

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
SCL Clock Frequency	f_{SCL}	See Note G	50	400	700	kHz
Low-level Input Voltage	V_{IL}		-0.5		0.3 × uVCC	V
High-level Input Voltage	V_{IH}		0.7 × uVCC		uVCC + 0.5 V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 × uVCC			V
Low-Level Output Voltage (Open Drain or Collector)	V_{OL}	uVCC >2.8 V 3 mA Sink Current	0		0.4	V
Low-level Output Current	I_{OL}		3			mA
Output Fall-Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	t_{OF}	Bus Capacitance from 10 pF to 400 pF	-		250	ns
SDA/SCL Input Current	I_I	(0.1 × uVCC) < (V_{SCL}/V_{SDA}) < (0.9 × uVCC)	-1		1	µA
SDA/SCL Capacitance	C_I		-		10	pF
Pulse Width of Spike Suppressed by Input Filter	t_{SP}		50			ns
High Period for SCL Clock	t_{HIGH}	f_{SCL} = 400 kHz	0.6			µs
Low Period for SCL Clock	t_{LOW}	f_{SCL} = 400 kHz	1.3			µs
Serial Data Set-up Time	$t_{SU:DAT}$		100			ns
Serial Data Hold time	$t_{HD:DAT}$		0			sec
Valid Data Time	$t_{VD:DAT}$	SCL Low to SDA Output Valid			0.9	µs
Valid Data Time for ACK	$t_{VD:ACK}$	ACK from SCL Low to SDA Low			0.9	µs
I²C Bus Free Time Between Start and Stop	t_{BUF}		1.3			µs
I²C Fall Time (Both SCL and SDA)	t_{fCL}				300	ns
I²C Rise Time (Both SCL and SDA)	t_{rCL}				300	ns
I²C Start or Repeated Start Condition Set-up Time	$t_{SU:STA}$		0.6			µs
I²C Start or Repeated Start Condition Hold Time	$t_{HD:STA}$		0.6			µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
I²C Stop Condition Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load	C_B				400	pF
Noise Margin at the Low Level	V_{NL}		0.1 × uVCC			V
Noise Margin at the High Level	V_{NH}		0.1 × uVCC			V
SCL Pin Interrupt Timer	$t_{INT(SCL)}$	T_J = 25 °C	50			µs

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. Use 1% tolerance resistor.
D. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

E. Settling delay in averaging register will increase total observed time under light and no-load conditions.
F. This parameter should be used only for calculation of typical value of current sense resistor. The value programmed in CC register (0x98) regulates the output current. The tolerance is specified in the Normalized Output Current parameter (I_{OUT}).
G. Guarantee minimum low period for SCL clock of 930 ns while operating at any SCL clock frequency. This may require using asymmetrical SCL clock (reduced duty cycle) at higher frequencies.

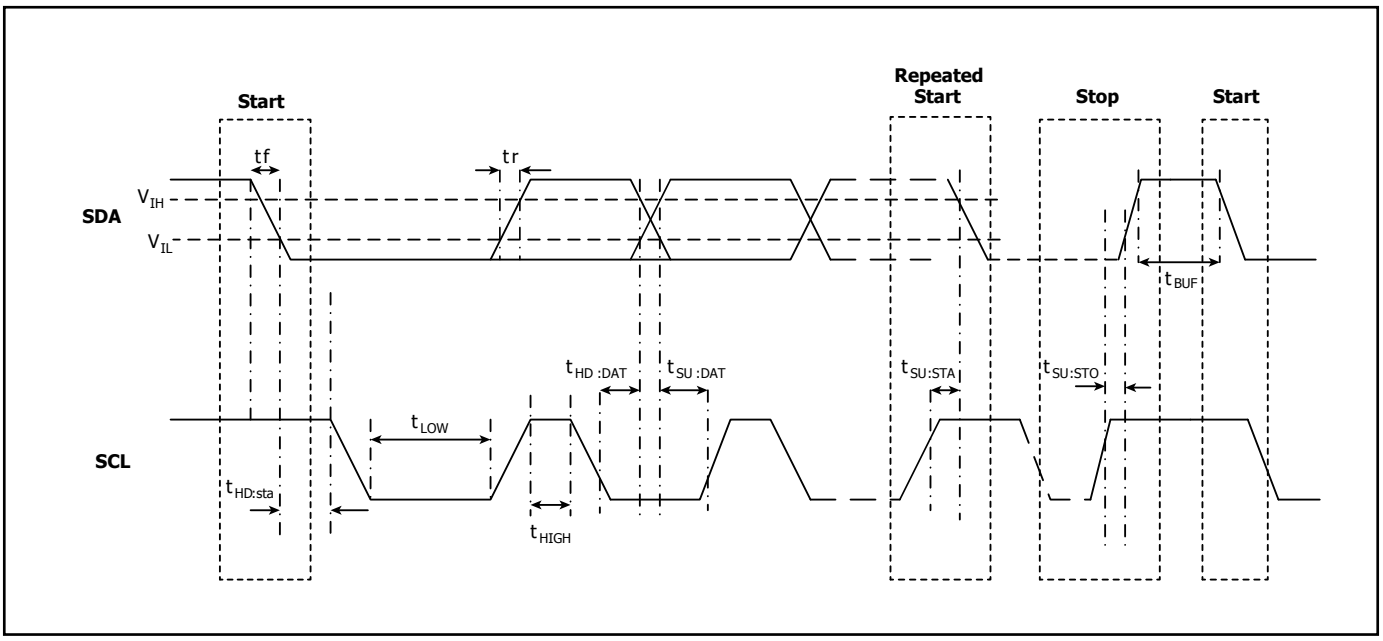


Figure 41. I²C Timing Diagram.

Typical Performance Curves

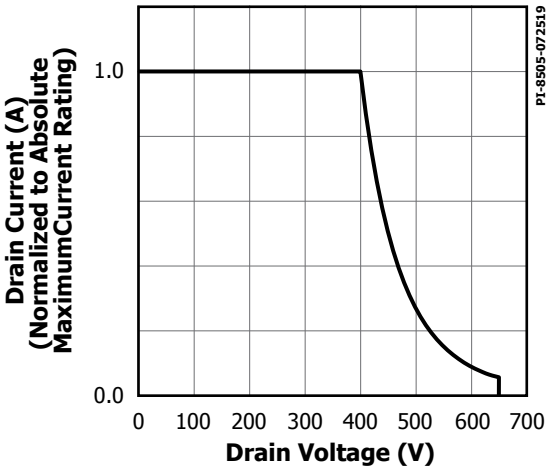


Figure 42. Maximum Allowable Drain Current vs. Drain Voltage (INN336x).

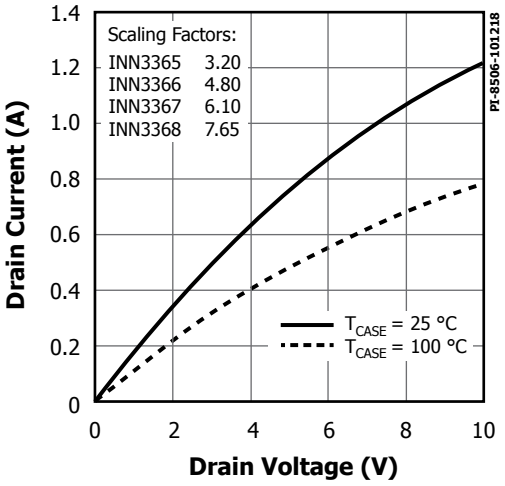


Figure 43. Output Characteristics.

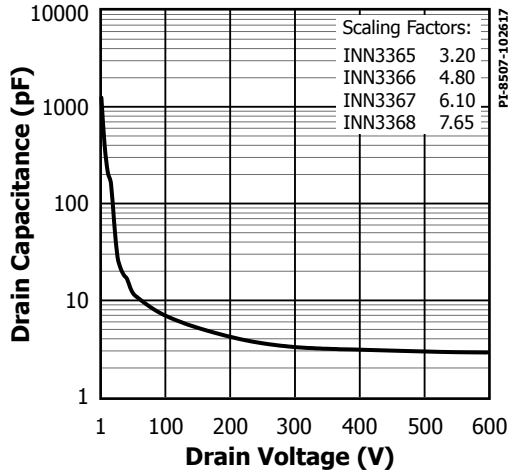


Figure 44. C_{OSS} vs. Drain Voltage.

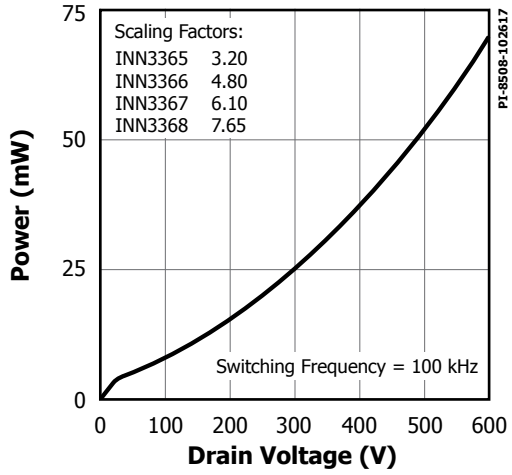


Figure 45. Drain Capacitance Power.

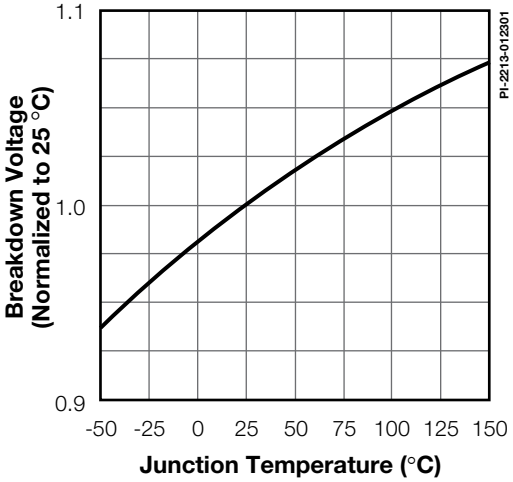


Figure 46. Breakdown vs. Temperature (Exclude INN3378C / INN3379C / INN3370C).

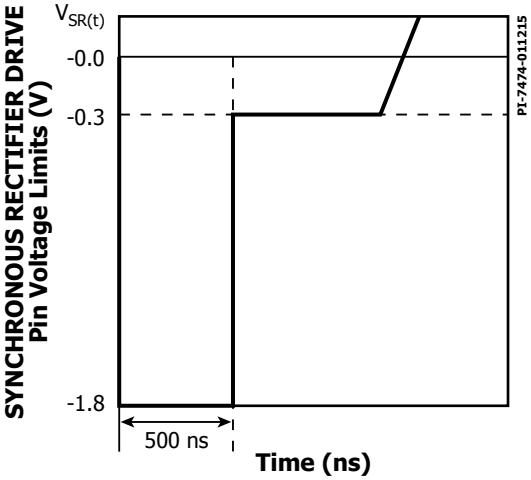


Figure 47. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

Typical Performance Curves (cont.)

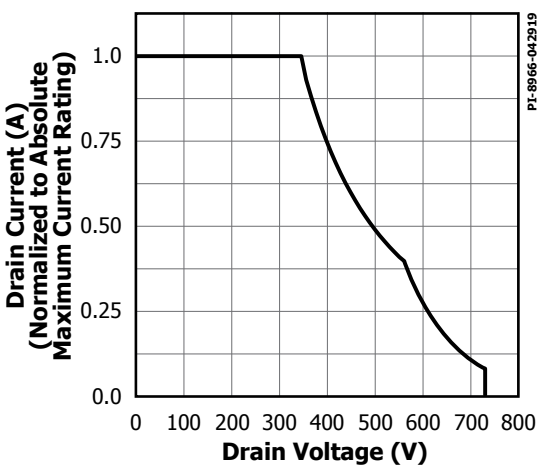


Figure 48. Maximum Allowable Drain Current vs. Drain Voltage (INN3375/76/77).

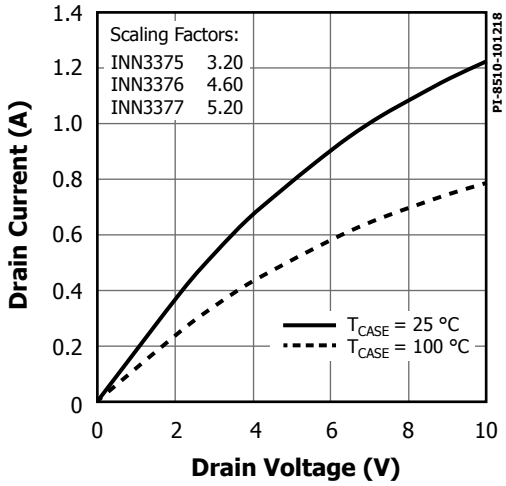


Figure 49. Output Characteristics.

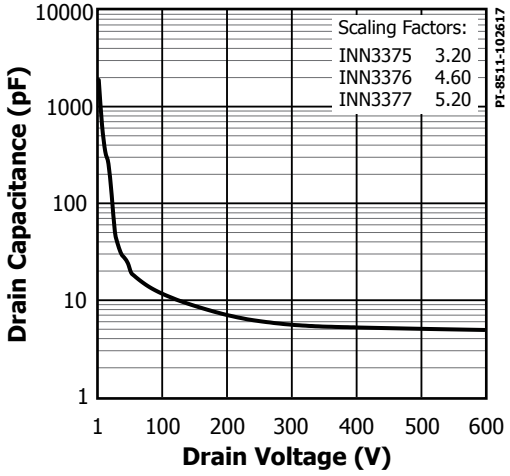


Figure 50. C_{OSS} vs. Drain Voltage.

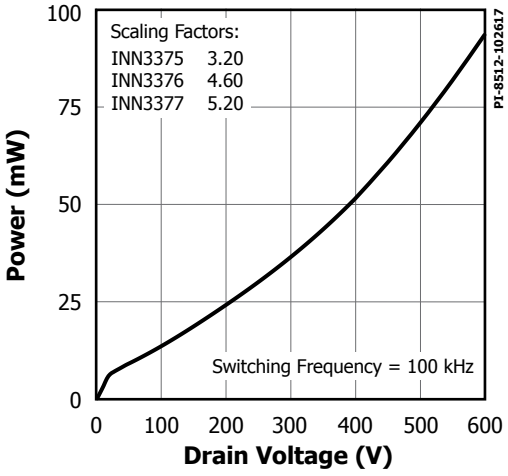


Figure 51. Drain Capacitance Power.

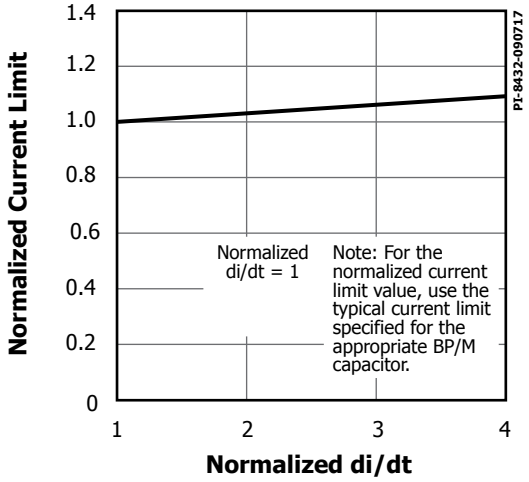


Figure 52. Standard Current Limit vs. di/dt.

Typical Performance Curves (cont.)

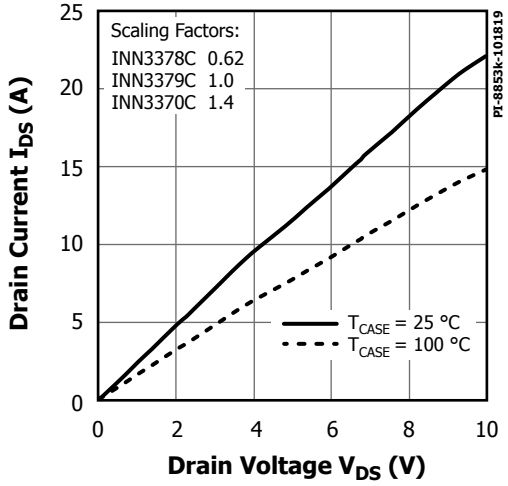


Figure 53. Output Characteristics.

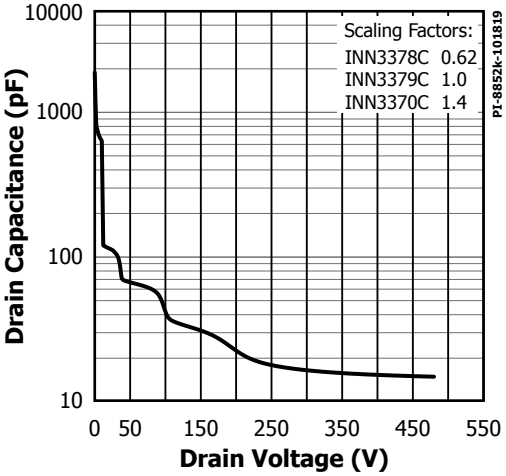


Figure 54. C_{OSS} vs. Drain Voltage.

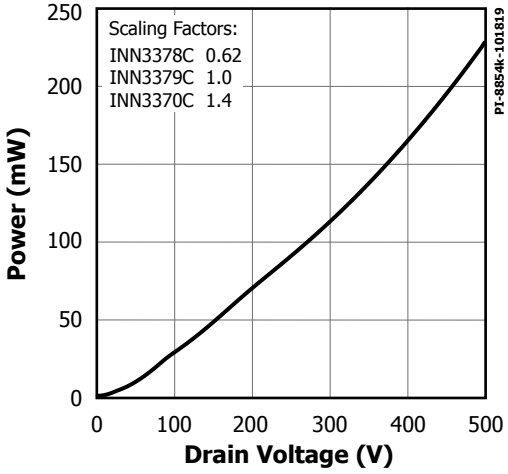


Figure 55. Drain Capacitance Power.

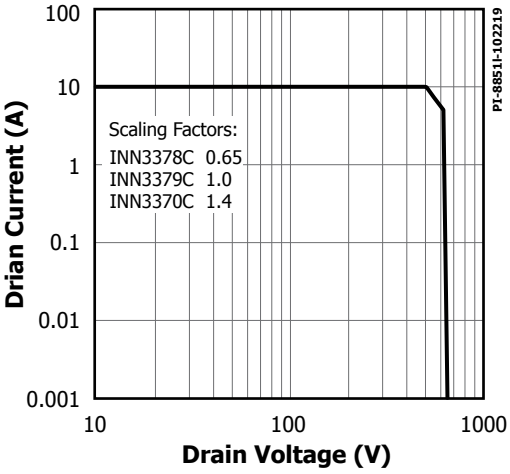
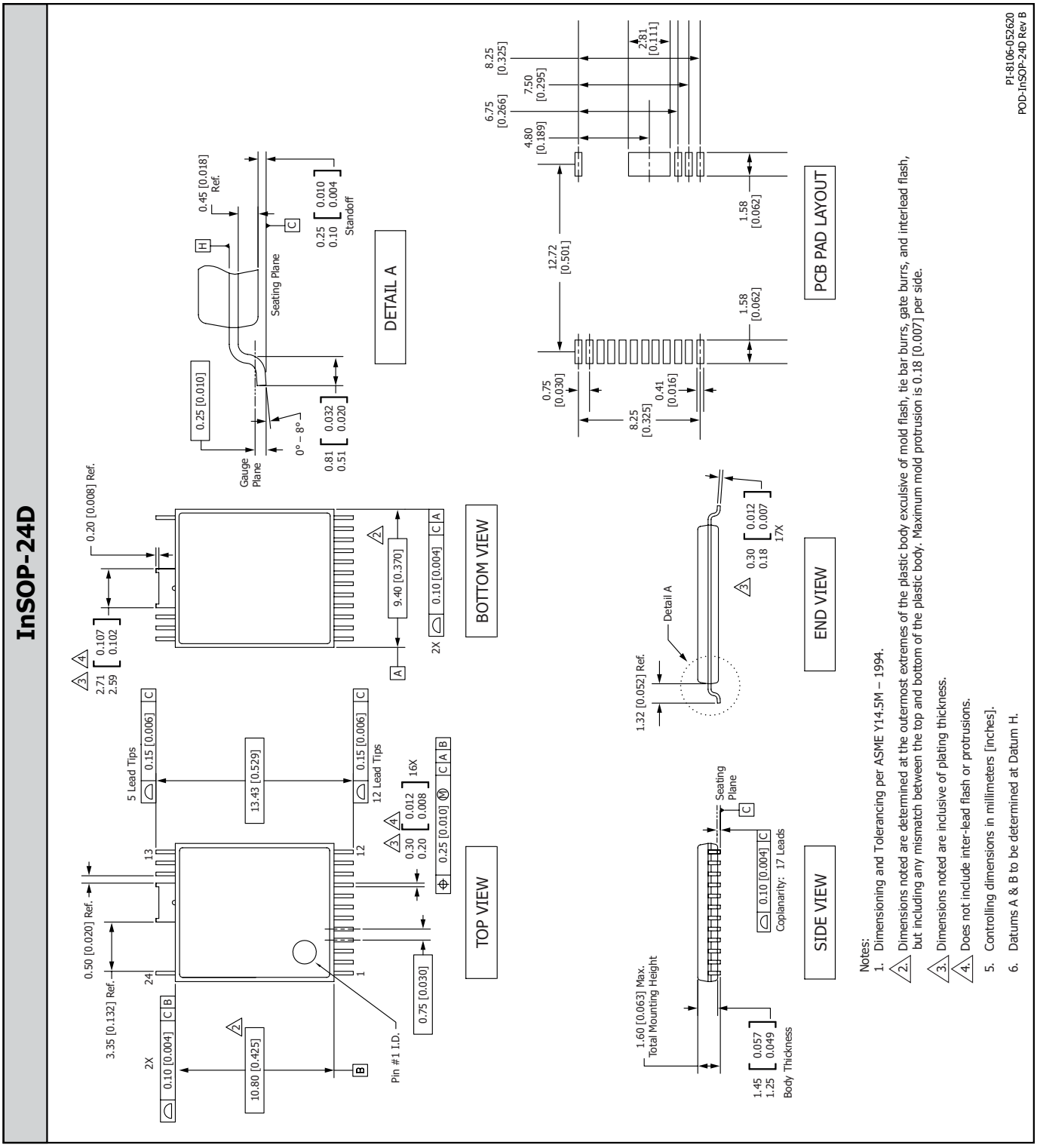


Figure 56. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices INN3378-INN3370).

InSOP-24D



Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

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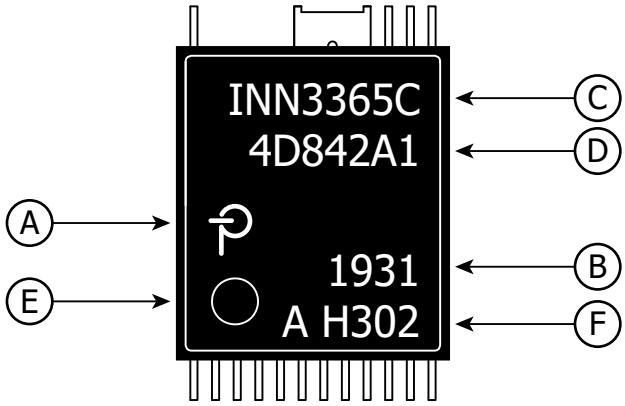
POD-InSOP-24D Rev B

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Test Lot Information

PI-8645i-081020

Feature Code Table

Summary Features	H301[1] / H302[2]
I_{LIM} Selectable	Yes
Over-Temperature Protection	Hysteretic
Line OV/UV	Enabled
Line UV Timer (35 ms or 400 ms)	35 ms

Note 1. Not available for PowiGaN Devices INN3378 – INN3370.
Note 2. Recommended for all new designs.

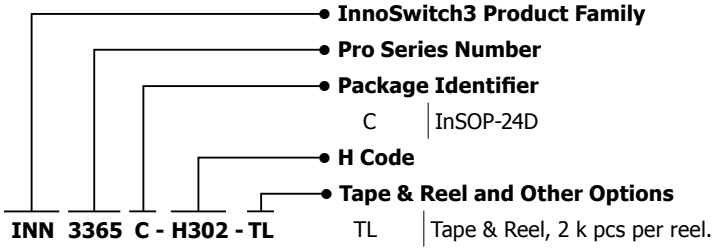
MSL Table

Part Number	MSL Rating
INN33xxC	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±1 kV on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±2 kV on all pins

Part Ordering Information



Revision	Notes	Date
C	Code L release.	03/18
D	Added READ13, 14, 15 telemetry registers. Updated H301 feature summary. Clarified register descriptions.	06/18
E	Register fixes, schematic updates, added CTI parameter.	08/18
F	Added H302 column to Part Ordering Table.	05/19
G	Code A release of PowiGaN Devices INN3379C and INN3370C. Updated $I_{DSS}1$ and I_{DSS2} parameters.	07/19
H	PCN-19432 – Updated Figure 35. Deleted $V_{BPP(H)}$ & $I_{OV(H)}$ Min & Max values. Updated I_{UV-} Min value, IVO_{BLD} Max value, I_{uVCC} Min value, $t_{SS(RAMP)}$ Max value, $I_{SR(PU)}$ Min value, $I_{SR(PD)}$ Option A & B Max values & R_{PU} Max & Min values. Updated t_{UV-} Typ value, included I_{OV-} Min value.	10/19
I	Code S release of PowiGaN Device INN3378C.	11/19
J	Code A release. Added new application design example.	01/20
K	Updated I_{DSS1} parameter to read V_{DS} = 80% Peak Drain Voltage.	03/20
L	Updated safety information on page 1 and corrected typo in Package drawing on page 53.	06/20
M	Updated Package Marking.	08/20
N	Corrected Figure 29 caption text.	09/20
O	Updated Figure 11, added new paragraph under SCL/SDA Pull-up Requirements section and Note reference for f_{SCL} parameter. Updated per PCN-18441.	11/20

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Patent Information

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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