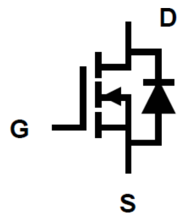
INN100W08

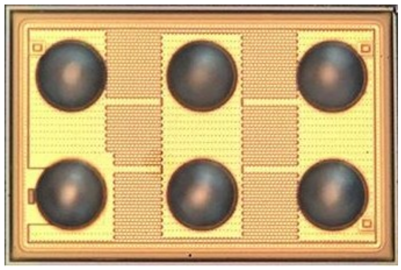
General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) with ultra-low on resistance.

Features

- GaN-on-Silicon E-mode HEMT technology
- Ultra High Switching Frequency
- Fast and Controllable Fall and Rise Time
- Ultra-low on Resistance





Applications

- High efficiency power conversion
- High density power conversion
- Industrial Automation
- DC-DC Converters

Package: WLCSP 2X3
Size: 1.508mm X 0.993mm

Maximum ratings

Symbol	Parameter	Max	Unit
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous Current	4	A
	Pulsed (25˚C, T_{Pulse} = 100 μs)	50	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.36	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	19.6	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	65	˚C/W

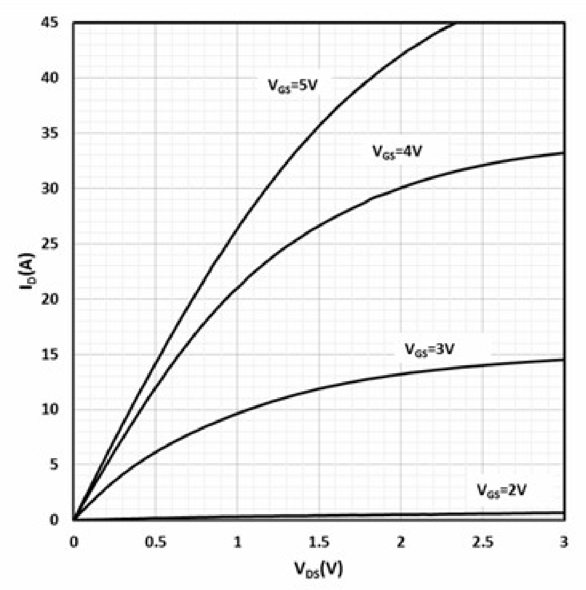
Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Electrical Characteristics (TJ =25°C unless otherwise stated)

Symbol	Parameter	Min	Typ.	Max	Unit	Test Condition
			Static Parameters			
BV_{DSS}	Drain-to-Source Voltage	100			V	V_{GS} = 0 V, I_D = 60 µA
I_{DSS}	Drain Source Leakage		10	40	µA	V_{GS} = 0 V, V_{DS} = 80 V
I_{GSS}	Gate-to-Source Forward Leakage		1	1000	µA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage		1	40	µA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.3	2.4	V	V_{DS} = V_{GS}, I_D = 0.9 mA
$R_{DS(on)}$	Drain-Source On Resistance		36	47	mΩ	V_{GS} = 5 V, I_D = 4 A
V_{SD}	Source-Drain Forward Voltage		1.9		V	I_S = 0.4 A, V_{GS} = 0 V
			Dynamic Parameters			
C_{iss}	Input Capacitance		153	191	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{oss}	Output Capacitance		74	107	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{rss}	Reverse Transfer Capacitance		0.7	1	pF	V_{GS} = 0 V, V_{DS} = 50 V
$C_{oss(er)}$	Energy Related Coss		97		pF	V_{GS} = 0 V, V_{DS} =0 to 50 V
$C_{oss(tr)}$	Time Related Coss		130		pF	V_{GS} = 0 V, V_{DS} =0 to 50 V
R_G	Gate Resistance		900		mΩ	
Q_G	Total Gate Charge		1.40	1.75	nC	V_{GS} = 5 V, V_{DS} = 50 V, I_D= 4 A
Q_{GS}	Gate to Source Charge		340		pC	V_{DS} = 50 V,I_D= 4 A
Q_{GD}	Gate to Drain Charge		240	480	pC	V_{DS} = 50 V,I_D= 4 A
$Q_{G(TH)}$	Gate Charge at Threshold		200		pC	V_{DS} = 50 V,I_D= 4 A
Q_{OSS}	Output Charge		6.70	9.40	nC	V_{DS} = 50 V, V_{GS} = 0 V

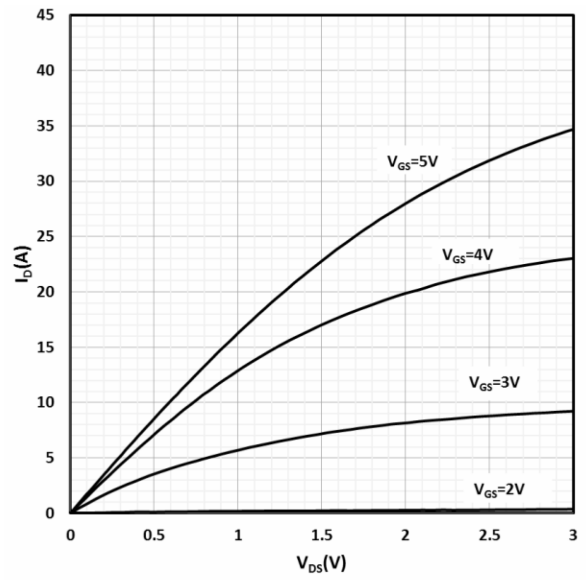
Electric characteristics diagrams

Fig. 1 Typ. Output Characteristics



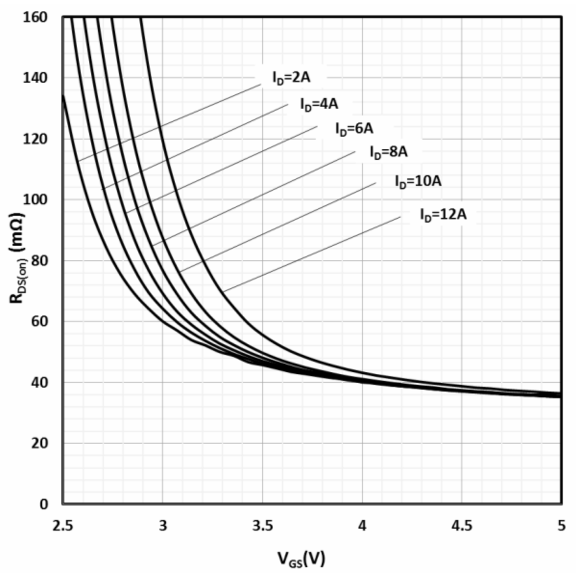
I_D=f(V_{DS},V_{GS}); T_J =25˚C

Fig. 2 Typ. Output Characteristics



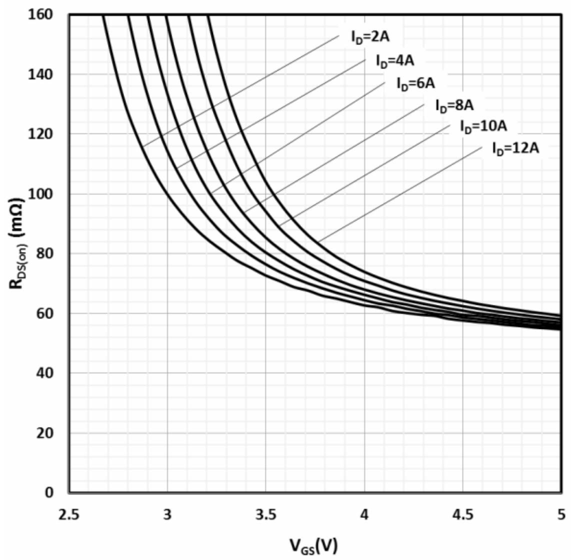
I_D=f(V_{DS},V_{GS}); T_J =125˚C

Fig. 3 Typ.Drain-Source On-State Resistance



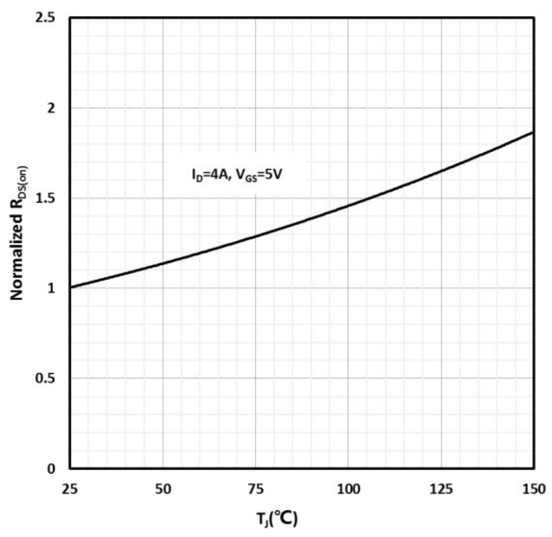
$R_{DS(on)}$=f(I_D,V_{GS}); T_J =25˚C

Fig. 4 Typ.Drain-Source On-State Resistance



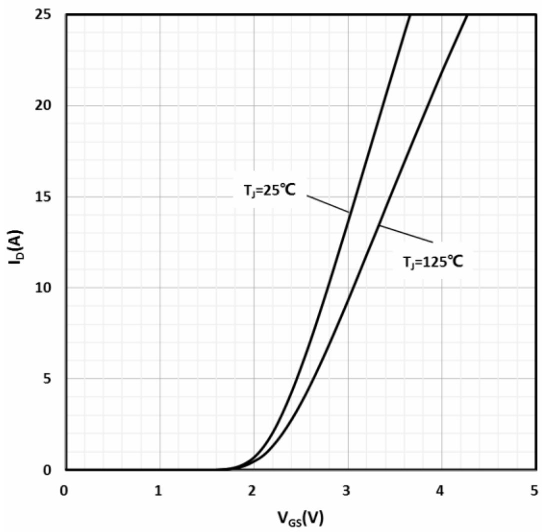
$R_{DS(on)}$=f(I_D,V_{GS}); T_J =125˚C

Fig. 5 Normalized On-State Resistance vs. Temp.



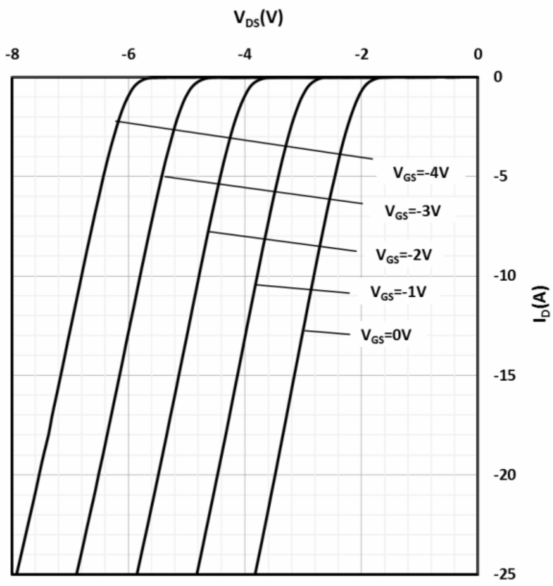
$R_{DS(on)}=f(T_J)$; I_D=4A

Fig. 6 Typ. Transfer Characteristics vs. Temp.



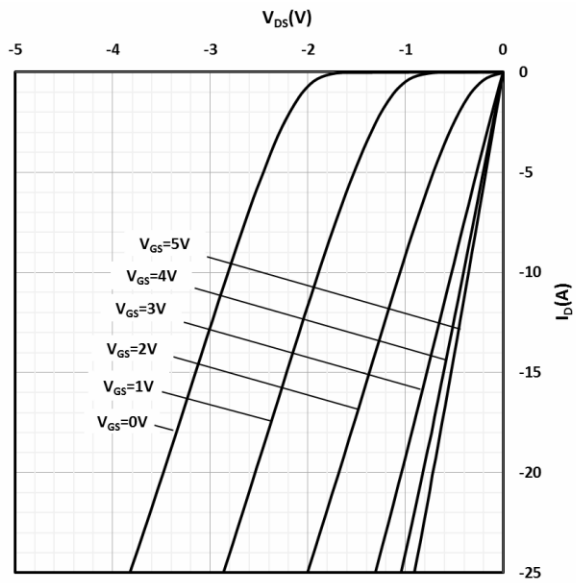
$I_D=f(V_{GS})$; V_{DS}=3V

Fig. 7 Typ. Reverse Drain-Source Characteristics



$I_D=f(V_{DS},V_{GS})$; T_J=25˚C

Fig. 8 Typ. Reverse Drain-Source Characteristics



$I_D=f(V_{DS},V_{GS})$; T_J=25˚C

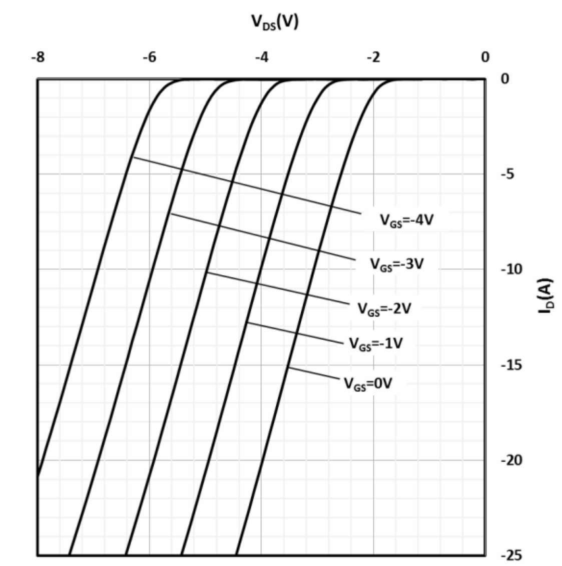
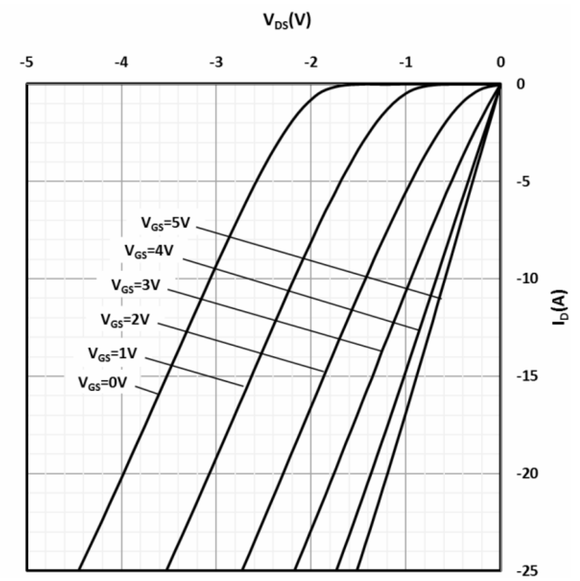
Fig. 9 Typ. Reverse Drain-Source Characteristics	Fig. 10 Typ. Reverse Drain-Source Characteristics
	
$I_D=f(V_{DS},V_{GS})$; $T_J=125^{\circ}C$	$I_D=f(V_{DS},V_{GS})$; $T_J=125^{\circ}C$

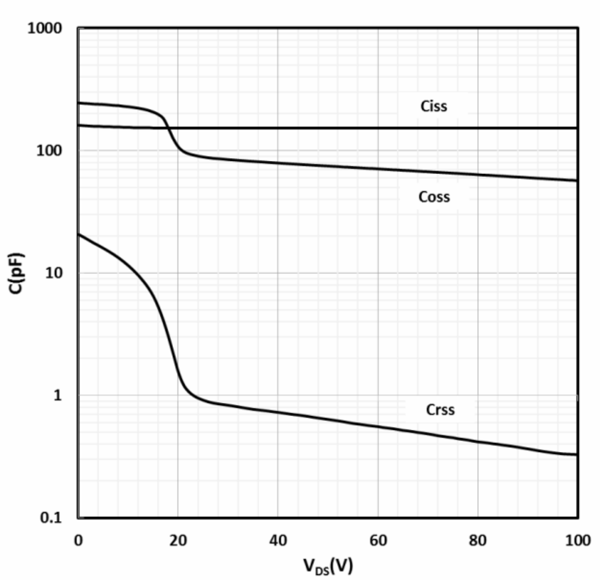
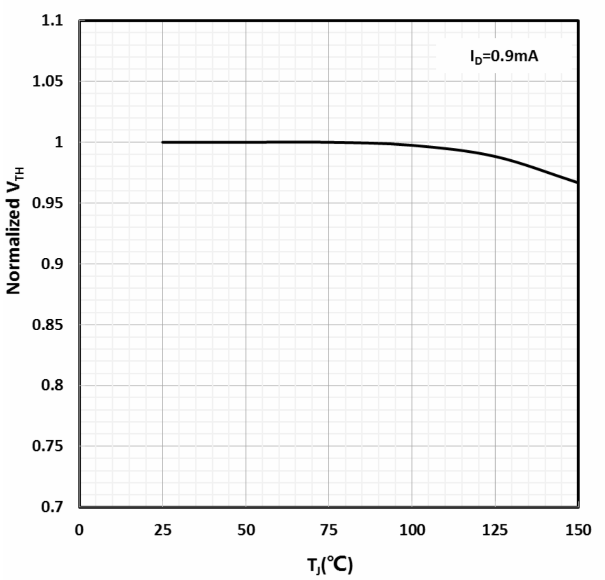
Fig. 11 Typ. Capacitances(Log Scale)	Fig. 12 Normalized Threshold Voltage vs. Temp.
	
$C_{XSS}=f(V_{DS})$	$V_{TH}=f(T_J)$; $V_{GS}=V_{DS}$; $I_D=0.9mA$

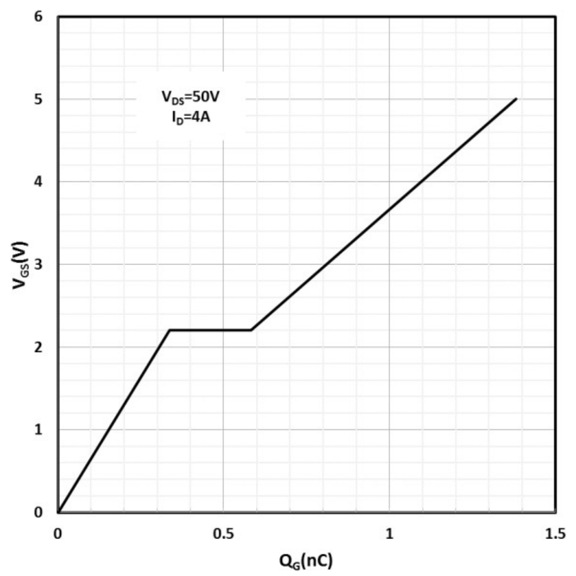
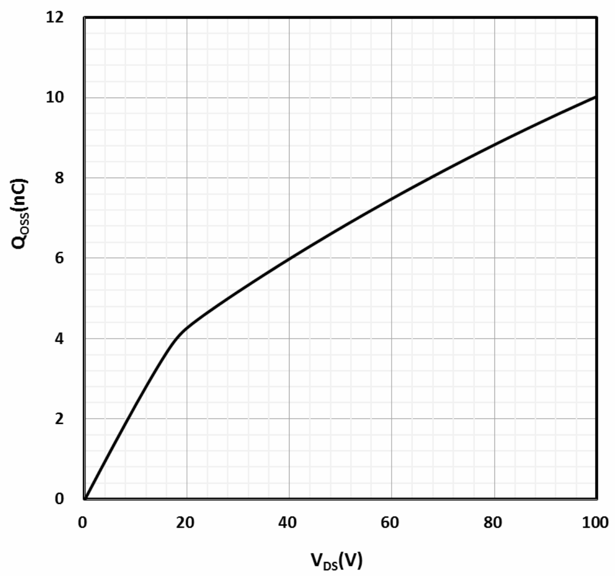
Fig. 13 Typ. Gate Charge	Fig. 14 Output Charge
	
$V_{GS}=f(Q_G)$; $V_{DS}=50V$;$I_D=4A$	$Qoss = f(V_{DS})$

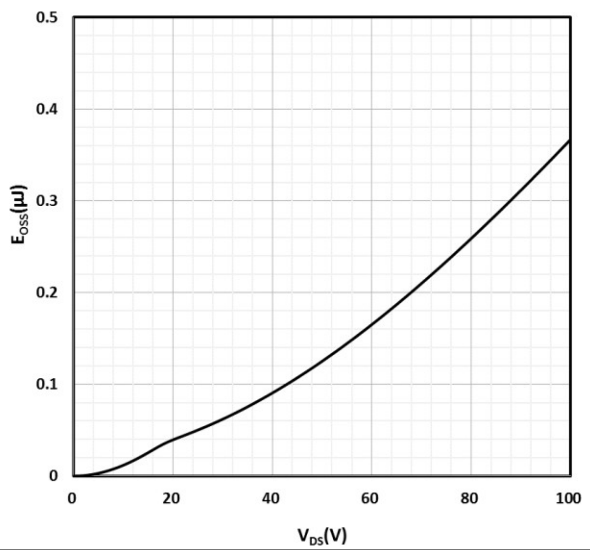
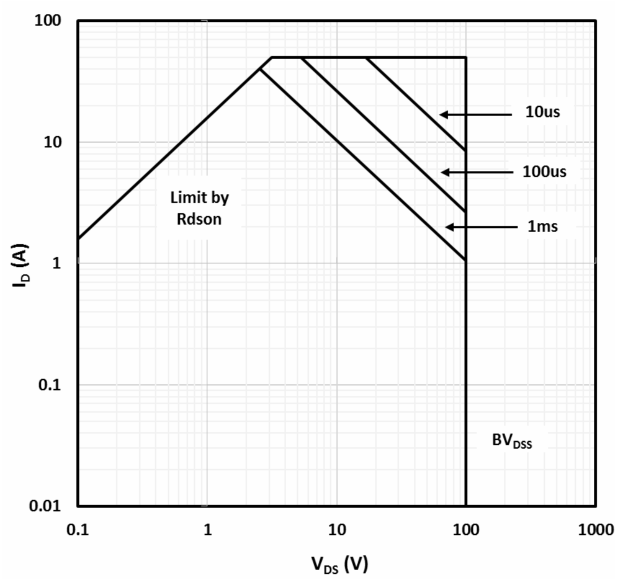
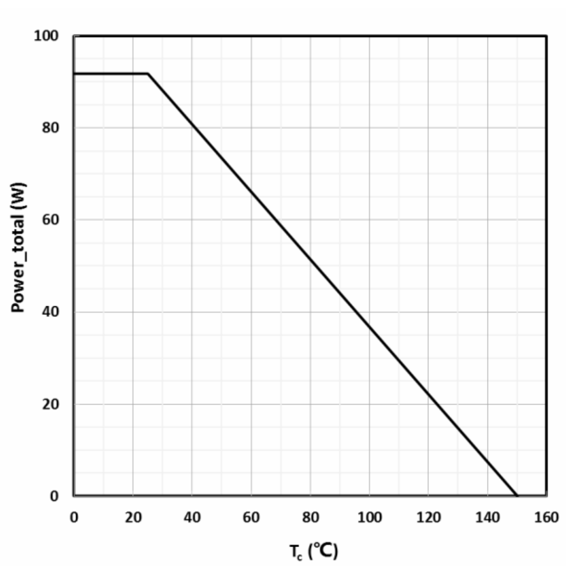
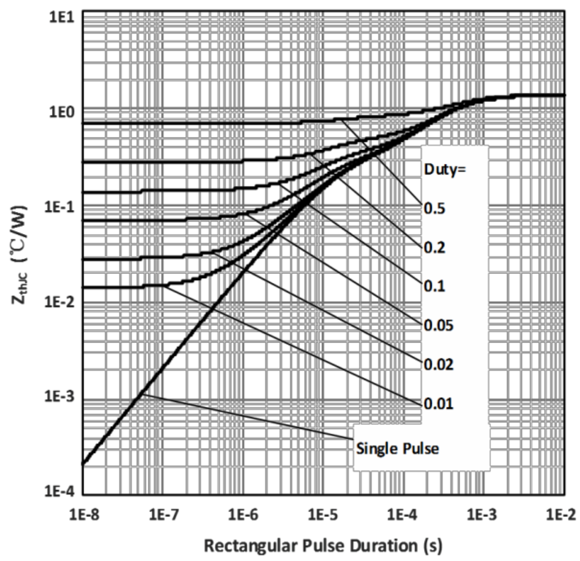
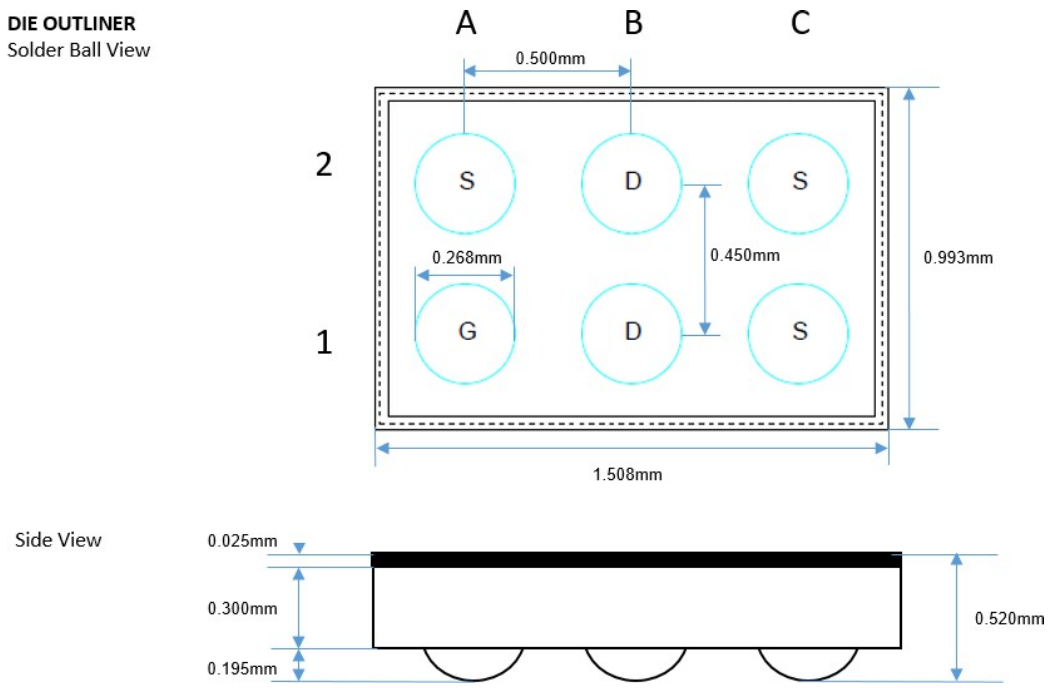
Fig. 15 Output Capacitance Stored Energy	Fig. 16 Safe Operating Area
	
$Eoss = f(V_{DS})$	$I_D=f(V_{DS})$; $T_C=25^{\circ}C$; parameter: t_p

Fig. 17 Power Dissipation	Fig. 18 Max. Transient thermal impedance
	
$P_{tot}=f(T_c)$	$Z_{thJC} = f(t_p)$; parameter: D= t_p / T

Package outlines



Marking Reference

Gate Position

Marking Line 1	Company Code
Marking Line 2	Product Code
Marking Line 3	Lot/ Package Code
Marking Line 4	Lot/ Package Code

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2020-05-30	1.0 version setup
2.0	2020-07-30	2.0 version setup

Important Notice

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