MAX77789

14VIN, 3AOUT 1-Cell Charger with Integrated USB Type-C Detection, DRP, and OTG

General Description

The MAX77789 is a standalone, 3.15A charger with integrated USB Type-C® CC detection and reverse-boost capability. The IC operates with an input voltage of 4.6V to 13.4V and has a maximum input current limit of 3A. The IC also implements the adaptive input current limit (AICL) function that regulates the input voltage by reducing input current, to prevent the voltage of a weak adapter from collapsing or folding back.

The USB Type-C Configuration Channel (CC) detection pins on the IC is operating in DRP (Dual Role Port) as a default and is capable of automatic USB Type-C power source detection and sink devices. To support a variety of legacy USB as well as proprietary adapters, the device also integrates BC1.2 detection using the D+ and D- pins. The IC runs the CC pin and BC1.2 detection automatically as soon as the USB plug is inserted without any software control.

The IC offers reverse-boost capability up to 5.1V, 1.5A, which can be enabled with automatic way or register set by system MCU. The STAT1 pin indicates charging status, while the INOKB pin indicates valid input voltage. The EXTSM pin can be used to exit ship mode and force system to reset (POR), and STAT2 pin indicates fault detection and charger detection done indication by register bit selection.

The IC is equipped with a Smart Power Selector™ and a battery true-disconnect FET to control the charging and discharging of the battery or isolate the battery in case of a fault. The IC supports Li-ion and $LiFePO_4$ batteries with various termination voltages from 3.6V to 4.55V. The IC comes in a 2.85mm x 2.85mm, 0.4mm pitch, 6 x 6 wafer-level package (WLP) making it suitable for low-cost PCB assembly.

Applications

- Mobile Point-of-Sale (mPOS) Terminals
- Portable Medical Devices
- Wireless Headphones
- GPS Trackers
- Charging Cradles for Wearable Devices
- Power Banks
- Mobile Routers

USB Type-C is a registered trademark of USB Implementers Forum.
Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

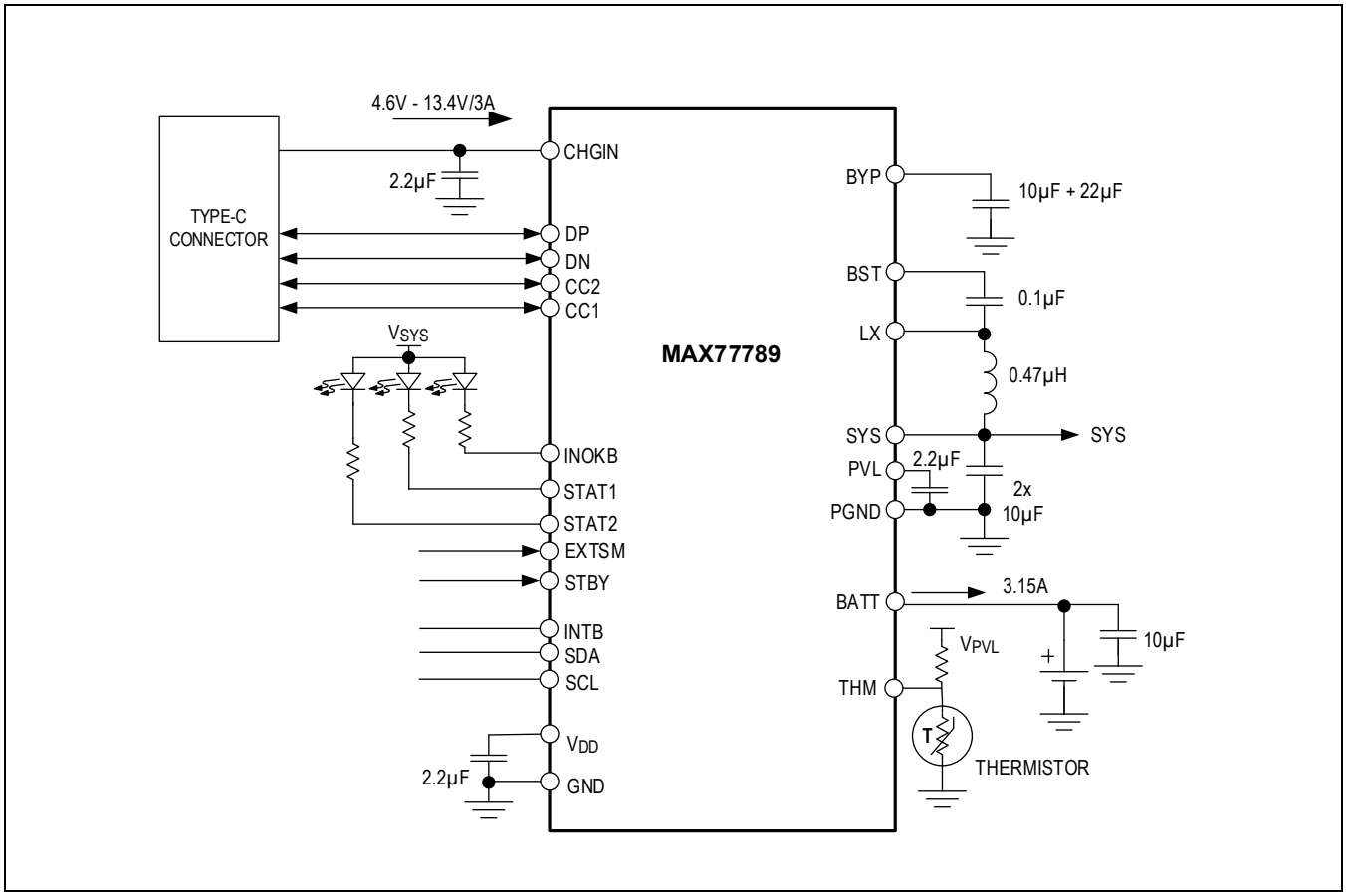
Benefits and Features

- Up to 16V Protection
- 13.4V Maximum Input Operating Voltage
- 3.15A Maximum Charging Current
- 6A Discharge Current Protection
- Integrated CC Detection for USB Type-C
- Supporting Dual Role Port (DRP)
- DP/DN Manual Control for the HVDCP
- Integrated BC1.2 Detection for Legacy SDP, DCP, CDP, and DCD Timeout
- Integrated USB Detection for Common Proprietary Charger Types
- Automatic Input Current Limit Configuration
- Input Voltage Regulation with Adaptive Input Current Limit (AICL)
- 5.1V, 1.5A OTG Mode and BYP Reverse Boost
- Safety
  - Charge Safety Timer
  - JEITA Compliance with NTC Thermistor Monitor
  - Thermal Shutdown
- Pin Control of all Functions
  - STAT1 Pin to Indicate Charging Status
  - STAT2 Pin to Indicate Fault and Charger Type Detection Complete
  - INOKB Pin to Indicate Input Power-OK
  - EXTSM Pin to Exit Ship Mode and System POR
  - STBY Pin to Support Suspend Mode
  - THM Pin to Monitor Thermistor
- Integrated Power Path
- Integrated Battery True-Disconnect FET
- I^2C Compatible with INTB
- 2.85mm x 2.85mm, 6x6 WLP Package

***Ordering Information* appears at end of data sheet.**

19-101660; Rev 2; 1/25

Simplified Block Diagram



Absolute Maximum Ratings

CHGIN to GND ..... -0.3V to +16.0V

BYP, LX to PGND ..... -0.3V to +16.0V

BATT, SYS, INOKB, STAT1, STAT2, EXTSM, STBY, INTB to GND ..... -0.3V to +6.0V

BST to PVL ..... -0.3V to +16.0V

BST to LX ..... -0.3V to +2.2V

DN, DP, CC1, CC2 to GND ..... -0.3V to +6.0V

THM to GND ..... -0.3V to V_{DD} + 0.3V

V_{DD}, PVL, SDA, SCL to GND ..... -0.2V to +2.2V

V_{CHGIN}, BYP Continuous Current ..... $3.2A_{RMS}$

LX, PGND Continuous Current ..... $3.5A_{RMS}$

SYS, BATT Continuous Current ..... $4.5A_{RMS}$

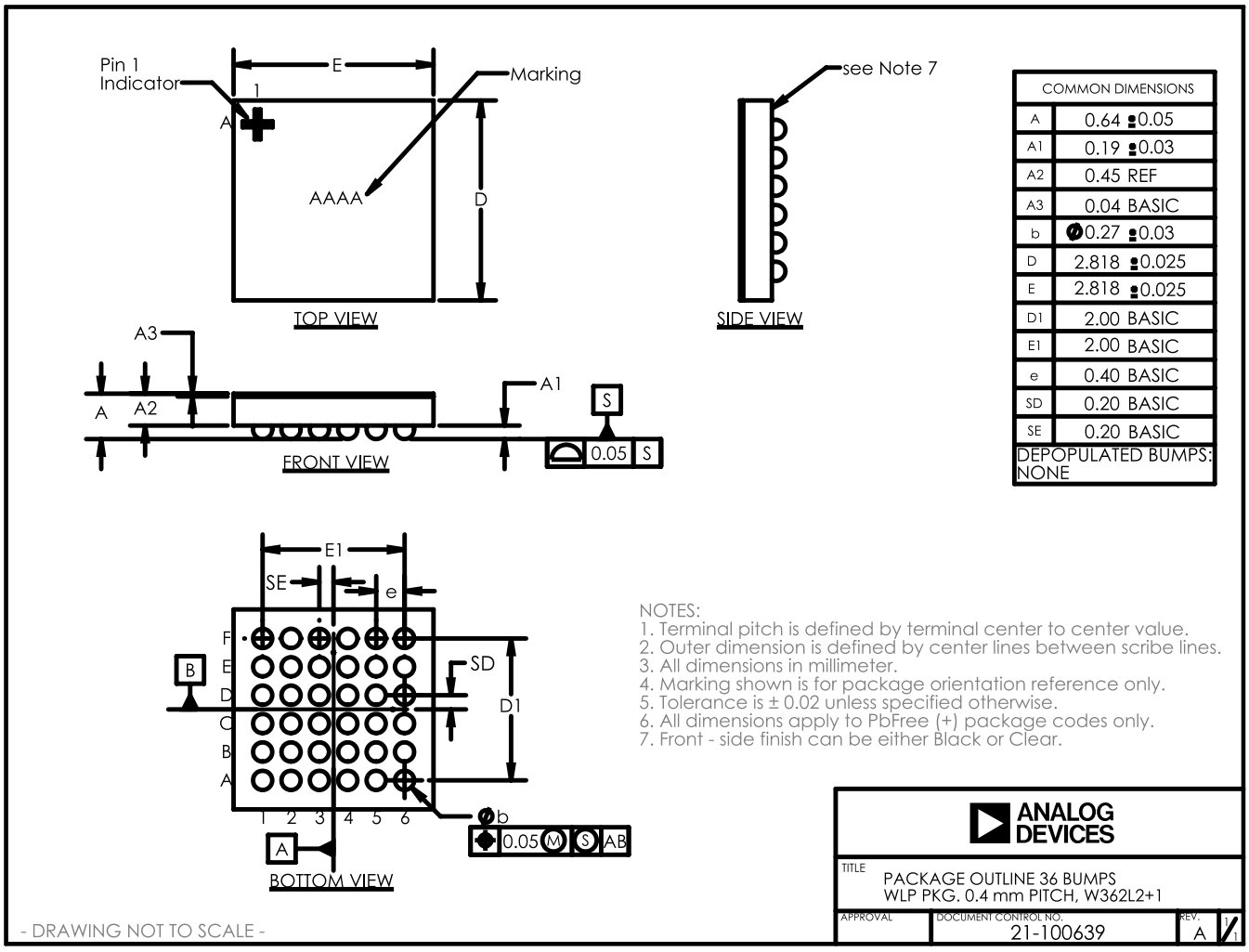
Operating Temperature Range ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W362L2+1
Outline Number	*21-100639*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	45.72°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	NA



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	⌀0.27 ±0.03
D	2.818 ±0.025
E	2.818 ±0.025
D1	2.00 BASIC
E1	2.00 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC

DEPOPULATED BUMPS: NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 36 BUMPS WLP PKG. 0.4 mm PITCH, W362L2+1

APPROVAL | DOCUMENT CONTROL NO.: 21-100639 | REV.: A | 1/1

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS						
SWITCHING MODE CHARGER						
CHGIN Voltage Range	V_{CHGIN}	Operating Voltage (*Note 1*)	V_{CHGIN_UVLO}		V_{CHGIN_OVLO}	V
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} rising	13.4	13.7	14	V
CHGIN Overvoltage Threshold Hysteresis	V_{CHGINH_OVLO}	V_{CHGIN} falling		300		mV
CHGIN to GND Minimum Turn-On Threshold Accuracy	$V_{CHGIN\ UVLO}$	V_{CHGIN} rising	4.6	4.7	4.8	V
CHGIN to SYS Minimum Turn-On Threshold	$V_{CHGIN2SYS}$	V_{CHGIN} rising	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
CHGIN Adaptive Voltage Regulation Threshold Accuracy	V_{CHGIN_REG}		4.4	4.5	4.6	V
CHGIN Quiescent Current (I_{SYS} = 0A)	I_{IN}	V_{CHGIN} = 5.0V, Charger enabled, V_{SYS} = V_{BATT} = 4.5V, (No switching, battery charged)		2.7	4	mA
	I_{IN_STBY}	STBY = H, DCDC off, V_{CHGIN} = 5V		0.2		
	I_{IN_EXTSM}	EXTSM = H(Q_{BAT} = Off), DCDC off, V_{CHGIN} = 5V, FSHIP MODE = 0		2.7		
BATT Quiescent Current (I_{SYS} = 0A)	I_{FSHIP}	FSHIP MODE = 1, V_{CHGIN} = 0V, V_{BATT} = 3.6V, Q_{BAT} is OFF, V_{SYS} = V_{DD} = 0V Factory ship mode, T_A = +25°C		3.0		µA
	I_{BATT}	I²C enabled, FSHIP MODE = 0, V_{CHGIN} = 0V, V_{BATT} = 4.5V		40	60	
CHGIN Current Limit Range	CHGIN_ILIM	Programmable, 500mA default, 25mA steps, production tested at 500mA,1000mA, and 3000mA settings only	0.1		3.2	A
CHGIN Input Current Limit	$I_{INLIMIT}$	Charger enabled, 500mA input current setting, T_A = -40°C to +85°C	480	485	500	mA
		Charger enabled, 1500mA input current setting, T_A = -40°C to +85°C	1400	1450	1500	
		Charger enabled, 3000mA input current setting, T_A = -40°C to +85°C	2800	2900	3000	
CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause CHGIN capacitor to decay from 6.0V to 4.3V		100		ms
CHGIN Input Self-Discharge Resistance	R_{INSD}			44		kΩ
CHGIN to BYP Resistance	$R_{CHGIN2BYP}$	Bidirectional		20		mΩ
LX High-Side Resistance	R_{HS}			41		mΩ

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Low-Side Resistance	R_{LS}			41		mΩ
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$			13		mΩ
CHGIN to BATT Dropout Resistance	$R_{CHGIN2BAT}$	Calculation estimates a 0.04Ω inductor resistance (R_L) $R_{CHGIN2BAT}$ = $R_{CHGIN2BYP}$ + R_{HS} + R_L + $R_{BAT2SYS}$		114		mΩ
LX Leakage Current		LvX = PGND or BYP, T_A = +25°C		0.01	10	µA
		LX = PGND or BYP, T_A = +85°C		1		
BST Leakage Current		BST = PGND or 1.8V, T_A = +25°C		0.01	10	µA
		BST = PGND or 1.8V, T_A = +85°C		1		
BYP Leakage Current		V_{BYP} = 5V, V_{CHGIN} = 0V, LX = 0V, charger Disabled, T_A = +25°C		0.01	10	µA
		V_{BYP} = 5V, V_{CHGIN} = 0V, LX = 0V, charger disabled, T_A = +85°C		1		
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +85°C		1		
Minimum ON Time	t_{ON-MIN}	Buck switching ON time		55		ns
Minimum OFF Time	$t_{OFF-MIN}$	Buck switching OFF time		55		ns
Buck Current Limit	I_{LIM}		5.16	6.0	6.84	A
Reverse Boost Quiescent Current		Non-switching: output forced 200mV above its target regulation voltage		2000		µA
Reverse Boost BYP Voltage in OTG Mode	$V_{BYP.OTG}$		4.94	5.1	5.26	V
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V < V_{BATT} < 4.5V, T_A = -40°C to +85°C	1500		1725	mA
Reverse Boost Output Voltage Ripple		Discontinuous inductor current (i.e., skip mode)		±150		mV
		Continuous inductor current		±150		
BATT Regulation Voltage Accuracy		T_A = +25°C, BATT regulation voltage	-0.7	-0.3	+0.1	%
BATT Regulation Voltage	V_{BATREG}	Programmable, 3.6V to 4.0V with 100mV steps and 4.0V to 4.55V with 10mV steps.	3.6		4.55	V
BATT Regulation Voltage Accuracy		T_A = 0°C to +85°C, BATT regulation voltage	-0.7	-0.3	+0.2	%
Fast-Charge Current Program Range		Programmable, 50mA steps Production tested at 100, 2000, 3000mA settings	0.1		3.15	A
Fast-Charge Currents	I_{FC}	T_A = -40°C to +85°C, V_{BATT} > V_{SYSMIN}, programmed for 3.0A	2850	3000	3150	mA
		T_A = -40°C to +85°C, V_{BATT} > V_{SYSMIN}, programmed for 2.0A	1900	2000	2100	
		T_A = -40°C to +85°C, V_{BATT} > V_{SYSMIN}, programmed for 0.5A	465	500	535	
Trickle Charge Threshold	$V_{TRICKLE}$	V_{BATT} rising	3.0	3.1	3.2	V
Precharge Threshold	V_{PRECHG}	V_{BATT} rising	2.4	2.5	2.6	V

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to both $V_{TRICKLE}$ and V_{PRECHG}		100		mV
Trickle Charge Current	$I_{TRICKLE}$	$I_{TRICKLE}$ for termination voltage from 4.1V to 4.5V option; trickle charge is disabled for 3.6V option	270	300	330	mA
Precharge Charge Current	I_{PRECHG}		40	55	80	mA
Charger Restart Threshold	V_{RSTRT}		50	100	150	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time		130		ms
Top-Off Current Program Range	I_{TO}	Programmable from 50mA to 350mA in 20mA steps	50		350	mA
Top-Off Current Accuracy		Programmed for 150mA, T_A = -40°C to +85°C	130	150	170	mA
		Programmed for 50mA, T_A = -40°C to +85°C	25	50	75	
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time		30		ms
Charger Soft-Start Time	t_{SS}			1.5		ms
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 10mA		70		mV
		Load regulation during the reverse regulation mode		1		mV/A
Minimum SYS Voltage	V_{SYSMIN}	For termination voltage from 4.1V to 4.5V		3.5		V
		For 3.6V termination voltage		3.0		
Minimum SYS Voltage Accuracy			-3		3	%
Prequalification Time	t_{PQ}	Applies to both low-battery precharge and trickle modes		30		min
Fast-Charge Constant Current Plus Fast-Charge Constant Voltage Time	t_{FC}	Programmable from 3hrs, 4hrs, 5hrs, 6hrs, 7hrs, 8hrs, 10hrs including a disable, 6hrs default		6		hours
Top-Off Time	t_{TO}	Programmable from 30s to 70min in 10min steps		30		s
Timer Accuracy			-20		20	%
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{JREG}	Junction temperature when charge current is reduced		130		°C
Thermal Regulation Gain	A_{TJREG}	I_{FC} = 3.15A		-157.5		mA/°C
THM Threshold, COLD	THM_COLD	V_{THM}/V_{PVL} rising, 1% hysteresis (thermistor temperature falling)	73.36	74.56	75.76	%
THM Threshold, COOL	THM_COOL	V_{THM}/V_{PVL} rising, 1% hysteresis (thermistor temperature falling)	58.8	60	61.2	%
THM Threshold, WARM	THM_WARM	V_{THM}/V_{PVL} falling, 1% hysteresis (thermistor temperature rising)	33.68	34.68	35.68	%
THM Threshold, HOT	THM_HOT	V_{THM}/V_{PVL} falling, 1% hysteresis (thermistor temperature rising)	21.59	22.5	23.41	%

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THM Input Leakage Current		V_{THM} = GND or V_{PVL}; T_A = +25°C		0.1	1	µA
		V_{THM} = GND or V_{PVL}; T_A = +85°C		0.1		
Battery Overcurrent Threshold	I_{BOVCR}			6.0		A
Battery Overcurrent Debounce Time	t_{BOVRC}		6			ms
Battery Overcurrent Retry	t_{OCP_RETRY}			0.15		sec
Battery Overcurrent Protection Quiescent Current	I_{BOVRC}			3 + I_{BATT}/18040		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} Rising, 100mV hysteresis	1.9	2.0	2.1	V
SYS Undervoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_UVLO\_R}$		2.74	2.8	2.86	V
SYS Undervoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_UVLO\_F}$		2.45	2.50	2.55	V
SYS Undervoltage-Lockout Hysteresis	$V_{SYS\_UVLO\_H}$			300		mV
SYS Overvoltage-Lockout Threshold (SYS Rising)	$V_{SYS\_OVLO\_R}$		5.35	5.425	5.50	V
SYS Overvoltage-Lockout Threshold (SYS Falling)	$V_{SYS\_OVLO\_F}$		5.20	5.275	5.35	V
SYS Overvoltage-Lockout Hysteresis	$V_{SYS\_OVLO\_H}$			150		mV
INOKB, STAT1, STAT2						
Logic Input Leakage Current				0.1	1	µA
Output Low Voltage INOKB, STAT1, STAT2	V_{OL}	I_Z = 5mA, T_A = +25°C			0.4	V
Output High Leakage INOKB, STAT1, STAT2		V_{SYS} = 5.5V, T_A = +25°C	-1	0	1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
INTB						
Logic Input Leakage Current				0.1	1	µA
Output Low Voltage INTB	V_{OL}	I_{SOURCE} = 1mA, T_A = +25°C			0.4	V
Output High Leakage INTB	I_{INTB}	V_{SYS} = 5.5V, T_A = +25°C	-1	0	1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
STBY						
Logic Input Low Threshold	V_{IL}				0.4	V
Logic Input High Threshold	V_{IH}		1.4			V

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input Leakage Current	I_{STBY}	V = 5.5V (including current through pulldown resistor)		24	60	µA
Pulldown Resistor	R_{STBY}			235		kΩ
EXTSM						
Logic Input Low Threshold	V_{IL}				0.3 x V_{BATT}	V
Logic Input High Threshold	V_{IH}		0.7 x V_{BATT}			V
Logic Input Leakage Current	I_{EXTSM}	V = 5.5V (including current through pulldown resistor)		24	60	µA
Pulldown Resistor	R_{EXTSM}			235		kΩ
CHARGER DETECTION						
BC1.2 State Timeout	t_{TMO}		180	200	220	ms
Data Contact Detect Time-Out	t_{DCDtmo}		700	800	900	ms
Proprietary Charger Debounce	t_{PRDeb}		5	7.5	10	ms
Primary to Secondary Timer	$t_{PDSDWait}$		27	35	39	ms
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
V_{BUS64} Threshold	V_{BUS64}	DP and DN pins. Threshold in percent of VBUS voltage 3V < V_{BUS} < 5.5V	57	64	71	%
V_{BUS64} hysteresis	V_{BUS64_H}			0.015		V
V_{BUS47} Threshold	V_{BUS47}	DP and DN pins. Threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V	43.3	47	51.7	%
V_{BUS47} hysteresis	V_{BUS47_H}			0.015		V
V_{BUS31} Threshold	V_{BUS31}	DP and DN pins. Threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V	26	31	36	%
V_{BUS31} hysteresis	V_{BUS31_H}			0.015		V
I_{WEAK} Current	I_{WEAK}		0.01	0.1	0.5	µA
R_{DM_DWN} Resistor	R_{DM_DWN}		14.25	20	24.8	kΩ
I_{DP_SRC} Current	I_{DP_SRC} / I_{DCD}	Accurate over 0V to 2.5V	7	10	13	µA
I_{DM_SINK} Current	I_{DM_SINK} / $I_{DATSINK}$	Accurate over 0.15V to 3.6V	45	80	125	µA
V_{LGC} threshold	V_{LGC}		1.62	1.7	1.9	V
V_{LGC} hysteresis	V_{LGC_H}			0.015		V
V_{DAT_REF} threshold	V_{DAT_REF}		0.25	0.32	0.4	V
V_{DAT_REF} hysteresis	$V_{DAT\_REF\_H}$			0.015		V
V_{D33} Voltage			2.6	3.0	3.4	V
V_{DN_SRC} Voltage	V_{DN_SRC} / V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DP_SRC} Voltage	V_{DP_SRC} / V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V

(V_{CHGIN} = 5.0V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMP2 Load Resistor	R_{USB}	Load Resistor on DP/DN	3	6.1	12	MΩ
CC DETECTION						
CC Pin Voltage in DFP 1.5A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load. IDFP1.5_CC enable and V_{AVL} ≥ 2.5V	1.85			V
CC Pin Clamp Voltage	V_{CC_ClAMP}	60µA ≤ $I_{CC\_}$ ≤ 600µA		1.1	1.32	V
CC Pin Clamp Voltage (5.5V)		$I_{CC\_}$ < 2mA		5.25	5.5	V
CC UFP Pulldown Resistance	R_{PD_UFP}		-10%	5.1k	10%	Ω
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC}$		-20%	80	20%	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$		-8%	180	8%	µA
CC RA RD Threshold	$V_{RA\_RD0.5}$		0.15	0.2	0.25	V
CC UFP 0.5A RD Threshold	$V_{UFP\_RD0.5}$		0.61	0.66	0.7	V
CC UFP 0.5A RD Hysteresis	$V_{UFP\_RD0.5\_H}$			0.015		V
CC UFP 1.5A RD Threshold	$V_{UFP\_RD1.5}$		1.16	1.23	1.31	V
CC UFP 1.5A RD Hysteresis	$V_{UFP\_RD1.5\_H}$			0.15		V
CC Pin Power-Up Time	$t_{ClampSwap}$	Max time allowed from removal of voltage clamp till 5.1k resistor attached			15	ms
CC Detection Debounce	t_{CCDeb}		100	119	200	ms
Type-C Debounce	t_{PDDeb}		10	15	20	ms
Type-C Quick Debounce	t_{QDeb}		0.9	1	1.1	ms
Type-C Error Recovery	$t_{ErrorRecovery}$		25			ms

Note 1: The CHGIN input must be less than V_{CHGIN_OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn on.

I²C Electrical Characteristics

(V_{VIO} = +1.8V, T_A = -40°C to +85°C)

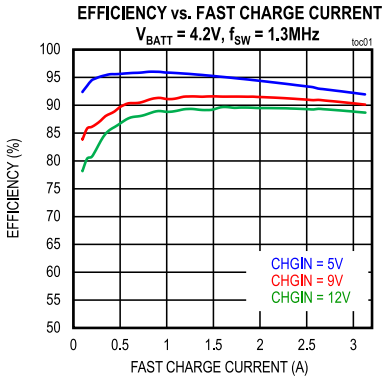
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA AND SCL I/O STAGE						
SCL, SDA Input Low Level		T_A = +25°C			0.3 x V_{VIO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 x V_{VIO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x V_{VIO}		V
SCL, SDA Logic Input Current		V_{SCL} = V_{SDA} = V_{VIO} = 1.8V	-10		+10	µA
SCL, SDA Input capacitance				10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter				50		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup Time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns

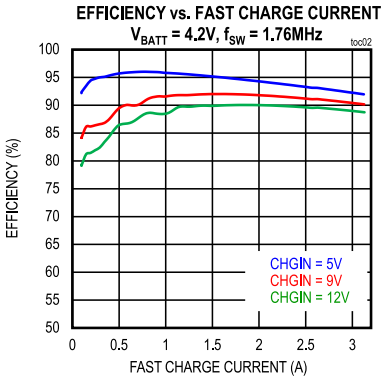
(V_{VIO} = +1.8V, T_A = -40°C to +85°C)

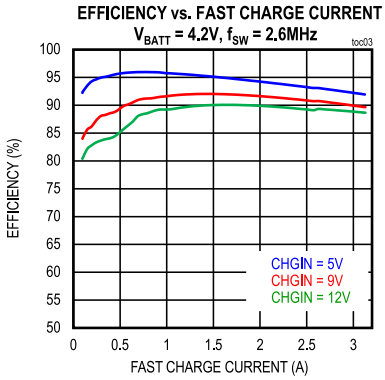
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Setup Time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter				10		ns

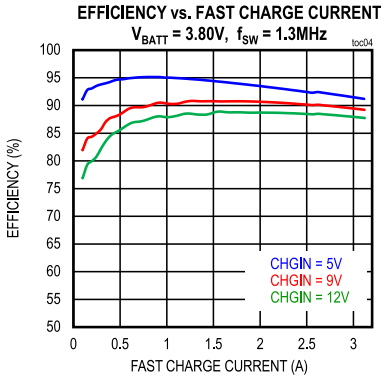
Typical Operating Characteristics

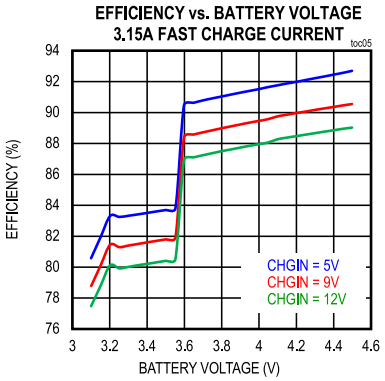
(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = +25°C, unless otherwise noted.

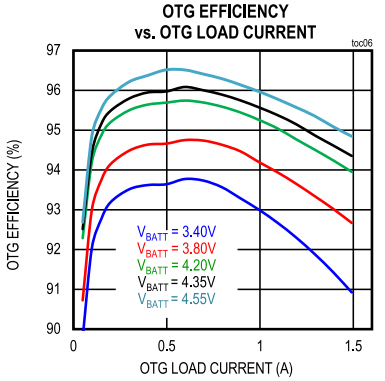


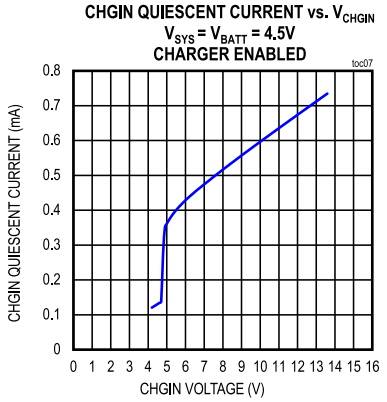


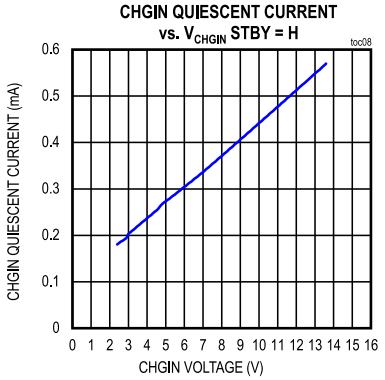


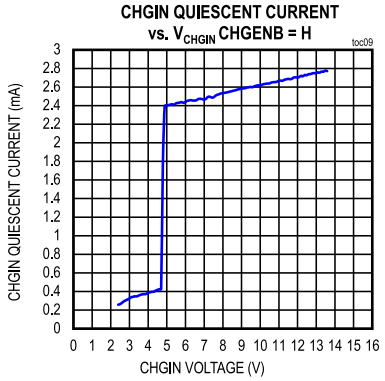






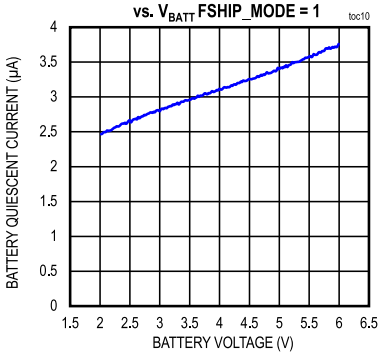




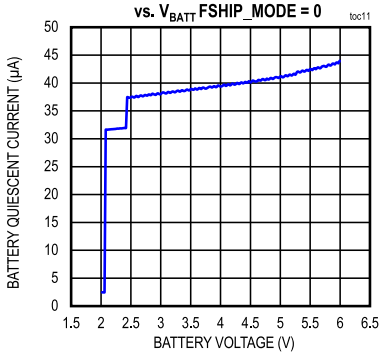


(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = +25°C, unless otherwise noted.

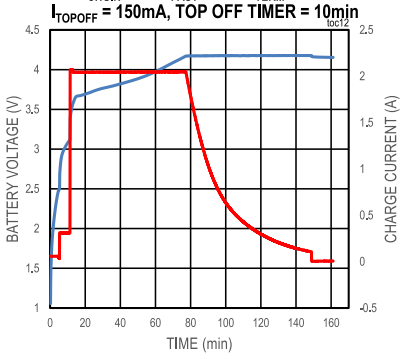
BATTERY QUIESCENT CURRENT vs. V_{BATT} FSHIP_MODE = 1



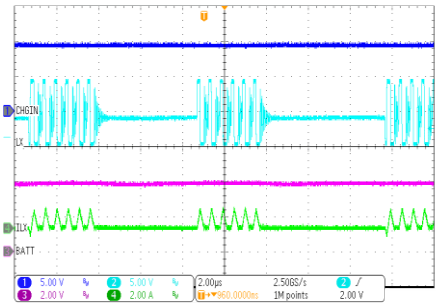
BATTERY QUIESCENT CURRENT vs. V_{BATT} FSHIP_MODE = 0



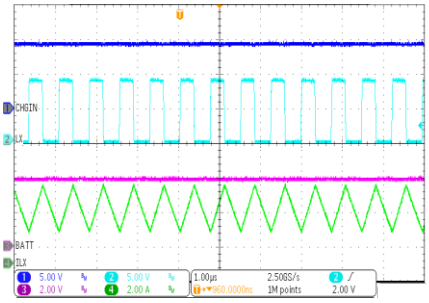
CHARGE PROFILE
V_{CHGIN} = 5V, I_{FAST} = 2A, V_{TERM} = 4.2V
I_{TOPOFF} = 150mA, TOP OFF TIMER = 10min



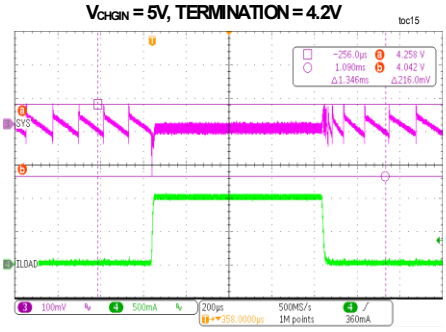
SWITCHING WAVEFORM
V_{CHGIN} = 9V, SYS LOAD CURRENT = 0.15A



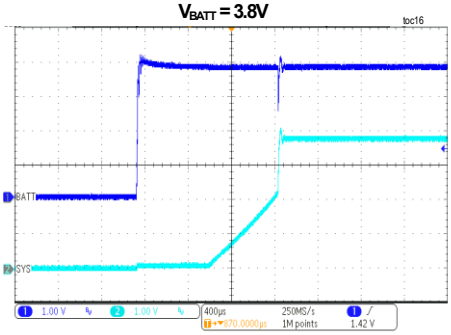
SWITCHING WAVEFORM
V_{CHGIN} = 9V, SYS LOAD CURRENT = 3.15A



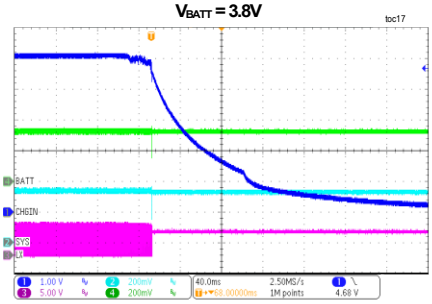
SYS LOAD TRANSIENT RESPONSE
V_{CHGIN} = 5V, TERMINATION = 4.2V



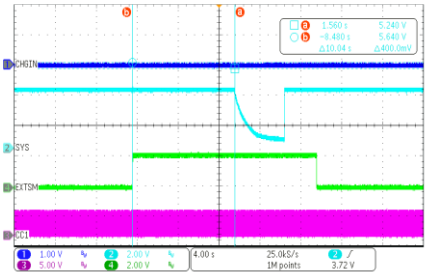
INPUT INSERTION
V_{BATT} = 3.8V



CHGIN REMOVAL WHILE CHARGING
V_{BATT} = 3.8V

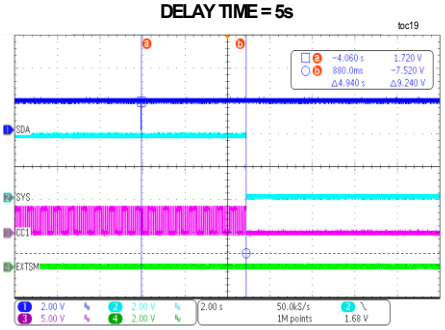


EXTSM
SYSTEM RESET (PUSH BUTTON)

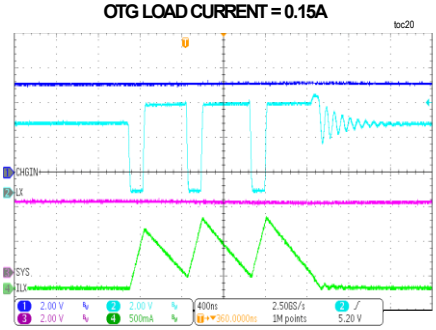


(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = +25°C, unless otherwise noted.

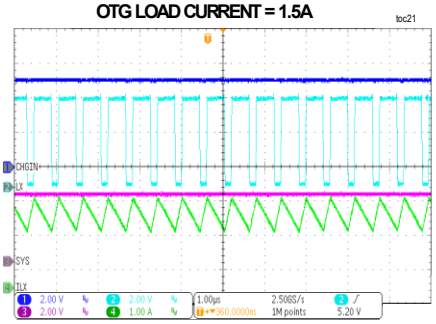
ENTERING FSHIP MODE DELAY TIME = 5s



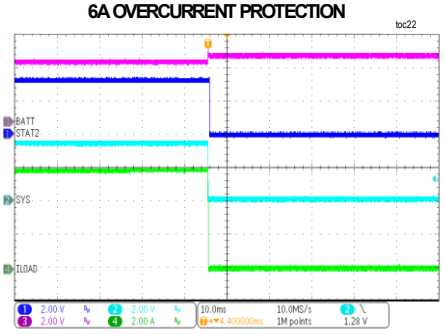
BOOST SWITCHING WAVEFORM OTG LOAD CURRENT = 0.15A



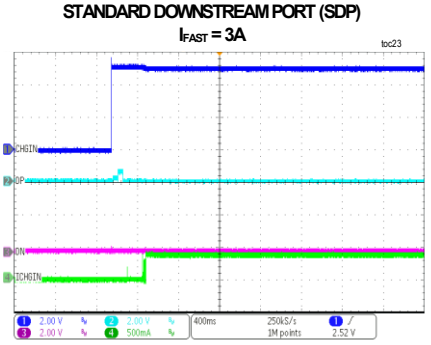
BOOST SWITCHING WAVEFORM OTG LOAD CURRENT = 1.5A



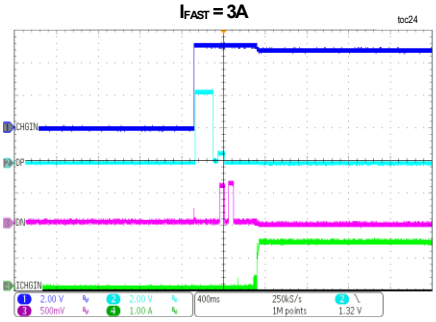
6A OVERCURRENT PROTECTION



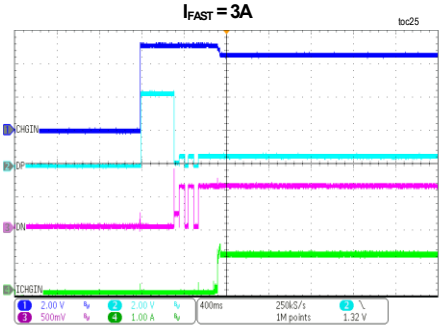
CHARGER DETECTION STANDARD DOWNSTREAM PORT (SDP) I_{FAST} = 3A



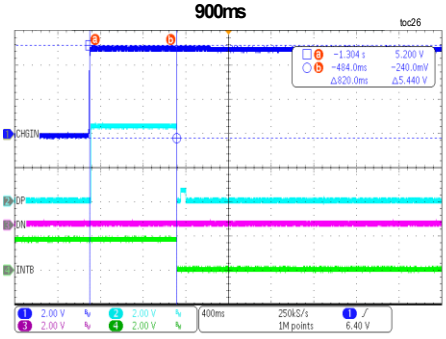
CHARGER DETECTION CHARGING DOWNSTREAM PORT (CDP) I_{FAST} = 3A



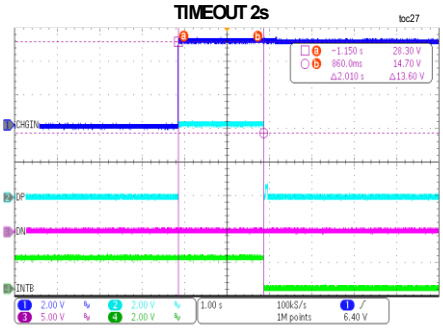
CHARGER DETECTION DEDICATED CHARGING PORT (DCP) I_{FAST} = 3A



CHARGER DETECTION DATA CONTACT DETECT TIMEOUT 900ms

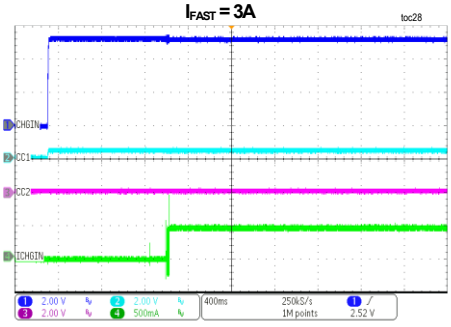


CHARGER DETECTION DATA CONTACT DETECT TIMEOUT 2s

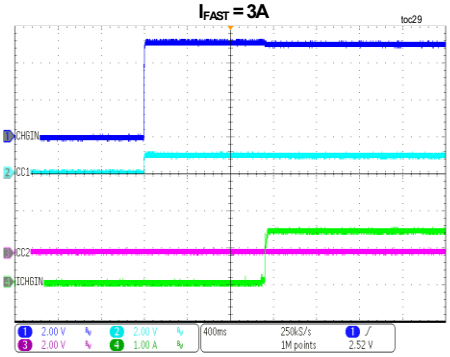


(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = +25°C, unless otherwise noted.

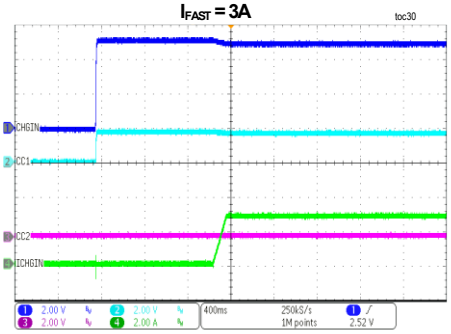
USB TYPE-C DETECTION SOURCE CAPABILITY 500mA
I_{FAST} = 3A



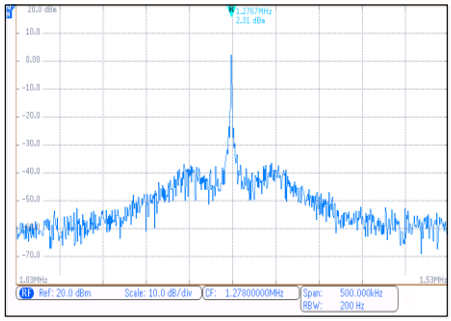
USB TYPE-C DETECTION SOURCE CAPABILITY 1500mA
I_{FAST} = 3A



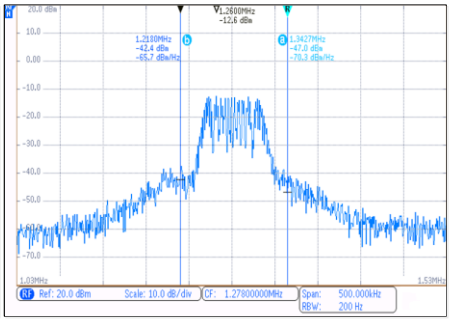
USB TYPE-C DETECTION SOURCE CAPABILITY 3000mA
I_{FAST} = 3A



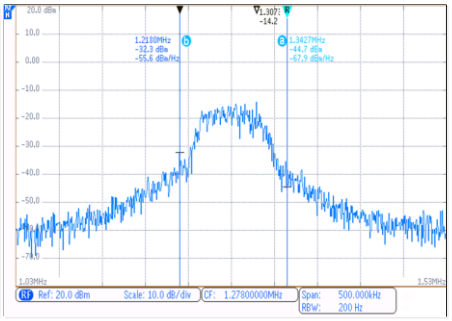
WITHOUT SPREAD SPECTRUM WAVEFORM
FSW = 1.3MHz



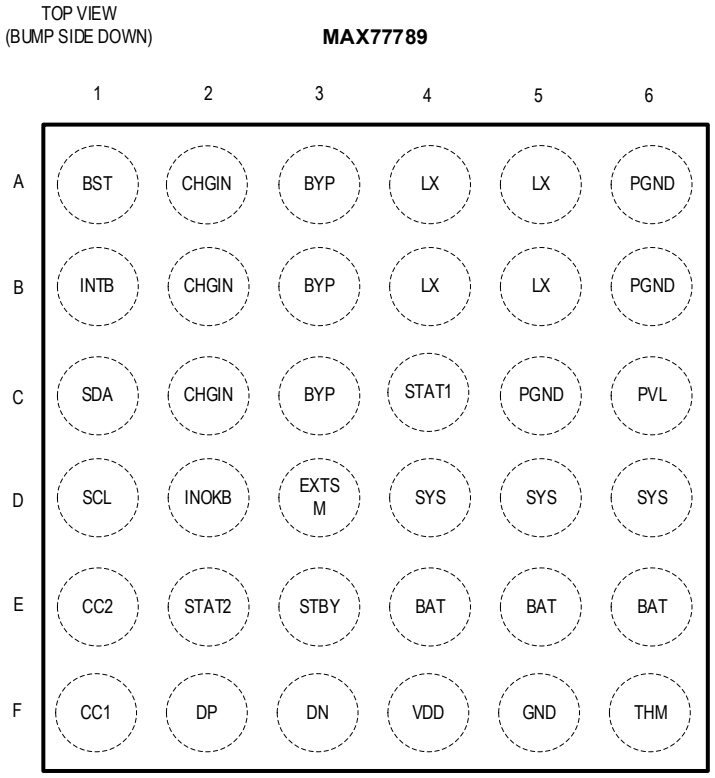
SPREAD SPECTRUM WAVEFORM
FSW = 1.3MHz, LINEAR, ±6%



SPREAD SPECTRUM WAVEFORM
FSW = 1.3MHz, PSEUDO RANDOM, ±6%



Pin Configuration

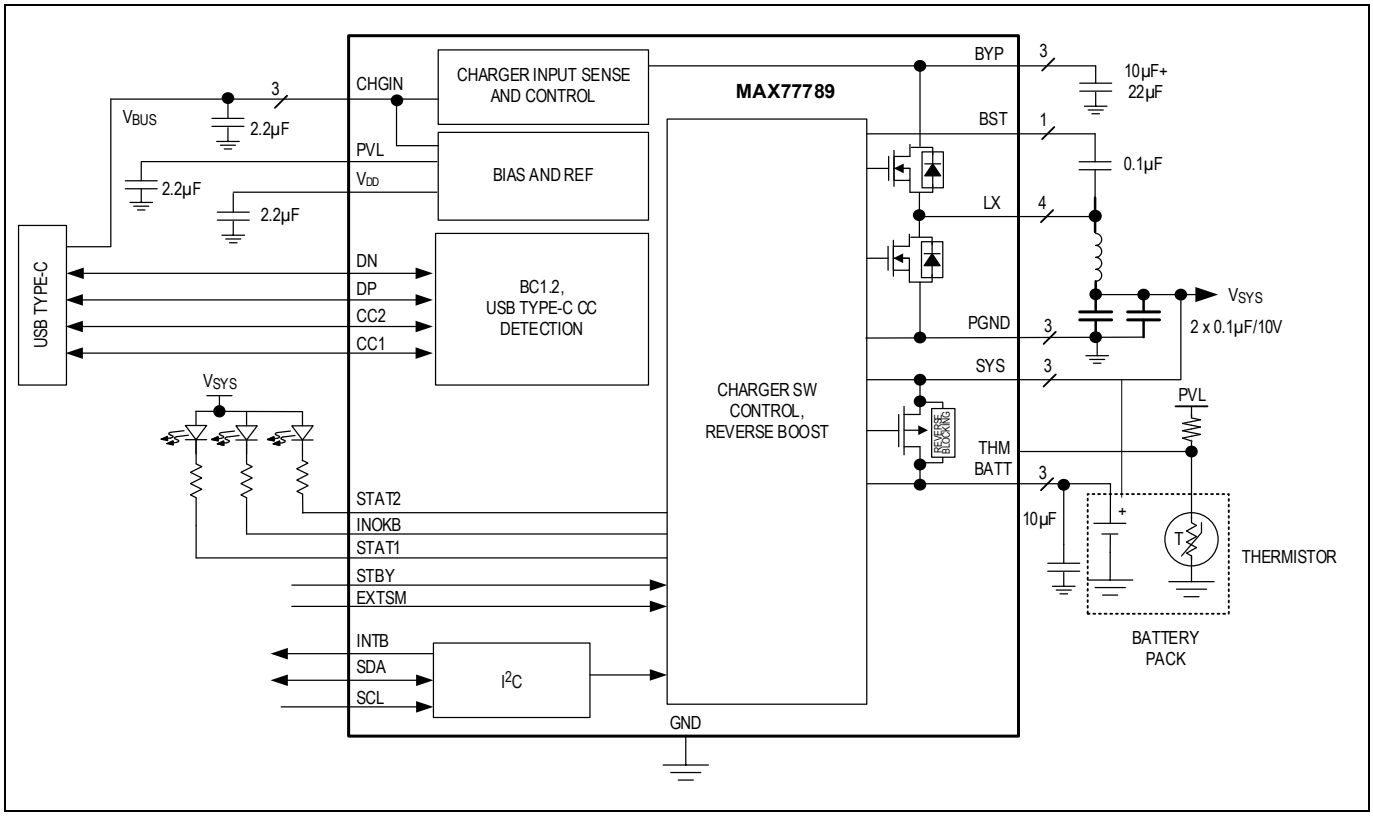


WLP
(2.85mm x 2.85mm, 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION
A1	BST	Provides Drive to High-Side Internal nMOS. Connect a 100nF/6.3V bootstrap capacitor between this pin and the LX node.
D2	INOKB	Charger Input Valid, Active-Low Logic Output Flag. The open-drain output indicates when a valid voltage is present at CHGIN.
C4	STAT1	Open-Drain Charge Status Indication Output. STAT is toggling low and high impedance during charge. STAT becomes low when top-off threshold is detected and in a done state. STAT becomes high impedance when charge faults happen.
E1	CC2	USB Type-C CC2 Connection
F1	CC1	USB Type-C CC1 Connection
F2	DP	Positive Line of the USB Data Line Pair. Connect to D+ on USB Type-C or micro USB connector.
F3	DN	Negative Line of the USB Data Line Pair. Connect to D- on USB Type-C or micro USB connector.
E2	STAT2	FAULT Indication and Charger type detection complete Active-Low
F5	GND	Analog Ground. Short to ground plane.
F4	V_{DD}	Output of On-Chip LDO Used to Power On-Chip, Low-Noise Circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND. Powering external loads from V_{DD} is not recommended other than pullup resistors.
F6	THM	Thermistor connection. Connect an external negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to PVL. See the *JEITA Compliance* for details.
B1	INTB	Active-Low, Open-Drain Interrupt Output. Connect a pullup resistor to the pullup power source.
E4, E5, E6	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li-ion battery. Bypass BATT to PGND ground plane with a 10µF ceramic capacitor.
D4, D5, D6	SYS	System Power Node. Bypass SYS to PGND with a 2 x 10µF/10V ceramic capacitor.
C6	PVL	Output of On-Chip LDO, Noisy Rail due to Bootstrap Operation. Bypass with a 2.2µF/10V ceramic capacitor to PGND. Powering external loads from PVL is not recommended.
A6, B6, C5	PGND	Power Ground. Connect the return of the buck output capacitor close to these pins.
A4, A5, B4, B5	LX	Switching Node. Connect an inductor between LX and SYS. When the buck converter is enabled, LX switches between BYP and PGND to control the input current, battery current, battery voltage, and die temperature.
A3, B3, C3	BYP	System Power Connection. Output of OVP adapter input block and input to switching charger. Bypass with a 22µF/16V ceramic capacitor from BYP to PGND.
A2, B2, C2	CHGIN	Charger Input. Up to 13.4V operating, 16VDC withstand input pin connected to an adapter or USB power source. Connect a 2.2µF/16V ceramic capacitor from CHGIN to GND.
C1	SDA	Serial Interface I^2C Data. Open-Drain output
D3	EXTSM	Active-High Ship Mode Exit Pin System Reset Pin
E3	STBY	Active-High Input. Connect high to disable the DCDC between CHGIN input and SYS output. CHGIN supply current reduces to I_{CHGIN_STBY}. The battery supplies the system power. Connect low to control the DCDC with the power path-state machine.
D1	SCL	Serial Interface I^2C Clock Input

Functional Diagram



Detailed Description

The MAX77789 is a highly integrated USB Type-C charger with I2C configuration. The IC can operate input range from 4.6V to 13.4V to support 5V, 9V, and 12V AC adapter and USB input. The fast-charge current is up to 3.15A and the max input current limit is 3.0A.

The IC can run BC1.2 and USB Type-C CC detection upon input insertion and configure the input source to max power option and charger input current limit to max power as a default operation and all the configurations that are set by detection results automatically can be overridden by the system MCU. *Table 1* shows BC1.2's typical detection timings and input current limits. TOC23 to TOC27 are the scope shots showing the timing from CHGIN insertion to charging starts or data contact detect timeout interrupt.

Table 1. BC1.2 Detection Timing and Input Current Limit

PORT TYPE	TYPICAL DETECTION TIME (ms)	INPUT CURRENT LIMIT (A)
SDP	144	0.5
CDP	230	1.5
DCP	230	1.5
Data Time Out	807/2010	3

Fast-charge current and top-off current threshold are programmable. Input voltage regulation feature (AICL) even allows users to use weak AC adapters without preventing charging.

Power path design provides system power even when battery is fully discharged, and it automatically supplements current from the battery when the system demands higher current than that of input power source capable.

Reverse boost from the battery can be enabled by setting the charger mode of 0x0A to allow 5.1V/1.5A OTG to V_{BUS} or BYP. In default operation, reverse boost enables automatically when a source device is detected because of DRP operation.

Top System Management

SYS Under Lock Out

Switching Mode Charger

Features

- Complete Li+/LiPoly/LiFePO$_4$ Battery Charger
  - Prequalification, Constant Current, Constant Voltage
  - 55mA Precharge Current
  - 300mA Trickle Charge Current for Charge Termination Voltage from 3.6V to 4.55V
  - 100mA to 3.15A Constant Current Charge
  - Battery Regulation Voltage 3.6V to 4.55V
    - -0.7%/+0.1% Accuracy at +25°C
    - -0.7%/0.2% Accuracy from 0°C to 85°C
- Synchronous Switch-Mode Based Design
- 3.0µA Battery Leakage Current in SHIP Mode
- Smart Power Selector
  - Optimally Distributes Power Between the Charge Adapter, System, and Main Battery
  - When Powered by a Charge Adapter, the Main Battery can Provide Supplemental Current to the System
  - The Charge Adapter can Support the System without the Main Battery
- No External MOSFETs Required
- Single Input Operation
  - Reverse Leakage Protection (Prevents the Battery Leaking Current to the Inputs)
  - V_{CHGIN_OVLO} = 13.4V
  - Supports AC-to-DC Wall Adapters
  - Programmable Input Current Limit Selection
- Programmable Charging Safety Timer
- Die Temperature Monitor with Thermal Foldback Loop
  - Die Temperature Thresholds: 130°C
- Input Voltage Regulation Allows Operation from High-Impedance Sources (AICL)
- BATT to SYS Switch is 20mΩ Typical
  - Capable of 4.5A Steady-State Operation from BATT to SYS
- Short-Circuit Protection
  - BATT to SYS Overcurrent Threshold: 6A
  - SYS Short-to-Ground
    - Buck Operates with Input Current Limit to 200mA when $V_{SYS} < V_{SYSPU}$

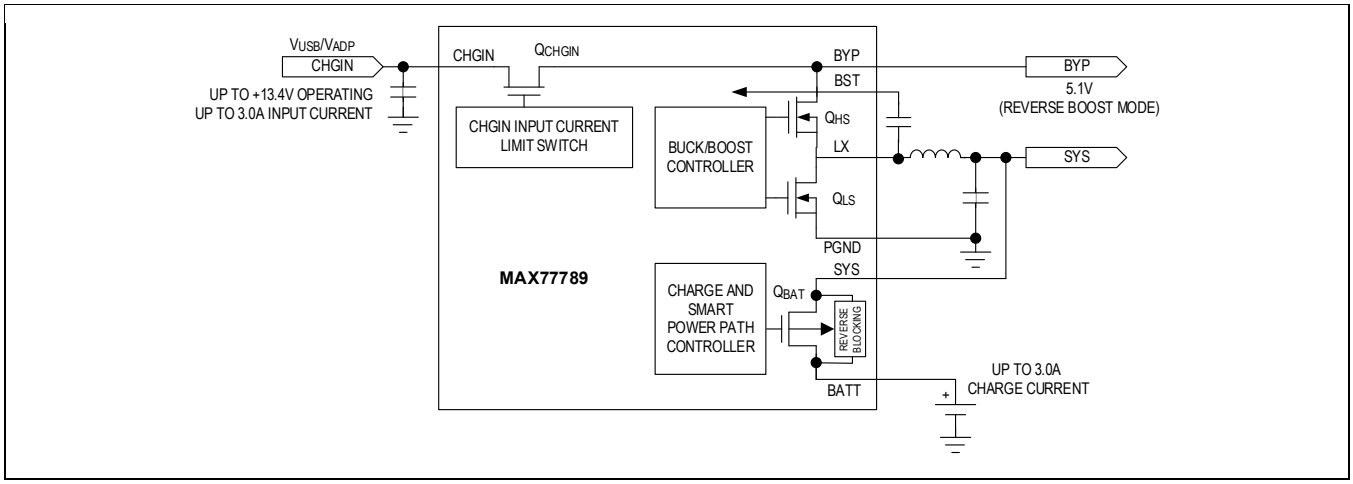


Figure 1. Simplified Functional Diagram

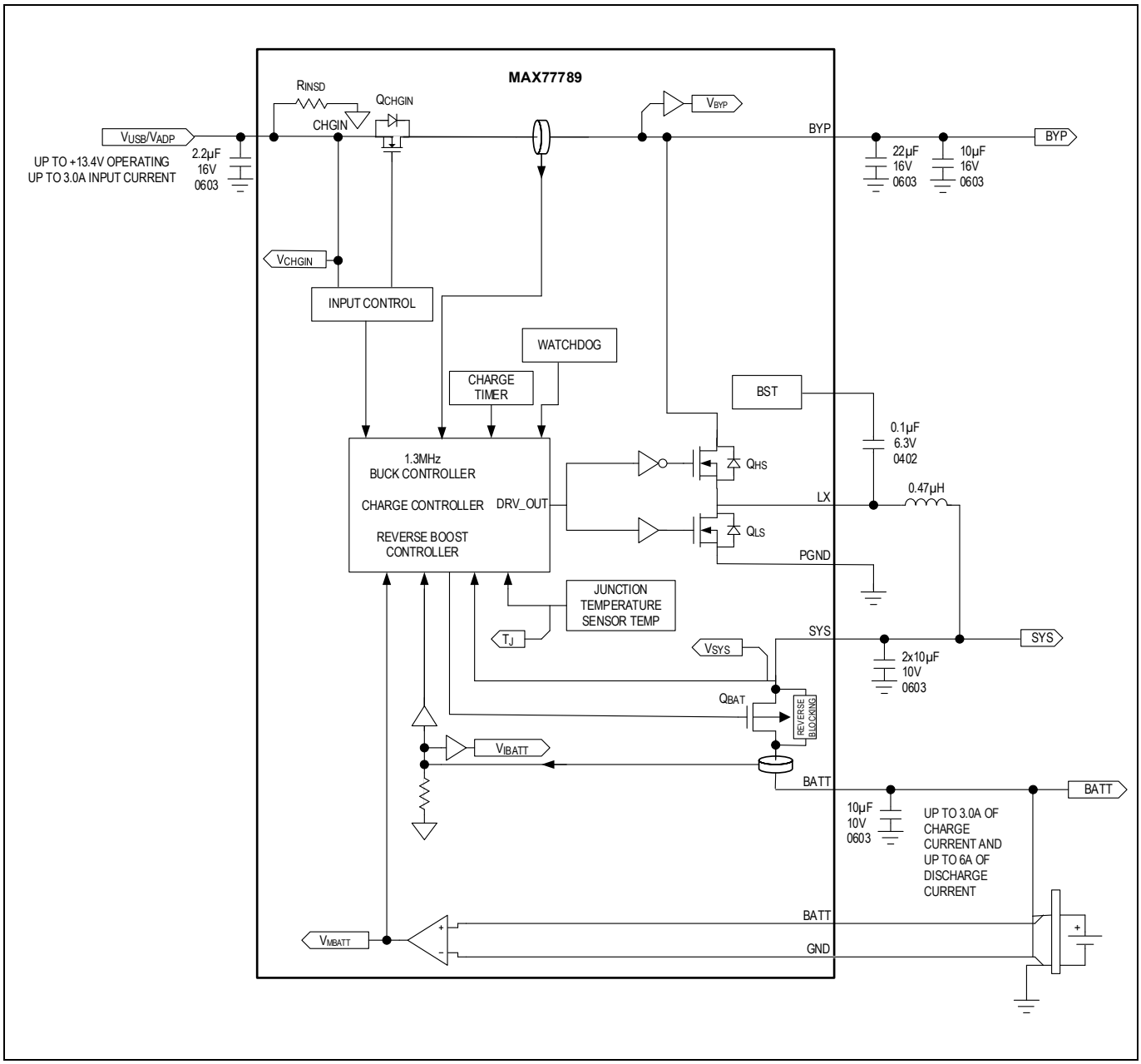


Figure 2. Main Battery Charger Detailed Functional Diagram

Detailed Description

The IC is a switch-mode charger for a one-cell lithium-ion (Li+), and lithium polymer (Li-polymer), or $LiFePO_4$ battery. As shown in *Figure 2*, the current limit for CHGIN input is configured allowing the flexibility to connect to either an AC-to-DC wall charger or a USB port.

The synchronous switch-mode DC-DC converter utilizes a high 1.3MHz switching frequency, which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery, the converter operates as a buck. The DC-DC buck operates from a 4.3V to 13.4V source and delivers up to 3.15A to the battery. The battery charge current is programmable from 100mA to 3.15A.

As a boost converter, the DC-DC uses energy from the main battery to boost the voltage at BYP. The boosted BYP voltage is used to supply the USB OTG voltage which is fixed to 5.1V.

Maxim Integrated's Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to buck current limit from the buck to the system. (Additionally, supplement mode provides additional current from the battery to the system up to B2SOVRC.) Adapter power that is not used for the system is used to charge the battery. All power switches for charging and switching the system load between the battery and adapter power are included on-chip—no external MOSFETs are required.

Maxim Integrated's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The total dropout resistance from adapter power input to the battery is 165mΩ (typ), assuming that the inductor has 0.04Ω of ESR. This 165mΩ typical dropout resistance allows for charging a battery up to 3.0A from a 5V supply. The resistance from the BATT-to-SYS node is 20mΩ, allowing for low power dissipation and long battery life.

A multitude of safety features ensures reliable charging. Features include a charge timer, junction thermal regulation, over/undervoltage protection, and short circuit protection.

The BATT-to-SYS switch has overcurrent protection (See the *Main Battery Overcurrent Protection During System Power-Up* section for more information).

Smart Power Selector (SPS)

The SPS architecture is a network of internal switches and control loops that distributes energy between external power sources CHGIN, BYP, SYS, and BATT.

Figure 1 shows a simplified arrangement for the smart power selector's power steering switches. *Figure 2* shows a more detailed arrangement of the smart power selector switches and with the following names: Q_{CHGIN}, Q_{HS}, Q_{LS}, and Q_{BAT}.

Switch and Control Loop Descriptions

- CHGIN Input Switch: Q_{CHGIN} provides the input overvoltage protection of +16V. The input switch is either completely on or completely off. As shown in *Figure 2*, there are SPS control loops that monitor the current through the input switches as well as the input voltage.
- DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.
- Battery-to-System Switch: Q_{BAT} controls the battery charging and discharging. Additionally, Q_{BAT} allows the battery to be isolated from the system (SYS). An SPS control loop monitors the Q_{BAT} current.

SYS Regulation Voltage

- When the DC-DC is enabled as a buck and the charger is enabled but in a non-charging state such as done, thermal shutdown, or timer fault, V_{SYS} is regulated to $V_{BATTREG}$ and Q_{BAT} is off.
- When the DC-DC is enabled as a buck and charging in trickle-charge, fast-charge, or top-off modes, V_{SYS} is regulated to V_{SYSMIN} when the $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$. And, when the DC-DC is enabled as a buck and charging in precharge mode ($V_{BATT} < V_{PRECHG}$), V_{SYS} is regulated to $V_{BATTREG}$. In these modes, the Q_{BAT} switch acts as a linear regulator and dissipates power ($P = (V_{SYS} - V_{BATT}) \times I_{BATT}$). When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} + I_{BATT} \times R_{BAT2SYS}$. In this mode, the Q_{BAT} switch is closed.

In all of the above modes, if the combined SYS loading exceeds the input current limit, then V_{SYS} drops to $V_{BATT} - V_{BSREG}$, and the battery provides supplemental current.

Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three characteristics to be valid:

- CHGIN must be above V_{CHGIN_UVLO} to be valid. Once CHGIN is above UVLO threshold, the information (together with LIN2SYS, described as follows) is latched and only can be reset when charger is in adaptive input current loop (AICL) and input current is lower than the IULO threshold of 60mA. Note that V_{CHGIN_REG} is lower than their UVLO falling threshold, respectively.
- CHGIN must be below its overvoltage lockout threshold (V_{CHGIN_OVLO}).
- CHGIN must be above the system voltage by $V_{CHGIN2SYS}$.

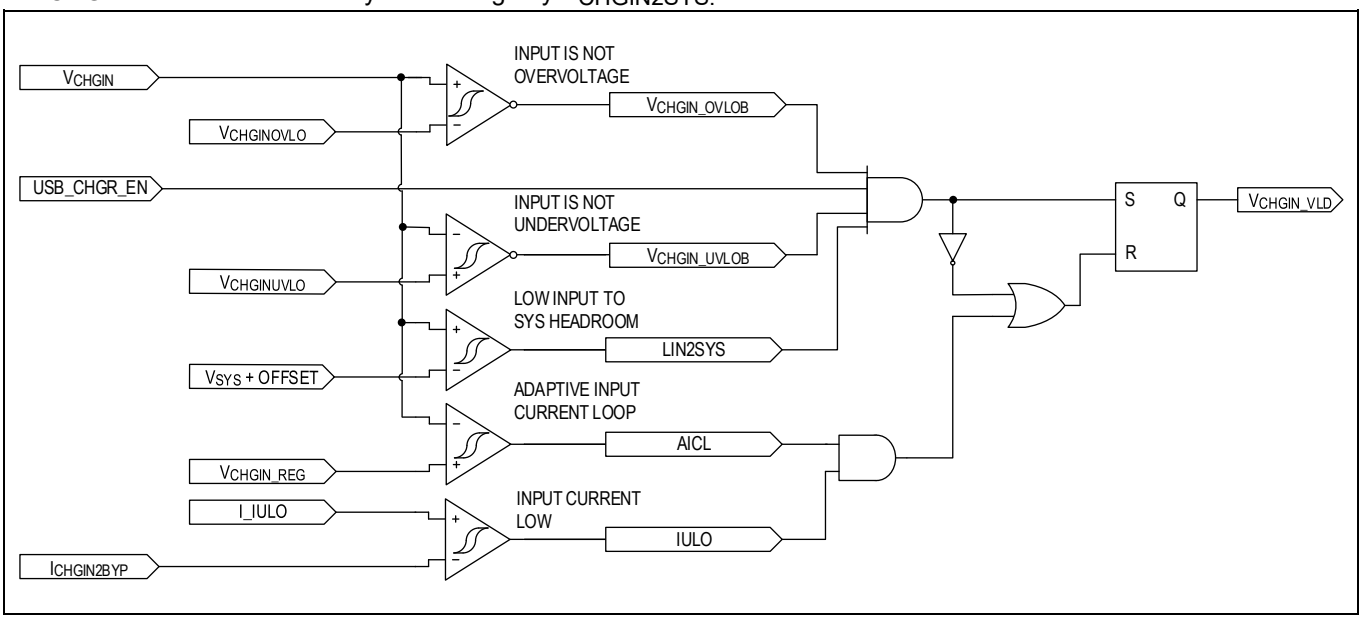


Figure 3. CHGIN Valid Signal Generation Logic

INOKB pin is pulled down when CHGINOK = 1 and the switcher starts.

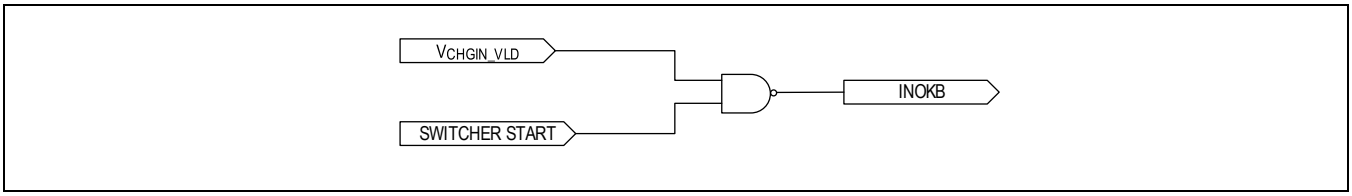


Figure 4. INOKB Signal Generation Logic

Input Current Limit

The default settings of the CHGIN_ILIM and MODE controls bits are such that when a charge source is applied to CHGIN, the MAX77789 will turn its DC-DC converter on in BUCK mode, limit V_{SYS} to $V_{BATTREG}$, and limit the charge source current to IINLIM.

Input Voltage Regulation Loop

An input voltage regulation loop allows the charger to function well when it is attached to a poor-quality charge source. The loop improves performance with relatively high resistance charge sources that exist when long cables are used or devices are charged with non-compliant USB hub configurations.

The input voltage regulation loop automatically reduces the input current limit to keep the input voltage at V_{CHGIN_REG}. If the input current limit is reduced to I_{ULO} threshold (60mA) and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off.

Input Self-Discharge

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed the input voltage decays below the UVLO threshold in a reasonable time (t_{INSD}). The input self-discharge is implemented with a 44kΩ resistor (R_{INSD}) from CHGIN input to ground.

Charger States

The MAX77789 utilizes several charging states to safely and quickly charge batteries, as shown in *Figure 5* and *Figure 6*. *Figure 5* shows an exaggerated view of the Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature: precharge → trickle → fast-charge → top-off → done.

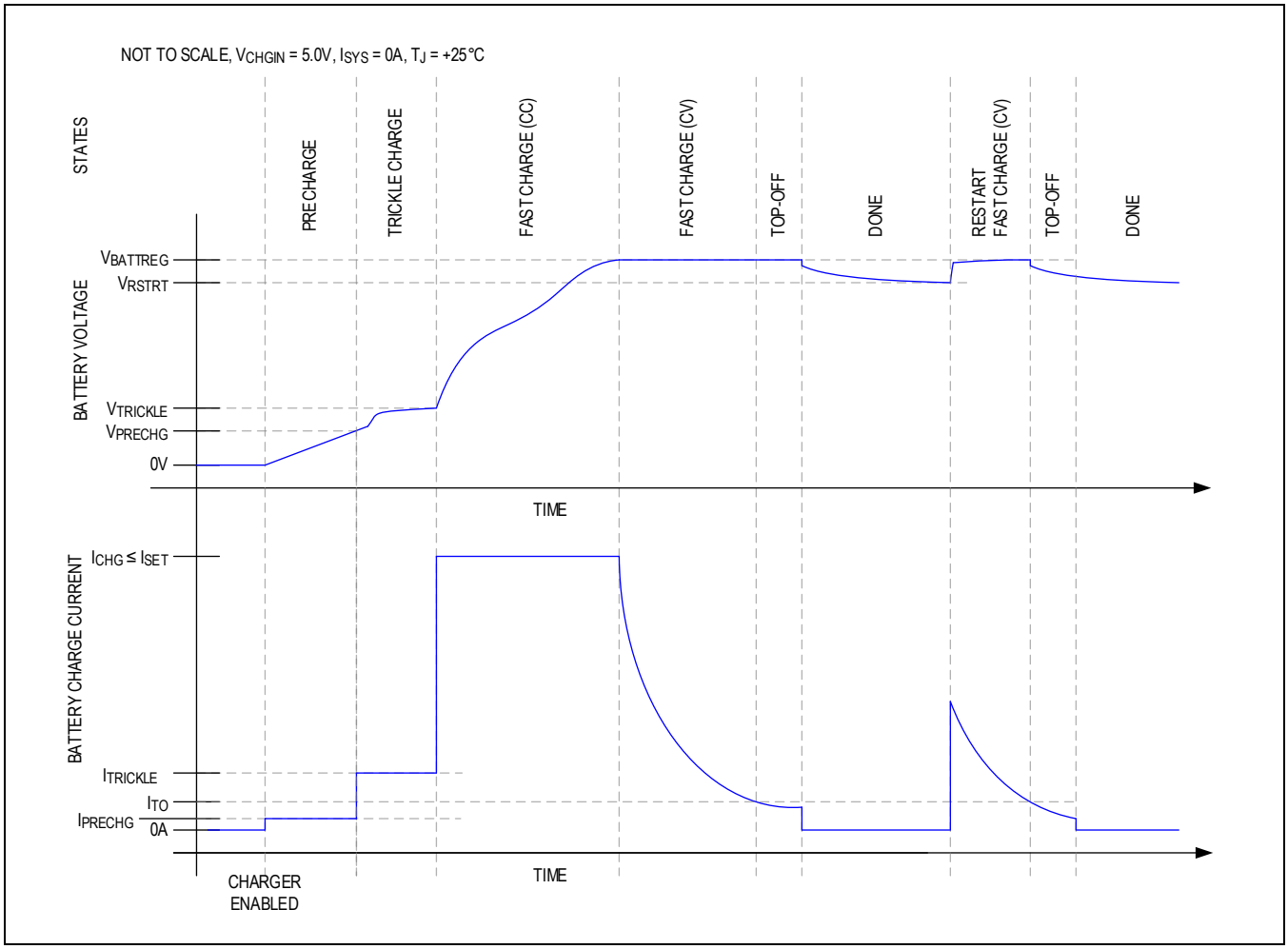


Figure 5. Li+/Li-Poly Charge Profile

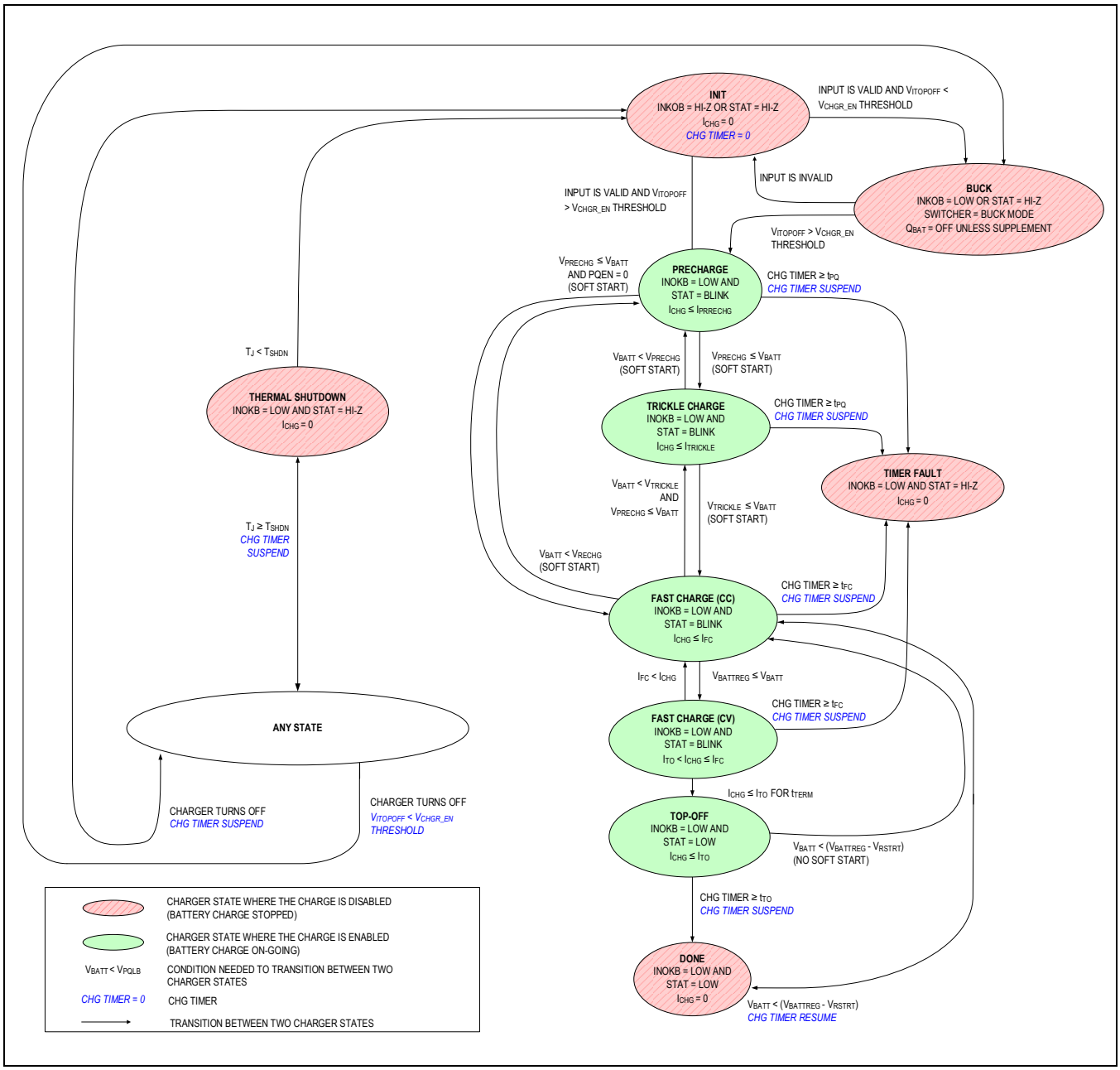


Figure 6. Charger State Diagram

INIT State

From any state shown in *Figure 6* except thermal shutdown, the “INIT” state is entered whenever the charger inputs CHGIN is invalid, or the charger timer is suspended.

While in the “INIT” state, the charger current is 0mA, the charge timer is forced to 0, and the power to the system is provided by the battery.

To exit the “INIT” state, the charger input must be valid.

Buck State

The chip has a state where battery charging is disabled, while the charger input CHGIN is valid. The state is called “buck” state. Entering or leaving the buck state is controlled by the EXTSM pin. If the voltage of this pin is pulled down by an external device (i.e., MCU) under V_{CHGR_EN}, the chip goes to the buck state from any state if CHGIN is valid, as shown in *Figure 6*. Charging is disabled in the “buck” state, which means Q_{BAT} is off unless it is in supplement mode. If the voltage of this pin is over V_{CHGR_EN}, the chip leaves the buck state, and resumes charging. It should be noted that charging can only be enabled or disabled when the CHGIN is valid. Therefore, the external device (i.e., MCU) should check the INOKB signal if CHGIN is valid before trying to enable or disable charging.

Precharge State

As shown in *Figure 6*, the precharge state occurs when the main battery voltage is less than V_{PRECHG}. In the precharge state, charge current into the battery is I_{PRECHG}.

The following events cause the state machine to exit this state:

- The main battery voltage rises above V_{PRECHG} and the charger enters the next state in the charging cycle, trickle charge.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the timer fault state.

Note that the precharge state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically a pack internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the precharge mode current flows into the 0V battery—this current raises the pack’s terminal voltage to the point where the internal pack protection switch closes.

Note that a normal battery typically stays in the precharge state for several minutes or less. Therefore, a battery that stays in the precharge state for longer than t_{PQ} might be experiencing a problem.

Trickle Charge State

The trickle charge mode descripted below is for Li-ion and Li-poly batteries only, with charge termination voltage from 4.1V to 4.5V (programmable range from 3.60V to 4.55V).

As shown in *Figure 6*, the trickle charge state occurs when $V_{BATT} > V_{PRECHG}$ and $V_{BATT} < V_{TRICKLE}$.

When the MAX77789 is in its trickle charge state, the charge current in the battery is less than or equal to $I_{TRICKLE}$.

Charge current might be less than $I_{TRICKLE}/I_{FC}$ for any of the following reasons:

- The charger input is under input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{TRICKLE}$, the charger enters the next state in the charging cycle, fast-charge constant current (CC).
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the timer fault state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less; therefore, a battery that stays in trickle charge for longer than t_{PQ} might be experiencing a problem.

There is no trickle stage for the LiFePO4 battery. This can be achieved by disabling low-battery prequalification mode in register CHG_CNFG_01 bit 7 through I^2C after power up. The minimum SYS voltage (CHG_CNFG_10[2:0]) and charge termination voltage (CHG_CNFG_04) need to be adjusted accordingly.

Fast-Charge Constant Current State

As shown in *Figure 6*, the fast-charge constant current (CC) state occurs when the main-battery voltage is greater than the trickle threshold and less than the battery regulation threshold ($V_{TRICKLE} < V_{BATT} < V_{BATTREG}$).

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

- The charger input is under input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle, fast-charge constant voltage (CV).
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced. See the *Thermal Foldback* section for more information.

Fast-Charge Constant Voltage State

As shown in *Figure 6*, the fast-charge constant voltage (CV) state occurs when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to I_{FC}. As shown in *Figure 5*, charger current decreases exponentially in this state as the battery becomes fully charged.

The smart power selector control circuitry might reduce the charge current lower than the battery can otherwise consume for any of the following reasons:

- The charger input is under input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below I_{TO} for t_{TERM}, the charger enters the next state in the charging cycle, top off.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

Top-Off State

As shown in *Figure 6*, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. In the top-off state, the battery charger tries to maintain $V_{BATTREG}$ across the battery and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry might reduce the charge current lower than the battery can otherwise consume for any of the following reasons:

- The charger input is under input current limit
- The charger input voltage is low
- The charger is in thermal foldback
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time (t_{TO}), the charger enters the next state in the charging cycle, done.
- If $V_{BATT} < V_{BATTREG} – V_{RSTRT}$, the charger goes back to the fast-charge (CC) state.

Done State

As shown in *Figure 6*, the battery charger enters the done state after the charger has been in the top-off state for t_{TO}.

The following event causes the state machine to exit this state:

- If $V_{BATT} < V_{BATTREG} – V_{RSTRT}$, the charger goes back to the fast-charge (CC) state

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low quiescent current to the battery. If the system load presented to the battery is low (<100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}), and the charger state machine transitions back into the fast-charge CC state. There is no soft-start (di/dt limiting) during the done-to-fast-charge state transition.

Timer Fault State

The battery charger provides a charge timer to ensure safe charging. As shown in *Figure 6*, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of the prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC}. Finally, the time that the charger is in the top-off state is t_{TO}. Upon entering the timer fault state, STAT2 becomes Hi-Z.

In the timer fault state, the charger is off. The charger input can be removed and re-inserted to exit the timer fault state (See the “any state” bubble in the lower left of *Figure 6*).

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The watchdog timer protects the battery from charging indefinitely if the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. The typical watchdog timer period is around 80s.

Thermal Shutdown State

As shown in *Figure 6*, the thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device’s thermal-shutdown threshold (T_{SHDN}). When T_J is close to REG, the charger folds back the input current limit to 0A so that the charger and inputs are effectively off.

In the thermal shutdown state, the charger is off.

Reverse Boost Mode

The DC-DC converter topology of the MAX77789 allows it to operate as a buck converter or as a reverse boost converter. The MAX77789 is detecting devices and turns on reverse boost mode in automatic fashion and the reverse boost mode is also activated by selecting 0x0A of the mode in CHG_CNFG_00[3:0]. The DC-DC converter operates in reverse boost mode allowing it to source current to BYP and CHGIN; this mode allows current to be sourced from CHGIN and is commonly referred to as OTG mode or a source role. When the OTG mode is enabled, the unipolar CHGIN transfer function measures current going out of CHGIN. The BYP to CHGIN switch automatically retries after 300ms if CHGIN loading exceeds the 1.5A current limit. If the overload at CHGIN persists, then the CHGIN switch toggles ON and OFF with approximately 60ms ON and 300ms OFF. The current through the BYP to CHGIN switch is limited to 1.5A minimum.

The MAX77789 also allows it to be sourced from BYP with selecting mode of 0x08 in CHG_CNFG_00[3:0].

Note that injecting the higher V_{CHGIN} than 5.1V in case of reverse boost mode enabled causes reverse boost to be abnormal.

Main Battery Overcurrent Protection During System Power-Up

The main battery overcurrent protection during system power-up feature limits the main battery to system current to I_{SYSPU} if V_{SYS} is less than V_{SYSPU}. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up. System power-up is any time that energy from the battery is supplied to SYS when $V_{SYS} < V_{SYSPU}$. This "system power-up" condition typically occurs when a battery is hot-inserted into an otherwise unpowered device.

When "system power-up" occurs due to hot-insertion into an otherwise unpowered device, a small delay is required for this feature's control circuits to activate. A current spike over I_{SYSPU} might occur during this time.

Main Battery Overcurrent Protection Due To Fault

The IC protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current can occur for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit.

When the main battery (BATT)-to-system (SYS) discharge current (I_{BATT}) exceeds 6A for at least t_{BOVRC}, then the IC disables the BATT-to-SYS discharge path (Q_{BAT} switch) and turns off the buck.

Under OCP fault condition, when SYS is low ($V_{SYS} < V_{SYSUP}$) for tocp_retry, the IC restarts on its own and attempts to pull up SYS again. If the fault condition remains, the whole cycle repeats until this fault condition is removed.

Thermal Management

The IC charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the IC junction temperature. As shown in *Figure 7*, when the die temperature exceeds the REGTEMP (T_{REG}), a thermal limiting circuit reduces the battery charger's target current by 5% of the fast-charge current per 1°C (A_{TJREG}), which corresponds to 157.5mA/°C when the fast-charge current is 3.15A. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA, the slope becomes shallower, but the charge current reduces to 0A if the junction temperature is 20°C above the programmed loop set point. The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current).

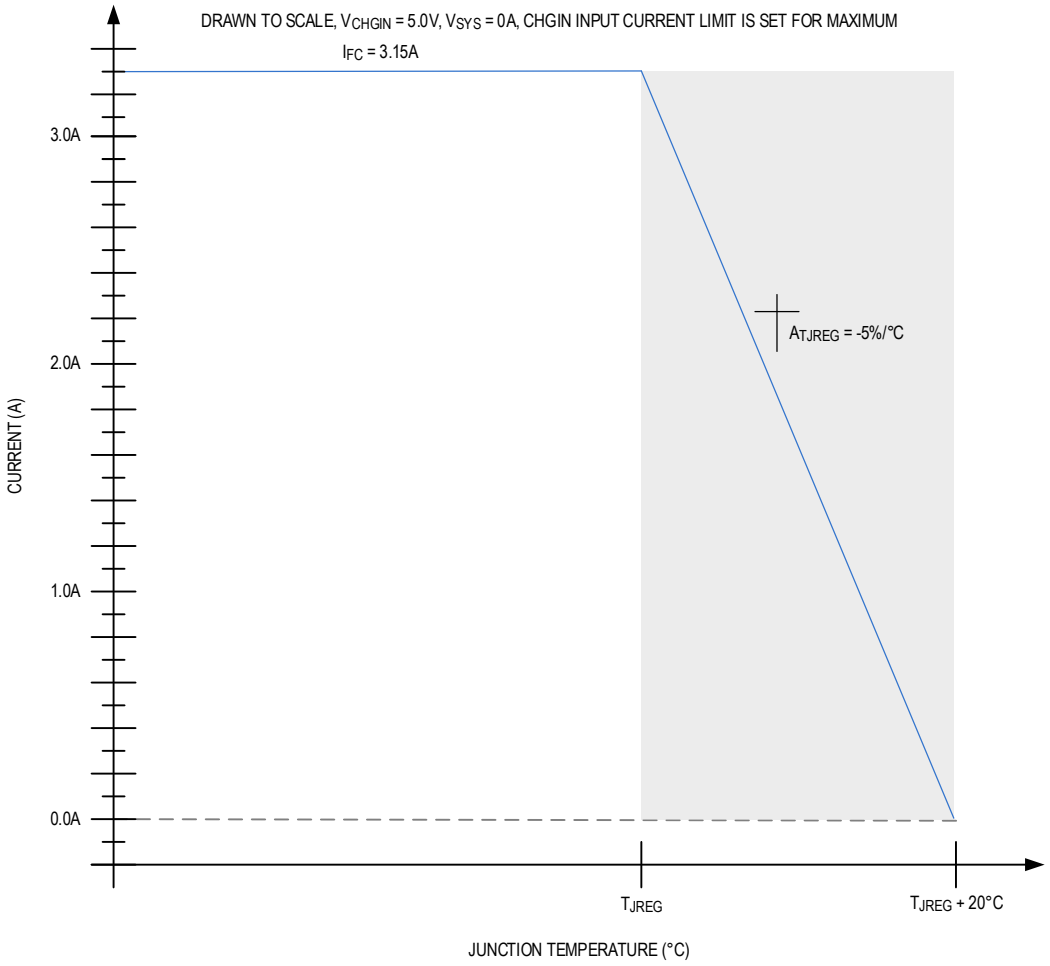


Figure 7. Charge Currents vs. Junction Temperature

Thermistor Input (THM)

The thermistor input can be utilized to achieve functions that include charge suspension, JEITA-compliant charging, and disabling the charger by pulling THM pin to GND.

JEITA Compliance

The MAX77789 safely charges battery in accordance with JEITA specification. The MAX77789 monitors the battery temperature with an NTC thermistor connected at THM pin and automatically adjusts the fast-charge current or charge termination voltage as the battery temperature varies.

The JEITA controlled charging can be disabled by register CHG_CNFG_00[5].

The JEITA controlled fast-charge current is programable to be 50% or 20% of the detected fast charge current for $T_{COLD} < T < T_{COOL}$. AP shall configure the register of CHG_CNFG_14[4:3]. The default set is a 50% reduction when JEITA is enabled.

The charger termination voltage for $T_{WARM} < T < T_{HOT}$ is also programable to be -150mV or -100mV of termination voltage setting, as shown in *Figure 7*. AP shall configure the register of CHG_CNFG_14[6:5]. The default setting is a 50% reduction when JEITA is enabled.

Charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

The MAX77789 features disabling the JEITA under warm and cool conditions and stops charging when the temperature is too hot or cold, when the register of CHG_CNFG_14[7] bit is set.

Temperature thresholds (T_{COLD}, T_{COOL}, T_{WARM}, and T_{HOT}) depend on the thermistor selection. See *Table 2* for more details.

Since the thermistor monitoring circuit employs an external bias resistor from THM to PVL, the thermistor is not limited only to 10kΩ (at +25°C); any resistance thermistor can be used if the value is equivalent to the thermistors +25°C resistance. The thermistor installed on the evaluation kit is 10kΩ with a beta of 3435.

The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{[\beta \times (\frac{1}{T+273} - \frac{1}{298})]}$$

where

R_T = The resistance in Ω of the thermistor at temperature T in Celsius

R_{25} = The resistance in Ω of the thermistor at +25ºC

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k

T = The temperature of the thermistor in Celsius

Table 2. Temperature Threshold for Different Thermistors

THERMISTOR PART NUMBER	BETA (β)	R25 (Ω)	EXTERNAL BIAS RESISTOR FROM THM TO PVL, RTB (Ω)	JEITA TEMPERATURE THRESHOLD (TYPICAL)			
				T_{COLD} (°C)	T_{COOL} (°C)	T_{WARM} (°C)	T_{HOT} (°C)
TX04F103F3380ER	3380	10000	10000	-0.2	9.6	45.5	60.5
NCP15XH103F03	3435	10000	10000	0.2	9.8	45.2	59.9
TH05-3N333FR	3725	33000	33000	2	10.9	43.5	56.9
TH05-4B473FR	4057	47000	47000	3.7	12	41.9	54
NTCG104EF104FT1X	4308	100000	100000	4.9	12.8	40.9	52.2

Note:

- Thermistor resistance tolerance, pullup resistance tolerance, and parasitic are not considered in this table.
- Listed part numbers are for reference only.

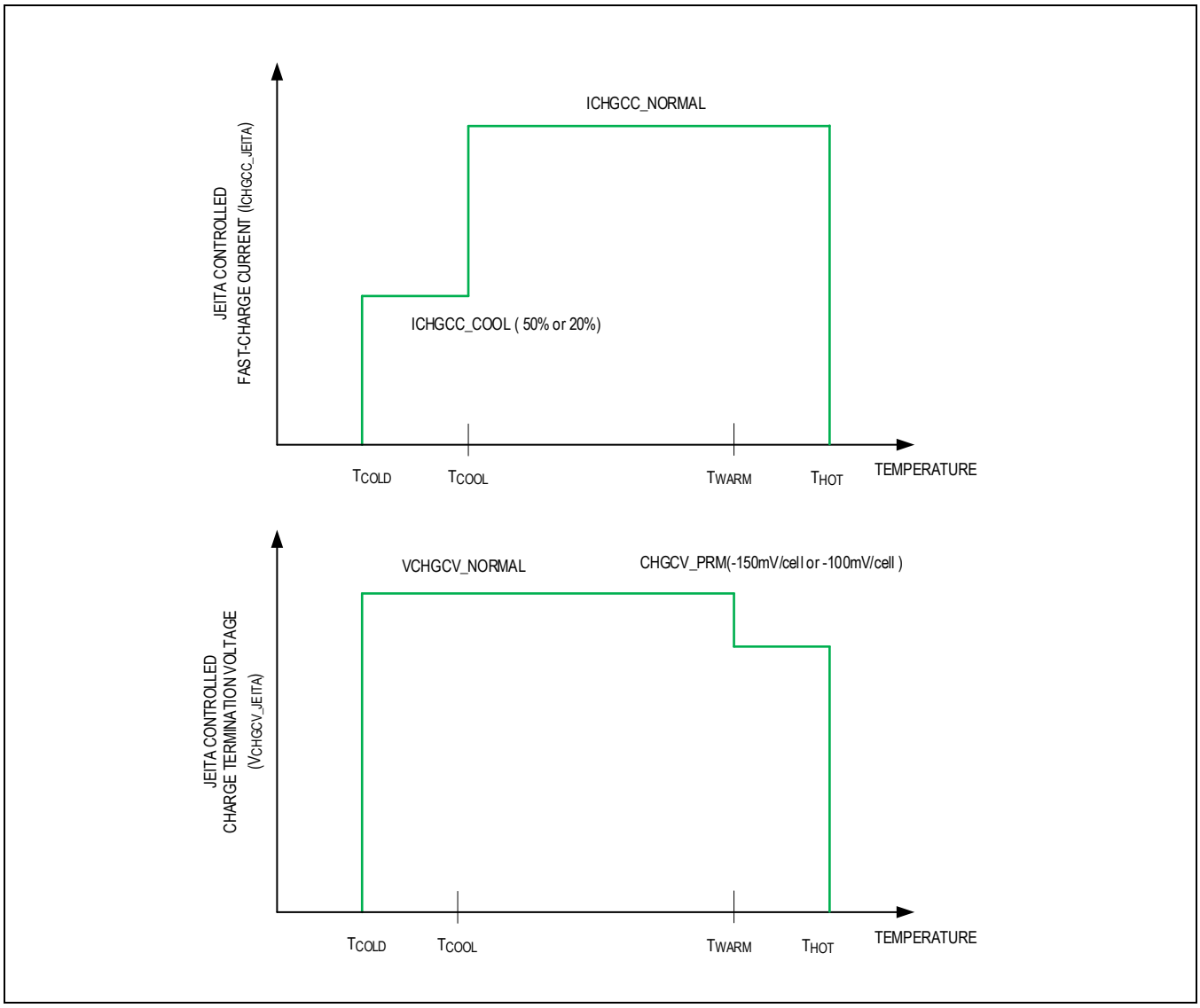


Figure 8. MAX77789 JEITA Compliance

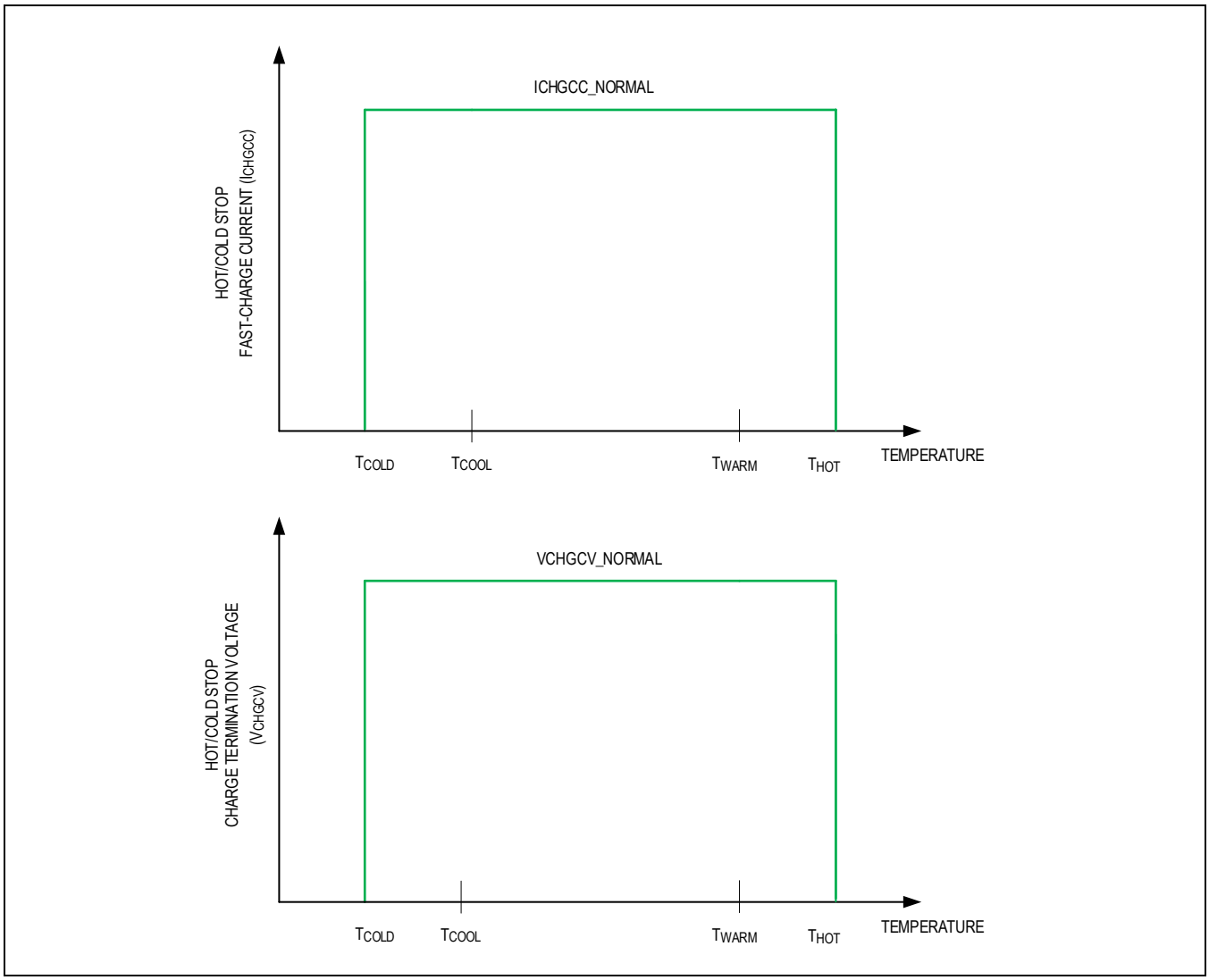


Figure 9. MAX77789 Hot/Cold Stop

V_{DD} Internal Supply

V_{DD} is the 1.8V power for the IC charger's analog circuit. V_{DD} is generated from the higher of BATT and CHGIN as power input source and generates an internal power supply. V_{DD} has a bypass capacitance of 2.2µF.

Ship Mode and EXTSM Pin Function

1. Entering Ship Mode

   To minimize power when the system is off during shipping or storage, MAX77789 turns off Q_{BAT} so that SYS and BATT are isolated to minimize the battery leakage current. when the system MCU sets the FSHIP bit in CHG_CNFG_07[0], the charger turns off the Q_{BAT} immediately or with a delay by t_{FSHIP_DLY} as configured in CHG_CNFG_13[1].

2. Exiting Ship Mode

   When the Q_{BAT} is disabled (Ship Mode) by setting the FSHIP bit, one of several events can make MAX77789 exit ship mode and restore system power.

   - CHGIN is valid
   - By pulling EXTSM high longer than 10mS

3. System Reset by Register or EXTSM pin

   When QBAT_RST = 1, FSHIP = 0 and CHGIN is invalid, the system reset function is enabled. By setting the Q_{BAT} reset bit in CHG_CNFG_13[4], Q_{BAT} turns off and the system enters the POR state as no power is on the SYS. EXTSM pin supports push-button function to reset whole system without MCU involved by pulling EXTSM high for 10s. After 1s or 5s duration, which could be selected in tQBAT_RST in CHG_CNFG_13[3], Q_{BAT} automatically turns on and the SYS voltage is back on, so the system starts the boot up sequence.

4. EXTSM pin

   EXTSM is an input control signal for battery charging with an external logic signal. When QBAT_RST = 0 and FSHIP = 0 and CHGIN is valid, if EXTSM is driven by high, the battery charging is disabled.

Spread-Spectrum Modulation

The buck-boost regulator can dither its switching frequency for noise-sensitive applications. The spread-spectrum modulation can be enabled/disabled by the SS_EN bit, and its modulation pattern is programmable either pseudo-random or triangular by the SS_PAT bit. The modulation envelope (ΔF_{SS}) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. The modulation envelope is programmable (±6% or ±9%) by the SS_ENV bit, and it controls 'how wide' the switching frequency dithers.

Pseudo-Random Pattern

As shown in *Figure 10*, the pseudo-random engine uses a 15-bit linear feedback shift register (LFSR) to create a pseudo-random value. The LFSR value is converted to an analog signal and then amplified before being added to the clock generation circuit, which increases or decreases the switching frequency. The refresh rate of the LFSR is 20kHz. This is the frequency at which one pseudo-random value changes to another.

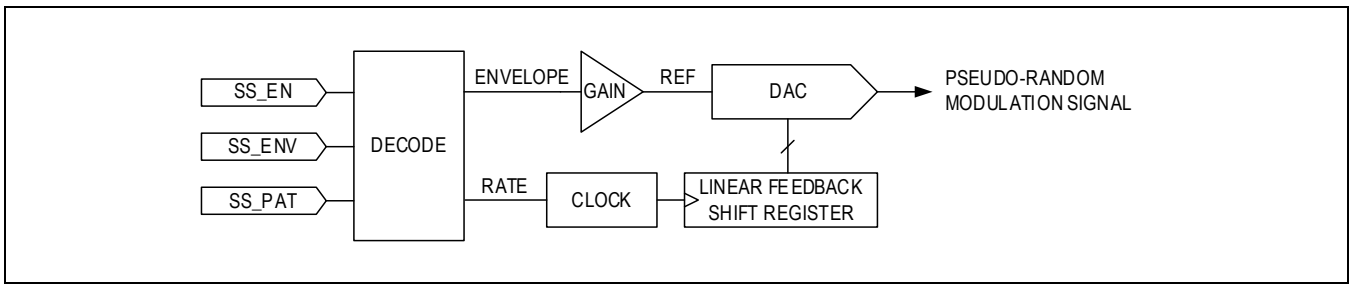


Figure 10. Pseudo-Random Modulator Engine

Triangular Pattern

As shown in *Figure 11*, the triangular engine uses an up/down synchronous counter to create a stepped triangular pattern. The counter value is converted to an analog signal and then amplified before being added to the clock generation circuit, which progressively increases and decreases the switching frequency.

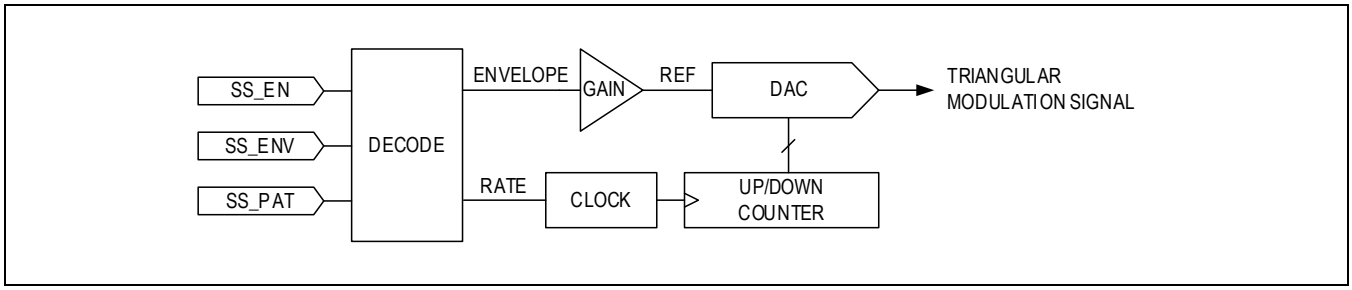


Figure 11. Triangular Modulator Engine

USB BC1.2 Charger Detection

Features

- D+/D- Charging Signature Detector
- D+/D- Manual Control Capability for the HVDCP
- USB BC1.2 Compliant
- SDP, DCP, and CDP Detection
- Detect Proprietary Charger Types
  - Apple® 500mA, 1A, 2A, 12W
  - Samsung® 2A

Description

The USB charger detection is USB BC1.2 compliant with the ability to automatically detect some common proprietary charger types.

The charger detection state machine follows USB BC1.2 requirements and detects SDP, CDP, and DCP types. The charger detection state machine indicates if D+/D- were found as open but ChgTyp indicates SDP as required by BC1.2 specifications.

In addition to the USB BC1.2 state machine, the IC also detects a limited number of proprietary charger types (Apple, Samsung, and generic 500mA). The IC automatically sets the CHGIN input current limiting based on the charger type detection results. The input current limit set value can be overridden by the system MCU.

Table 3. BC1.2 Charger Type

USB BC1.2 DETECTED CHARGER TYPE	
CHARGER TYPE VALUE	**CHARGER DETECTED**
00	No CHGIN
01	SDP
10	CDP
11	DCP

Table 4. Proprietary Charger Type

DETECTED PROPRIETARY CHARGER TYPE	
PROPRIETARY CHARGER TYPE	**CHARGER DETECTED**
000	No Proprietary Charger
001	Samsung 2A
010	Apple 500mA
011	Apple 1A
100	Apple 2A
101	Apple 12W
110	RFU
111	RFU

D+/D- Manual Control

The MAX77789 provides D+/D- manual control options. When the DPDNMan bit is set, D+ pin and D- pin can be driven to be GND, 0.6V, 3.0V, and open, respectively, by an external controller (i.e., MCU). The MAX77789 automatically set D+ pin and D- pin of 3.0V when the MAX77789 is in the source mode when both the DPDNAuto bit and the DetAbrt_Dis bit are set to high.

USB Type-C CC Detection

Features

- Current power roles (SINK or SOURCE)
- DFPs current capability
- Active CC pin status
- Current advertisement (1.5A) in source mode
- 1V internal clamp circuit allowing for unpowered UFP identification
- Try.Sink state
- Error recovery state
- V_{BUS} Status

CC Description

The MAX77789 operates in DRP (Dual Role Port) by default. The USB Type-C functions are controlled by a logic state machine that follows the USB Type-C requirements. The device provides the options for sink only mode and source only mode as well by setting the register of CC_MODE. There is support for the optional Try.Sink function, which places priority on the sink role.

USB Type-C Definitons

- UFP: Upstream Facing Port. Typical USB device role for data transfer.
- DFP: Downstream Facing Port. Typical USB device role for data transfer.
- DRP: Dual Role Port. USB Type-C port that can operate in either DFP or UFP.
- SOURCE: Initial power state for a DFP.
- SINK: Initial power state for a UFP.

DRP

The MAX77789 supports DRP operation. The port cycles between advertising DFP/SOURCE and UFP/SINK operations while waiting for a port to be connected. The internal state machine handles all the tasks of detecting and configuring the CC pins for the correct mode. A manual mode allows forcing either the DFP or UFP operation in cases where the DRP operation is not appropriate.

Detecting Connected DFP

When a DFP/SOURCE is detected (either from DRP mode or force UFP mode), the USB Type-C connection state machine detects the active CC line and reports this with an interrupt to the host application processor (AP). The USB Type-C connection state machine also auto detects the DFP advertised current (default, 1.5A and 3.0A).

Detecting Connected UFP

When a UFP is detected (either from DRP mode or force DFP mode), a 1.5A source current capability is advertised, and the USB Type-C State Machine detects the active CC line. It automatically enables reverse boost to provide 5.1V on the V_{BUS} in the default operation of the MAX77789. (**Note:** Changing OTG_ILIM does not affect the advertised source current limit.)

The system MCU can also enable or disable reverse boost accordingly by charger mode configuration when the OTG_EN bit = 0.

Try.SNK Support

The MAX77789 operates as a DRP (Dual Role Port) by default. This type of port can act as either a power sink/USB data peripheral or a power source/USB data host. The Type-C logic state machine cycles between source and sink at a rate typically around 75ms. This means that when the MAX77789 is connected to another device that is also a DRP (example: a PC with a C port), the source and sink roles are randomly assigned. The MAX77789 includes support for Try.SNK,

which allows the MAX77789 to be set to strongly prefer the sink role if connected to a standard DRP. In case of system where Try.SNK is not appropriate, the Type-C logic state machine bypasses the Try.SNK state when CC_TRYSNK = 0.

Error Recovery Support

The MAX77789 is supporting the Error Recovery state as described in the Type-C specification. Both CC1 and CC2 become floating when the forced error recovery bit is set by the user.

Serial Interface (I²C)

Overview

The I²C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 12 shows an example of a typical I²C system. A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77789 I²C-compatible interface is operating, it is a slave on the I²C bus, and it can be both a transmitter and a receiver.

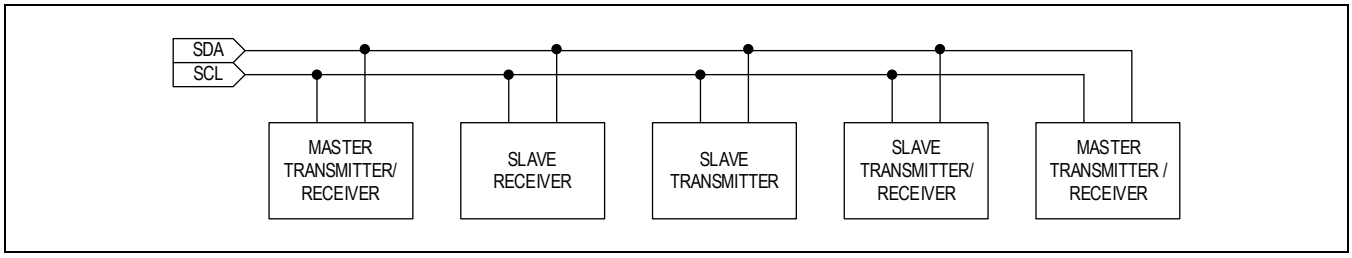


Figure 12. Functional Logic Diagram for Communications Controller

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA, while SCL is high, are control signals (START and STOP conditions).

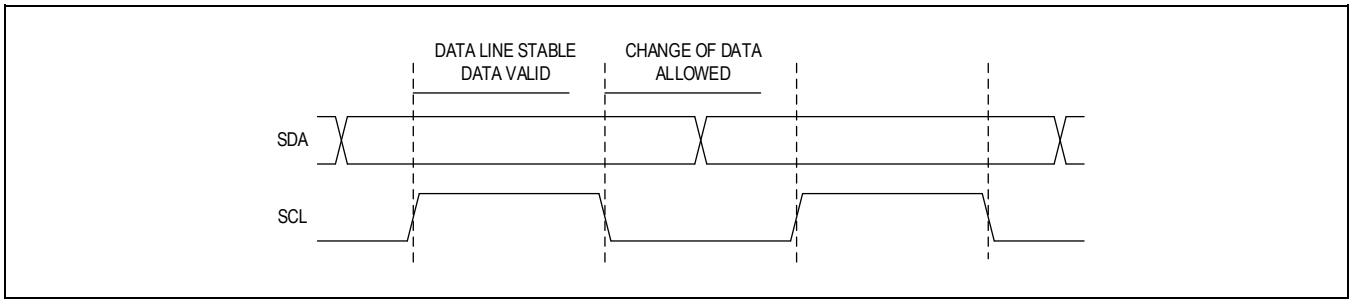


Figure 13. I²C Bit Transfer

START And STOP Conditions

When the I²C serial interface is inactive, SDA and SCL are idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the I2C serial interface until the next START condition, minimizing digital noise and feed-through.

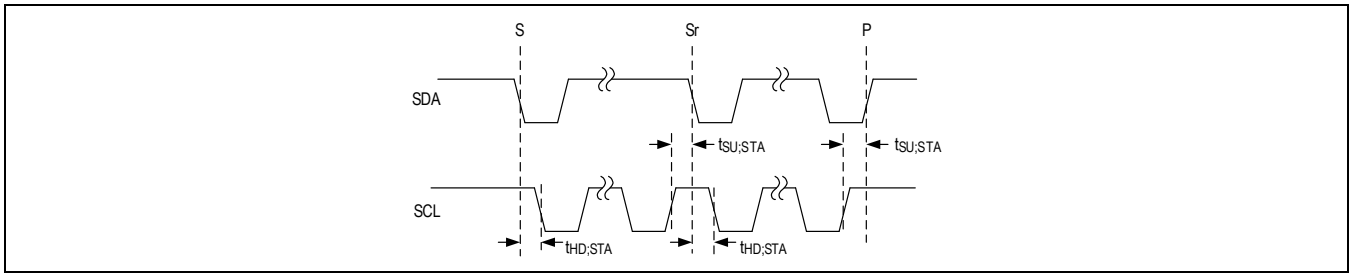


Figure 14. I2C Start and Stop Condition

Acknowledge

Both the I2C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication later.

Slave Address

REGISTER TYPE	SLAVE ADDRESS (7-BIT)	SLAVE ADDRESS (WRITE)	SLAVE ADDRESS (READ)
Charger	0x69 0b110 1001	0xD2 0b1101 0010	0xD3 0b1101 0011

Clock Stretching

In general, the clock signal generation for I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The IC does not implement an I2C specification general call address. If the IC sees general call address (0b00000000), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides I2C 3.0-compatible (1MHz) serial interface.

- I2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
- Does not Utilize I2C Clock Stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the "*Pullup Resistor Sizing*" section of the I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I2C 3.0 specification. The major considerations with respect to the IC are:

- I2C bus master uses current source pullups to shorten the signal rise times.
- I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section.

Communication Protocols

Writing to a Single Register

Figure 15 shows the protocol for the I2C master device to write one byte of data to the IC. This protocol is the same as SMBus specification's "Write Byte" protocol.

The "Write Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

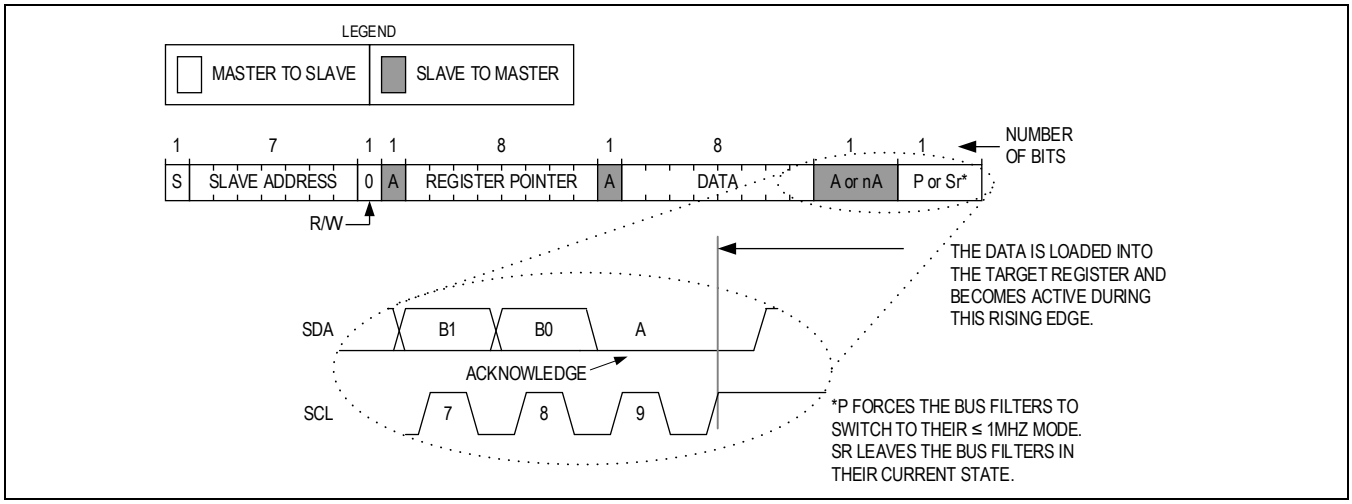


Figure 15. Writing to a Single Register with the Write Byte Protocol

Writing To Sequential Registers

Figure 16 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The “Writing to Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

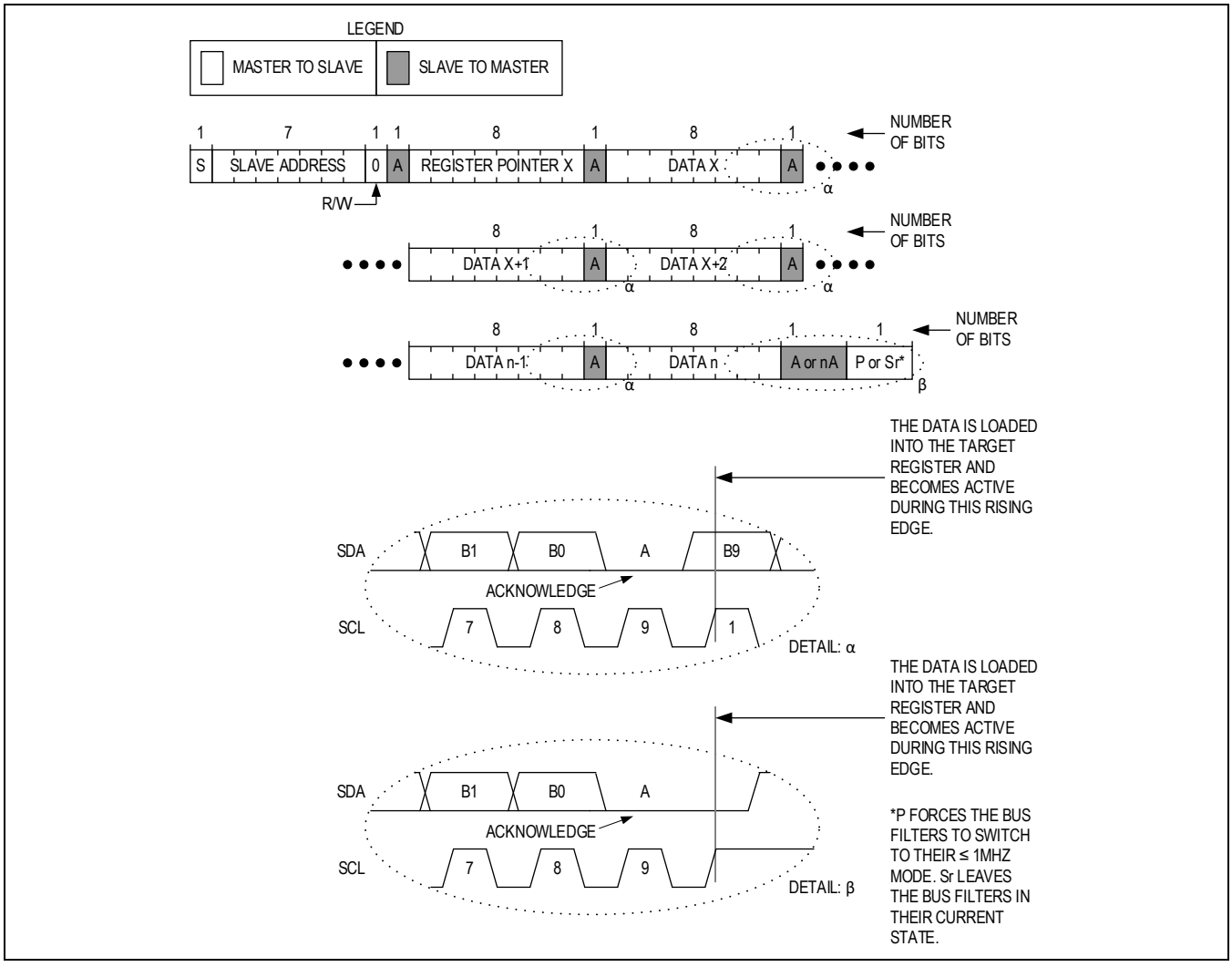


Figure 16. Writing to Sequential Register X to N

Reading from a Single Register

The I2C master device reads one byte of data to the IC. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

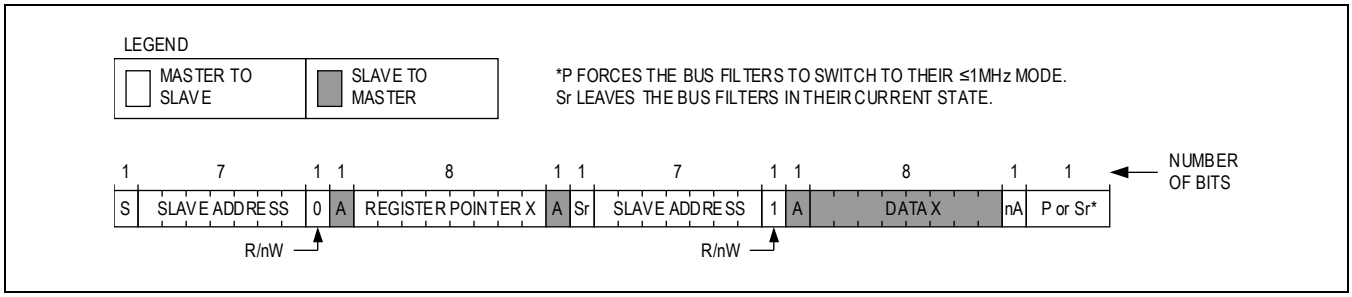


Figure 17. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 18 shows the protocol for reading from sequential registers. This protocol is similar to the "Read Byte" protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data—When the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The "Continuous Read from Sequential Registers" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ =1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

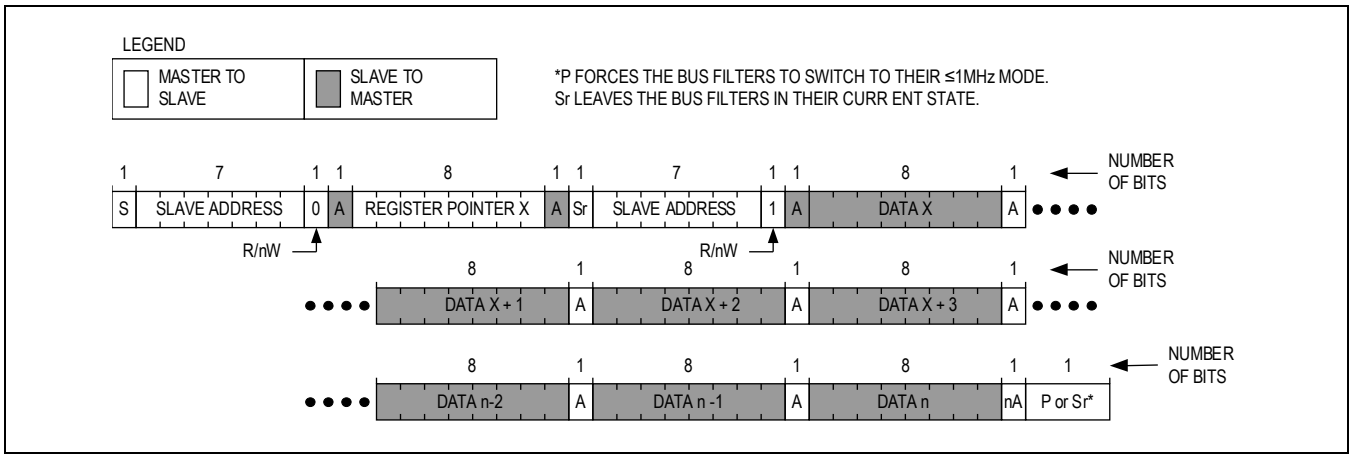


Figure 18. Reading Continuously from Sequential Registers X To N

Engaging HS-Mode for Operation up to 3.4MHz

Figure 19 shows the protocol for engaging HS-Mode operation. HS-Mode operation allows for a bus operating speed up to 3.4MHz.

The “Engaging HS-Mode” protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START command (S).
3. The master sends the 8-bit master code of 0000 1XX0b, where ‘XX’ are don’t care bits.
4. The addressed slave issues a not-acknowledge (nA).
5. The master can increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation.

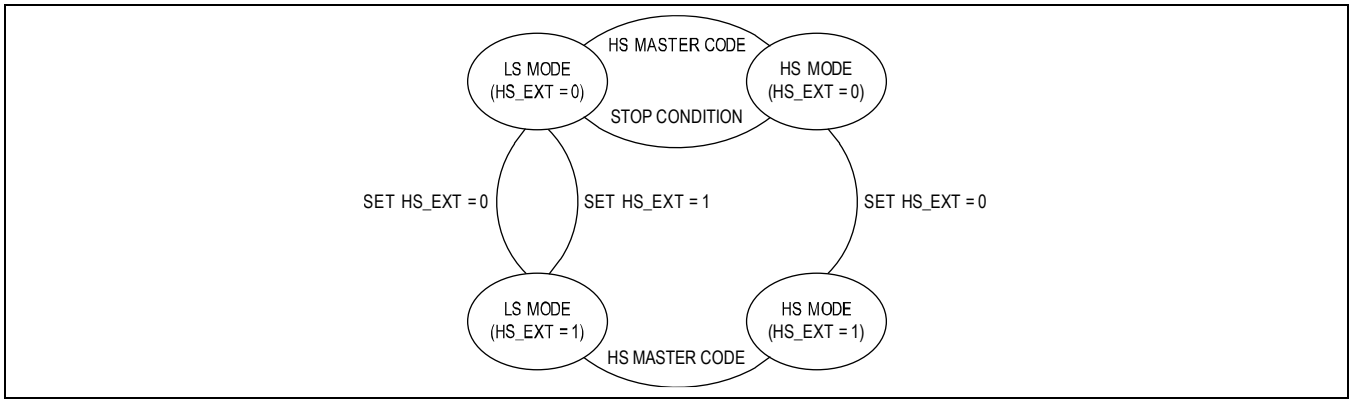


Figure 19. Engaging HS-Mode

The MAX77789 I2C supports the HS mode extension feature. The HS extension feature keeps the high-speed operation even after a ‘STOP’ condition. This eliminates the need for an HS master code issued by the I2C master controller when the I2C master controller wants to stay in HS mode for multiple read/write cycles.

As shown in *Figure 20*, the HS extension mode can be enabled by setting the HS_EXT bit in the I2C_CFG register (ADDR 0x15) from LS mode only (entering the HS extension mode from HS mode is not supported).

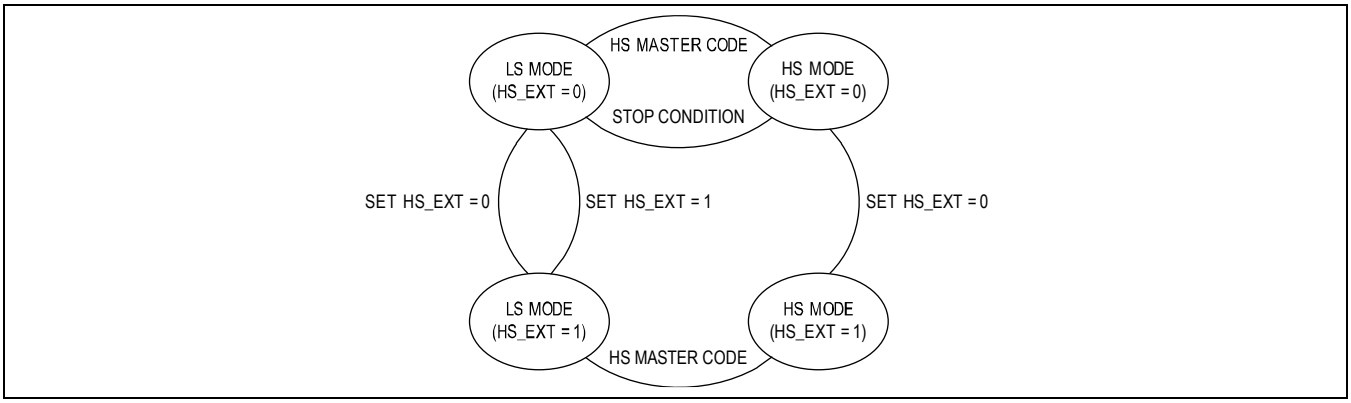


Figure 20. I²C Operating Mode State Diagram

Register Map

CHARGER

ADDRESS	NAME	MSB							LSB
TOP_FUNC									
0xA0	CHIP_ID[7:0]	CID[7:0]							
0xA1	CHIP_REVISION[7:0]	REVISION[3:0]				VERSION[3:0]			
0xA2	SWRST[7:0]	SW_RST[7:0]							
0xA3	TOP_INT[7:0]	–	–	BC_I	CC_I	CHG_I	TSHDN_I	SYSOVLO_I	SYSUVLO_I
0xA4	TOP_INT_MASK[7:0]	–	–	BC_M	CC_M	CHG_M	TSHDN_M	SYSOVLO_M	SYSUVLO_M
0xA5	TOP_INT_OK[7:0]	–	–	–	–	–	TSHDN_OK	SYSOVLO_OK	SYSUVLO_OK
CHARGE_FUNC									
0xB0	CHG_INT[7:0]	TOPOFF_I	AICL_I	B2SOVRC_I	INLIM_I	CHGIN_I	CHG_I	BAT_I	BYP_I
0xB1	CHG_INT_MASK[7:0]	TOPOFF_M	AICL_M	B2SOVRC_M	INLIM_M	CHGIN_M	CHG_M	BAT_M	BYP_M
0xB2	CHG_INT_OK[7:0]	TOPOFF_OK	AICL_OK	B2SOVRC_OK	INLIM_OK	CHGIN_OK	CHG_OK	BAT_OK	BYP_OK
0xB3	CHG_DETAILS_00[7:0]	–	CHGIN_DTLS[1:0]		–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0xB4	CHG_DETAILS_01[7:0]	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
0xB5	CHG_DETAILS_02[7:0]	–	THM_DTLS[2:0]			BYP_DTLS[3:0]			
0xB6	CHG_DETIALS_03[7:0]	–	–	–	–	–	–	–	–
0xB7	CHG_CNFG_00[7:0]	–	DISIBS	JEITA_DIS	WDTEN	MODE[3:0]			
0xB8	CHG_CNFG_01[7:0]	PQEN	LSEL	CHG_RSTRT[1:0]		RECYCLE_EN	FCHGTIME[2:0]		
0xB9	CHG_CNFG_02[7:0]	OTG_ILIM[1:0]		CHGCC[5:0]					
0xBA	CHG_CNFG_03[7:0]	–	TO_TIME[2:0]			TO_ITH[3:0]			
0xBB	CHG_CNFG_04[7:0]	–	–	CHG_CV_PRM[5:0]					
0xBC	CHG_CNFG_05[7:0]	–	–	–	–	B2SOVRC[3:0]			
0xBD	CHG_CNFG_06[7:0]	B2SOVRC_DTC	–	–	DIS_AICL	CHGPROT[1:0]		WDTCLR[1:0]	
0xBE	CHG_CNFG_07[7:0]	WD_QBATOFF	REGTEMP[3:0]			–	–	FSHIP_MODE	
0xBF	CHG_CNFG_08[7:0]	–	–	–	–	–	–	FSW[1:0]	
0xC0	CHG_CNFG_09[7:0]	CHG_EN	CHGIN_ILIM[6:0]						
0xC1	CHG_CNFG_10[7:0]	INLIM_CLK[1:0]		–	–	–	MINVSYS[2:0]		
0xC2	CHG_CNFG_11[7:0]	–	–	–	–	–	–	–	–
0xC3	CHG_CNFG_12[7:0]	NO_AUTOISET	–	–	VCHGIN_REG[1:0]		–	–	DISKIP
0xC6	CHG_CNFG_13[7:0]	–	–	STBY_EN	QBAT_RST	tQBAT_RST	FSHIP_DLY	tFSHIP_DLY	–

ADDRESS	NAME	MSB							LSB
0xC7	CHG_CNFG_14[7:0]	HOTCOLD_EN	VCHG_CV_WARM[1:0]		ICHG_CC_COOL[1:0]		SS_PAT	SS_ENV	SS_EN
0xD5	CHG_CNFG_15[7:0]	–	–	–	–	VCHG_CV_COOL_EN	STAT2_USAGE	STAT2_CTL	STAT2_MAN_CTL
OVERLAP									
USBC_FUNC									
0xC4	USB_TYPE_DTLS[7:0]	–	CHG_TYP[1:0]		PR_CHG_TYP[2:0]			CC_CURR[1:0]	
0xC5	USB_ILIM_DTLS[7:0]	–	USB_INLIM[6:0]						
0xC8	BC_CTRL1[7:0]	–	–	–	–	DCDCpl	–	DetAbrt_Dis	ChgDetEn
0xC9	BC_CTRL2[7:0]	–	–	–	–	CHGIN_INLIM_Gate	SDPMaxCurr[1:0]		CDPMaxCurr
0xCA	CC_CTRL1[7:0]	–	–	–	–	–	–	–	CCDetEn
0xCB	BC_INT[7:0]	VBUSDetI	–	–	–	–	propChgTypI	dcdTmoI	chgTypI
0xCC	CC_INT[7:0]	–	VSAFE0VI	DetAbrtI	–	CCPinStatI	CCIStatI	–	CCStatI
0xCD	BC_INTMASK[7:0]	VBUSDetM	–	–	–	–	propChgTypM	dcdTmoM	chgTypM
0xCE	CC_INTMASK[7:0]	–	VSAFE0VM	DetAbrtM	–	CCPinStatM	CCIStatM	–	CCStatM
0xCF	BC_STATUS1[7:0]	VBUSDet	–	–	–	–	DCDTmo	–	–
0xD0	CC_STATUS1[7:0]	CCPinStat[1:0]		CCIStat[1:0]		–	CCStat[2:0]		
0xD1	CC_STATUS2[7:0]	CC1VRA	CC2VRA	CC_VUFP_RD0P5	CC_VUFP_RD1P5	VSAFE0V	DetAbrt	–	–
0xD2	BC_CTRL3[7:0]	–	DPDNMan	DPDrv[1:0]		DNDrv[1:0]		DPDNAuto	–
0xD3	CC_CTRL2[7:0]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0xD4	CC_CTRL3[7:0]	–	–	CC_FORCE_ERROR	CC_TRYSNK	CC_MODE[1:0]		CC_DFP_LP	OTG_EN

Register Details

CHIP_ID (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	CID[7:0]							
Reset	0b01010000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CID	7:0	ID for BC89	0x50: ID for BC89

CHIP_REVISION (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	REVISION[3:0]				VERSION[3:0]			
Reset	0b0001				0b0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
REVISION	7:4	Silicon Revision	0x1: Pass1
VERSION	3:0		0

SWRST (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	SW_RST[7:0]							
Reset	0b00							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_RST	7:0	Software Reset	0xA5: Type-O registers are reset. SW_RST register is auto-clear as under Type-O reset control. Type-O registers including CHG_CNFG_00, CHG_CNFG_01, CHG_CNFG_02, CHG_CNFG_03, CHG_CNFG_04, CHG_CNFG_05, CHG_CNFG_06, CHG_CNFG_07, CHG_CNFG_08, CHG_CNFG_09, CHG_CNFG_10, CHG_CNFG_12, CHG_CNFG_13, CHG_CNFG_14, CHG_CNFG_15, SWRST, TOP_INT_MASK, BC_INTMASK, CC_INTMASK. The registers reset 10µs after the software reset command is received. All others: No Reset

TOP_INT (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BC_I	CC_I	CHG_I	TSHDN_I	SYSOVLO_I	SYSUVLO_I
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BC_I	5	BC Interrupt	0x0: No interrupt detected 0x1: Interrupt detected
CC_I	4	CC Interrupt	0x0: No interrupt detected 0x1: Interrupt detected
CHG_I	3	Chager Interrupt	0x0: No interrupt detected 0x1: Interrupt detected
TSHDN_I	2	Thermal Shutdown Interrupt	0x0: No interrupt detected 0x1: Interrupt detected
SYSOVLO_I	1	SYSOVLO Interrupt	0x0: No interrupt detected 0x1: Interrupt detected
SYSUVLO_I	0	SYSUVLO Interrupt	0x0: No interrupt detected 0x1: Interrupt detected

TOP_INT_MASK (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BC_M	CC_M	CHG_M	TSHDN_M	SYSOVLO_M	SYSUVLO_M
Reset	–	–	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BC_M	5	BC Interrupt Mask	0x0: Unmasked 0x1: Masked
CC_M	4	CC Interrupt Mask	0x0: Unmasked 0x1: Masked
CHG_M	3	Charger Interrupt Mask	0x0: Unmasked 0x1: Masked
TSHDN_M	2	Thermal Shutdown Interrupt Mask	0x0: Unmasked 0x1: Masked
SYSOVLO_M	1	SYSOVLO Interrupt Mask	0x0: Unmasked 0x1: Masked
SYSUVLO_M	0	SYSUVLO Interrupt Mask	0x0: Unmasked 0x1: Masked

TOP_INT_OK (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TSHDN_OK	SYSOVLO_OK	SYSUVLO_OK
Reset	–	–	–	–	–	0b1	0b1	0b1
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TSHDN_OK	2	Thermal Shutdown Status Indicator	0x0: Device is in thermal shutdown 0x1: Device is not in thermal shutdown
SYSOVLO_OK	1	SYSOVLO Status Indicator	0x0: SYS voltage is above SYSOVLO threshold 0x1: SYS voltage is below SYSOVLO threshold
SYSUVLO_OK	0	SYSUVLO Status Indicator	0x0: SYS voltage is below SYSUVLO threshold 0x1: SYS voltage is above SYSUVLO threshold

CHG_INT (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	TOPOFF_I	AICL_I	B2SOVRC_I	INLIM_I	CHGIN_I	CHG_I	BAT_I	BYP_I
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
TOPOFF_I	7	Top-off Interrupt	0b0: TOPOFF_OK bit has not changed since the last time this bit was read. 0b1: TOPOFF_OK bit has changed since the last time this bit was read.
AICL_I	6	AICL Interrupt	0b0: AICL_OK bit has not changed since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1: AICL_OK bit has changed since the last time this bit was read.
B2SOVRC_I	5	Battery to SYS Overcurrent Interrupt	0b0: B2SOVRC_OK bit has not changed since the last time this bit was read. 0b1: B2SOVRC_OK bit has changed since the last time this bit was read.
INLIM_I	4	CHGIN Input Current Limit Interrupt	0b0: INLIM_OK bit has not changed since the last time this bit was read. 0b1: INLIM_OK bit has changed since the last time this bit was read.
CHGIN_I	3	CHGIN Interrupt	0b0: CHGIN_OK bit has not changed since the last time this bit was read. 0b1: CHGIN_OK bit has changed since the last time this bit was read.
CHG_I	2	Charger Interrupt	0b0: CHG_OK bit has not changed since the last time this bit was read. 0b1: CHG_OK bit has changed since the last time this bit was read.
BAT_I	1	Battery Interrupt	0b0: BAT_OK bit has not changed since the last time this bit was read. 0b1: BAT_OK bit has changed since the last time this bit was read.
BYP_I	0	Bypass Node Interrupt	0b0: BYP_OK bit has not changed since the last time this bit was read. 0b1: BYP_OK bit has changed since the last time this bit was read.

CHG_INT_MASK (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	TOPOFF_M	AICL_M	B2SOVRC_M	INLIM_M	CHGIN_M	CHG_M	BAT_M	BYP_M
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TOPOFF_M	7	Top-off Interrupt Mask	0b0: Unmasked 0b1: Masked
AICL_M	6	AICL Interrupt Mask	0b0: Unmasked 0b1: Masked
B2SOVRC_M	5	Battery to SYS Overcurrent Interrupt Mask	0b0: Unmasked 0b1: Masked
INLIM_M	4	CHGIN Input Current Limit Mask	0b0: Unmasked 0b1: Masked
CHGIN_M	3	CHGIN Interrupt Mask	0b0: Unmasked 0b1: Masked
CHG_M	2	Charger Interrupt Mask	0b0: Unmasked 0b1: Masked
BAT_M	1	Battery Interrupt Mask	0b0: Unmasked 0b1: Masked
BYP_M	0	Bypass Interrupt Mask	0b0: Unmasked 0b1: Masked

CHG_INT_OK (0xB2)

BIT	7	6	5	4	3	2	1	0
Field	TOPOFF_OK	AICL_OK	B2SOVRC_OK	INLIM_OK	CHGIN_OK	CHG_OK	BAT_OK	BYP_OK
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TOPOFF_OK	7	Top-off Status Indicator	0b0: The charger is not in TOPOFF state 0b1: The charger is in TOPOFF state
AICL_OK	6	AICL Status Indicator	0b0: AICL mode 0b1: Not in AICL mode
B2SOVRC_OK	5	Battery to SYS Overcurrent Status Indicator	0b0: BATT to SYS exceeds the current limit 0b1: BATT to SYS does not exceed the current limit
INLIM_OK	4	CHGIN Input Current Limit Status Indicator	0b0: CHGIN input has reached the current limit 0b1: CHGIN input has not reached the current limit
CHGIN_OK	3	CHGIN Input Status Indicator	0b0: The CHGIN input is invalid. CHGIN_DTLS ≠ 0x03 0b1: The CHGIN input is valid. CHGIN_DTLS = 0x03
CHG_OK	2	Charger status indicator	0b0: The charger has suspended charging or TREG = 1 0b1: The charger is okay or the charger is off
BAT_OK	1	Battery Status Indicator	0b0: The battery has an issue or the charger has been suspended. BAT_DTLS ≠ 0x03, ≠ 0x04 and ≠ 0x07 0b1: The battery is okay. BAT_DTLS = 0x03,0x04 or 0x07
BYP_OK	0	Bypass Status Indicator	0b0: Something powered by the bypass node has hit current limit. BYP_DTLS ≠ 0x00 0b1: The bypass node is okay. BYP_DTLS = 0x00

CHG_DETAILS_00 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	–	CHGIN_DTLS[1:0]		–	–	–	–	–
Reset	–	0b00		–	–	–	–	–
Access Type	–	Read Only		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_DTLS	6:5	CHGIN Details	0b00: V_{BUS} is invalid. V_{CHGIN} rising: $V_{CHGIN} < V_{CHGIN\_UVLO}$ V_{CHGIN} falling: $V_{CHGIN} < V_{CHGIN\_REG}$ (AICL) 0b01: V_{BUS} is invalid. $V_{CHGIN} < V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0b10: V_{BUS} is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0b11: V_{BUS} is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ and $V_{CHGIN} > V_{BATT} + V_{CHGIN2SYS}$ and $V_{CHGIN} < V_{CHGIN\_OVLO}$

CHG_DETAILS_01 (0xB4)

BIT	7	6	5	4	3	2	1	0

Field	TREG	BAT_DTLS[2:0]	CHG_DTLS[3:0]
Reset	0b0	0b000	0b0000
Access Type	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	7	Temperature Regulation Status	0b0: The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 0b1: The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.
BAT_DTLS	6:4	Battery Details	0b000: No battery and the charger is suspended 0b001: V_{BATT} < V_{PQLB}. This condition is also reported in the CHG_DTLS as 0x00 0b010: The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06 0b011: The battery is okay and its voltage is greater than the minimum system voltage (V_{SYSMIN} < V_{BATT}), Q_{BAT} is on and V_{SYS} is approximately equal to V_{BATT}. 0b100: The battery is okay but its voltage is low: V_{PQLB} < V_{BATT} < V_{SYSMIN}. Q_{BAT} is operating like an LDO to regulate V_{SYS} to V_{SYSMIN}. 0b101: The battery voltage has been greater than the battery overvoltage flag threshold (CHG_CV_PRM + 200mV) for the last 30ms. Note that this flag is only generated when there is a valid input. 0b110: The battery has been overcurrent for at least 3ms since the last time this register has been read. 0b111: Battery level not available. In Only Battery mode, all battery comparators are off.
CHG_DTLS	3:0	Charger Details	0x00: Charger is in dead-battery prequalification or low-battery prequalification mode CHG_OK = 1 and V_{BATT} < V_{PQLB} and T_J < T_{SHDN} 0x01: Charger is in fast-charge constant current mode CHG_OK = 1and V_{BATT} < $V_{BATTREG}$ and T_J < T_{SHDN} 0x02: Charger is in fast-charge constant voltage mode CHG_OK = 1 and V_{BATT} = $V_{BATTREG}$ and T_J < T_{SHDN} 0x03: Charger is in top-off mode CHG_OK = 1 and V_{BATT} = $V_{BATTREG}$ and T_J < T_{SHDN} 0x04: Charger is in done mode CHG_OK = 0 and V_{BATT} > $V_{BATTREG}$ - V_{RSTRT} and T_J < T_{SHDN} 0x05: reserved 0x06: Charger is in timer fault mode CHG_OK = 0 and if BAT_DTLS=0b001 then V_{BATT} < V_{PQLB} or V_{BATT} < V_{PQDB} and T_J < T_{SHDN} 0x07: Charger is off because battery removal is detected on THM pin. CHG_OK = 0 0x08: Charger is off, charger input invalid and/or charger is disabled CHG_OK = 1 0x09: reserved 0x0A: Charger is off and the junction temperature is > T_{SHDN} CHG_OK = 0 0x0B: Charger is off because the watchdog timer expired CHG_OK = 0 0x0C: Charger is suspended or charge current or voltage is reduced based on JEITA control. This condition is also reported in THM_DTLS CHG_OK = 0

BITFIELD	BITS	DESCRIPTION	DECODE
			0x0D: reserved 0x0E: reserved 0x0F: reserved

CHG_DETAILS_02 (0xB5)

BIT	7	6	5	4	3	2	1	0
Field	–	THM_DTLS[2:0]			BYP_DTLS[3:0]			
Reset	–	0b000			0b0000			
Access Type	–	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
THM_DTLS	6:4	JEITA Temperature Status Details	0b000: Charger off due to cold status 0b001: Charging current reduction due to cool temperature 0b010: Normal condition 0b011: Termination voltage reduction due to warm temperature 0b100: Charger off due to hot status 0b101: No battery connected 0b110: THM disconnected 0b101 - 111: Reserved
BYP_DTLS	3:0	Bypass Node Details	0x0: The bypass node is okay 0x1: OTG_ILIM when CHG_CNFG_00. MODE = 0xA or 0xE or 0xF The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. UNO_ILIM when CHG_CNFG_00. MODE = 0x8 or 0xC or 0xD BYP_DTLS[0] status bit is latched until CHG_DETAILS_02 register read access is performed by AP. 0x2: BSTILIM The BYP reverse boost converter has hit its current limit and condition persisted for 30ms 0x4: BCKNeglLIM The BYP buck converter has hit the max negative demand current limit BYP_DTLS[2] status bit is latched until CHG_DETAILS_02 register read access is performed by AP.

CHG_CNFG_00 (0xB7)

BIT	7	6	5	4	3	2	1	0
Field	–	DISIBS	JEITA_DIS	WDTEN	MODE[3:0]			
Reset	–	0b0	0b0	0b0	0b0101			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DISIBS	6	BATT to SYS FET Disable Control	0b0: BATT to SYS FET is controlled by the power path state machine 0b1: BATT to SYS FET is forced off
JEITA_DIS	5	JEITA Enable	0b0: JEITA Enable 0b1: JEITA Disable
WDTEN	4	Watchdog Timer Enable Bit	0b0: Watchdog Timer Disabled 0b1: Watchdog Timer Enabled
MODE	3:0	Smart Power Selector Configuration	0x0: charger = off, OTG = off, buck = off, boost = off. The Q_{BAT} switch is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability 0x1: same as 0b0000 0x2: same as 0b0000 0x3: same as 0b0000 0x4: charger = off, OTG = off, buck = on, boost = off. When there is a valid input, the buck converter regulates the system voltage to be the maximum of (V_{SYSMIN} and CHG_CV_PRM). V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x5: charger = on, OTG = off, buck = on, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} x $R_{BAT2SYS}$. V_{BYP} is equal to V_{CHGIN} minus the resistive drops. 0x6: same as 0b0101 0x7: same as 0b0101 0x8: charger = off, OTG = off, buck = off, boost = on. BYP voltage is regulated to 5.1V (VBYP.OTG). 0x9: reserved 0xA: charger = off, OTG = on, buck = off, boost = on. The Q_{BAT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. Q_{CHGIN} is on allowing it to source current up to $I_{CHGIN.OTG.LIM}$. The boost target voltage is 5.1V ($V_{BYP.OTG}$). 0xB: reserved 0xC: reserved 0xD: reserved 0xE: reserved 0xF: reserved

CHG_CNFG_01 (0xB8)

BIT	7	6	5	4	3	2	1	0
Field	PQEN	LSEL	CHG_RSTRT[1:0]		RECYCLE_EN	FCHGTIME[2:0]		
Reset	0b1	0b00	0b00		0b1	0b100		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PQEN	7	Low-Battery Prequalification Mode Enable	0b0: Low-Battery prequalification mode is disabled 0b1: Low-Battery prequalification mode is enabled
LSEL	6	Inductor Selection	0b0: 0.47µH inductor 0b1: 1µH inductor
CHG_RSTRT	5:4	Charger Restart Threshold	0b00: 100mV below the value programmed by CHG_CV_PRM 0b01: 150mV below the value programmed by CHG_CV_PRM

BITFIELD	BITS	DESCRIPTION	DECODE
			10: 200mV below the value programmed by CHG_CV_PRM 11: disabled
RECYCLE_EN	3	B2S OCP or DISIBS Event Recycle Option	0b0: In case of B2S OCP **or** DISIBS events, buck is disabled (OFF) and Q_{BAT} FET is opened. System will recycle after 150ms (min) only in case a valid charger is present. 0b1: In case of B2S OCP **or** DISIBS events, buck is disabled (OFF) and Q_{BAT} FET is opened. System will recycle after 150ms (min).
FCHGTIME	2:0	Fast-Charge Timer setting (t_{FC}, hrs)	0b000: disable 0b001: 3 0b010: 4 0b011: 5 0b100: 6 0b101: 7 0b110: 8 0b111: 10

CHG_CNFG_02 (0xB9)

BIT	7	6	5	4	3	2	1	0
Field	OTG_ILIM[1:0]		CHGCC[5:0]					
Reset	0b11		0b001010					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
OTG_ILIM	7:6	CHGIN Output Current Limit (mA)	0b00: 500 0b01: 900 0b10: 1200 0b11: 1500
CHGCC	5:0	Fast-Charge Current Selection(mA). When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.10A (0x00) to 3.0A (0x3C) in 50mA step. Note that the first 3 codes are all 100mA. Note that the thermal foldback loop can reduce the battery charger's target current by $A_{TJREG.}$	0x00: 100 0x01: 100 0x02: 100 0x03: 150 0x04: 200 0x05: 250 0x06: 300 0x07: 350 0x08: 400 0x09: 450 0x0A: 500 0x0B: 550 0x0C: 600 0x0D: 650 0x0E: 700 0x0F: 750 0x10: 800 0x11: 850 0x12: 900 0x13: 950 0x14: 1000 0x15: 1050 0x16: 1100 0x17: 1150 0x18: 1200 0x19: 1250 0x1A: 1300

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1B: 1350 0x1C: 1400 0x1D: 1450 0x1E: 1500 0x1F: 1550 0x20: 1600 0x21: 1650 0x22: 1700 0x23: 1750 0x24: 1800 0x25: 1850 0x26: 1900 0x27: 1950 0x28: 2000 0x29: 2050 0x2A: 2100 0x2B: 2150 0x2C: 2200 0x2D: 2250 0x2E: 2300 0x2F: 2350 0x30: 2400 0x31: 2450 0x32: 2500 0x33: 2550 0x34: 2600 0x35: 2650 0x36: 2700 0x37: 2750 0x38: 2800 0x39: 2850 0x3A: 2900 0x3B: 2950 0x3C: 3000 0x3D: 3050 0x3E: 3100 0x3F: 3150

CHG_CNFG_03 (0xBA)

BIT	7	6	5	4	3	2	1	0
Field	–	TO_TIME[2:0]			TO_ITH[3:0]			
Reset	–	0b000			0b0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TO_TIME	6:4	Top-Off Timer Setting	0b000: 30sec 0b001: 10min 0b010: 20min 0b011: 30min 0b100: 40min 0b101: 50min 0b110: 60min 0b111: 70min

BITFIELD	BITS	DESCRIPTION	DECODE
TO_ITH	3:0	Top-Off Current Threshold (mA). The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME.	0b0000: 50 0b0001: 70 0b0010: 90 0b0011: 110 0b0100: 130 0b0101: 150 0b0110: 170 0b0111: 190 0b1000: 210 0b1001: 230 0b1010: 250 0b1011: 270 0b1100: 290 0b1101: 310 0b1110: 330 0b1111: 350

CHG_CNFG_04 (0xBB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CHG_CV_PRM[5:0]					
Reset	–	–	0b011000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV_PRM	5:0	Charge Termination Voltage Setting(V) The voltage options are from 3.6V to 4.0V in 100mV step, from 4.0V to 4.55V in 10mV step.	0x00: 3.600 0x01: 3.700 0x02: 3.800 0x03: 3.900 0x04: 4.000 0x05: 4.010 0x06: 4.020 0x07: 4.030 0x08: 4.040 0x09: 4.050 0x0A: 4.060 0x0B: 4.070 0x0C: 4.080 0x0D: 4.090 0x0E: 4.100 0x0F: 4.110 0x10: 4.120 0x11: 4.130 0x12: 4.140 0x13: 4.150 0x14: 4.160 0x15: 4.170 0x16: 4.180 0x17: 4.190 0x18: 4.200 0x19: 4.210 0x1A: 4.220 0x1B: 4.230 0x1C: 4.240 0x1D: 4.250 0x1E: 4.260 0x1F: 4.270 0x20: 4.280 0x21: 4.290

BITFIELD	BITS	DESCRIPTION	DECODE
			0x22: 4.300 0x23: 4.310 0x24: 4.320 0x25: 4.330 0x26: 4.340 0x27: 4.350 0x28: 4.360 0x29: 4.370 0x2A: 4.380 0x2B: 4.390 0x2C: 4.400 0x2D: 4.410 0x2E: 4.420 0x2F: 4.430 0x30: 4.440 0x31: 4.450 0x32: 4.460 0x33: 4.470 0x34: 4.480 0x35: 4.490 0x36: 4.500 0x37: 4.510 0x38: 4.520 0x39: 4.530 0x3A: 4.540 0x3B: 4.550 0x3C: 4.550 0x3D: 4.550 0x3E: 4.550 0x3F: 4.550

CHG_CNFG_05 (0xBC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	B2SOVRC[3:0]			
Reset	–	–	–	–	0b1110			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
B2SOVRC	3:0	BATT to SYS Overcurrent Threshold (A)	0x0: Disabled 0x1: 3.0 0x2: 3.5 0x3: 4.0 0x4: 4.2 0x5: 4.4 0x6: 4.5 0x7: 4.6 0x8: 4.8 0x9: 5.0 0xA: 5.2 0xB: 5.4 0xC: 5.6 0xD: 5.8 0xE: 6.0 0xF: 6.2

BITFIELD	BITS	DESCRIPTION	DECODE

CHG_CNFG_06 (0xBD)

BIT	7	6	5	4	3	2	1	0
Field	B2SOVRC_DTC	–	–	DIS_AICL	CHGPROT[1:0]		WDTCLR[1:0]	
Reset	0b0	–	–	0b0	0b0		0b00	
Access Type	Write, Read	–	–	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
B2SOVRC_DTC	7	BATT to SYS Overcurrent Debounce to Q_{BAT} clear control.	0x0: Tocp is 6ms 0x1: Tocp is 100ms
DIS_AICL	4	AICL Disable feature.This applies for both CHGIN and WCIN inputs	0b0: AICL feature is not disabled 0b1: AICL feature is disabled
CHGPROT	3:2	Charger Settings Protection Bits. Writing 0x3 to these bits unlocks the write capability for the registers which are "Protected with CHGPROT". Writing any value besides 0x3 locks the protected registers.	0x0: Write capability locked. 0x1: Write capability locked. 0x2: Write capability locked. 0x3: Write capability unlocked.
WDTCLR	1:0	Watchdog Timer Clear Bit. Writing "01" to these bits clears the watchdog timer when the watchdog timer is enabled.	0b00: the watchdog timer is not cleared 0b01: the watchdog timer is cleared 0b10: the watchdog timer is not cleared 0b11: the watchdog timer is not cleared

CHG_CNFG_07 (0xBE)

BIT	7	6	5	4	3	2	1	0
Field	WD_QBATOFF	REGTEMP[3:0]				–	–	FSHIP_MODE
Reset	0b0	0b1001				–	–	0b0
Access Type	Write, Read	Write, Read				–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WD_QBATOFF	7	Q_{BAT} FET control under Watchdog condition.	0b0: When watchdog timer expires, turn off only the charger 0b1: When watchdog timer expires, turn off buck, charger, and Q_{BAT} switch for 150ms
REGTEMP	6:3	Junction Temperature Thermal Regulation (°C). The charger's target current limit starts to foldback and	0x0: 85 0x1: 90 0x2: 95

BITFIELD	BITS	DESCRIPTION	DECODE
		the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x3: 100 0x4: 105 0x5: 110 0x6: 115 0x7: 120 0x8: 125 0x9: 130
FSHIP_MODE	0	Factory Ship Mode. When asserted to "1", system enters in Factory Ship mode. This bit can be reset by battery removal or on a valid charger input plug.	0b0: Not Factory Ship mode 0b1: Factory Ship mode

CHG_CNFG_08 (0xBF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FSW[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FSW	1:0	Switching Frequency Options (MHz)	0b00: 2.6MHz 0b01: 1.76MHz 0b10: 1.3MHz 0b11: Forbidden

CHG_CNFG_09 (0xC0)

BIT	7	6	5	4	3	2	1	0
Field	CHG_EN	CHGIN_ILIM[6:0]						
Reset	0b0	0b0010011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_EN	7	Charger Software enable. Enable charger without waiting for enable signal from USBC.	0b0: Don't enable charger. Charger is only enabled by USBC 0b1: Enable charger without waiting for enable from USBC
CHGIN_ILIM	6:0	CHGIN Input Current Limit(mA). 7-bit adjustment from100mA to 3.2A in 25mA steps. Note that the first 4 codes are all 100mA.	0x00: 100 0x01: 100 0x02: 100 0x03: 100 0x04: 125 0x05: 150 0x06: 175 0x07: 200 0x08: 225 0x09: 250

BITFIELD	BITS	DESCRIPTION	DECODE
			0x0A: 275 0x0B: 300 0x0C: 325 0x0D: 350 0x0E: 375 0x0F: 400 0x10: 425 0x11: 450 0x12: 475 0x13: 500 0x14: 525 0x15: 550 0x16: 575 0x17: 600 0x18: 625 0x19: 650 0x1A: 675 0x1B: 700 0x1C: 725 0x1D: 750 0x1E: 775 0x1F: 800 0x20: 825 0x21: 850 0x22: 875 0x23: 900 0x24: 925 0x25: 950 0x26: 975 0x27: 1000 0x28: 1025 0x29: 1050 0x2A: 1075 0x2B: 1100 0x2C: 1125 0x2D: 1150 0x2E: 1175 0x2F: 1200 0x30: 1225 0x31: 1250 0x32: 1275 0x33: 1300 0x34: 1325 0x35: 1350 0x36: 1375 0x37: 1400 0x38: 1425 0x39: 1450 0x3A: 1475 0x3B: 1500 0x3C: 1525 0x3D: 1550 0x3E: 1575 0x3F: 1600 0x40: 1625 0x41: 1650 0x42: 1675 0x43: 1700 0x44: 1725 0x45: 1750 0x46: 1775 0x47: 1800 0x48: 1825 0x49: 1850 0x4A: 1875 0x4B: 1900 0x4C: 1925 0x4D: 1950 0x4E: 1975 0x4F: 2000

BITFIELD	BITS	DESCRIPTION	DECODE
			0x50: 2025 0x51: 2050 0x52: 2075 0x53: 2100 0x54: 2125 0x55: 2150 0x56: 2175 0x57: 2200 0x58: 2225 0x59: 2250 0x5A: 2275 0x5B: 2300 0x5C: 2325 0x5D: 2350 0x5E: 2375 0x5F: 2400 0x60: 2425 0x61: 2450 0x62: 2475 0x63: 2500 0x64: 2525 0x65: 2550 0x66: 2575 0x67: 2600 0x68: 2625 0x69: 2650 0x6A: 2675 0x6B: 2700 0x6C: 2725 0x6D: 2750 0x6E: 2775 0x6F: 2800 0x70: 2825 0x71: 2850 0x72: 2875 0x73: 2900 0x74: 2925 0x75: 2950 0x76: 2975 0x77: 3000 0x78: 3025 0x79: 3050 0x7A: 3075 0x7B: 3100 0x7C: 3125 0x7D: 3150 0x7E: 3175 0x7F: 3200

CHG_CNFG_10 (0xC1)

BIT	7	6	5	4	3	2	1	0
Field	INLIM_CLK[1:0]		–	–	–	MINVSYS[2:0]		
Reset	0b10		–	–	–	0b101		
Access Type	Write, Read		–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
INLIM_CLK	7:6	Input current limit soft start clock(µsec)	0b00: 8 0b01: 256

BITFIELD	BITS	DESCRIPTION	DECODE
			0b10: 1024 0b11: 4096
MINVSYS	2:0	Minimum SYS Voltage	0x0: 3.0V 0x1: 3.1V 0x2: 3.2V 0x3: 3.3V 0x4: 3.4V 0x5: 3.5V 0x6: 3.6V 0x7: 3.7V

CHG_CNFG_12 (0xC3)

BIT	7	6	5	4	3	2	1	0
Field	NO_AUTOISET	–	–	VCHGIN_REG[1:0]		–	–	DISKIP
Reset	0b0	–	–	0b00		–	–	0b0
Access Type	Write, Read	–	–	Write, Read		–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
NO_AUTOISET	7	Bypass USBC control for INLIM	0x0: USBC 0x1: CHGIN_ILIM
VCHGIN_REG	4:3	CHGIN Voltage Regulation Threshold (VCHGIN_REG) Adjustment. The CHGIN to GND Minimum Turn-On Threshold (VCHGIN_UVLO) also scales with this adjustment.	0b00: VCHGIN_REG = 4.5V and VCHGIN_UVLO = 4.7V 0b01: VCHGIN_REG = 4.6V and VCHGIN_UVLO = 4.8V 0b10: VCHGIN_REG = 4.7V and VCHGIN_UVLO = 4.9V 0b11: VCHGIN_REG = 4.85V and VCHGIN_UVLO = 5.05V
DISKIP	0	Charger skip mode disable	0b0: Auto Skip mode 0b1: Disable skip mode

CHG_CNFG_13 (0xC6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	STBY_EN	QBAT_RST	tQBAT_RST	FSHIP_DLY	tFSHIP_DLY	–
Reset	–	–	0b0	0b00	0b1	0b1	0b0	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
STBY_EN	5	CHGIN Standby Enable	0b0: DC-DC is controlled by the power-path state machine 0b1: Force DC-DC off. Device goes to CHGIN low quiescent current standby.
QBAT_RST	4	Q_{BAT} reset	0b0: Q_{BAT} is ON 0b1: Q_{BAT} is OFF
tQBAT_RST	3	Q_{BAT} reset timing	0b0: 1s 0b1: 5s

BITFIELD	BITS	DESCRIPTION	DECODE
FSHIP_DLY	2	Delay for entering FSHIP Mode	0b0: enter immediately FSHIP Mode when FSHIP bit is set 0b1: enter FSHIP in tFSHIP_DLY when FSHIP bit is set
tFSHIP_DLY	1	Delay entering FSHIP Mode	0b0: 1s 0b1: 5s

CHG_CNFG_14 (0xC7)

BIT	7	6	5	4	3	2	1	0
Field	HOTCOLD_EN	VCHG_CV_WARM[1:0]		ICHG_CC_COOL[1:0]		SS_PAT	SS_ENV	SS_EN
Reset	0b0	0b11		0b11		0b1	0b00	0b00
Access Type	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HOTCOLD_EN	7	JEITA Enable when HOT or COLD	0b0: HOTCOLD Enable 0b1: HOTCOLD Disable
VCHG_CV_WARM	6:5	JEITA controller battery termination voltage when thermistor temperature is between T_{WARM} and T_{HOT}	0x0, 0x1: Battery termination voltage is set by CHG_CV_PRM 0x2: Battery termination voltage is set by (CHG_CV_PRM - 100mV) 0x3: Battery termination voltage is set by (CHG_CV_PRM - 150mV)
ICHG_CC_COOL	4:3	JEITA controller battery fast-charge current when thermistor temperature is between T_{COLD} and T_{COOL}	0x0, 0x1 : Battery fast-charge current is set by CHGCC 0x2: Battery fast-charge current is reduced to 20% of CHGCC 0x3: Battery fast-charge current is reduced to 50% of CHGCC
SS_PAT	2	Spread-Spectrum Pattern Setting	0b0: Linear pattern 0b1: Pseudo-random pattern
SS_ENV	1	Spread-Spectrum Envelope Setting	0b0: ±6% 0b1: ±9%
SS_EN	0	Spread Spectrum Enable	0b0: Disable 0b1: Enable

CHG_CNFG_15 (0xD5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VCHG_CV_COOL_EN	STAT2_USAGE	STAT2_CTL	STAT2_MAN_CTL
Reset	–	–	–	–	0b1	0b00	0b00	0b00
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VCHG_CV_COOL_EN	3	Enable CHGCV Reduction in Cool	0b0: No Change in CHGCV when cool 0b1: CHGCV is reduced according to VCHG_CV_WARM if reduced CHGCC reaches 100mA limit
STAT2_USAGE	2	STAT2 PIN Usage	0b0: FAULT Indication 0b1: Adaptor detection done Indication
STAT2_CTL	1	STAT2 PIN Control	0b0: STAT2 PIN is controlled via State machine 0b1: STAT2 PIN is manually controlled via FAULTP_MAN_CTL
STAT2_MAN_CTL	0	STAT2 PIN Manual Control	0b0: High 0b1: Low

USB_TYPE_DTLS (0xC4)

BIT	7	6	5	4	3	2	1	0
Field	–	CHG_TYP[1:0]		PR_CHG_TYP[2:0]			CC_CURR[1:0]	
Reset	–	0b0					0b0	
Access Type	–	Read Only		Read Only			Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_TYP	6:5	Readback BC1.2 standard adaptor detection:	0x0: No adaptor found 0x1: SDP (500mA input current) 0x2: CDP (1.5A input current) 0x3: DCP (1.5A input current)
PR_CHG_TYP	4:2	Readback type of proprietary adaptor detected:	0x1: Samsung 2A 0x2: Apple 500mA 0x3: Apple 1A 0x4: Apple 2A 0x5: Apple 12W (Input current = 2.5A) 0x6: DCP 3A 0x7: Unknown
CC_CURR	1:0	Readback CC current capability detection.	0x0: Not connected 0x1: 500mA input current 0x2: 1.5A input current 0x3: 3.0A input current

USB_ILIM_DTLS (0xC5)

BIT	7	6	5	4	3	2	1	0
Field	–	USB_INLIM[6:0]						
Reset	–	0b0						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
USB_INLIM	6:0	Readback USB adaptor input current limit. Settings corresponds to charger input current limit. See tab Chgr Settings for current threshold

BC_CTRL1 (0xC8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DCDCpl	–	DetAbrt_Dis	ChgDetEn
Reset	–	–	–	–	0b1	–	0b0	0b1
Access Type	–	–	–	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DCDCpl	3	Data Contact Detection Time Out	0b0: 2s 0b1: 900ms
DetAbrt_Dis	1	BC1.2 Dependency from Type C	0b0: Type C will stop BC1.2 detection 0b1: BC1.2 is now independent of Type C
ChgDetEn	0	Enable Charger Detection	0b0: Not Enabled 0b1: Enabled. Charger detection runs every time V_{BUS} > V_{VBDET} and DetAbrt = 0

BC_CTRL2 (0xC9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CHGIN_INLIM_Gate	SDPMaxCurr[1:0]		CDPMaxCurr
Reset	–	–	–	–	0b0	0b00		0b0
Access Type	–	–	–	–	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_INLIM_Gate	3	CHGIN_INLIM Control Options	0b0: No gating of CHGIN_INLIM setting by BC1.2 FSM 0b1: Gate changes in CHGIN_ILIM until BC1.2 FSM completes
SDPMaxCurr	2:1	SDP non-standard type-C cable control. Requires CHGIN_INLIM_Gate = '1' Type-C to Type A cable may have incorrect CC resistor indicating 1.5A/3A.	0b00: No modification of CHGIN_INLIM 0b01: CHGIN_INLIM = 500mA 10: CHGIN_INLIM = 1A 11: CHGIN_INLIM = 1.5A
CDPMaxCurr	0	CDP non-standard type-C control. Requires CHGIN_INLIM_Gate = '1' Type C to type A cable may have incorrect CC resistor indicating 1.5A/3A.	0x0: No modification of CHGIN_INLIM 0x1: CHGIN_INLIM = 1.5A (0x2D)

CC_CTRL1 (0xCA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CCDetEn
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CCDetEn	0	Enable CC pin detection	0b0: Disable 0b1: Enable

BC_INT (0xCB)

BIT	7	6	5	4	3	2	1	0
Field	VBUSDetI	–	–	–	–	propChgTypI	dcdTmoI	chgTypI
Reset	0b0	–	–	–	–	0b0	0b0	0b0
Access Type	Read Clears All	–	–	–	–	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUSDetI	7	V_{BUS} Voltage Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
propChgTypI	2	Proprietary Charger Type Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
dcdTmoI	1	Data Contact Detect (DCD) Timer Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
chgTypI	0	Charger Type Interrupt	0b0: No Interrupt 0b1: Interrupt Detected

CC_INT (0xCC)

BIT	7	6	5	4	3	2	1	0
Field	–	VSAFE0VI	DetAbrtI	–	CCPinStatI	CCIStatI	–	CCStatI
Reset	–	0b0	0b0	–	0b0	0b0	–	0b0
Access Type	–	Read Clears All	Read Clears All	–	Read Clears All	Read Clears All	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VSAFE0VI	6	VSAFE0V Status Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
DetAbrtI	5	Charger Abort Detection Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
CCPinStatI	3	CCPinStat Status Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
CCIStatI	2	CCIStat Status Interrupt	0b0: No Interrupt 0b1: Interrupt Detected
CCStatI	0	CCStat Status Interrupt	0b0: No Interrupt 0b1: Interrupt Detected

BC_INTMASK (0xCD)

BIT	7	6	5	4	3	2	1	0
Field	VBUSDetM	–	–	–	–	propChgTypM	dcdTmoM	chgTypM
Reset	0b1	–	–	–	–	0b1	0b1	0b1
Access Type	Write, Read	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBUSDetM	7	V_{BUS} Voltage Interrupt Mask	0b0: Unmasked 0b1: Masked
propChgTypM	2	Proprietary Charger Type Interrupt Mask	0b0: Unmasked 0b1: Masked
dcdTmoM	1	Data Contact Detect (DCD) Timer Interrupt Mask	0b0: Unmasked 0b1: Masked
chgTypM	0	Charger Type Interrupt Mask	0b0: Unmasked 0b1: Masked

CC_INTMASK (0xCE)

BIT	7	6	5	4	3	2	1	0
Field	–	VSAFE0VM	DetAbrtM	–	CCPinStatM	CCIStatM	–	CCStatM
Reset	–	0b1	0b1	–	0b1	0b1	–	0b1
Access Type	–	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VSAFE0VM	6	VSAFE0V Status Interrupt Mask	0b0: Unmasked 0b1: Masked
DetAbrtM	5	Charger Abort Detection Mask	0b0: unmasked 0b1: masked
CCPinStatM	3	CCPin Status Interrupt Mask	0b0: Unmasked 0b1: Masked

BITFIELD	BITS	DESCRIPTION	DECODE
CCIStatM	2	CCIStat Status Interrupt Mask	0b0: Unmasked 0b1: Masked
CCStatM	0	CCStat Status Interrupt Mask	0b0: Unmasked 0b1: Masked

BC_STATUS1 (0xCF)

BIT	7	6	5	4	3	2	1	0
Field	VBUSDet	–	–	–	–	DCDTmo	–	–
Reset	0b0	–	–	–	–	0b0	–	–
Access Type	Read Only	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VBUSDet	7	Status of V_{BUS} Detection	0x0: VBUS < VBDET 0x1: VBUS > VBDET
DCDTmo	2	During Charger Detection, DCD detectnion timed out. Indicates D+/D- are open. BC1.2 detection continues as required by BC1.2 specification but SDP most likely is found.	0x0: No Timeout or detction has not run 0x1: DCD Timeout occurred

CC_STATUS1 (0xD0)

BIT	7	6	5	4	3	2	1	0
Field	CCPinStat[1:0]		CCIStat[1:0]		–	CCStat[2:0]		
Reset	0b00		0b00		–	0b00		
Access Type	Read Only		Read Only		–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
CCPinStat	7:6	Output of Active CC Pin	0x0: No Determination 0x1: CC1 Active 0x2: CC2 Active 0x3: RFU
CCIStat	5:4	CC Pin Detected Allowed V_{BUS} Current in UFP mode	0x0: Not in UFP mode 0x1: 500mA 0x2: 1.5A 0x3: 3.0A
CCStat	2:0	CC Pin State Machine Detection	0x0: No Connection 0x1: SINK 0x2: SOURCE 0x3: RFU

CC_STATUS2 (0xD1)

BIT	7	6	5	4	3	2	1	0
Field	CC1VRA	CC2VRA	CC_VUFP_RD0P5	CC_VUFP_RD1P5	VSAFE0V	DetAbrt	–	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CC1VRA	7	CC1_VRA_RD0.5 Status	0x0: CC1 < 600mV (CC_DFP_LP = 1) / 200mV (CC_DFP_LP = 0) 0x1: CC1 > 600mV (CC_DFP_LP = 1) / 200mV (CC_DFP_LP = 0)
CC2VRA	6	CC2_VRA_RD0.5 Status	0x0: CC2 < 600mV (CC_DFP_LP = 1) / 200mV (CC_DFP_LP = 0) 0x1: CC2 > 600mV (CC_DFP_LP = 1) / 200mV (CC_DFP_LP = 0)
CC_VUFP_RD0P5	5	CC_VUFP_RD0.5 Status	0x0: CC < 400mV (in DFP) / 660mV (in UFP) 0x1: CC > 400mV (in DFP) / 660mV (in UFP)
CC_VUFP_RD1P5	4	CC_VUFP_RD1.5 Status	0x0: CC < 1.8V (in DFP) / 1.25V (in UFP) 0x1: CC > 1.8V (in DFP) / 1.25V (in UFP)
VSAFE0V	3	Status of VBUS Detection	0x0: V_{BUS} < VSAFE0V 0x1: V_{BUS} > VSAFE0V. Valid only in Attached.SRC_CCx, Attached.SNK_CCx state
DetAbrt	2	Charger Abort Detection	0b0: 0: Charger detection runs if ChgDetEn = 1 and V_{BUS} is valid for the debounce time. 0b1: 1: Charger detection is aborted by Type-C state machine. Charger does not run if Chg EetEn = 1 and V_{BUS} is valid for the debounce time. DetAbrt = 1 immediately stops the in progress detection.

BC_CTRL3 (0xD2)

BIT	7	6	5	4	3	2	1	0
Field	–	DPDNMan	DPDrv[1:0]		DNDrv[1:0]		DPDNAuto	–
Reset	–	0b0	0b0		0b00		0b1	–
Access Type	–	Write, Read	Write, Read		Write, Read		Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
DPDNMan	6	DPDN Manual Control Enabled	0x0: Resources on DP and DN are controlled by charger detection(ChgDetEn bit) 0x1: Drive voltages on DP and DN according to DPDrv and DNDrv values
DPDrv	5:4	DP Drive	0x0: GROUND (15k resistor to GND) 0x1: 0.6V 0x2: 3.3V 0x3: Open
DNDrv	3:2	DN Drive	0x0: GROUND (15k resistor to GND) 0x1: 0.6V 0x2: 3.3V 0x3: Open

BITFIELD	BITS	DESCRIPTION	DECODE
DPDNAuto	1	DP/DN automatic configuration	0x0: DP/DN configured by DPDNMan 0x1: DP/DN configured by CCstat = 0x02(source) DP = 3.3V DN = 3.3V

CC_CTRL3 (0xD4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CC_FORCE_ERROR	CC_TRYSNK	CC_MODE[1:0]		CC_DFP_LP	OTG_EN
Reset	–	–	0b0	0b1	0b11		0b1	0b1
Access Type	–	–	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_FORCE_ERROR	5	CC Force Error	0x0: Normal Operation 0x1: State Machine Forced to Reset
CC_TRYSNK	4	Try Sink Functionality	0x0: Try.SNK Disabled 0x1: Try.SNK Enabled
CC_MODE	3:2	DRP Mode setting	0x1: SNK Mode 0x2: SRC Mode 0x3: DRP Mode
CC_DFP_LP	1	Enabling 80uA current source when detecting SNK Device	0x0: High-Powe Mode - 80µA Current Source Used when Detecting SNK Device 0x1: Low-Power Mode - 1.2/5µA Current Source Used when Detecting SNK Device (5µA is selected using an OTP option)
OTG_EN	0	OTG Enable Configuration	0x0: Reverse Boost Enabled via Charger Mode 0x1: Reverse Boost Enabled via CCStat Bit

Applications Information

Charger Register Protection Bit

The MAX77789 charger registers are protected by default; AP requires unlocking in CHG_CNFG_06[3:2] in order to configure a new set. The CHGPROT bit is locking the CHG_CNFG_01:05 and 07:15 registers.

Input Current Limit Setting (CHGIN_INLIM)

The MAX77789 is configurable through I^2C communication. The CHGIN input current limit can be reprogrammed with CHGIN_ILIM [6:0] from 100mA to 3.2A in 25mA steps, and the 0x00, 0x01, 0x02, and 0x03 are all set to 100mA; the default setting after POR is set by the information of the charger type detection result.

Battery Termination Voltage Setting (CHG_CV_PRM)

The MAX77789 is configurable through I^2C communication. The battery termination voltage (VBATREG) can be reprogrammed with register of CHG_CV_PRM [5:0] from 3.6V to 4.0V in 100mV steps and from 4.0V to 4.55V in 10mV steps.

The default setting of termination voltage is 4.20V (0x18).

Fast-Charge Current Setting (CHGCC)

While a valid input source is present, the battery charger attempts to charge the battery with a fast-charge current determined by the register of CHGCC[5:0]. The range of the setting is from 100mA to 3.0A in 50mA steps. Note that the first three bit, 0x00, 0x01, and 0x02 are all 100mA. The default setting of CHGCC is 500mA (0x0A).

TOP-OFF Current and Time Setting (TO_ITH / TO_TIME)

When the battery charging current is detected in I_{TO} for $t_{TERM,}$ the MAX77789 enters the top-off state.

The top-off current threshold (I_{TO}) can be programmed using the TO_ITH[3:0] register, and the top-off time can be set using the TO_TIME[6:4] register.

Charger Status Outputs (INOKB / STAT1)

Input Status (INOKB)

INOKB is an open-drain and active-low output that indicates input status. If a valid input source is inserted and the buck converter starts switching, INOKB pulls low. When the reverse boost is enabled, INOKB pulls low to indicate a 5V output from CHGIN. INOKB can be used as a logic output for the system processor by adding a 200kΩ pullup resistor to the system IO voltage and can also be used as a LED indicator driver by adding a current limit resistor and a LED to SYS.

Charging Status Output (STAT1)

STAT1 is an open-drain and active-low output that indicates charge status. STAT1 status changes as shown in *Table 5*.

Table 5. STAT Output Per Charging Status

CHARGING STATUS	STAT1	LOGIC STATE	CHARGE STATUS LED
No input	High impedance	High	Off
Trickle, pre-charge, fast charge	Repeat low and high impedance with 1Hz, 50% duty cycle	After an external diode and a capacitor rectifier, high	Blinking with 1Hz, 50% duty cycle.
Top-off and done	Low	Low	Solid on
Faults	High impedance	High	Off

STAT1 can be used as a logic output for the system processor by adding a 200kΩ pullup resistor to the system IO voltage and a rectifier (a diode and a capacitor).

STAT1 can also be used as a LED indicator driver by adding a current limit resistor and a LED to SYS.

STAT2 pin

STAT2 is an open-drain and active-low output indicate either the fault indication or the charger type detection done indication. The MA77789 provides flexibility in the usage of the STAT2 pin through the register setting STAT2_USAGE.

The STAT2 pin also has options to be controlled by either a state machine or an external MCU through the register STAT2_CTL. In case of STAT2_CTL =1, the user can control STAT2 pin high or low through STAT2_MAN_CTL.

USAGE	INPUT	INITIAL STATE	AFTER STATE
Fault indication	Charger timer fault THERMAL Shutdown SYS OVLO / UVLO	High	Low
Charger type detection done	DCP	Low	Low
	SDP / CDP	Low	High

EXTSM pin

The EXTSM pin is an active-high input. When the EXTSM pin is pulled high. The MAX77789 is operating in three ways based on the status of the IC.

1. Exit from Ship Mode.

   When the MAX77789 is under factory ship mode by FSHIP_MODE = 1, pulling the EXTSM pin high for 10ms forces the MAX77789 to exit from ship mode, hence Q_{BAT} is turning ON.

2. System Reset

   When the MAX77789 is under the status that FSHIP_MODE = 0, QBAT_RST = 0, and CHGIN invalid, pulling the EXTSM pin high for 10s forces the MAX77789 enter the system reset mode, in which the battery and SYS are isolated, Q_{BAT} is turned off, Hence the SYS voltage drops under the System POR threshold. After releasing the EXTSM pin, Q_{BAT} is turning ON to provide Power to SYS.

3. Disable Battery Charging

   When the MAX77789 is charging the battery and its status is FSHIP_MODE = 0, QBAT_RST = 0, and CHGIN valid.

   The logic high on the EXTSM pin have the MAX77789 stop charging the battery and Q_{BAT} is turned off.

STBY Pin for USB Suspend Mode

The host can reduce the CHGIN supply current of the MAX77989 by driving the STBY pin to high. When STBY is pulled high or the register of STBY_EN = 1, the DC-DC turns off. When STBY is pulled low or the register STBY_EN = 0, the DC-DC is controlled by the power path state machine.

D+/D- Multiplexing

USB D+/D- lines, which are used for the detection of BC1.2 and proprietary TAs (Travel Adaptors), can be used for USB 2.0 data communication. If a MCU handles this communication in the target system, the D+/D- lines can be connected to the MAX77789 and the MCU like in *Figure 21*. As shown in *Figure 21*, switchers are required for each D+ and D- lines to guarantee Hi-Z for the connections to the MCU in order to avoid the wrong detections of TAs. The STAT2 pin function can be repurposed to indicate the completion of BC1.2 detection and Proprietary TA detection. In order for the STAT2 pin to indicate BC1.2 and Proprietary TA detection completed, the MCU is configured as STAT2_USAGE = 1.

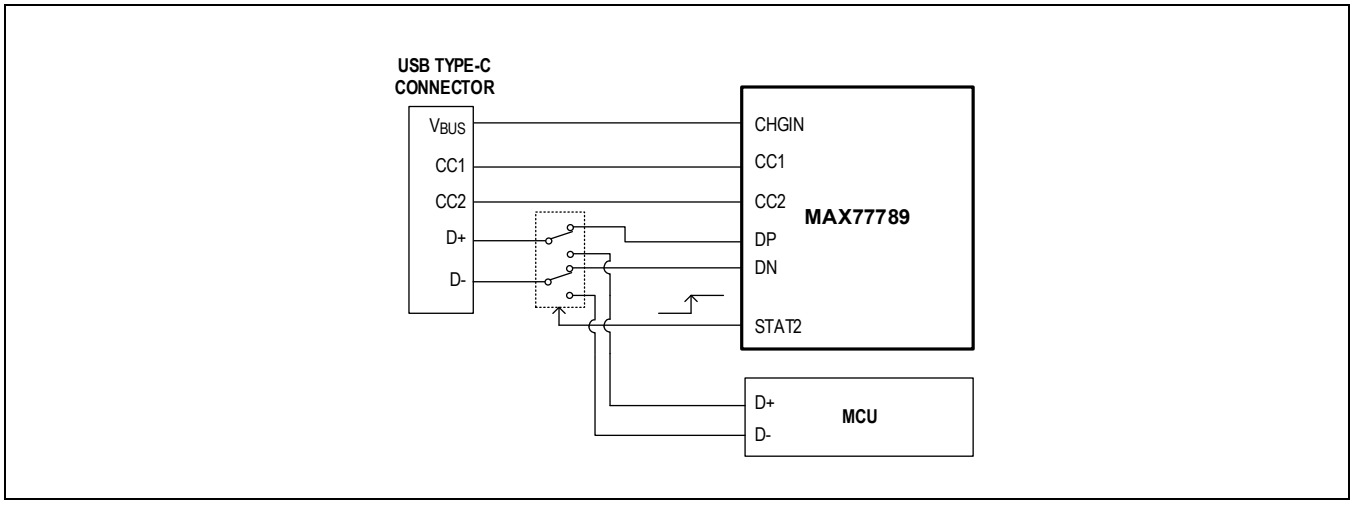


Figure 21. D+/D- Connections in a Reference System

Type-C Error Recovery State

The MAX77789 supports ErrorRecovery state based on the Type-C specification. The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for ErrorRecovery followed by transitioning to appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.

The host forces the system to enter ErrorRecovery by writing CC_CTRL3[5] =1, and this register bit should be reset by the host after ErrorRecovery is completed.

Capacitor Selection

All capacitors should be X5R dielectric or better. Be aware that multilayer ceramic capacitors have large voltage coefficients. Before selecting capacitors, check for sufficient voltage rating and derated capacitance at max operating voltage condition. *Table 6* shows the proper capacitors after considering the derating and operating voltage.

Table 6. Capacitor Selections

PIN	TYPE
CHGIN Capacitor	2.2µF/16V
BYP Capacitor	10µF + 22µF/16V
SYS Capacitor	2 x 10µF/10V
BATT Capacitor	10µF/10V
VDD Capacitor	2.2µF/10V
PVL Capacitor	2.2µF/10V
BST Capacitor	100nF/6.4V

Recommended PCB Layout and Routing

Place all the bypass capacitors for CHGIN, BYP, SYS, V_{DD}, and BATT as close as possible to the IC. Connect the battery to BATT as close as possible to the IC to provide accurate battery voltage sensing. Provide a large copper ground plane to allow the PGND pad to sink heat away from the device. Use wide and short traces for high current connections such as CHGIN, BYP, SYS, and BATT to minimize voltage drops. The MAX77789 has two kinds of ground pins, which are PGND, and GND. Care should be taken to connect PGND since it is the switching node ground of charger buck. It should be tied to the ground of the SYS capacitor and the BYP capacitor and connected to the ground plane directly without sharing another ground. The GND can be connected to the ground plane.

Figure 22 is a recommended placement and layout guide.

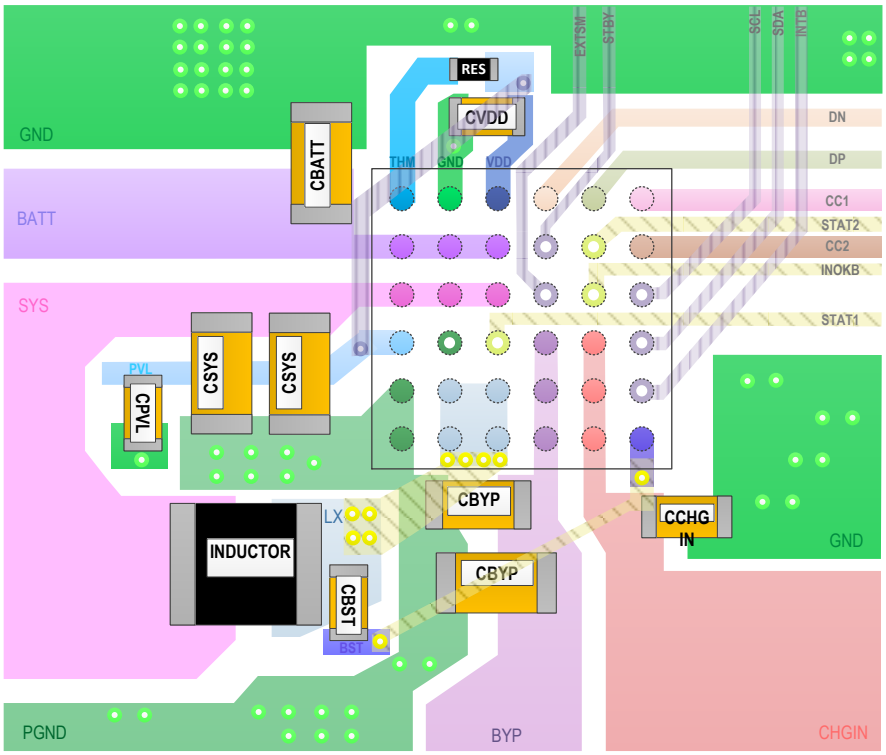


Figure 22. Recommended Placement and Layout

Inductor Selection

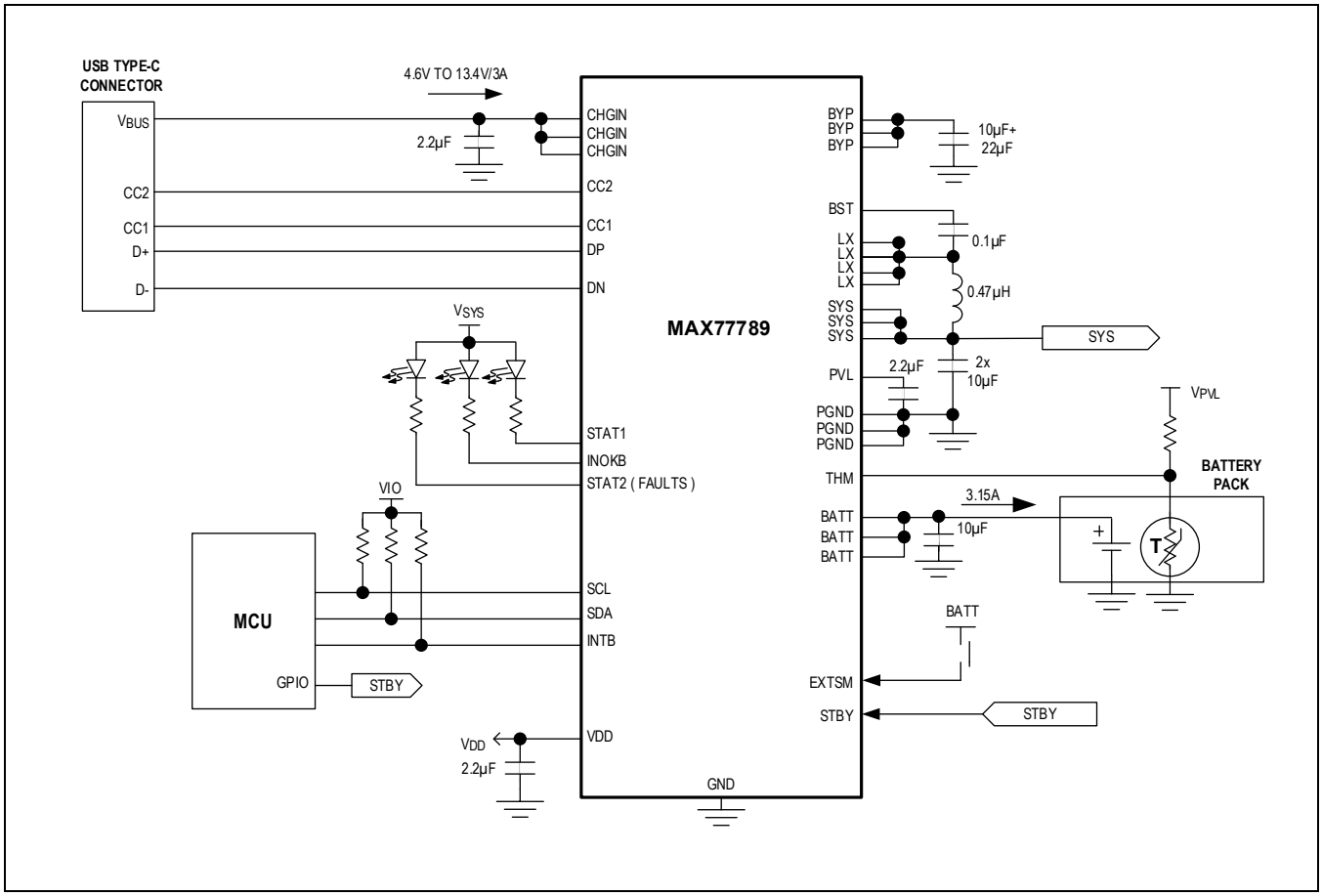
The MAX77789's control scheme requires an external inductor from 0.47µH to 1µH for proper operation.

Table 7. Recommended Inductors

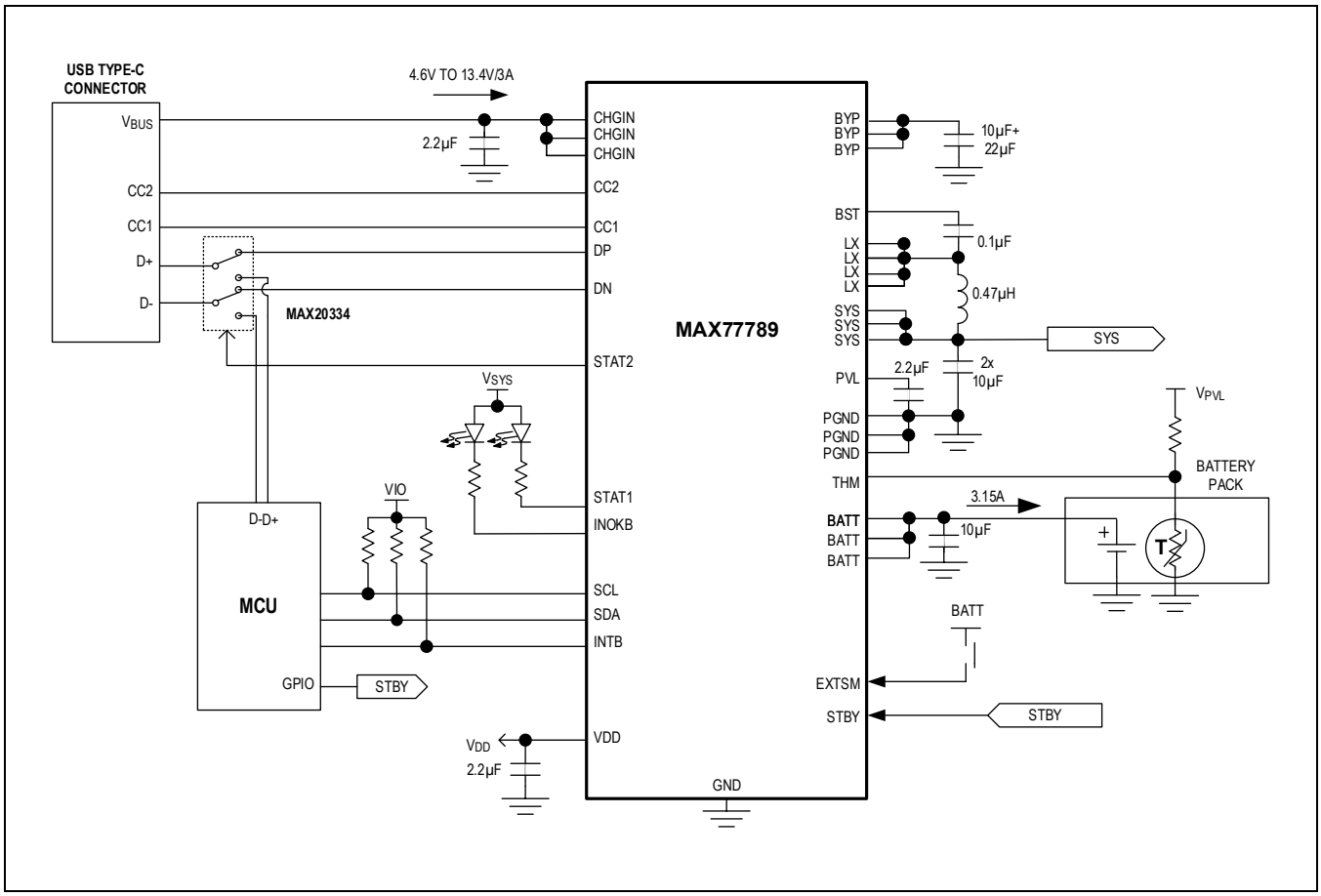
MANUFACTURER	PART NUMBER	Inductance (µH)	$I_{SAT(TYP)}$ (A)	$I_{RMS(TYP)}$ (A)	DCR (TYP) (mΩ)	Size (L x W x T) (mm)
SEMCO	CIGT252008LMR47MNE	0.47	5.5	4.5	24	2.5 x 2.0 x 0.8
SEMCO	CIGT252010LMR47MNE	0.47	6	4.5	24	2.5 x 2.0 x 1.0
SEMCO	CIGT201610EHR47MNE	0.47	5.9	5	18	2.0 x 1.6 x 1.0
CYNTEC	HTGH25201T-R47MSR-68	0.47	6.6	5.6	16.5	2.5 x 2.0 x 1.0

Typical Application Circuit

Typical Application Circuit



In the typical application circuit, the STAT2 pin is for fault indication.



Application with USB2.0 communication, the STAT2 pin is the charger detection completion indicator.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77789EWX+	-40°C to +85°C	2.85mm x 2.85mm 36-Bump WLP
MAX77789EWX+ T	-40°C to +85°C	2.85mm x 2.85mm 36-Bump WLP

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/23	Release for Market Intro	—
1	7/23	Updated *Package Information* section, *Electrical Characteristics* table, and *Typical Application Circuit* section	3, 7, 76
2	1/25	Added *Watchdog Timer* section, updated *Detailed Description* section, added a new Table 1 and renumbered all following tables, updated *Detecting Connected UFP* section, and *Register Map*	19, 28, 31, 35, 36, 47, 51, 53, 72, 74, 75