PD82000 Datasheet
RPF DPU Controller

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

LPS address corrected from 0x40 to 0x6E. Status events table changed to IRQ pins and registers tables. Pin 51 name updated from ADC5_IN to I2C_ADDR. Additional information added to pin descriptions.

1.2 Revision 1.0

Application information section added. Pin description, absolute maximum rating, electrical characteristics, and PD82000 labels updated.

1.3 Revision 0.3

PCB layout recommendation, supply current, and pin description table/pin configuration updated.

1.4 Revision 0.1

Revision 0.1 was the first publication of this document.

2 Overview

Microsemi's Reverse Power Feeding (RPF) chip set is used to allow Customer Premises Equipment (CPE) devices and Distribution Point Unit (DPU) to share and deliver power and data over the same cable.

Microsemi's RPF DPU Controller, PD82000, is a cost-effective, pre-programmed MCU designed to support monitoring and control of the RPF functions, and implement the RPF macros as defined in ETSI TS 101 548. The RPF DPU Controller in conjunction with Microsemi's PD ICs (PD70x01/PD81x0), supports safe power feeding, port disconnection in case of an error condition, DPU host communication for line status telemetry, multi-line FairPower™ sharing with battery backup support, and monitor and report of error fault conditions.

PD82000 utilizes an NXP microcontroller with Microsemi's Intellectual Property (IP) firmware, which provides features flexibility and scalability to support multi-lines DPU applications.

PD82000 is available in a 64-pin, 10 mm x 10 mm LQFP package.

2.1 Features and Benefits

- I^2C communication with DPU host up to 400 kHz
- Up to 16 lines FairPower sharing
- Per line current measurement
- Output voltage monitoring
- Supports Power Good Status (PGS) and DPU Dying Gasp (DDG) IRQ signals to host
- Supports ACM/BAT/DGL signaling detection from PSE and indication to host DPU
- Per line cable disconnect detection
- Supports Low Power Mode (LPM) to save PSE battery power
- Internal power on reset
- Internal Flash
- Software download by I^2C
- Programmable non-volatile parameters
- Wide ambient temperature range:–40 °C to 85 °C
- MSL1, RoHS-compliant

3 Functional Descriptions

The following sections describe the functional aspects of the PD82000 device.

3.1 Signaling

Microsemi's RPF-DPU reference design supports detection of signaling generated by PSE and indications to the DPU host using I2C communication. The signaling pulses represents specific indications as defined by the ETSI TS 101 548 standard and summarized in the following table.

Table 1 • **Signaling Definition**

Signal Name	Full Name	Description
DGL	Dying Gasp Loss	PSE lost power dying gasp indication
BAT	Battery	Operation on battery indication
ACM	AC Mains	Operation on mains power and no PSE battery backup available indication

Signaling is performed by modulation of the RPF voltage and detection by PD82000 through PGn inputs pins.

3.2 Interrupt Outputs

The PD82000 supports two interrupt signals to the DPU host, IRQ_OUT_PSE and IRQ_OUT_DPL.

3.2.1 IRQ_OUT_PSE

PD82000 asserts this interrupt when it detects a PSE port status event from one or more DPU PD ports.

PD82000 supports detection and indication of the following port status events.

- PD Power Good—PD powered-up successfully by the PSE and receives power
- Port Disconnection—the port lost power as a result of a disconnection event (port cable unplugged or PSE port disabled) between the PSE port (U-R2P) and DPU input port (U-O)
- PSE Dying Gasp Loss (DGL)—the PSE lost both AC mains power and battery power (if available)
- PSE AC mains operation (ACM)—the PSE operates on mains power
- PSE Battery operation (BAT)— the PSE operates on backup battery

The indications of the port(s) that caused the interrupt are indicated in the IRQ_OUT register (address 0x00). Once the host received IRQ_OUT_PSE, it can access the status registers to get the IRQ cause. The IRQ is cleared once the host reads IRQ_OUT register.

3.2.2 IRQ_OUT_DPL

PD82000 asserts this interrupt when the DPU has no RPF source available (for instance, when the last DPU port lost power) so the DPU will shut-down after its energy-bank has run out.

3.3 Port Status Indications

PD82000's port status indication registers consist of 16 bits per port, and are utilized to indicate each port status independently. PD82000 asserts the IRQ_OUT_PSE interrupt to the host right after an update of one or more port status registers.

3.3.1 Power-Good Status (PGS) <address 0x62>

Power-Good bit indication is per port (16 bits total). PD82000 asserts bit "n" (PGS[n]) high when it gets a high signal level on PGn input pin.

PSE signaling pulses (ACM/BAT/DGL) over the power-good signal do not affect the PGS register during transmission. PD82000 de-asserts PGS[n] after receiving one of the following indications on PGn input pin.

- DGL signal—after receiving DGL signal, the PGn pin input may remain high until PSE energy bank is discharged. However, PD82000 de-asserts PGS[n] right after receiving the DGL indication and does not wait for complete discharge of the PSE energy bank.
- Port disconnection—port cable unplug event or PSE port disable leads to immediate loss of power-good signal at PGn input pin so that PGS[n] bit is de-asserted.

PD82000 updates counter registers to provide statistics of the power-loss reasons previously described.

3.3.2 Dying-Gasp status (DGS) <address 0x02>

Dying gasp indication per port (16 bits total).

PD82000 asserts DGS[n] after receiving DGL (Dying-Gasp loss) signalling pulse from port n's PSE unit.

3.3.3 Battery Operation Status (BTS) <address 0x66>

Battery operation status indication is per port (16 bits total). This status register indicates whether or not PSE operates from backup battery. PD82000 asserts the BTS[n] bit after BAT signaling is received from PSE or a command from the DPU host is received through I2C communication.

3.3.4 LPM Status (LPS) <address 0x6E>

The PD82000 supports PSE battery power-saving by excluding ports that operate on backup-battery from power sharing, when it possible (i.e. when the ports operates from AC mains has enough accumulated power budget to provides DPU power demand)

Ports that excluded from power sharing, referred to be operated in Low Power Mode (LPM). These ports should keep minimum power signature to holds PSE power on state.

When ports granted a LPM operation, PD82000 sends control signal ("FB_DOWN") through Latch_data pins to disable the corresponding DC/DC modules.

The following tables summarize PD82000 status event previously described where H is VDD, L is GND, 1 is bit H and 0 is bit L, X is "don't care" and X|Y is X or Y.

Table 2 • **PD82000 status events (IRQ Outputs)**

	IRQ_OUT_PSE (pin 62)		IRQ_OUT_DPL (pin 36)	
Event	**Previous**	**Next**	**Previous**	**Next**
PD power good	X	L	H	H
Port disconnect	X	L	H	H|L[1]
DGL	X	L	H	H|L[1]
BAT	X	L	H	H
ACM	X	L	H	H

1. IRQ_OUT_DPL is low if the last port disconnected.

Table 3 • **PD82000 Status Events (registers)**

	IRQ_OUT (Reg 0x00)		PGS (Reg 0x62)		DGS (Reg 0x02)		BTS (Reg 0x66)		LPS (0x6E)	
Event	**Previous**	**Next**	**Previous**	**Next**	**Previous**	**Next**	**Previous**	**Next**	**Previous**	**Next**
PD power good	X	1	0	1	0	0	X	0	0	0
Port disconnect	X	1	1	0	0	0	X	0	X	0
DGL	X	1	1	0	0	1	X	0	X	0
BAT	X	1	1	1	0	0	X	1	X	1|0[1]
ACM	X	1	1	1	0	0	X	0	X	0

1. LPM status equals 1 if the ports operating from AC mains are able to provide DPU power while all ports operate from battery in LPM mode.

3.4 Power Sharing

The PD82000 supports FairPower sharing up to 16 ports. For more details about current sharing implementation with PD82000, refer to application note PD82000_AN_221.

3.5 I²C Communication

I²C interface between Host CPU and PD82000 controller requires setting PD82000 address. this is done by applying a specific voltage level to pin I2C_ADDR (#51) as shown in Table 8. PD82000 supports clock stretching. I²C bus rate range 100k- 400kHz. For more information refer to PD82000 user guide.

Table 4 • **I²C Address Selection**

I²C Address (hex)	Valid Voltage Range (V_{DC})	Pull-Down to DGND (KΩ)	Pull-Up to 3.3 V (KΩ)
0x02	0.00 to 0.21	10	N.C
0x04	0.21 to 0.41	10	97.6
0x08	0.41 to 0.62	10	53.6
0x0c	0.62 to 0.83	10	35.7
0x10	0.83 to 1.03	10	25.5
0x14	1.03 to 1.24	10	19.1
0x18	1.24 to 1.44	10	14.7
0x1c	1.44 to 1.65	10	11.3
0x20	1.65 to 1.86	10	8.87
0x24	1.86 to 2.06	10	6.81
0x28	2.06 to 2.27	10	5.23
0x2c	2.27 to 2.48	10	3.92
0x30	2.48 to 2.68	10	2.8
0x34	2.68 to 2.89	10	1.87
0x38	2.89 to 3.09	10	1.02
0x3c	3.09 to 3.30	10	0.324

4 Electrical Specifications

This section provides the electrical specifications for the PD82000 device.

4.1 Absolute Maximum Ratings

This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Table 5 • **Limiting Values**

PIN	Min	Max	Units
VDD, VDD (I/O)	–0.5	3.6	V
VI (on all digital pins)	–0.5	3.6	V
I^2C_SCL, I^2C_SDA	0	5.5	V
Junction temperature (TJ)		150	°C
Lead soldering temperature (40 s, reflow)		260	°C
Storage temperature (TS)	–65	150	°C
ESD rating—HBM (all pins)	–8	8	kV

4.2 PD82000 Electrical Characteristics

Unless otherwise specified under conditions, the minimum and maxim um ratings stated below apply over the entire specified operating ratings of the device.

Table 6 • **PD82000 Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}, $V_{DD(I/O)}$	Supply voltage		3		3.6	V
I_{DD}	Supply current			25		mA
V_I	Input voltage	Digital pin	0		$V_{DD(I/O)}$	
V_{IL}	Low-level input voltage	Digital pin/I^2C bus			0.3 $V_{DD(I/O)}$	V
V_{IH}	High-level input voltage	Digital pin/ I^2C Bus	0.7 $V_{DD(I/O)}$			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OH} = 2 mA	$V_{DD(I/O)}$ – 0.4			V
I_{OL}	Low-level output current	V_{OL} = 0.4 V	2			mA
I_{OH}	High-level output current	V_{OH} = $V_{DD(I/O)}$ – 0.4 V	–2			mA

Table 6 • **PD82000 Electrical Characteristics *(continued)***

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OLS}	Low-level short-circuit output current	$V_{OL} = V_{DD}$			50	mA
I_{OHS}	High-level short-circuit output current	$V_{OH} = 0$ V			–45	mA
$I_{PULL-UP}$	Pull-up current	$V_I = 0$ V	–50	–80	–100	µA
F_{CLK}	Internal clock frequency			48		MHz

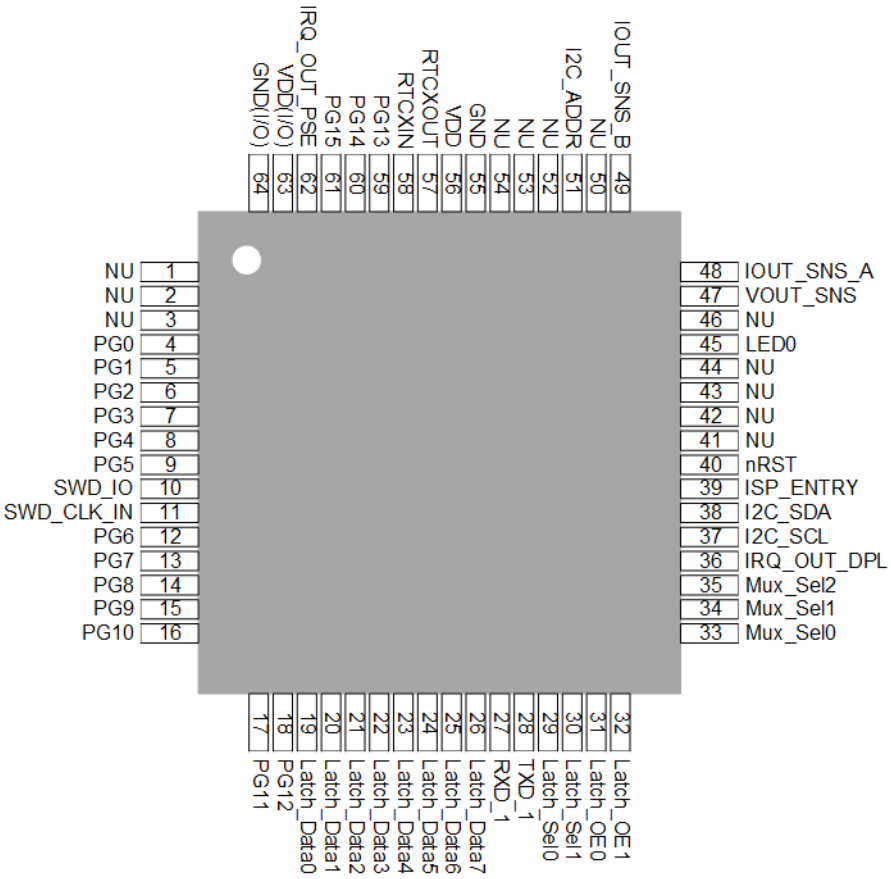
5 Pin Descriptions

The PD82000 device has 64 pins, which are described in this section.

5.1 Pin Diagram

The following illustration is a representation of the PD82000 device, as seen from the top view.

Figure 1 • **PD82000 Pin Diagram**



5.2 Pins by Function

The following table shows the functional pin descriptions for the PD82000 device.

Table 7 • **PD82000 Pin Descriptions**

Pin Number	Pin Designator	Pin Type	Pin Description
1	NU		Not used. Do not connect externally.
2	NU		
3	NU		

Table 7 • **PD82000 Pin Descriptions *(continued)***

Pin Number	Pin Designator	Pin Type	Pin Description
4	PG0	IRQ_IN	Positive-logic power good input signal. PG input capacitance (external) should be lower than 220 pF.
5	PG1	IRQ_IN	
6	PG2	IRQ_IN	
7	PG3	IRQ_IN	
8	PG4	IRQ_IN	
9	PG5	IRQ_IN	
10	SWD_IO	DEBUG	Serial wire debug I/O—not used. Connect to 10k Ω pull-up resistor externally.
11	SWD_CLK_IN	DEBUG	Serial wire clock—not used. Connect to 10k Ω pull-down resistor externally.
12	PG6	IRQ_IN	Positive-logic power good input signal. PG input capacitance (external) should be lower than 220 pF.
13	PG7	IRQ_IN	
14	PG8	IRQ_IN	
15	PG9	IRQ_IN	
16	PG10	IRQ_IN	
17	PG11	IRQ_IN	
18	PG12	IRQ_IN	
19	Latch_Data0	OUT	On/off control signal (per channel, internal pull-up) to disable DC/DC PWM switching when channel is operated in Low Power Mode (LPM). In a multi-port DPU system (up to 8 ports) these pins should connect to the data inputs of a single octal D flip-flop latch. In a 16-port DPU system, these pins should connect to data inputs of two octal D flip-flop latches. The first latch (Latch 0) is used to control ports 0–7, and second latch (Latch 1) is used to control ports 8–15. In a 1-port DPU system, these pins are not used (do not connect externally).
20	Latch_Data1	OUT	
21	Latch_Data2	OUT	
22	Latch_Data3	OUT	
23	Latch_Data4	OUT	
24	Latch_Data5	OUT	
25	Latch_Data6	OUT	
26	Latch_Data7	OUT	
27	RXD_1	IN	Reserved. Do not connect externally.
28	TXD_1	OUT	Reserved. Do not connect externally.
29	Latch_Sel0	OUT	Latch CLK signal (internal pull-up). Latch_Sel0 should be connected to clock pulse input of ports 0–7 latch (Latch 0). Used to control ports 0–7.

Table 7 • **PD82000 Pin Descriptions *(continued)***

Pin Number	Pin Designator	Pin Type	Pin Description
30	Latch_Sel1	OUT	Latch CLK signal (internal pull-up). Latch_Sel1 should be connected to clock pulse input of ports 8–15 latch (Latch 1). Used to control ports 8–15 in a16-port DPU application. In a DPU system with 8 ports or less, this pin is not used and should not be connected externally.
31	Latch_OE0	OUT	Output-enable signal to latch0 (internal pull-up). Latch_OE0 should be connected to negative-logic latch output-enable input. Used to control ports 0–7.
32	Latch_OE1	OUT	Output-enable signal to latch1 (internal pull-up). Latch_OE1 should be connected to negative-logic latch output-enable input. Used to control ports 8–15 in a16-port DPU application. In a DPU system with 8 ports or less, this pin is not used and should not be connected externally.
33	Mux_Sel0	OUT	Channel selection for current sense MUX (internal pull-up). Should be connected to 3 digital select input of 8-channel analog MUX(s). In a 16-port DPU application, use two analog multiplexers (8 channels each). The first MUX (MUX_A) is used to sense current of ports 0–7. MUX_A common output should be connected to IOUT_SNS_A input (pin 48). The second MUX (MUX_B) used to sense current of ports 8–15. MUX_B common output should be connected to IOUT_SNS_B input (pin 49). In a multiport DPU with 8 ports or less, use only MUX_A. In a 1-port DPU application, these pins are not used and should not be connected externally.
34	Mux_Sel1	OUT	
35	Mux_Sel2	OUT	
36	IRQ_OUT_DPL	OUT	DPU power loss interrupt output (active low with internal pull-up). DPL IRQ asserted when the last PD channel disconnected to indicate DPU system has no available RPF source left.
37	I^2C_SCL	IN	Host I^2C clock. Connect external pull-up resistor between this pin and VDD (10k Ω).

Table 7 • **PD82000 Pin Descriptions *(continued)***

Pin Number	Pin Designator	Pin Type	Pin Description
38	I^2C_SDA	IN/OUT	Host I^2C data.Connect external pull-up resistor between this pin and VDD (10k Ω).
39	ISP_ENTRY	IN	Not used. Connect to 100k Ω pull-up resistor externally.
40	nRST	IN	External reset (active low, internal weak pull-up). Minimum reset pulse width is 200 ns. The reset pin can be connected to open-drain or push-pull driver output. If the reset source is from open-drain output, then external pull-up resistor (10k) is recommended. If the reset source is from a push-pull driver output, then a serial resistor between driver output and xRESET pin is optional. Adding a capacitor (10 nF or higher) between this pin and GND(I/O) (pin 64) is recommended.
41	NU		Not used
42	NU		
43	NU		
44	NU		
45	LED0	OUT	Debug LED. LED Blinks (1 Hz) during normal operation.
46	NU	IN	Not used. Connect 10k Ω–100k Ω pull-down resistor externally.
47	VOUT_SNS	IN	Output voltage measurement. Connect to 12 V rail through voltage divider as follows: Connect 240k Ω pull-up resistor from the pin to 12 V (shared DC/DCs output). Connect 20k Ω pull-down resistor from the pin to ADC analog ground (pin 55), with 100 nF capacitor in parallel.

Table 7 • **PD82000 Pin Descriptions *(continued)***

Pin Number	Pin Designator	Pin Type	Pin Description
48	IOUT_SNS_A	IN	Channels 0–7 current measure. In multiport DPU application, connect to common output of analog multiplexer while the analog multiplexer independent inputs are connected to current sense amplifiers output from isolated DC/DC outputs, and the multiplexer select input connected to Mux_Sel0-2 (pins 33–35). Add 1 nF capacitor between this pin and ADC analog GND (pin 55).
49	IOUT_SNS_B	IN	Channels 8–15 current measure. In a 16-port DPU application, connect to common output of analog multiplexer (MUX_B) while the analog multiplexer independent inputs are connected to current sense amplifiers output from isolated DC/DC outputs, and the multiplexer select input connected to Mux_Sel0-2 (pins 33–35). Add 1 nF capacitor between this pin and ADC analog GND (pin 55). If IOUT_SNS_B not used, (8-port or less DPU application), connect 20k Ω pull-down resistor from this pin to ADC analog GND.
50	NU		Not used. Connect 1k Ω pull-up resistor to VDD(3V3) pin 56.
51	I2C_ADDR	IN	Analog input to program PD81000 I2C address. In order to set default address (0x20), connect pull-up resistor 8.87k Ω from this pin to VDD (3.3 V), and connect pull-down resistor 10k Ω from this pin to ground (GND).
52	NU	OUT	Reserved
53	NU		Not used
54	NU		
55	GND	PWR	Ground
56	VDD	PWR	3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage.
57	RTCXOUT	OUT	Reserved
58	RTCXIN	IN	Reserved

Table 7 • **PD82000 Pin Descriptions *(continued)***

Pin Number	Pin Designator	Pin Type	Pin Description
59	PG13	IRQ_IN	Power good interrupt input. PG Input capacitance (external) should not be higher than 220 pF.
60	PG14	IRQ_IN	
61	PG15	IRQ_IN	
62	IRQ_OUT_PSE	IRQ_OUT	PSE port status event interrupt output (active low with internal pull-up). IRQ is asserted when PD82000 detects a port status events from one or more ports. PD82000 indicates the IRQ reason through status resisters.
63	VDD(I/O)	PWR	I/O supply voltage
64	GND(I/O)	PWR	I/O supply RTN

6 Package Information

The PD82000 package is a 10 mm x 10 mm LQFP package, as described in the following section.

6.1 Package Drawing

The following illustration shows the package drawing for the PD82000 device.

Figure 2 • **Package Drawing**

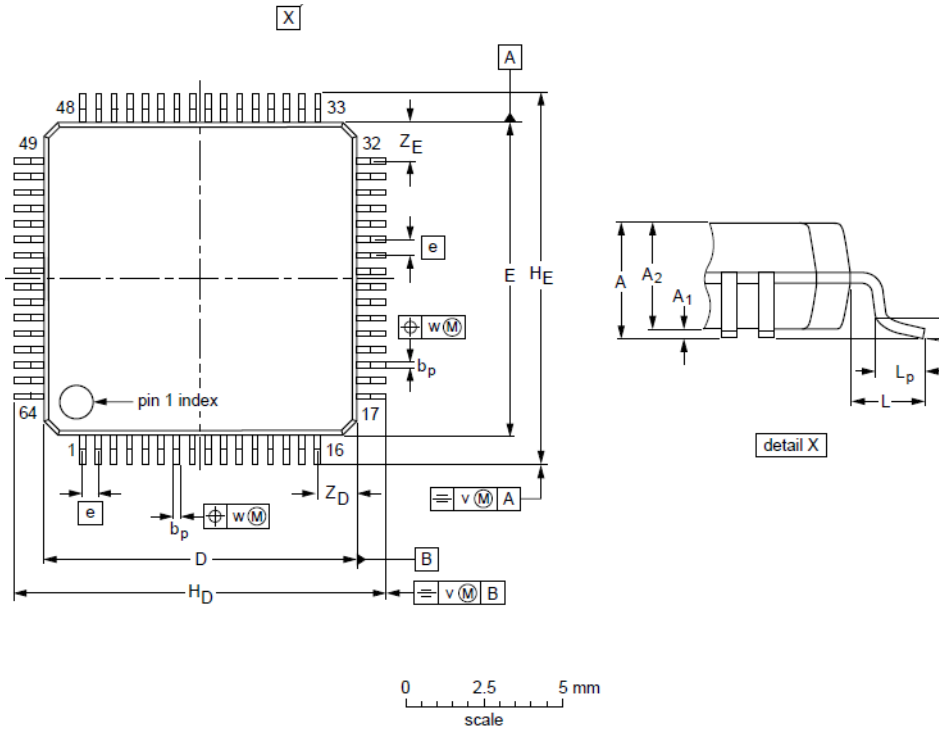
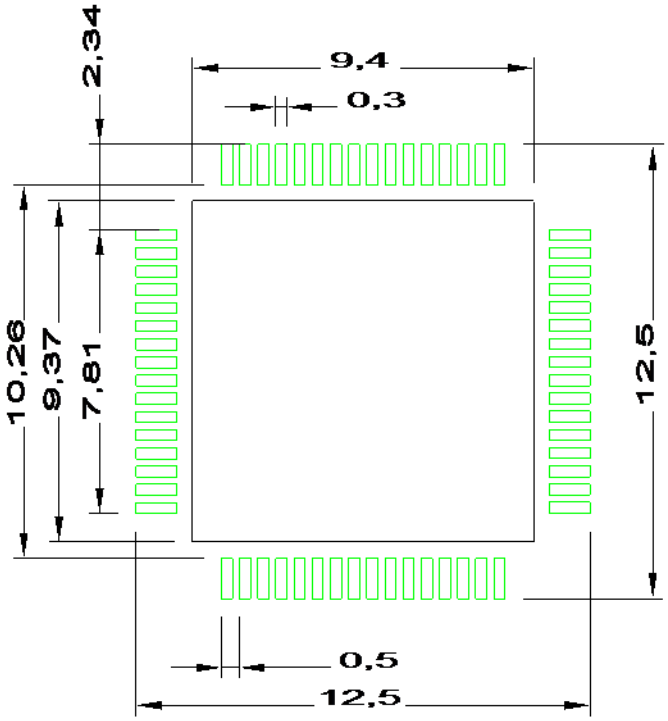


Table 8 • **Dimensions (mm are the original dimensions)**

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_P	v	w	y	$Z_D^{(1)}$	$Z_E^{(1}$	Θ
mm	1.6	0.20	1.45	0.2	0.27	0.18	10.1	10.1	0.5	12.15	12.15	1	0.75	0.2	0.12	0.1	1.45	1.45	7 °
		0.05	1.35	5	0.17	0.12	9.9	9.9		11.85	11.85		0.45				1.05	1.05	0 °

Figure 3 • **Recommended PCB Layout for 64-Pin LQFP 10 mm × 10 mm**



6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 9 • **Thermal Characteristics**

Thermal Resistance	PD82000	Units	Notes
Θ_{JA}	61	°C/W	Mount on PCB of 76 mm × 114 mm
Θ_{JC}	19	°C/W	Junction to top case

Note: Θ_{JA} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \Theta_{JA})$. In particular, Θ_{JA} is a function of PCB construction.

The following table describes the classification reflow profiles for the device. All temperatures refer to topside of the package, measured on the package body surface.

Table 10 • **Classification Reflow Profiles**

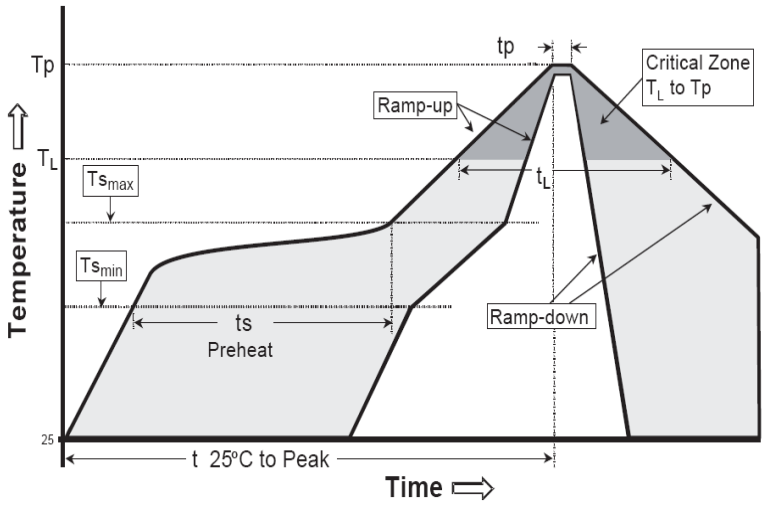
Profile Feature	Sn-Pb Eutectic Assembly	PB-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/second max.	3 °C/second max.
Preheat Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} to ts_{max})	 100 °C 150 °C 60 seconds–120 seconds	 150 °C 200 °C 60 seconds–150 seconds

Table 10 • **Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	PB-Free Assembly
Time maintained above: Temperature (T_L) Time (t_L)	 183 °C 60 seconds–150 seconds	 217 °C 60 seconds–150 seconds
Time within 5 °C of actual peak temperature (tp)	10 seconds–30 seconds	20 seconds–40 seconds
Ramp-down rate	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

The following illustration shows the classification reflow profile.

Figure 4 • **Classification Reflow Profile**



The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means peak reflow temperature 0 °C— for example, 260 °C + 0 °C) at the rated MSL level.

Table 11 • **SnPb Eutectic Process: Classification Temperature**

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 + 0/–5 °C	225 + 0/–5 °C
2.5 mm[1]	225 + 0/–5 °C	225 + 0/–5 °C

1. Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

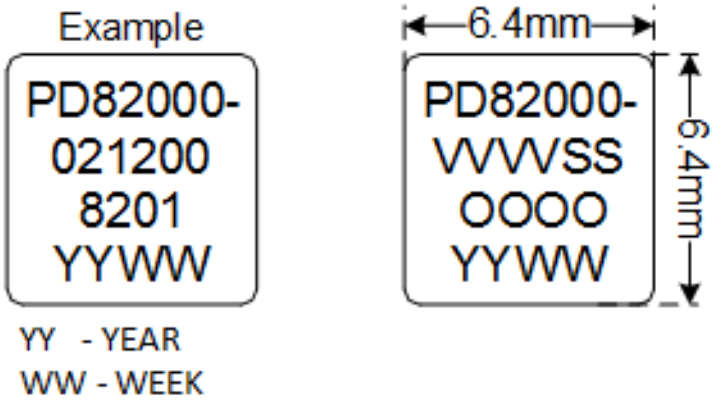
Table 12 • **Pb-Free Process: Package Classification Reflow Temperatures**

Package Thickness	Volume mm^3 <350	Volume mm^3 350–2000	Volume mm^3 >2000
<1.6 mm	260 +0 °C*	260 +0 °C*	260 +0 °C*
1.6 mm–2.5 mm	260 +0 °C*	250 +0 °C*	245 +0 °C*
≥2.5 mm	250 +0 °C*	245 +0 °C*	245 +0 °C*

Note: Exceeding these ratings may cause damage to the device.

The following illustration shows the label for the PD82000 device.

Figure 5 • **PD82000 Label**



7 Ordering Information

The following table lists the ordering information for the PD82000 device.

Table 13 • **Ordering Information**

Part Order Number	Description
PD82000-VVVVSS	Lead-free, RoHS and MSL1-compliant 64-pin plastic LQFP package with a 10 mm × 10 mm body size. The operating temperature is – 40 °C ambient to 85 °C junction. The tray marking is PD82000-VVVVSS PD-OOOOG3bb[1] YYWW

1. MKTG Product Type/Version/SW Parameters/Operation P/N

For the latest firmware version available, refer to the Microsemi's website. Initial burning of controller's firmware is performed in factory. Firmware upgrades can be performed using the communication interface.