

PROTECTION PRODUCTS

Description

uClamp®0512ZA is an ultra small ESD protection device designed to protect two high-speed lines in an 0201 footprint. This revolutionary package design reduces board space requirements by more than 50% over existing single line solutions. uClamp0512ZA is a three pin device with identical TVS diodes connected to each pin. Any two pins may be connected to vulnerable lines, while the third pin is connected to ground. This gives the designer maximum flexibility in pcb routing. These devices feature extremely good ESD protection characteristics highlighted by low dynamic resistance, low peak ESD clamping voltage, and high ESD withstand voltage (+/-12kV contact per IEC 61000-4-2).

uClamp0512ZA is in a 3-pin SLP0603P3X3F package. It measures 0.62 x 0.32 mm with a nominal height of only 0.25mm. Leads are finished with lead-free NiAu. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablets.

Features

- High ESD withstand voltage
 - ♦ IEC 61000-4-2 (ESD) 15kV (air), 12kV (contact)
- Very small PCB area
- Protects two data lines
- Working Voltage: 5V
- Low reverse leakage current
- Low ESD peak clamping voltage
- Low dynamic resistance
- Solid-State silicon-avalanche technology

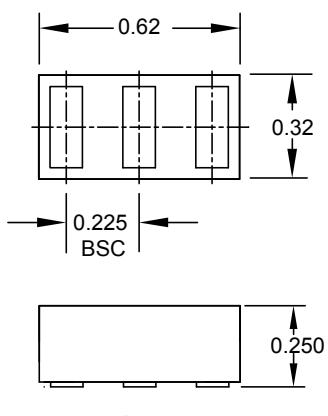
Mechanical Characteristics

- SLP0603P3X3F Package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal dimensions: 0.62 x 0.32 x 0.25 mm
- Lead finish: NiAu
- Marking : Marking code + date code
- Packaging : Tape and Reel

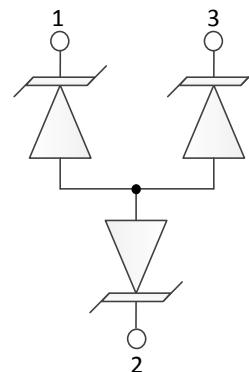
Applications

- Cellular Handsets & Accessories
- Keypads, Side Keys, Audio Ports
- Portable Instrumentation
- Notebook Computers
- Tablet PC

Nominal Dimensions



Functional Schematic



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 1.2/50μs)	P _{PK}	30	W
Peak Pulse Current (tp = 1.2/50μs)	I _{PP}	2	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾	V _{ESD}	±15	kV
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾		±12	
Operating Temperature	T _J	-40 to +125	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}	-40°C to 125°C Between any two pins			5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA, Between any two pins	-40°C to 125°C	6.5	8	9.5
Reverse Leakage Current	I _R	V _{RWM} = 5V Between any two pins	T = 25°C	0.03	0.050	μA
Clamping Voltage	V _C	I _{PP} = 2A, tp = 8/20μs, Between any two pins		10.5	15	V
ESD Clamping Voltage ²	V _C	I _{PP} = 4A, tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2	10.5		V
			Pin 1 to 3	11		V
ESD Clamping Voltage ²	V _C	I _{PP} = 16A, tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2	17.5		V
			Pin 1 to 3	20		V
Dynamic Resistance ^{2,3}	R _{DYN}	tp = 0.2/100ns (TLP)	Pin 1 to 2, Pin 3 to 2	0.58		Ohms
			Pin 1 to 3	0.75		Ohms
Junction Capacitance	C _J	V _R = 0V, f = 1MHz Between any two pins	T = 25°C	5	7	pF

Notes:

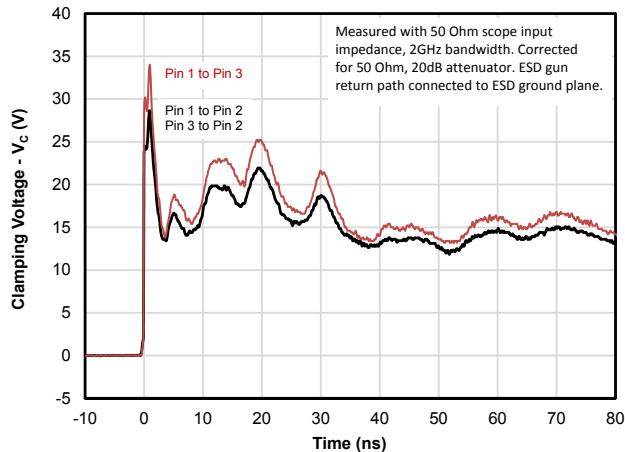
(1): ESD Gun return path to Ground Reference Plane (GRP)

(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns.

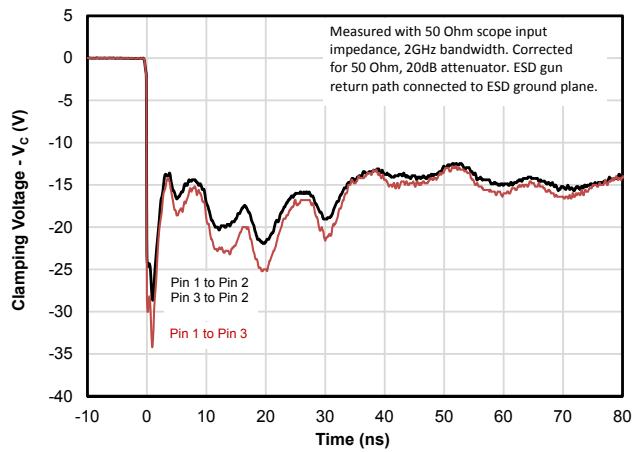
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

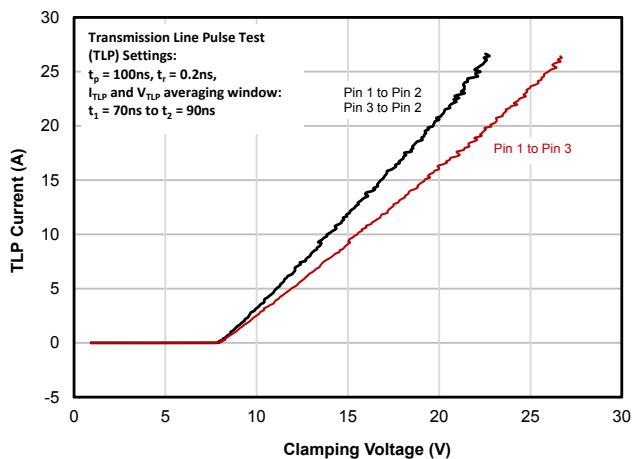
ESD Clamping (+8kV Contact per IEC 61000-4-2)



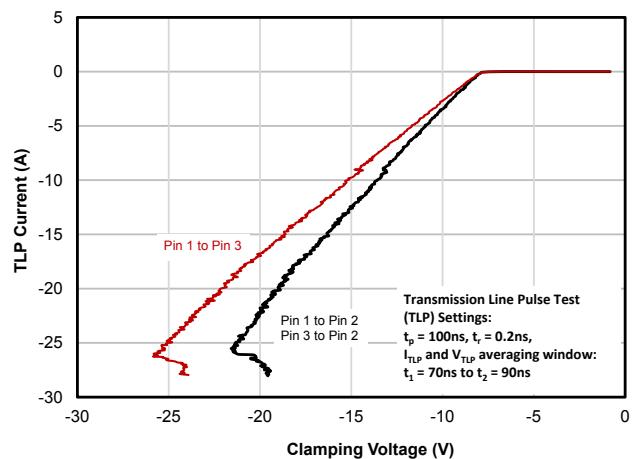
ESD Clamping (-8kV Contact per IEC 61000-4-2)



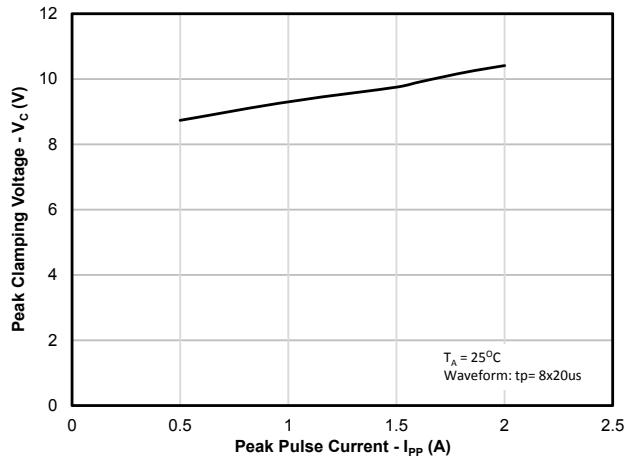
TLP IV Curve (Positive Pulse)



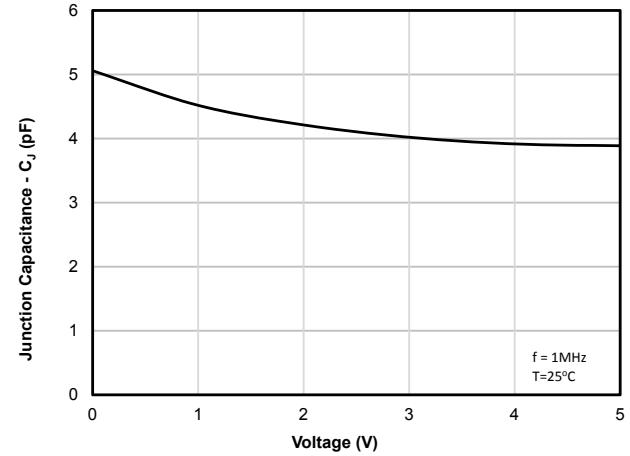
TLP IV Curve (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current ($t_p=8/20\mu\text{s}$)

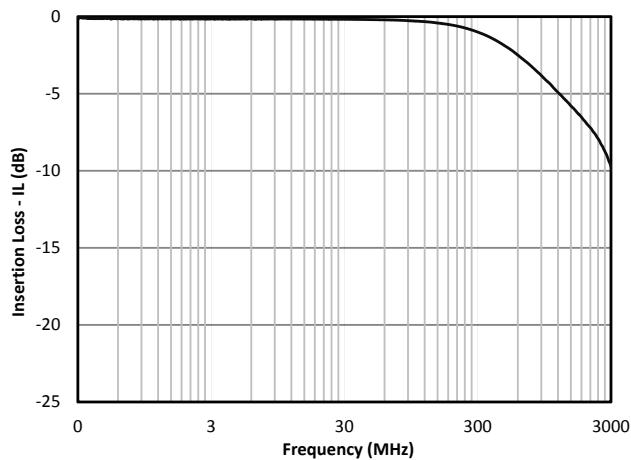


Capacitance vs. Reverse Voltage

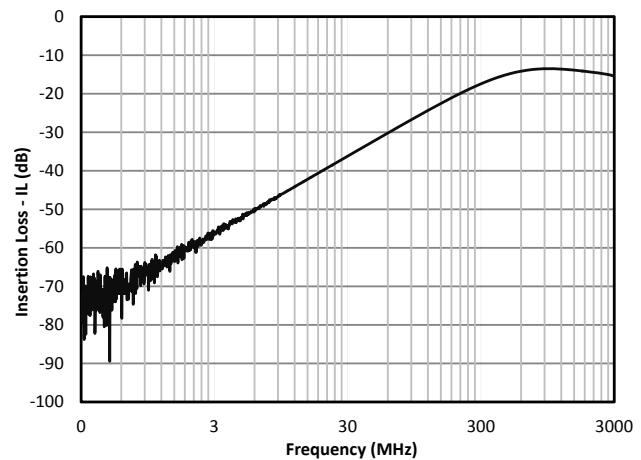


Typical Characteristics (Continued)

Insertion Loss - S21



Analog Crosstalk



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

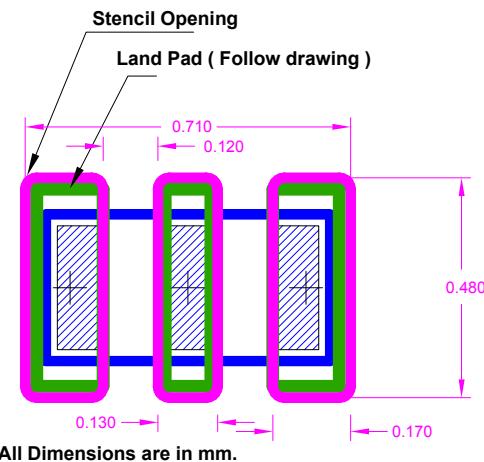
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

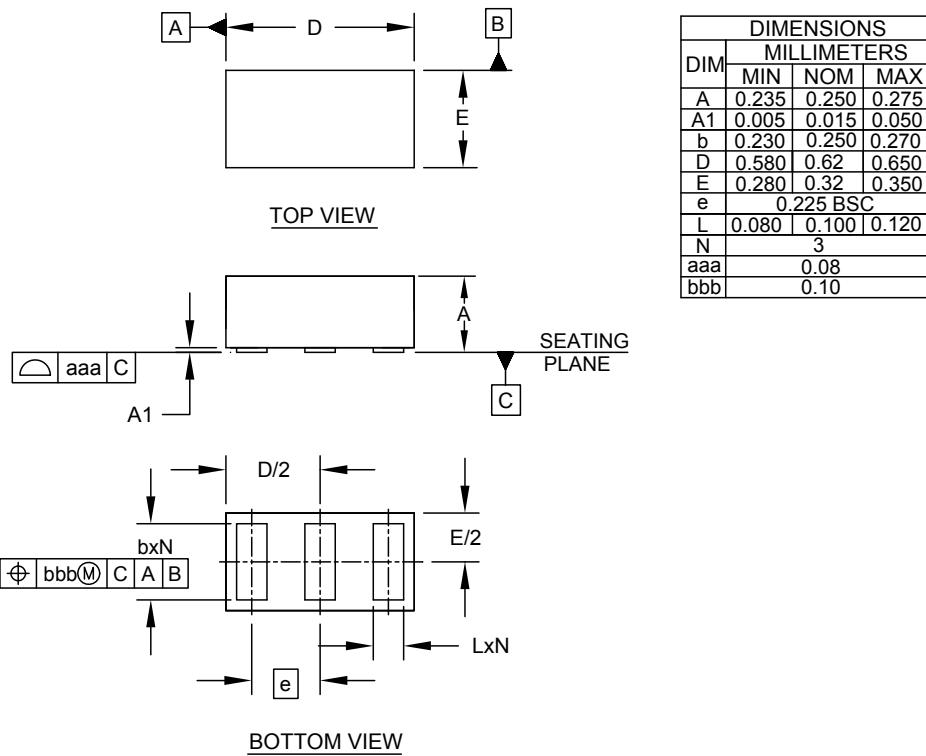


All Dimensions are in mm.
Land Pad. Stencil opening Component

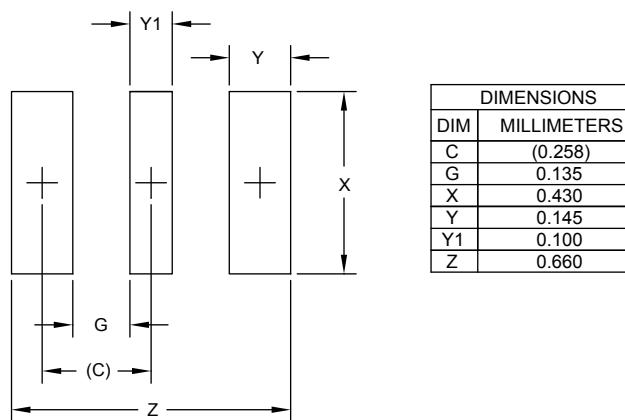
Table 1 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

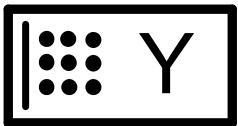
Outline Drawing - SLP0603P3X3F



Land Pattern - SLP0603P3X3F

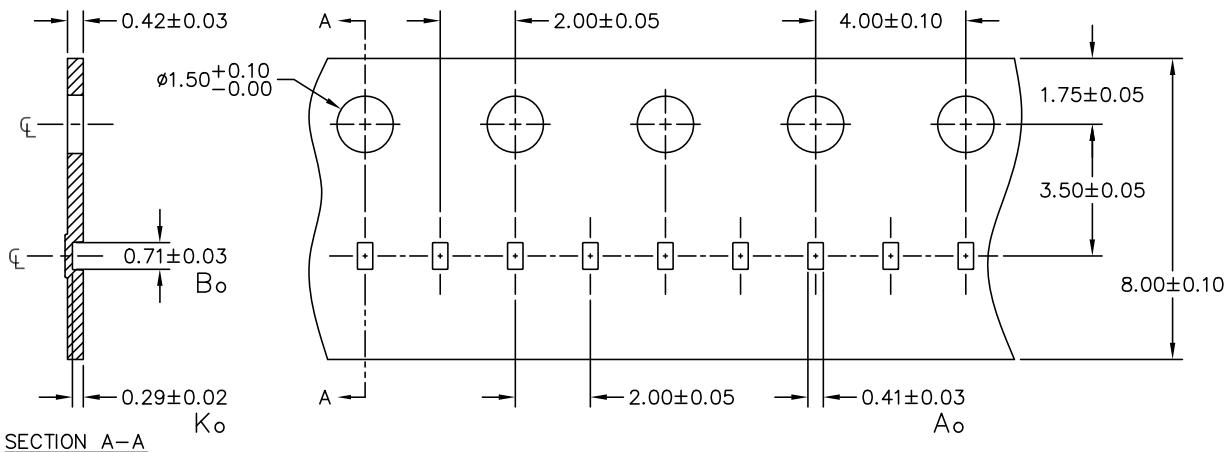


Marking Code

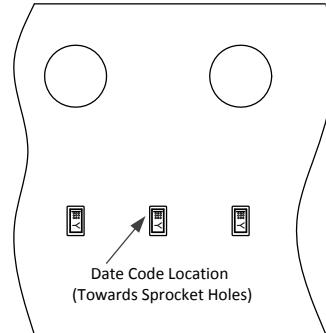


Notes: Device is electrically symmetrical

Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
uClamp0512ZATFT	15000	7 Inch
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