FEATURES

- Dual 4A Output Power supply with 1.5A VLDO
- Short-Circuit and Overtemperature Protection
- Power Good indicators

Switching Regulators Section - Current Mode Control

- Input Voltage Range: 2.375V to 5.5V
- 4A DC Typical, 5A Peak Output Current Each
- 0.8V Up to 5V Output Each, Parallelable
- ±2.5% Total DC Output Error
- Output Voltage Tracking
- Up to 95% Efficiency
- Programmable Soft-Start

VLDO Section

- VLDO, 1.14V to 3.5V Input Range
- VLDO, 0.4V to 2.6V, 1.5A Output
- VLDO, 40dB Supply Rejection at fsw
- ±1.5% Total DC Output Error
- 16mm x 16mm x 3.0mm LGA

DESCRIPTION

The LTM4615CN is a complete 4A dual output switching mode DC/DC power supply plus an additional 1.5A VLDO (very low dropout) linear regulator. Included in the package are the switching controllers, power FETs, inductors, a 1.5A regulator and all support components. The dual 4A DC/DC converters operate over an input voltage range of 2.375V to 5.5V, and the VLDO operates from a 1.14V to 3.5V input. The LTM4615CN supports output voltages ranging from 0.8V to 5V for the DC/DC converters, and 0.4V to 2.6V for the VLDO. The three regulator output voltages are set by a single resistor for each output. Only bulk input and output capacitors are needed to complete the design.

The low profile package (3.0mm) enables utilization of unused space on the bottom of PC boards for high density point of load regulation. High switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability. The device supports output voltage tracking for supply rail sequencing.

Additional features include overvoltage protection, overcurrent protection, thermal shutdown and programmable soft-start. The power module is offered in a space saving and thermally enhanced 16mm × 16mm × 3.0mm LGA package. The LTM4615CN is RoHS c ompliant with Pb-free finish.

TYPICAL APPLICATION

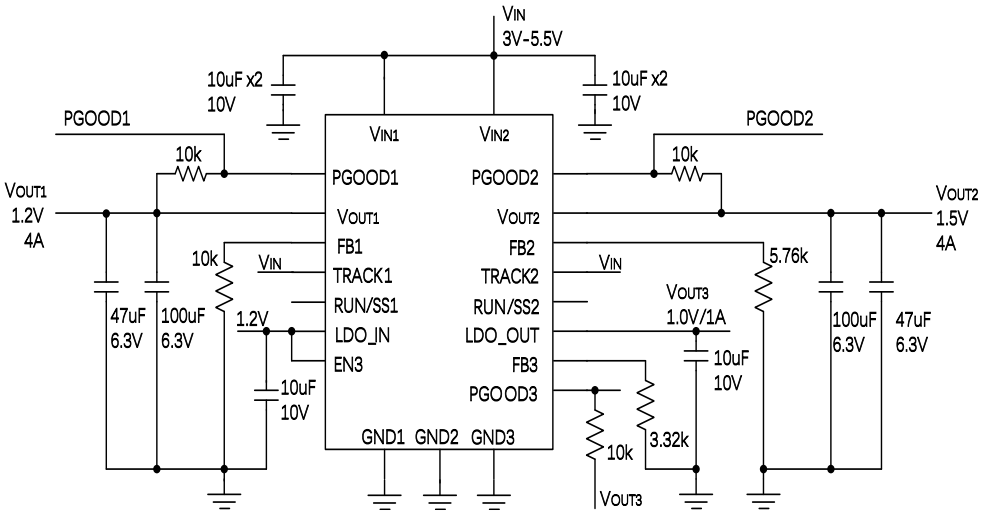
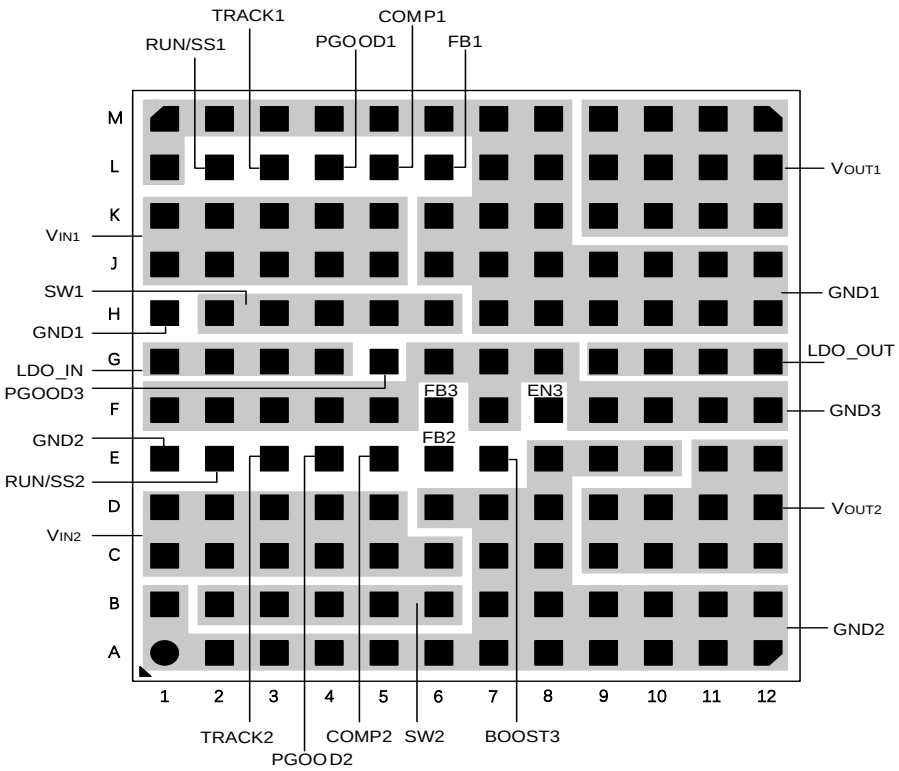


Fig1. 1.2V at 4A, 1.5V at 4A and 1V at 1A with Triple Outputs

PIN CONFIGURATION



LGA PACKAGE
144-LEAD (16mm × 16mm × 3.0 mm)

Fig2. LTM4615CN Top View

ABSOLUTE MAXIMUM RATINGS【Note1】

Switching Regulators	
V_{IN1}, V_{IN2}, PGOOD1, PGOOD2	-0.3V to 6V
COMP1, COMP2, RUN/SS1, RUN/SS2, V_{FB1}, V_{FB2}, TRACK1, TRACK2	-0.3V to V_{IN}
SW, V_{OUT}	-0.3V to (VIN+0.3V)
VLDO Regulators	
LDO_IN, PGOOD3, EN3	-0.3V to 6V
LDO_OUT	-0.3V to 4V
FB3	-0.3V to (LDO_IN+0.3V)

Internal Operating Temperature Range	-40℃ to 125℃
Junction Temperature	125℃
Storage Temperature Range	-55℃ to 125℃
Peak Solder Reflow Package Body Temperature	260℃
Internal solder paste melting point	262℃

ELECTRICAL CHARACTERISTICS【Note 2】

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel					
$V_{IN(DC)}$		2.375	-	5.5	V
$V_{OUT(DC)}$		0.8	-	5.0	V
$V_{OUT(DC)}$	C_{IN}=22uF, C_{OUT}=100uF, R_{FB}=5.76K	1.45	1.49	1.53	V
V_{IN}（UVLO）	I_{OUT}=0A		2		V
$I_{Q(VIN)}$	RUN=0, V_{IN}=5V	-	7	-	uA
$I_{S(VIN)}$	V_{IN}=2.375V, V_{OUT}=1.5V,I_{OUT}=4A		3.2		A
	V_{IN}=5.5V, V_{OUT}=1.5V,I_{OUT}=4A		1.48		A
$I_{OUT(DC)}$	V_{IN}=5.5V, V_{OUT}=1.5V	0	-	4	A
$\Delta V_{OUT(LINE+LOAD)}/V_{OUT}$	V_{OUT}=1.5V, V_{IN}=2.375V-5.5V, I_{OUT}=0A-4A	-	1.0		%
$V_{OUT(AC)}$	I_{OUT}=0A, C_{OUT}=100uF, V_{IN}=5.5V, V_{OUT}=1.5V	-	15		mV_{P-P}
$t_{(START)}$	C_{OUT}=100μF, I_{OUT}=1 Aresistive Load,RUN/SS=Float, V_{IN}=5V,TRACK=V_{IN}	-	0.5	-	ms

$t_{(SETTLE)}$	Load: 0% to 50% to 0% of Full Load, COUT = 100µF, VIN = 5V, VOUT = 1.5V	-	15	-	µs
I_{OUTPK}	V_{IN}=5V V_{OUT}=1.5V	-	8	-	A
fS	I_{OUT}=0A,V_{IN}=5V,V_{OUT}=1.5V		1.25		MHz
V_{FB}	V_{OUT}=1.5V, I_{OUT}=0A	0.786	0.8	0.809	V
I_{TRACK}			0.2		µA
$V_{TRACK\ (OFFSET)}$	TRACK=0.4V	-	30		mV
$V_{TRACK\ (RANGE)}$		0		0.8	V
R_{FBHI}		4.94	4.99	5.04	kΩ
V_{PGOOD}		-	±7.5	-	%
R_{PGOOD}			90		Ω
VLDO Section					
V_{LDO_IN}	Note3	1.14		3.5	V
$I_{IN(LDO\_IN)}$	IOUT = 0mA, VOUT = 1V, EN3 = 1.2V	-	1	-	mA
$I_{IN(SHDN)}$	EN3 = 0V, LDO_IN = 1.5V		1		uA
V_{BOOST3}	EN3 = 1.2V	4.8	5	5.2	V
$V_{BOOST3\ (UVLO)}$			4.3		V
V_{FB3}	1mA ≤ IOUT ≤ 1.5A, 1.14V ≤ VLDO_IN ≤ 3.5V, BOOST3 = 5V, 1V ≤ VOUT ≤ 2.59V	0.395	0.4	0.405	V
V_{LDO_OUT}		0.4		2.6	V
V_{DO}	VLDO_IN = 1.5V, VFB3 = 0.38V, IOUT = 1.5A, V_{DO}=V_{LDO_IN} - V_{LDO_OUT}		100	275	mV
LDO_RHI	LDO Top Feedback Resistor	4.94	4.99	5.04	kΩ
I_{OUT}		1.5			A
I_{LIM}			2.5		A
V_{IH_EN3}	1.14V ≤ VLDO_IN ≤ 3.5V	1			V
V_{IL_EN3}	1.14V ≤ VLDO_IN ≤ 3.5V			0.4	V
V_{OL_PGOOD3}	IPGOOD3 = 2mA		0.1	0.4	V
PGOOD	PGOOD3 High to Low PGOOD3 Low to High		-12 -3		% %

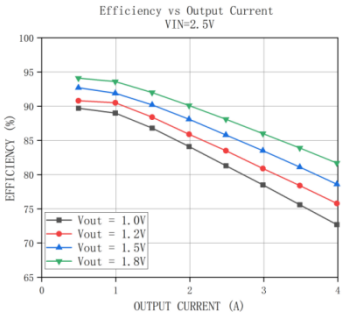
Note1： Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note2：The LTM4615CN has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature is activated. Continuous overtemperature activation can impair long-term reliability.

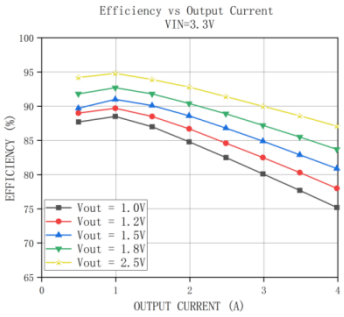
Note3：The minimum working voltage:V_{IN}≥$V_{OUT(MIN)}$+$V_{DROPOUT}$

TYPICAL PERFORMANCE CHARACTERISTICS

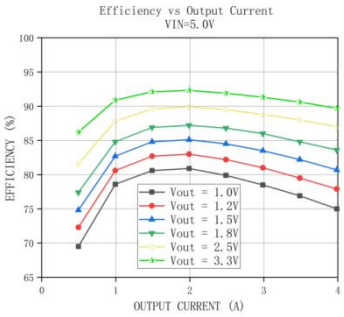
DC-DC Typical Performance:



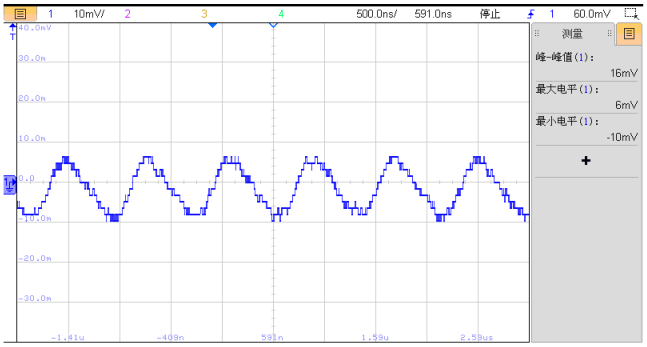
2.5VIN Efficiency



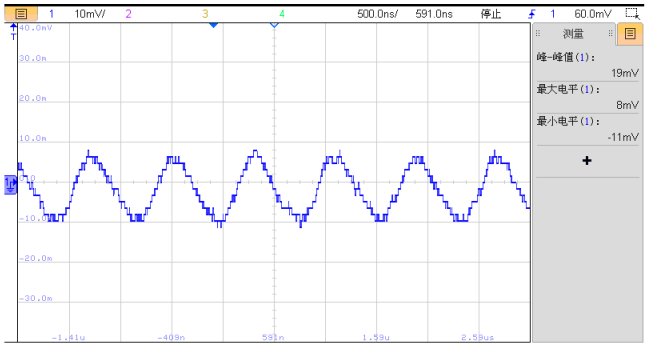
3.3VIN Efficiency



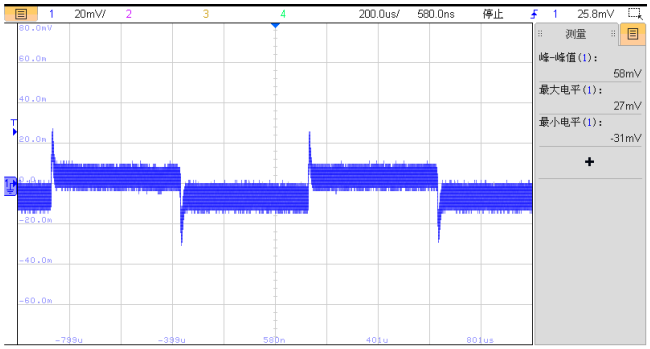
5VIN Efficiency



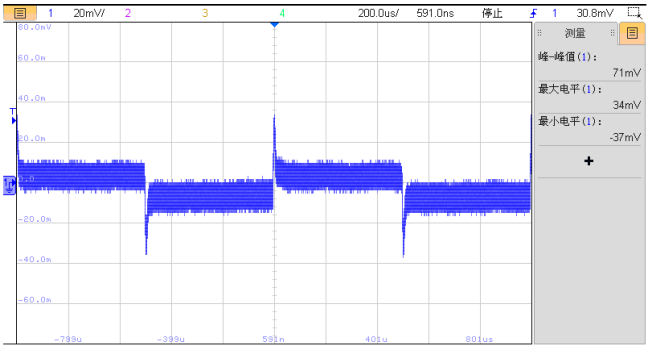
VIN=5V,VO=1.5V at 0A Load



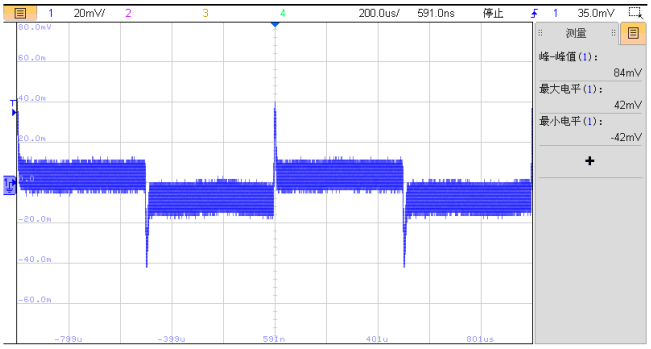
VIN=5V,VO=1.5V, at 4A Load



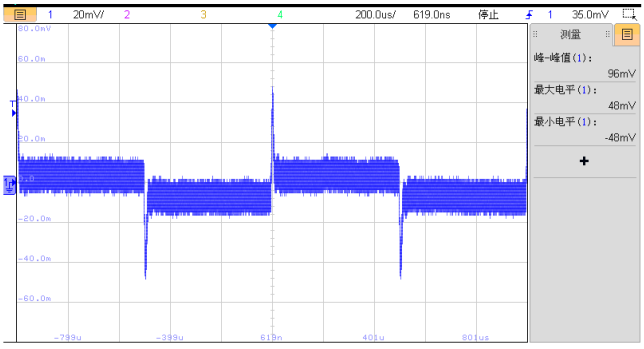
VIN=5V,VO=1.2V, 0-4A Load, 2.5A/us



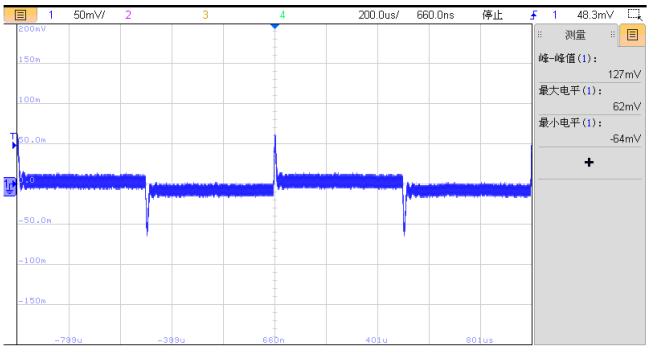
VIN=5V,VO=1.5V,0-4A Load, 2.5A/us



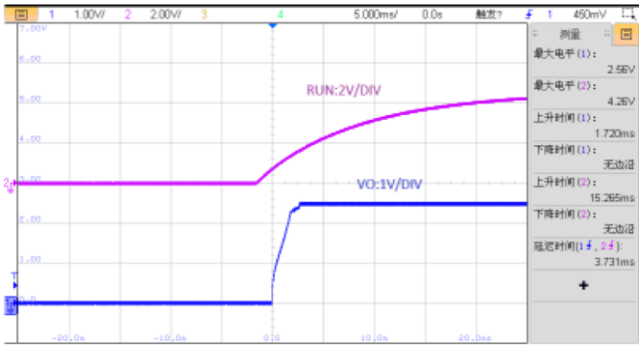
VIN=5V,VO=1.8V,0-4A Load, 2.5A/us



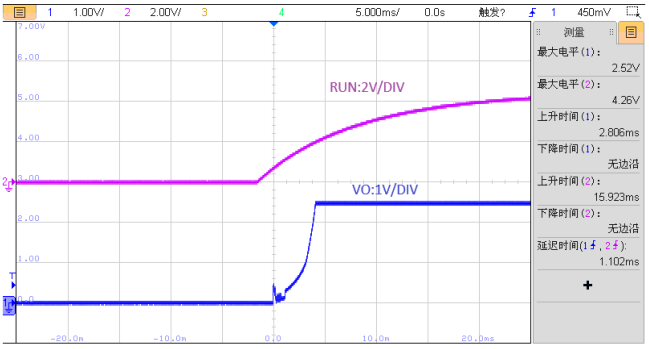
VIN=5V,VO=2.5V,0-4A Load, 2.5A/us



VIN=5V,VO=1.8V,0-4A Load, 2.5A/us

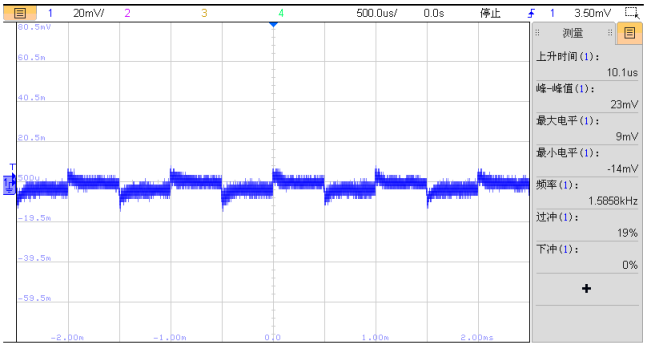


VIN=5V,VO=2.5V, at 0A Load, Css=0.01uF, EN Start-Up

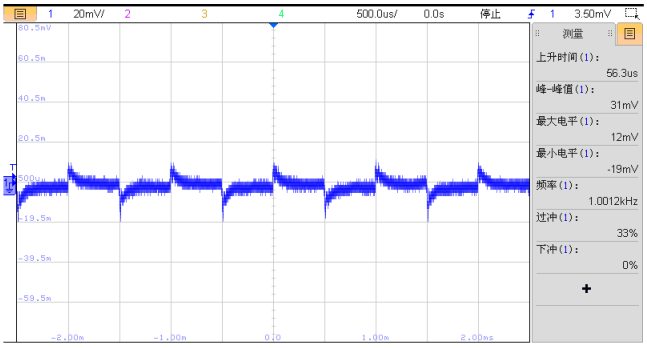


VIN=5V,VO=2.5V at 4A Load, Css=0.01uF, EN Start-Up

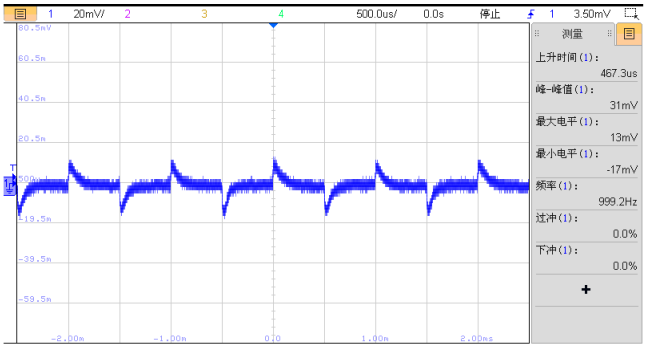
VLDO Typical Performance:



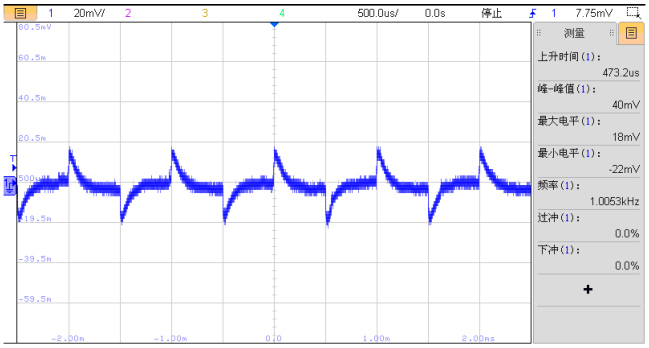
VIN=1.14V, VO=0.6V,0-1.5A Load, 2.5A/us



VIN=1.375V, VO=1.0V,0-1.5A Load, 2.5A/us



VIN=1.7V, VO=1.5V,0-1.5A Load, 2.5A/us



VIN=3.3V, VO=2.5V,0-1.5A Load, 2.5A/us

PIN FUNCTIONS

VIN, VIN2(J1-J5, K1-K5; C1-C6, D1-D5): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between VIN pins and GND pins.

VOUT1, VOUT2 (K9-K12, L9-L12, M9-M12; C9-C12, D9-D12, E11-E12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND1, GND2 (H1, H7-H12, J6-J12, K6-K8, L1, L7-L8, M1-M8; A1-A12, B1, B7-B12, C7-C8, D6-D8, E1, E8-E10): Power Ground Pins for Both Input and Output Returns.

TRACK1, TRACK2 (L3, E3): Output Voltage Tracking Pins. When the module is configured as a master output, then a soft-start capacitor is placed on the RUN/SS pin to ground to control the master ramp rate, or an external ramp can be applied to the master regulator's track pin to control it. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin on the slave regulator. If tracking is not desired, then connect the TRACK pin to VIN. Load current must be present for tracking. See the Applications Information section.

FB1, FB2 (L6, E6): The Negative Input of the Switching Regulators' Error Amplifier. Internally, these pins are connected to VOUT with a 4.99k precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins. Two power modules can current share when this pin is connected in parallel with the adjacent module's FB pin.

FB3 (F6): The Negative Input of the LDO Error Amplifier. Internally the pin is connected to LDO_OUT with a 4.99k resistor. Different output voltages can be programmed with an additional resistor between the FB3 and GND pins.

COMP1, COMP2 (L5, E5): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Two power modules can current share when this pin is connected in parallel with the adjacent module's COMP pin. Each channel has been internally compensated.

PGOOD1, PGOOD2 (L4, E4): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN/SS1, RUN/SS2 (L2, E2): Run Control and Soft-Start Pin. A voltage above 0.8V will turn on the module, and below 0.5V will turn off the module. This pin has a 1M resistor to VIN and a 1000pF capacitor to GND.

SW1, SW2 (H2-H6, B2-B6): The switching node of the circuit is used for testing purposes. This can be connected to copper on the board for improved thermal performance. SW1 and SW2 must be floating on separate copper planes.

LDO_IN (G1-G4): VLDO Input Power Pins. Place input capacitor close to these pins.

LDO_OUT (G9-G12): VLDO Output Power Pins. Place output capacitor close to these pins. Minimum 1mA load is necessary for proper output voltage accuracy.

BOOST3 (E7): Boost Supply for Driving the Internal VLDO NMOS Into Full Enhancement. The pin is use for testing the internal boost converter. The output is typically 5V.

GND3 (F1-F5, F7, F9-F12, G6-G8): The power ground pins for both input and output returns for the internal VLDO.

PGOOD3 (G5): VLDO Power Good Pin.

EN3 (F8): VLDO Enable Pin.

OPERATION

Dual Switching Regulator Section

The LTM4615CN is a standalone dual non-isolated switching mode DC/DC power supply with an additional onboard 1.5A VLDO. It can deliver up to 4A of DC output current for each channel with few external input and output capacitors. This module provides two precisely regulated output voltages programmable via one external resistor for each channel from 0.8V DC to 5V DC over a 2.375V to 5.5V input voltage range. The VLDO is an independent 1.5A linear regulator that can be powered from either switching converter. The typical application schematic is shown in Figure 1.

The LTM4615CN has two integrated constant frequency current mode regulators, with built-in power MOSFETs with fast switching speed. The typical switching frequency is 1.25MHz. With current mode control and internal feedback loop compensation, these switching regulators have sufficient stability margins and good transient performance under a wide range of operating conditions, and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, current limiting is provided in an overcurrent condition with thermal shutdown. In addition, internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the particular output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET, M1, is turned off and bottom FET, M2, is turned on and held on until the overvoltage condition clears, or current limit is exceeded.

Pulling each specific RUN/SS pin below 0.8V forces the specific regulator controller into its shutdown state, turning off both M1 and M2 for each power stage. At low load current, each regulator works in continuous current mode by default to achieve minimum output voltage ripple. The TRACK pins are used for power supply tracking for each specific regulator. See the Applications Information section.

The FB pins are used to program the specific output voltage with a single resistor to ground.

VLDO Section

The VLDO (very low dropout) linear regulator operates from a 1.14V to 3.5V input. The VLDO uses an internal NMOS transistor as the pass device in a source-follower configuration. The BOOST3 pin is the output of an internal boost converter that supplies the higher supply drive to the pass device for low dropout enhancement. The internal boost converter operates on very low current, thus optimizing high efficiency for the VLDO in close to dropout operation.

An undervoltage lockout comparator on the LDO ensures that the boost voltage is greater than 4.2V before enabling the LDO, otherwise the LDO is disabled. The LDO provides a high accuracy output capable of supply 1.5A of output current with a typical drop out of 100mV. A single ceramic 10µF capacitor is all that is required for output capacitor bypassing. A low reference voltage allows the VLDO to have lower output voltages than the commonly available LDO.

The device also includes current limit and thermal overload protection. The NMOS follower architecture has fast transient response without the traditional high drive currents in dropout. The VLDO includes a soft-start feature to prevent excessive current on the input during start-up. When the VLDO is enabled, the soft-start circuitry gradually increases the reference voltage from 0V to 0.4V over a period of approximately 200µs.

APPLICATIONS INFORMATION

Dual Switching Regulator

The typical LTM4615CN application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 1 for specific external capacitor requirements for a particular application.

VIN to VOUT Step-Down Ratios

There are restrictions in the maximum VIN to VOUT stepdown ratio that can be achieved for a given input voltage on the two switching regulators. The LTM4615CN is 100% duty cycle, but the VIN to VOUT minimum dropout will be a function the load current. A typical 0.5V minimum is sufficient.

Output Voltage Programming

Each regulator channel has an internal 0.8V reference voltage. As shown in the block diagram, a 4.99k internal feedback resistor connects the VOUT and FB pins together. The output voltage will default to 0.8V with no feedback resistor. Adding a resistor RFB from the FB pin to GND programs the output voltage:

$$R_{FB} = \frac{4.99k}{\frac{V_{OUT}}{0.8V} - 1}$$

VOUT	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
FB	OPEN	10k	5.76k	3.92k	2.37k	1.62k

Input Capacitors

The LTM4615CN module should be connected to a low AC impedance DC source. One 4.7µF ceramic capacitor is included inside the module for each regulator channel. Additional input capacitors are needed if a large load step is required, up to the full 4A level, and for RMS ripple current requirements. A 47µF bulk capacitor can be used for more input capacitance.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

η% is the estimated efficiency of the power module. D is the switching duty cycle:

$$D = \frac{V_{OUT}}{V_{IN}}$$

In the above equation, η% is the estimated efficiency of the power module. If a low inductance plane is used to power the device, then no input capacitance is required. The internal 4.7µF ceramics on each channel input are typically rated for 1A of RMS ripple current up to 85°C operation. The worse-case ripple current for the 4A maximum current is 2A or less. An additional 10µF or 22µF ceramic capacitor can be used to supplement the internal capacitor with an additional 1A to 2A ripple current rating.

Output Capacitors

The LTM4615CN switchers are designed for low output voltage ripple on each channel. The bulk output capacitors are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. The output capacitors can be a low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range is 66µF to 100µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 1 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2.5A/ µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

Fault Conditions: Current Limit and Overtemperature Protection

The LTM4615CN has current mode control, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient. Along with current limiting in the event of an overload condition, the LTM4615CN has overtemperature shutdown

protection that inhibits switching operation around 150°C for each channel.

Run Enable and Soft-Start

The RUN/SS pins provide a dual function of enable and soft-start control for each channel. The RUN/SS pins are used to control turn on of the LTM4615CN. While each enable pin is below 0.5V,the LTM4615CN will be in a low quiescent current state. At least a 0.8V level applied to the enable pins will turn on the LTM4615CN regulators. This pin can be used to sequence the regulator channels. The soft-start control is provided by a 1M pull-up resistor (RSS) and a 1000pF capacitor (CSS) as drawn in the block diagram for each channel. An external capacitor can be applied to the RUN/SS pin to increase the soft-start time. A typical value is 0.01µF. The approximate equation for soft-start:

$$t_{ss} = \ln\left(\frac{V_{IN}}{V_{IN} - 1.8V}\right) \cdot R_{ss} \cdot C_{ss}$$

The soft-start function can also be used to control the output ramp-up time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. Either output can be tracked up or down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4615CN uses a very accurate 4.99k resistor for the internal top feedback resistor. Figure 2 shows an example of coincident tracking.Equations:

$$TRACK1 = \frac{R_{FB1}}{4.99k + R_{FB1}} \cdot Master$$

$$SLAVE = \left(1 + \frac{4.99k}{R_{FB1}}\right) \cdot TRACK1$$

TRACK1 is the track ramp applied to the slave's track pin. TRACK1 applies the track reference for the slave output up to the point of the programmed value at which TRACK1 proceeds beyond the 0.8V reference value. The TRACK1 pin must go beyond the 0.8V to ensure the slave output has reached its final value.

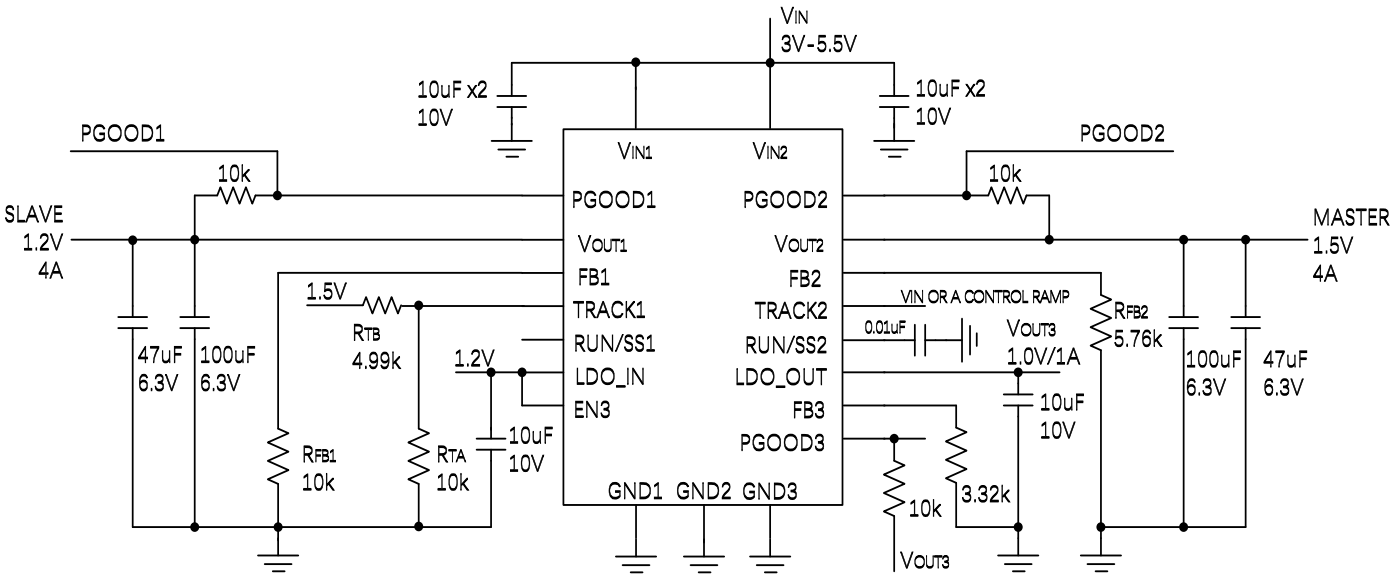


Fig2. Dual Outputs (1.5V and 1.2V) with Tracking

Power Good

PGOOD1 and PGOOD2 are open-drain pins that can be used to monitor valid output voltage regulation. These pins monitor a ±7.5% window around the regulation point. If the output is disabled, the respective pin will go low.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for all output voltages. Table 1 is provided for most application requirements.

VLDO SECTION

Adjustable Output Voltage

The output voltage is set by the ratio of two resistors. A 4.99k resistor is built onboard the module from LDO_OUT to FB3. An additional resistor (R_{FBLDO})is required from FB3 to GND3 to set the output voltage over a range of 0.4V to 2.6V. Minimum output current of 1mA is required for full output voltage range.

Equation:

$$V_{LDO\_OUT} = 0.4V \cdot \frac{\frac{4.99k}{N} + R_{FBLDO}}{R_{FBLDO}}$$

Power Good Operation

The VLDO includes an open-drain power good (PGOOD3) pin with hysteresis. If the VLDO is in shutdown or under UVLO conditions (BOOST3 < 4.2V), then PGOOD3 is low impedance to ground. PGOOD3 becomes high impedance when the VLDO output voltage rises to 93% of its regulated voltage. PGOOD3 stays high impedance until the output voltage falls to 91% of its regulated voltage. A pull-up resistor can be inserted between the PGOOD3 pin and a positive logic supply such as the VLDO output or VIN. LDO_IN should be at least 1.14V or greater for power good to operate properly.

Output Capacitance and Transient Response

The VLDO is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitors affects stability, especially smaller value capacitors. An output capacitor of 10µF or greater with an ESR of 0.05Ω or less is recommended to ensure stability. Larger value capacitors can be used to reduce the transient deviations under load changes. Bypass capacitors that are used at the load device can also increase the effective output capacitance. High ESR tantalum or electrolytic bulk capacitance can be used, but a ceramic capacitor must be used in parallel at the output. Extra consideration should be given to the use of ceramic capacitors related to dielectrics, temperature and DC bias effects on the capacitor. The VLDO requires a minimum 10µF value. The X7R and X5R dielectrics are more stable with DC bias and temperature, thus more preferred.

Parallel Switching Regulator Operation

The LTM4615CN switching regulators are inherently current mode control. Paralleling will have very good current sharing. This will balance the t hermals on the design.

Figure 4 shows a schematic of a parallel design. The voltage feedback equation changes with the variable N as channels are paralleled.

$$V_{OUT} = 0.8V \cdot \frac{\frac{4.99k}{N} + R_{FB}}{R_{FB}}$$

N is the number of paralleled channels.

Short-Circuit/Thermal Protection

The VLDO has built-in short-circuit current limiting of ~3A as well as overtemperature protection. During short-circuit conditions the device is in control to 3A, and as the internal temperature rises to approximately 150°C, then the internal boost and LDO are shut down until the internal temperature drops back to 140°C. The device will cycle in and out of this mode with no latchup or damage. Long term over stress in this condition can degrade the device over time.

Reverse Current Protection

The VLDO features reverse current protection to limit current draw from any supplementary power source at the output. Reverse input current will spike up as LDO_IN gets to within about 30mV of LDO_OUT as reverse current protection circuitry is disabled and normal operation resumes. As LDO_IN transitions above LDO_OUT the reverse current transitions into short circuit current as long as LDO_OUT is held below the regulation voltage.

Safety Considerations

The LTM4615CN modules do not provide galvanic isolation from VIN to VOUT. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4615CN makes the PCB board layout very simple and easy.However,to optimize its electrical and thermal performance,some layout considerations are still necessary.

- Use large PCB copper areas for highcurrent path, including VIN, GND and VOUT. lt helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the GND and VOUT pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection betweenthe top layer and other power layers.
- Do not put via directly on pads unless the via is capped.

Figure 3 gives a good example of the recommended layout.

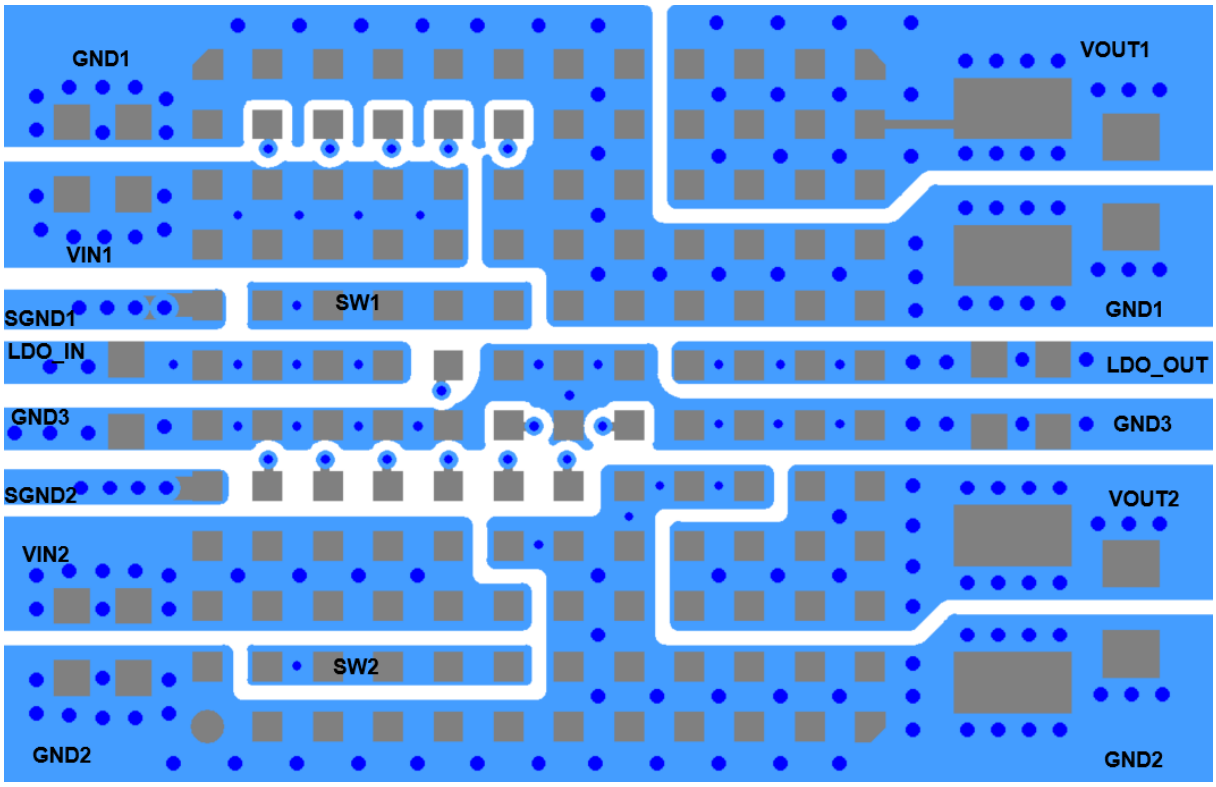


Fig3. Recommended PCB Layout

Table1. Output Voltage Response vs Component Matrix (Refer to Figure 1)

C_{OUT} VENDORS	PART NUMBER	DESCRIBTION
Murata	GRM188Z71A106KA	10μF、10V、X7R、0603
Fenghua	0603BT106K100NT	10μF、10V、X7T、0603
Murata	GRM32EC70J107ME	100μF、6.3V、X7S、1210
Fenghua	1210BS107M6R3NT	100μF、6.3V、X7S、1210
Murata	GRM21BR61A476ME	47μF、10V、X5R、0805
Fenghua	0805X476M100NT	47μF、10V、X5R、0805

V_{OUT1}, V_{OUT2} (V)	V_{IN1}, V_{IN2} (V)	R_{FB1}, R_{FB2} (kΩ)	C_{IN1} (CERAMIC)	C_{IN2} (CERAMIC)	C_{OUT1} (CERAMIC)	C_{OUT2} (CERAMIC)
1	3.3	20	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1	5	20	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.2	3.3	10	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.2	5	10	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.5	3.3	5.76	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.5	5	5.76	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.8	3.3	3.92	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
1.8	5	3.92	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
2.5	3.3	2.37	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
2.5	5	2.37	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF
3.3	5	1.62	10μF x 2	10μF x 2	47μF + 100μF	47μF + 100μF

V_{LDO_OUT} (V)	V_{LDO_IN} (V)	R_{FB3} (kΩ)	C_{IN3} (CERAMIC)	C_{OUT3} (CERAMIC)
0.6	1.2	10	10μF	10μF
0.6	3.3	10	10μF	10μF
0.8	1.2	4.99	10μF	10μF
0.8	3.3	4.99	10μF	10μF
1.0	1.2	3.3	10μF	10μF
1.0	3.3	3.3	10μF	10μF
1.2	1.5	2.49	10μF	10μF
1.2	3.3	2.49	10μF	10μF
1.5	1.8	1.82	10μF	10μF
1.5	3.3	1.82	10μF	10μF
1.8	2.5	1.43	10μF	10μF
1.8	3.3	1.43	10μF	10μF
2.5	3.3	0.953	10μF	10μF

APPLICATIONS INFORMATION

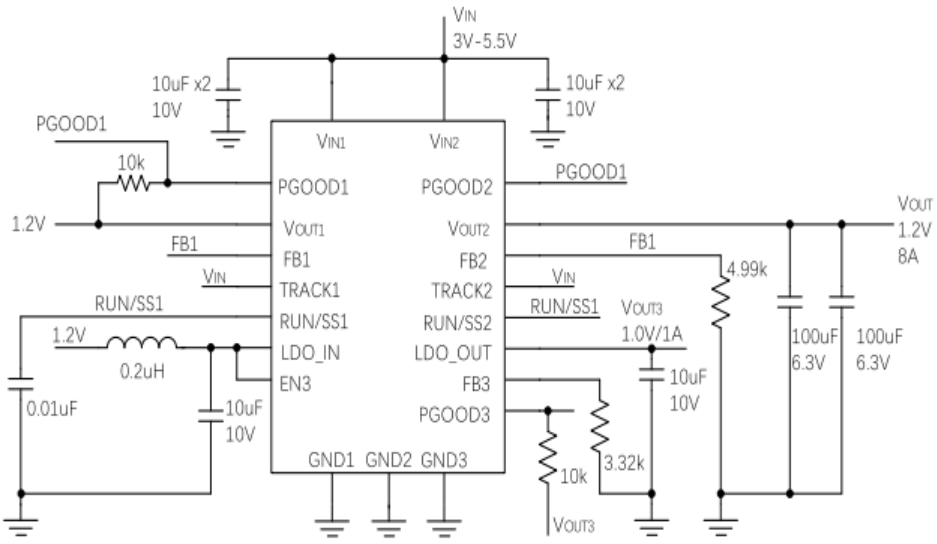


Fig4. Parallel 1.2V at 8A Design

Humidity sensitivity before SMT upper plate

LTM4615CN products must be dried before plate, otherwise it may cause poor welding or even damage due to moisture. According to JEDEC standard J-STD-033 "Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices" , please use the following conditions to baking the module: The temperature is 125 °C for 48 hours or more. Please refer to Fig.5 for the temperature curve of SMT reflow soldering.

A reminder: Please try to avoid using high temperature welding methods (such as high temperature heat gun, high temperature hot plate, etc.) that exceed the peak temperature of SMT reflow soldering to solder the upper plate, or disassemble the LTM4615CN product module. Any high temperature welding and disassembly methods that exceed the peak temperature of SMT reflow soldering may cause irreversible damage to the product. For products that exceed the peak temperature of SMT reflow soldering and disassembling, manufacturers will not guarantee the performance of the product, and it is difficult to make an accurate failure analysis.

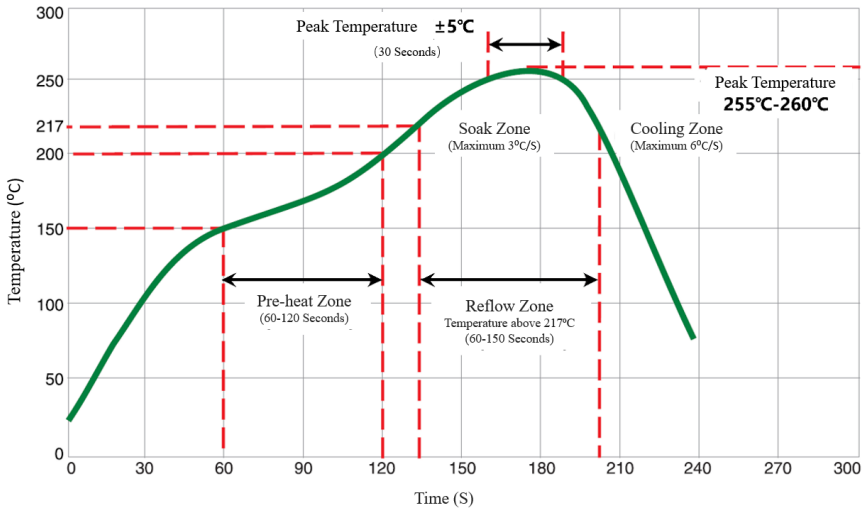
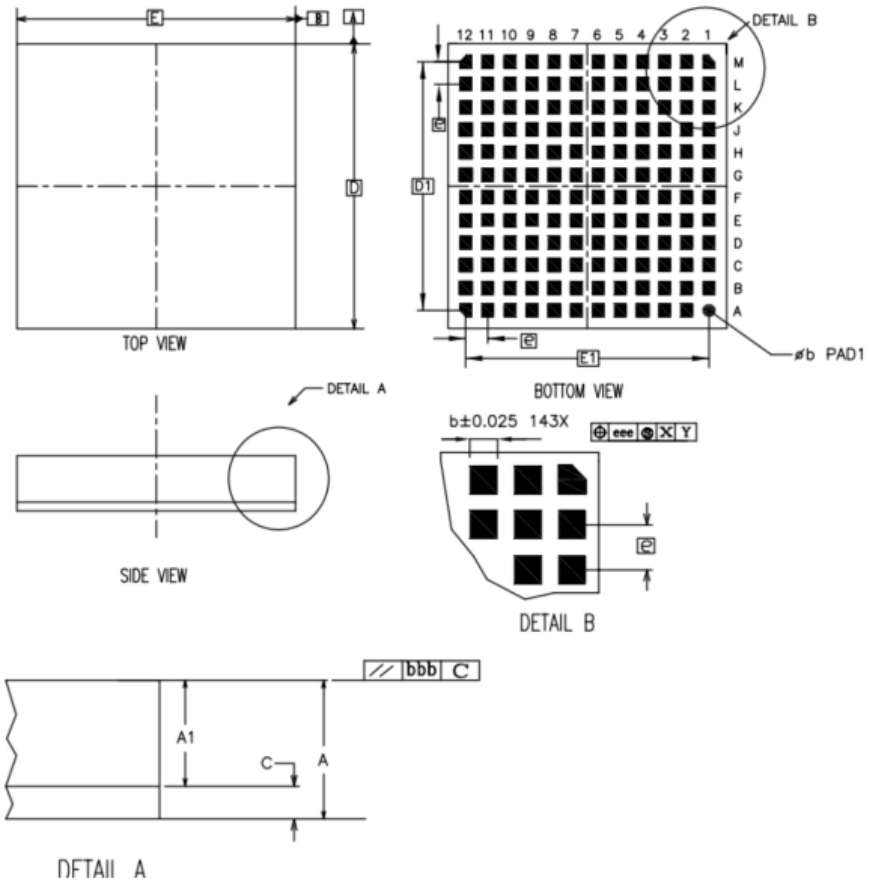


Fig5. Reflow Soldering Temperature Curve

PACKAGING DESCRIPTION



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.9	3.0	3.1
A1	2.45	2.5	2.55
c	0.45	0.5	0.55
D	15.90	16.00	16.10
D1		13.97 BSC.	
E	15.90	16.00	16.10
E1		13.97 BSC.	
b	0.60	0.63	0.66
e		1.27 BSC.	
bbb		0.10	
eee		0.05	
N		144	
REF: JEDEC MS-028			

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