PRELIMINARY

PSoC 4 HV Precision Analog 144k Datasheet

Programmable System-on-Chip (PSoC)

General Description

PSoC™ 4 HV Precision Analog (PA) is a fully integrated programmable embedded system for lead acid battery monitoring and management. The system features an Arm® Cortex® M0+ processor and programmable and reconfigurable analog and digital blocks.

Features

Automotive Electronics Council (AEC) AEC-Q100 Qualified

32-bit MCU Subsystem

- 24- or 48-MHz Arm Cortex M0+ CPU with DMA Controller
- Up to 128 KB of code flash with ECC
- Up to 8 KB of data flash with ECC
- Up to 8 KB of SRAM with ECC
- 1 KB of Supervisory Flash (SFlash) available for storing constants

Precision Analog

- Two Precision ΔΣ ADCs (16-20+ bits)
- Current Channel with automatic gain
- Voltage Channel with HV input divider
- Temperature and Diagnostic Channels
- Supports both internal and external temperature sensing
- Digital filtering, accumulators, and threshold comparisons on all channels

High-voltage subsystem

- Operates directly off 12-V/24-V battery (tolerates up to 42 V)
- Integrated LIN transceiver
- ADC input voltage divider

Functional Safety for ASIL-B

- The device will be developed according to the development process of ISO 26262 for ASIL B as a Safety Element out of Context (acc. ISO26262-10:2018E, clause 9)
- Memory Protection Unit (MPU)
- Window Watchdog Timer (WDT) with Challenge-Response functionality
- Supply monitoring; detection of overvoltage and brownout events for 3.3-V and 1.8-V supplies
- Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash)
- Analog diagnostics (backup reference voltage, redundancy in voltage, current, and temperature measurement paths)

Timing and Pulse-Width Modulation

- Four 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and pseudo-random modes
- Quadrature decoder

Clock Sources

- ±2% up to 49.152-MHz Internal Main Oscillator (IMO)
- ±1% 2-MHz High-Precision Oscillator (HPOSC)
- ±5% 32-kHz Precision Internal Low-power Oscillator (PILO)
- ±1% accuracy on IMO and PILO when software calibrated to the HPOSC
- 40-kHz Internal Low-speed Oscillator (ILO)

Communication

- One independent run-time reconfigurable serial communication block (SCB) with re-configurable I^2C, SPI, UART, or LIN Slave functionality
- One independent Local Interconnect Network (LIN) block
- LIN protocol compliant with LIN 2.2A and ISO 17987

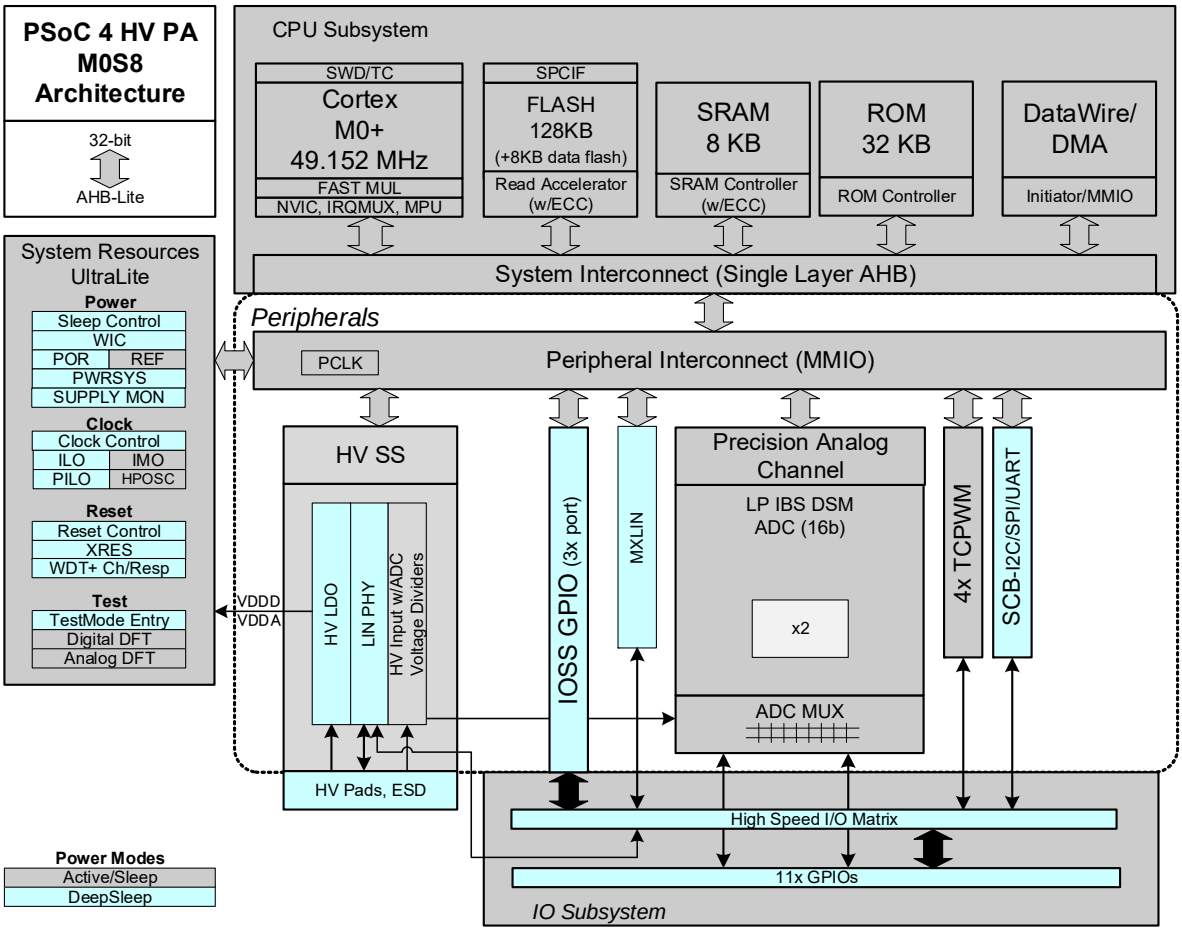
Package

- 32-QFN with wettable flanks (6 x 6 mm)
- Up to 11 GPIOs

Contents

1. Block Diagram

Figure 1-1. Block Diagram



PSoC 4 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The SWD interface is fully compatible with industry-standard third-party tools. PSoC 4 provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus, firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4, with device security-enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4 allows the customer to make.

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2. Functional Definition

2.1 CPU and Memory Subsystem

2.1.1 CPU

The Cortex-M0+ CPU in the PSoC 4 HV PA is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0+ CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

Programs can execute from SROM, SRAM, or Flash memory.

The CPU also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4 HV PA has four break-point (address) comparators and two watchpoint (data) comparators. The CPU also implements a design time configurable Memory Protection Unit (MPU).

2.1.2 Memory with ECC

Flash and SRAM include Error Correction Code (ECC) circuitry capable of correcting single-bit errors and detecting 2-bit errors. If a single-bit error occurs, the data is corrected in-line, error information is stored (address and data), and an error flag is set which can generate an interrupt. If a multi-bit error is detected, the error information is stored and either an interrupt or reset is generated.

2.1.3 Flash

The PSoC 4 HV PA has a flash module with separate controllers for code flash and data flash. The flash is with an accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% single-cycle SRAM access performance on average. Part of a flash module can be used to emulate EEPROM.

2.1.4 SRAM

Volatile static memory (SRAM) is used by the processor for storing variables and can program code, which can be written and executed in SRAM. SRAM memory is retained in all power modes (Active, Sleep, and Deep Sleep). At power-up, SRAM is uninitialized and should be written by application code before reading.

2.1.5 SROM

A supervisory read-only memory (ROM) contains boot and configuration routines which can't be modified.

2.1.6 DMA

A DMA engine with eight channels is provided that can do 32-bit transfers and has chainable ping-pong descriptors. This DMA engine allows data transfer between memory, registers, and peripherals without CPU intervention. DMA transfers can occur while the CPU is powered down. Descriptors identify the data source and destination along with other information.

2.2 System Resources

2.2.1 Power System

The power system includes regulators to generate appropriate voltages. The PSoC 4 HV PA operates at full performance from a single supply on VBAT over a voltage range of 3.6 V to 28 V and remains functional up to 42 V. In addition to an active mode, the PSoC 4 HV PA has two low-power modes called Sleep and Deep Sleep. Transitions between the three power modes are managed by the power system in the system resources subsystem (SRSS).

The high-voltage regulator generates a 3.3-V supply from VBAT for V_{DDD} and V_{DDA}. V_{DDA} powers analog circuits, while V_{DDD} provides power for I/Os (GPIOs) and the 1.8-V core power regulators. There are different internal core regulators to support the various power modes. These include Active Digital regulator and Deep Sleep regulator.

Refer to Figure 2-1 and Table 2-1 for the power system block diagram and current specifications.

Figure 2-1. Power System Block Diagram

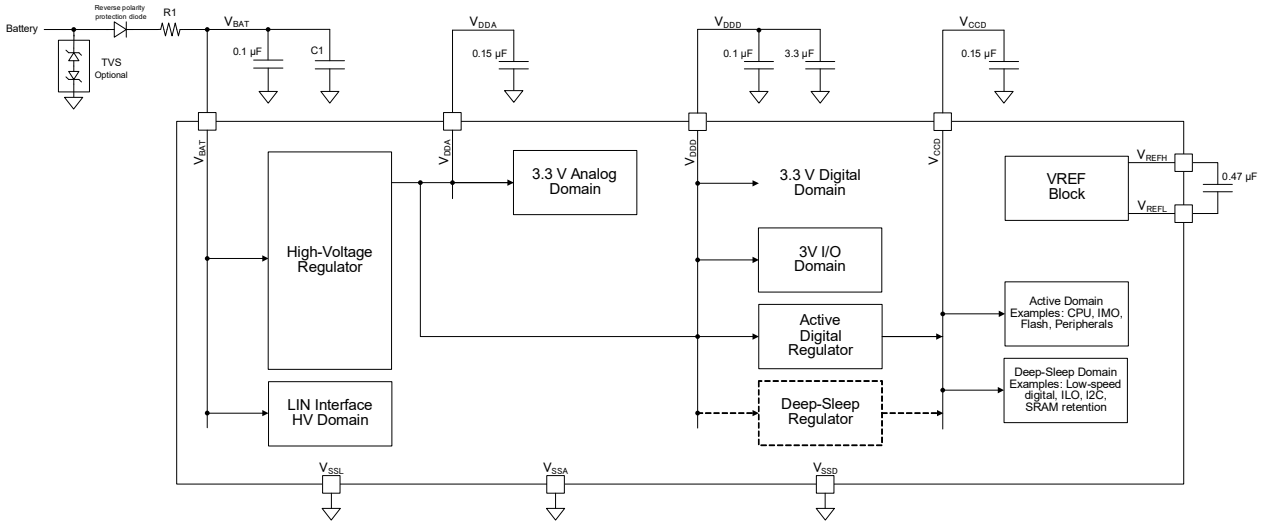


Table 2-1. R1/C1 Max Current Specifications

Configuration	R1	C1	Max Current
1	10-15 ohm	1.1 µF	20 mA
2	6.6-10 ohm	2 × 2.2 µF	30 mA

Bypass capacitors must be used from V_{DDD}, V_{DDA}, and V_{CCD} to ground. These capacitors should typically be X7R ceramic or better.

Table 2-2. Bypass Capacitors

Supply Pair	Nominal Cap	Tolerance
$V_{BAT} - V_{SSD}$	0.1 µF 2.2 µF	+65% / -65% +10% / -50%
$V_{DDD} - V_{SSD}$	0.1 µF 3.3 µF	+65% / -65% +10% / -50%
$V_{DDA} - V_{SSA}$	0.15 µF	+10% / -50%
$V_{CCD} - V_{SSD}$	0.15 µF	+10% / -50%
$V_{REFH} - V_{REFL}$	0.47 µF	+38% / -48%

The system has a high-voltage (HV) regulator which generates 3.3-V supplies and several regulators for various low-voltage core domains. The analog circuits run directly from the VDDA supply generated by the HV regulator. The core regulators include an Active Digital regulator for digital circuitry and a separate regulator for Deep Sleep. The Deep Sleep regulator has switches to pass high power regulator voltages to loads when the low-power regulators are not required.

The HV regulator is always enabled. The Active Digital regulator is enabled during the Active or Sleep power modes. It is turned off in the Deep Sleep power mode. The Deep Sleep regulator fulfills power requirements in the low-power modes.

Table 2-3. Regulators and Operating Modes

Mode	HV Regulator	Active Regulator	Deep Sleep Regulator
Active	On	On	On
Sleep	On	On	On
Deep Sleep	On	Off	On

2.2.2 Power System Supervision and Monitoring

The power supply includes supervision and monitoring to assure voltage levels as required exist for the respective modes. The voltage monitoring system includes power-on-reset (POR) and brownout detection (BOD). The supervisor either delays mode transitions (on POR, for example) until required voltage levels are achieved for proper function or generates resets (BOD, OVD) as appropriate.

Power-On-Reset (POR): POR circuits provide a reset pulse during the initial power ramp. POR circuits monitor V_{CCD} (core) voltage. The POR threshold is between 0.8 V and 1.5 V and guarantees all circuits have been properly initialized prior to release. POR circuits are used during initial chip power-up and then disabled.

Brownout Detect (BOD): The BOD circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. BOD circuit monitors the V_{CCD} voltage. The BOD circuit generates a reset if core voltage dips below the minimum safe operating voltage (1.48 V–1.62 V in Active/Sleep and 1.11 V–1.5 V in Deep Sleep). The system will not come out of RESET until the supply is detected to be valid again.

To enable firmware to distinguish a normal power cycle from a brownout event, a special register is provided (RES_CAUSE), which will not be cleared after a BOD generated RESET. However, this register will be cleared if the device goes through POR or XRES.

Voltage References: The SRSS includes a bandgap and current references for use by analog circuits and SRSS voltage regulators. The HV regulator has another reference and the precision analog subsystem has a high-precision voltage reference which provides accurate voltage references for the ADCs. The ADCs may measure the SRSS and HV regulator references and all supply voltages (V_{DDD}, V_{DDA}, V_{CCD}, and V_{SS} and V_{SSA}) pins for diagnostic purposes. To allow better SNR and better absolute accuracy, an external reference or an external capacitor on the reference pin can improve accuracy by reducing noise.

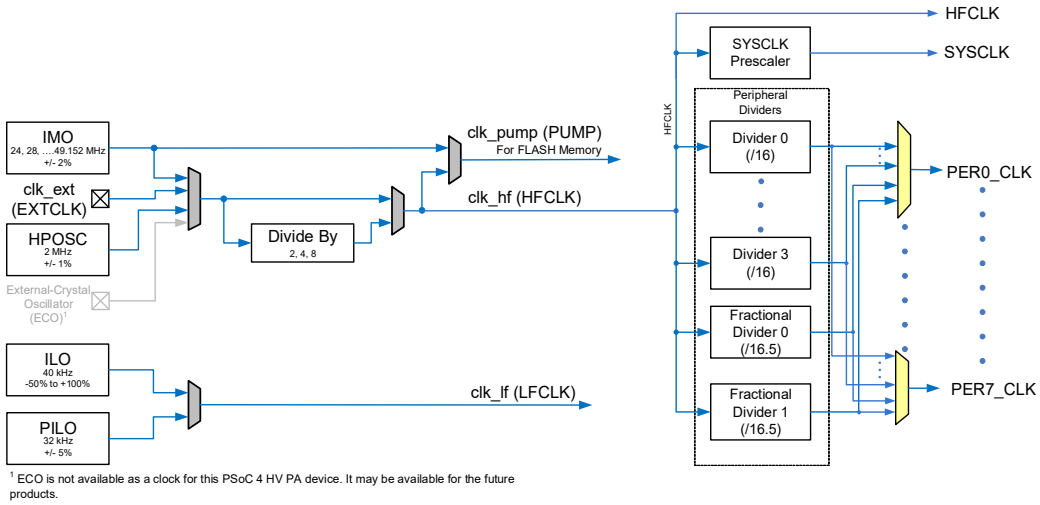
2.2.3 Clock System

The PSoC 4 HV PA clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching and for synchronizing clocks operating on different frequency domains to prevent meta-stable conditions. There are four oscillators implemented:

- One IMO for CPU and peripheral clock generation, which is usually configured for 24 MHz but can be programmed for frequencies from 24 MHz to 48 MHz in 4-MHz steps. The 48-MHz setting can be boosted to 49.152 MHz.
- One high-precision fixed frequency 2-MHz oscillator for precision timing (HPOSC)
- One low-power 40-kHz low-speed oscillator (ILO)
- One 32-kHz precision low-power oscillator (PILO) for wakeup timers and watchdog timers.

There are also provisions for an external clock supplied by a GPIO pin. The ILO and PILO are permanently powered in all power modes.

Figure 2-2. PSoC 4 HV PA Clocking Architecture



Software can lock the IMO and ILO to the HPOSC to increase precision of those oscillators. Software can also lock any of the oscillators to external time references such as the external clock input or LIN bit rate. Software lock is accomplished with dedicated calibration counters that will be available in the system resources subsystem. The oscillators are designed in such a way that trim changes do not glitch or disturb clock outputs.

IMO Clock Source: The IMO is the primary source of internal clocking in the PSoC 4 HV PA. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The 48-MHz setting can be boosted to 49.152 MHz using "Special" calibration data stored in SFLASH. IMO tolerance with Cypress-provided calibration settings is ±2%. This clock runs in Active and Sleep modes.

HPOSC Clock Source: The HPOSC is a 2 MHz 1% precision oscillator, which is on in Active power and Sleep mode and off in Deep Sleep modes. During Active mode, high-frequency precision is required for accurate timing of ADC measurements to accurately determine charge and discharge energy (amp-hour) balance. This is achieved with the IMO slaved to the HPOSC with software tracking.

PILO Clock Source: The Precision Internal Low Speed Oscillator (PILO) is a very low power oscillator with a nominal frequency of 32 kHz. It is primarily used to generate clocks for peripherals in low power modes. The PILO is implemented with the focus on low-power in the deep-sleep to keep supply current under 50uA. The accuracy over temperature and lifetime without periodic synchronization to the HPOSC is FLSO_ACCY1 (±5%, see parameter section). By means of regular synchronization with the HPOSC at least once per second, the same accuracy as in normal mode can be achieved (FLSO_ACCY2, ±1%, see parameter section). This accuracy can be maintained at least 60s after the last synchronization calibration while temperature and voltage are stable.

The PILO clocks low-power digital blocks including the watchdog timers and a lifetime counter. In active mode, it can also generate strobes enabling TCPWM counters to be used with software for calibrating of the ILO.

ILO Clock Source: The ILO operates with no external components and outputs a stable clock at 40-kHz nominal. The ILO is relatively low power and low accuracy. The ILO is available in all power modes. The ILO is a relatively inaccurate (–50% to +100% over voltage and temperature) oscillator, which is used to generate low-frequency clocks.

Lifetime Counter: A 32-bit lifetime counter with a prescaler (/1 to /32) is available and triggered from the PILO clock. This counter runs in all modes and can be reset by POR. With the prescaler, the net resolution of the counter becomes 37-bit causing an overflow every 50 days. The counter will continue counting upon overflow.

Reset: The PSoC 4 HV PA can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

The following events cause resets:

- POR
- Brownout/Overvoltage
- Watchdog Reset
- Software Reset
- External Reset via XRES pin
- Fault system
- Protection violation

Watchdog Timers (WDT) . The WDTs are used to automatically reset the device in the event of an unexpected firmware execution path. They are also used as a wakeup source to periodically generate interrupts as a wakeup source in low-power modes. There are two WDTs, one that is implemented in HV logic (will reset the part if VCCD goes illegal) and a challenge-response WDT (CRWDT) implemented in the LV logic.

The CRWDT includes a window watchdog function, generating timeout events if the CRWDT is serviced too soon, too late, or with the wrong software key. A register identifies the timeout cause. It generates a watchdog reset or interrupt if serviced too soon or too late. Service too soon potentially means an infinite loop including watchdog service is executing, while too late means the processor could be stuck and not processing properly. The challenge/response means the watchdog service routines must present specific data or “keys” in the order expected by the watchdog or a fault will occur. The fault will generate a watchdog reset or interrupt with the reset recorded in the Reset Cause register. The causes can be conditions such as watchdog too soon, watchdog late, or wrong key received.

Further details of the CRWDT can be found in the technical reference manual.

2.3 Fixed Function Digital

2.3.1 Timer/Counter/PWM (TCPWM) Block

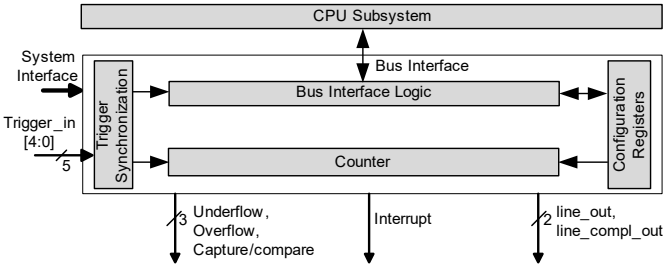
The TCPWM in PSoC 4 HV PA implements 16-bit timer, counter, pulse width modulator (PWM), and quadrature decoder functionality. Four TCPWM blocks exist on PSoC 4 HV PA. The block can be used to measure the period and pulse width of an input signal (timer), count several events (counter), generate PWM signals, or decode quadrature signals.

The block provides true and complementary outputs with programmable offset between them to allow dead-band between outputs for driving complementary PWM loads. It also has a Kill input to force outputs to a predetermined state; this is used to inhibit outputs when faults are detected without requiring the need and delay of software intervention.

Features:

- The TCPWM block supports the following operational modes:
  - Timer, Counter, Capture, Quadrature decoding
  - Pulse width modulation (PWM) including Pseudo-random PWM and PWM with dead time
  - PWM uses a period counter and capture counter - complementary outputs are available
- Multiple counting modes - up, down, and up/down
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Generate triggers based on Compare, Overflow, or Underflow.
- Supports interrupt on:
  - Terminal Count: The final value in the counter register is reached (zero or period count)
  - Capture: When a capture event occurs (the counter value at the time of capture is saved)
  - Compare: When the count equals the compare value
  - Synchronized counters: The counters can reload, start, stop, and count at the same time

Figure 2-3. TCPWM Block Diagram



2.4 Local Interconnect Network (LIN) Block

PSoC 4 HV PA features a dedicated LIN communication block that supports autonomous transfer of the LIN frame to offloading the CPU. Some of the key features of this block include:

- Certified at C&S according to LIN 2.2A / ISO 17987 standards
- Can be used with external LIN PHY, or routed through the internal LIN PHY.
- LIN protocol support in hardware according to LIN 2.2A / ISO 17987 standard
  - Master and slave functionality
  - Master node
    - Autonomous header transmission and autonomous response transmission and reception
  - Slave node
    - Autonomous header reception and autonomous response transmission and reception
  - Message buffer for PID, data, and checksum fields
  - Classic and enhanced checksum
  - Timeout detection
  - Error detection
  - Test modes including hardware error injection
  - Baud rate detection
  - 16x bit time oversampling

2.5 Serial Communication Block (SCB)

SCB supports three serial interface protocols: SPI, UART, and I^2C. Only one of the protocols is supported by an SCB at any given time. The PSoC 4 HV PA has one SCB.

This block supports the following features:

- UART with standard, SmartCard reader, Local Interconnect Network (LIN), and IrDA protocols
- UART with LIN slave functionality with LIN v1.3 and LIN v2.1/2.2/2.2A specification compliance
- SPI master and slave functionality with Motorola, TI, and NSC protocols
- I^2C master and slave functionality
- EZ mode for SPI and I^2C, which enables operation without CPU intervention
- Low-power (Deep Sleep) mode of operation for SPI and I^2C protocols (using external clocking)

2.5.1 UART Mode

This is a full-feature UART operating at up to 1 Mbps supporting automotive single-wire interface (LIN), infra-red interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the PSoC 4 HV PA UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

The Universal Asynchronous Receiver/Transmitter (UART) protocol is an asynchronous serial interface protocol. UART communication is typically point-to-point.

The UART interface consists of two signals:

- TX: Transmitter output
- RX: Receiver input

The UART can also connect to the internal Local Interconnect Network (LIN) PHY.

The UART mode has the following features:

- Asynchronous transmitter and receiver functionality
- Supported UART protocols include Standard UART, LIN, SmartCard (ISO7816) reader, and IrDA
- LIN support includes
  - Break detection
  - Baud rate detection
  - Collision detection (detect a dominant bus state when transmitting a recessive bit)
- Multi-processor mode
- Data frame size programmable from 4 to 9 bits
- Programmable number of STOP bits, which can be set in terms of half-bit periods between 1 and 4
- Parity (odd and even parity)
- Interrupt or polling CPU interface
- Programmable oversampling

2.5.2 SPI Mode

The Serial Peripheral Interconnect (SPI) mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

The SPI protocol is a synchronous serial interface protocol. Devices operate in either master or slave mode. The master initiates the data transfer. The SCB supports single-master-multiple-slaves topology for SPI. Multiple slaves are supported with individual slave select lines.

You can use the SPI master mode when the PSoC must communicate with one or more SPI slave devices. The SPI slave mode can be used when the PSoC must communicate with an SPI master device.

The SPI mode has the following features:

- Supports master and slave functionality
- Supports three types of SPI protocols:
  - Motorola SPI - modes 0, 1, 2, and 3
  - Texas Instruments SPI, with coinciding and preceding data frame indicator for mode 1
  - National Semiconductor (MicroWire) SPI for mode 0
- Supports up to four slave select lines
- Data frame size programmable from 4 bits to 16 bits
- Interrupts or polling CPU interface
- Programmable oversampling
- Supports EZ mode of operation - EZSPI mode allows for operation without CPU intervention
- Supports externally clocked slave operation:
  - In this mode, the slave operates in Active, Sleep, and Deep Sleep system power modes

A standard SPI interface consists of four signals as follows. These signals connect to GPIO pins:

- SCLK: Serial clock (clock output from the master, input to the slave).
- MOSI: Master-out-slave-in (data output from the master, input to the slave).
- MISO: Master-in-slave-out (data input to the master, output from the slave).
- Slave Select (SS): Usually an active low signal (output from the master, input to the slave).

2.5.3 I^2C Mode

The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4 HV PA and effectively reduces I^2C communication to reading from and writing to an array in memory. The block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

PSoC 4 HV PA is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system

The I²C mode has the following features:

- Master, slave, and master/slave mode
- Slow-mode (50 kbps), standard-mode (100 kbps), fast-mode (400 kbps), and fast-mode plus (1000 kbps) data-rates
- 7- or 10-bit slave addressing (10-bit addressing requires firmware support)
- Clock stretching and collision detection
- Programmable oversampling of I²C clock signal (SCL)
- Error reduction using a digital filter on the input path of the I²C data signal (SDA)
- Glitch-free signal transmission with an analog glitch filter
- Interrupt or polling CPU interface

2.5.4 LIN Slave Mode

The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN Slave is compliant with LIN v1.3, v2.1/2.2, ISO 17987-6, and SAE J2602-2 specification standards. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length.

2.6 GPIO

This section describes the PSoC 4 HV PA I/O system. The GPIO pins are grouped into ports; a port can have a maximum of eight GPIOs. The PSoC 4 HV PA has 11 GPIOs.

The GPIOs have these features:

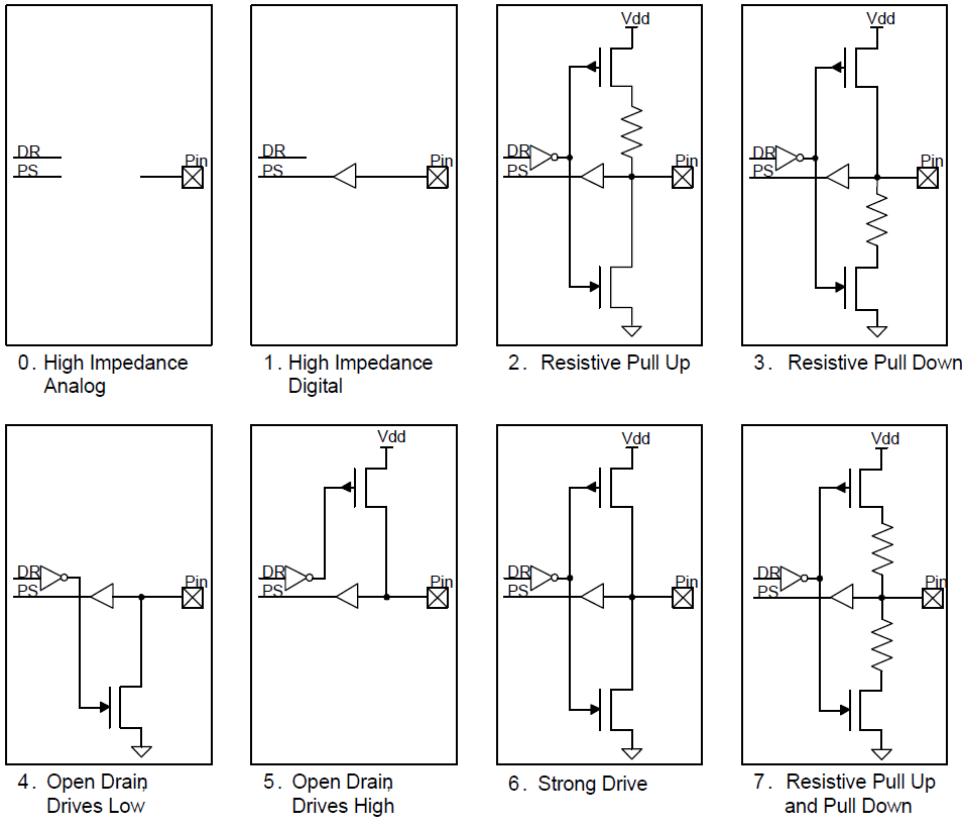
- Output drive modes include push-pull (strong or weak), open drain/source, high-z, and pull-up/pull-down
- Selectable CMOS and low-voltage LVTTL input buffer mode
- Edge-triggered interrupts on rising edge, falling edge, or on both the edges, on pin basis
- Individual control of input and output disables
- Hold mode for latching previous state (for retaining I/O state in Deep Sleep)
- Selectable slew rates allowing dV/dt control to assist with noise control to improve EMI

All GPIOs can be used to receive analog input signals for the ADCs.

During power-on and reset, GPIO outputs are disabled to prevent conflict with externally applied signals and prevent crowbar and/or excessive turn-on current. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. An interconnect network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin.

The following diagram illustrates the various available GPIO output drive modes.

Figure 2-4. GPIO Output Drive Modes



Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

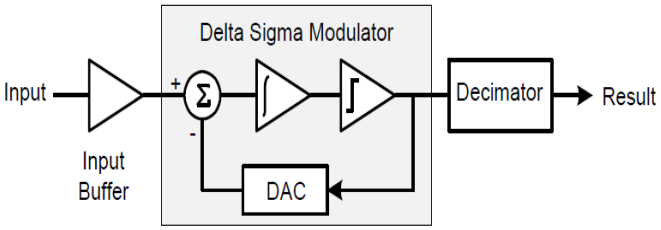
The PSoC 4 HV PA HV V_{DDD} regulator has enough capacity to drive internal loads and external loads up to 10 mA. DC GPIO loads are considered external loads. The combined DC GPIO and external load current must not exceed the available 10 mA. Care must be taken when driving DC loads, such as LEDs, to make sure the total current being sourced from the GPIOs does not exceed this limit.

2.7 Precision Analog Channel Subsystem (PACSS)

The PSoC 4 HV PA Precision Analog Channel Subsystem (PACSS) is a high-performance data acquisition system consisting of two delta-sigma analog-to-digital converters (ADCs) and support circuitry. The two ADCs can quickly switch between input sources to create a third “virtual” ADC. The PACSS includes an analog input multiplexer, input buffer amplifiers, delta-sigma modulators, decimators, and digital signal processing channels. There is also a precision voltage reference, current references, and temperature sensors.

The following is a simplified picture of a delta sigma ADC.

Figure 2-5. PACSS Overview



The delta-sigma ADC works by using a modulator, taking the difference between input and feedback signals (delta) and accumulating that difference (sigma) to produce a digital output. The digital stream goes to a decimator which converts the fast-oversampled bit stream into slower high-resolution results.

The PSoC 4 HV PA PACSS has two delta-sigma analog-to-digital converters (ADCs) to perform 16-bit measurements at a sample rate of up to 48 ksps for continuous measurements. Higher resolution can be achieved at slower sample rates by accumulating more modulator results in the decimator.

The PSoC 4 HV PA PACSS analog multiplexer selects between the differential input voltages including two HV voltage dividers, GPIO pads, internal temperature sensors, an external NTC temperature sensor, and diagnostic voltages. All analog signals can be supplied to either of the analog ADCs, which improves diagnostics since both ADCs can measure and compare the same signals.

The analog portion of the ADCs consists of a programmable gain amplifier, an anti-alias filter, a buffer, and a multi-level delta-sigma modulator (DSM). The output of the modulator goes to the digital portion of the channel and features a scaler, decimator, FIR filter, adder/multiplier to reduce gain and offset errors, averaging, and threshold comparisons.

There are four digital channels, which process outputs from either of the two analog DSMs. Two channels are with the FIR filter, and the other two are without the FIR Filter. The channels are typically used for current, voltage, temperature, and diagnostic measurements although they can be associated with any inputs (for example, V_{SENSE} can be measured by one channel while V_{DIAG} is measured by another).

The current channel has an automatic gain control, which allows a large dynamic range that enables measuring large starting currents or small battery-off currents. The gain of the current channel ranges from 1 to 512. Automatic gain can be disabled and set to a fixed value. A scaler between the modulator and decimator adjusts the weight of modulator data based on gain so the input to the LSB of the data going into the decimator is always 0.715 mA.

The gain of other channels is static instead of dynamic. Static gain is typically set to 1 but any value from 1 to 512 in powers of 2 can be used. The HV input channels have resistor voltage dividers, which attenuate the input voltage. The nominal divider ratio is 24x (28.8 V full-scale) with an optional value of 16x (19.2 V full scale).

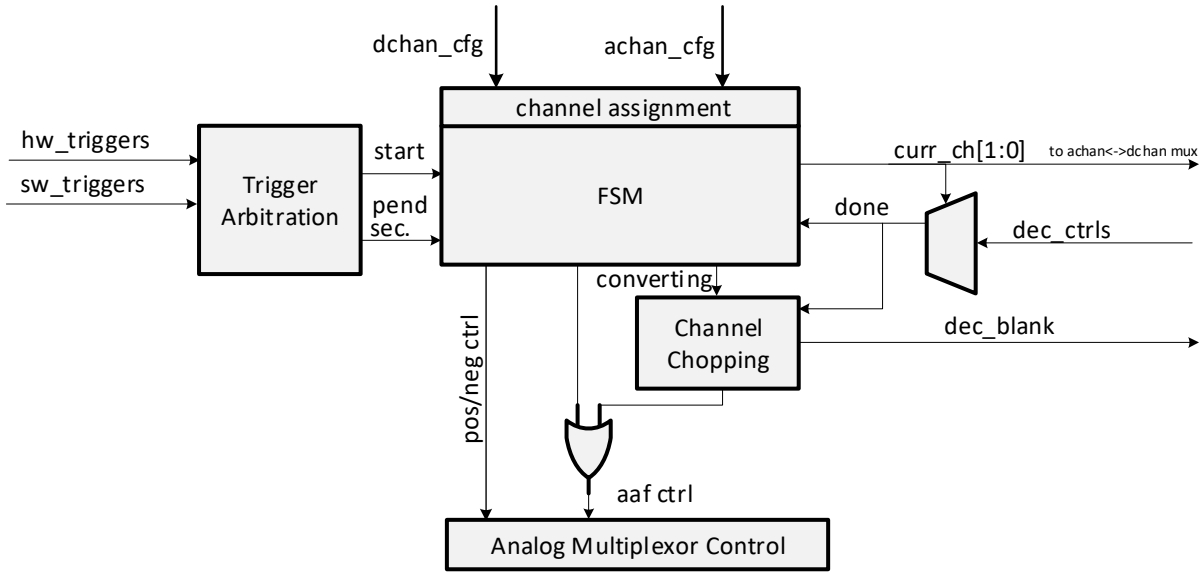
Chopping is used to minimize offset voltage error. Channel chopping is implemented to further reduce offset error. Channel chopping is making a measurement followed by a second measurement with inputs swapped and result multiplied by -1. The two samples are averaged, which removes any residual channel offset.

ADC measurements can be triggered by software or hardware. Hardware triggers can be generated by timers or GPIO inputs. The ADCs can be triggered independently or simultaneously. A SYNC function can be implemented to allow multiple PSoC 4 HV PA chips to perform simultaneous measurements. One device uses a GPIO output to simultaneously trigger the on-chip ADC measurements while signaling other PSoC 4 HV PA chips to trigger measurements. The SYNC signal can be set using either a timer or software to write to the GPIO.

2.7.1 PACSS Sequencer and Timing

The PACSS sequencer generates control signals for performing analog-to-digital conversion. A block diagram of the sequencer is shown here.

Figure 2-6. PACSS Sequencer



A peripheral clock from the System Wide Resource clock system is used for sequencer timing. The same clock is used for all ADC channels. The clock goes to the delta-sigma modulator (DSM) controller, which generate timing strobes with a finite state machine which are used by other sections of the sequencer. The DSM controller also includes control and status registers which are accessed from the µC and DMA channels using the AHB bus. The controller also generates interrupt and DMA requests.

ADC conversions are initiated by triggers from generated by other sources. Those sources include timers (TCPWM), input signals from GPIOs, software requests, and end-of-conversion commands from an active ADC. Triggers can start one or two ADCs - when triggering two ADCs, both ADCs start together. An arbiter is used to prioritize ADC conversion requests and start conversions when the ADCs become available.

The arbiter also controls the analog multiplex or control block, which selects the analog input associated with the trigger. The analog multiplex or control sends the appropriate select signals to the analog multiplex or to connect analog inputs to the ADCs.

The two ADC channels have a channel controller which generates timing for that channel. There are separate controls for the analog and digital portion of the channels. The analog timing signals control the delta-sigma modulator and chopping switches, while the digital timing signals clock data path registers including the decimator, finite impulse response filter, and comparators and accumulators.

At the beginning of the conversion sequence, a four-cycle reset of the modulator clears state from previous conversions (the integrators in the modulator are initialized by this reset). The length of a conversion cycle requires the same number of clocks as the OSR setting. After the modulator is reset, the decimation filter needs to stabilize before output data is valid. For continuous measurements, the decimator needs to be one order higher than the modulator to maintain stability over time, and therefore a Sinc4 decimator (one order higher than the third order modulator) is used. This means that the decimator output is valid after the fourth conversion and then every conversion thereafter. For example, an OSR of 64 with a 3.072-MHz clock requires ~1.3 µs for reset, ~20.8 µs per conversion (or 48 ksps) in continuous mode, and 86.6 µs for the initial result.

For incremental (one-shot) conversions, the decimator can be the same order as the modulator, so a Sinc3 is used which reduces latency to three conversion cycles. Using the same conditions as the example above, the result requires 64 µs.

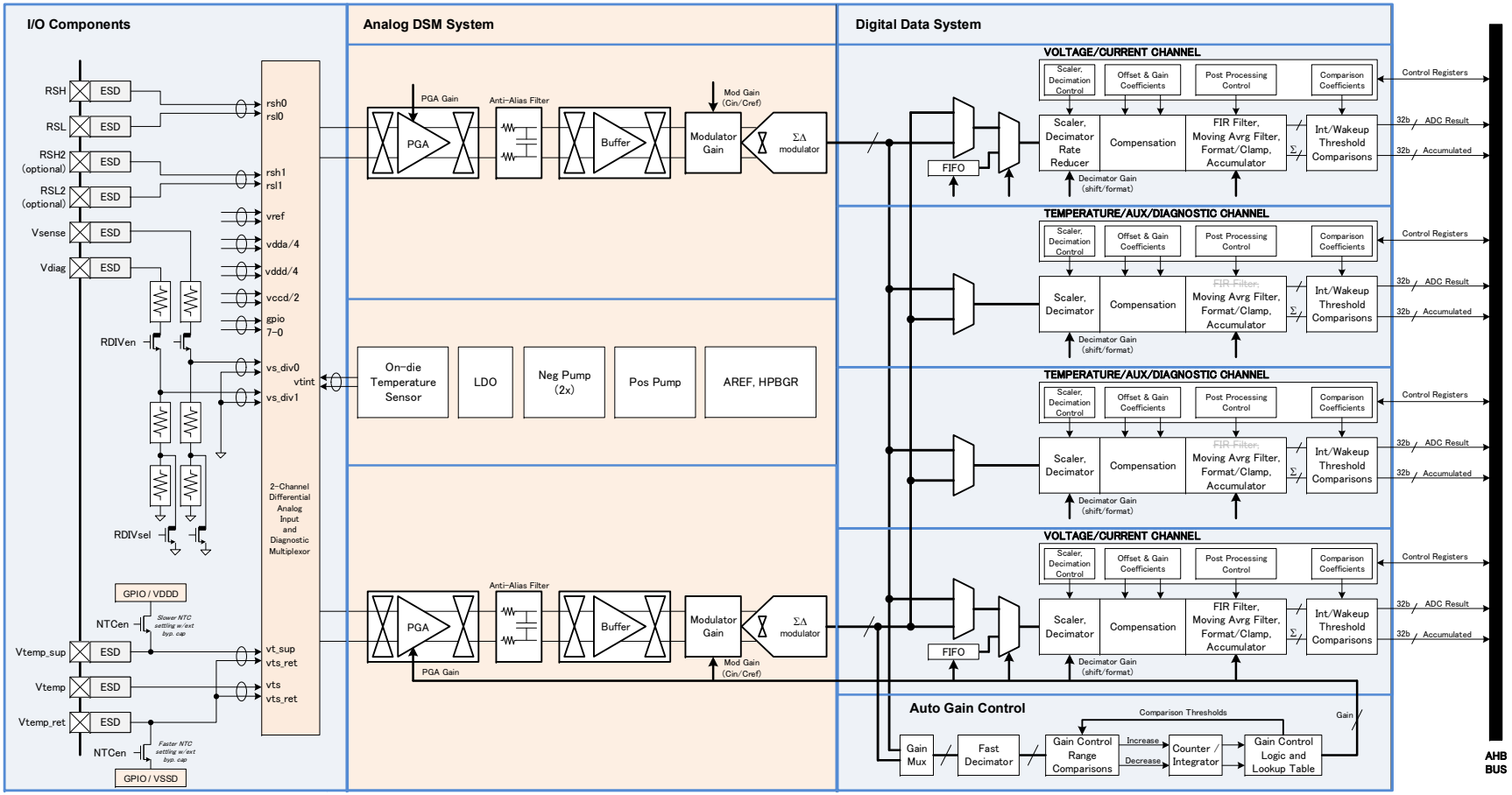
The incremental measurement mode can be used to measure several different voltage sources each conversion sequence while maintaining an aggregate sample rate. The sample rate can be adjusted by changing the OSR setting. With an OSR of 64 and a 3.072-MHz clock, the incremental sample rate is 16 ksps. If this mode is used to measure continuously, measure two different sources, the sample rate for each signal is half of the single source rate.

PSoC 4 HV PA takes advantage of the incremental mode to create three channels with only two analog front-ends.

Since lead-acid battery sensing applications only need 8 ksps on the main voltage and current channels, the third channel can use either one of the analog front-ends, which is not being used between V/I measurements. This channel can be used for temperature measurement, to measure other signals, or for diagnostics. Diagnostics can include measuring power supplies, references, and even the same signal measured by the other channel. The main advantage of using shared analog front-ends is power reduction.

2.8 PACSS Measurement/Acquisition System

Figure 2-7. PACSS Measurement/Acquisition

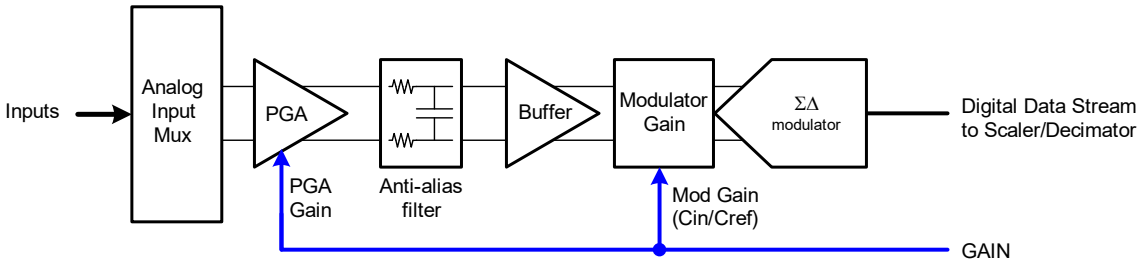


An analog multiplexer connects input signals to the two physical analog DSM channels. Several input sources are available including signals from I/O input. The analog channels have choppers, gain, filters, and DSM modulators. Several integrated multiplexers facilitate diagnostics and channel switching without disturbing filters. The digital section has three channels with one dedicated channel for each analog channel and a third channel, which can use either analog channel. The following sections provide more details about these blocks.

2.8.1 Analog DSM Channel

A simplified diagram of an analog delta-sigma modulator (DSM) channel and part of the digital channel is shown below. For better clarity, the diagram omits analog multiplexers to bypass and swap blocks for diagnostics.

Figure 2-8. Analog DSM Channel

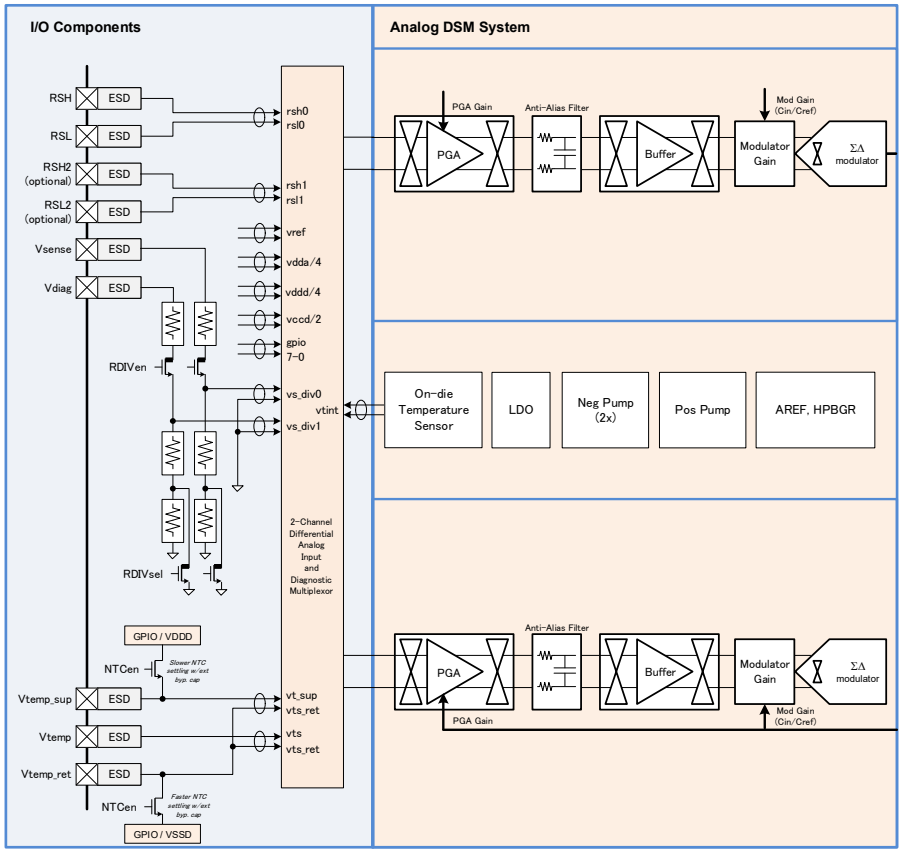


The analog DSM channel receives a differential signal selected by an analog multiplexer. This differential signal is received by a programmable gain amplifier (PGA). The output of the PGA feeds a low-pass anti-alias filter (AAF) with a bandwidth of ~30 kHz. A buffer amplifier drives the DSM modulator - this amplifier has high bandwidth to settle the modulator capacitors to better than 16 bits each time they are settled. The modulator uses capacitor dividers to set gain - the modulator disturbs its input each time the input is sampled - the inputs need to settle before the next sample or errors result. The modulator is a third order with switched capacitor amplifier circuits. The modulator produces a multi-level digital bitstream sent to the digital channel.

2.8.2 Analog DSM System

The analog DSM system is shown in the following diagram.

Figure 2-9. Analog DSM System



The DSM sequencer previously described controls conversions. The sequencer selects the analog input signal by controlling the analog mux, connecting the input to an analog DSM channel. Signals from GPIOs, on-chip power supplies and grounds, the high-voltage input voltage divider, and on-chip sensors and references can be selected.

GPIOs not directly connected to the analog multiplexer can use an analog input bus called the analog multiplex bus (AMUXBUS). The AMUXBUS has two signals (AMUXBUSA and AMUXBUSB), which can connect GPIOs to ADC using software controlled analog switches inside each I/O.

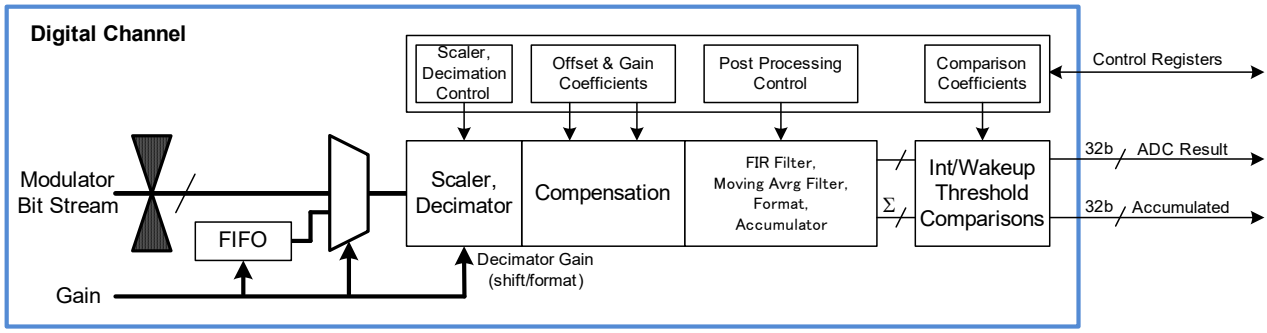
The analog DSM channel includes choppers and multiplexers in addition to the PGA, anti-alias filter, buffer amplifier, and DSM modulator. The choppers minimize offset error while the multiplexers assist input signal switching and diagnosis. To alternately measure two signals with one channel, the anti-alias filter can be bypassed since the AAF needs about 60 µs to settle to 16 bits before conversions can start - the measurement sample rate needs to slow to 4 ksps if the AAF is not bypassed. The other paths allow the input, PGA, and AAF signals to be swapped to the other channel for diagnostics.

This section also includes a precision reference system (voltage and current) and temperature sensor.

2.8.1 Digital Channel Data Path

The digital data channel converts the modulator bit-stream output to parallel data and includes scaling, filtering and compensation. It also compares ADC values with thresholds to generate interrupts when thresholds are exceeded. A block diagram of the digital channel path is shown below.

Figure 2-10. Digital Channel Data Path



The modulator bit stream first goes to a channel chopper, which can multiply the bit stream by +1 or –1 (corresponding with a chopper that swaps inputs in the analog signal path). The voltage channel uses programmable fixed gain while the current channel can use either fixed or automatic gain.

A scaler is used so that the LSB of the ADC can have the same weight regardless of gain. The LSB is established by the ADC resolution at maximum gain – for the current channel, the LSB is 0.715 mA with a gain of 512. The scaler multiplies the output of the modulator by 512/Gain to normalize results and maintain 0.715 mA for the LSB regardless of gain setting. To multiply by 2, the scaler shifts results up one bit. To cover a gain range of 1 to 512 means results can be shifted up to 9 bits.

The output of the decimator goes to a compensation block, which multiplies results for gain adjustment and adds constants for offset correction. A 16-stage finite impulse filter (FIR) with programmable coefficients follows the compensation block. Results are then normalized to remove unused bits and averaging, accumulation, and threshold detection can be performed. Threshold comparison uses a window comparator, which can be programmed for high and low thresholds which trigger interrupts.

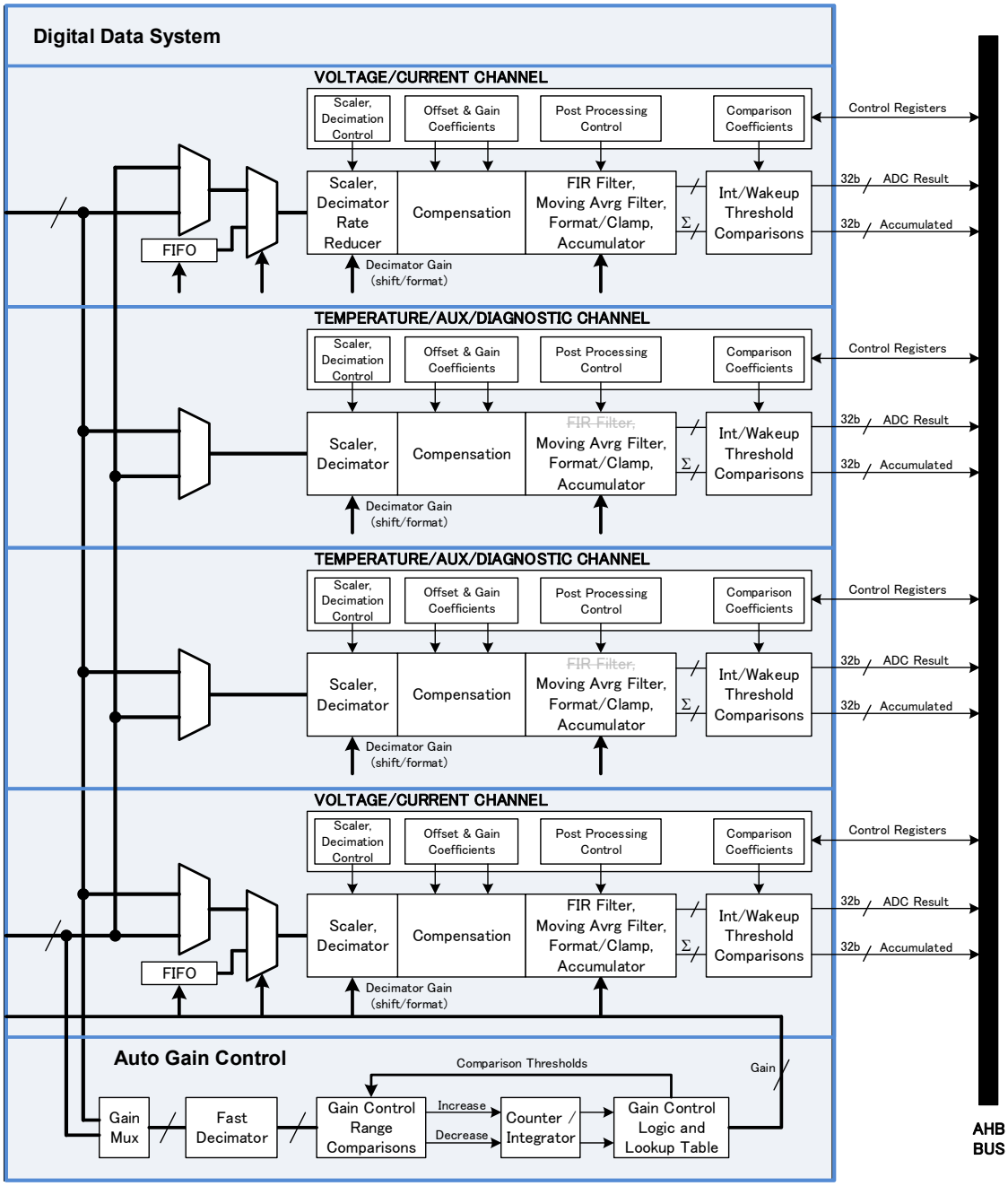
Channel control registers are programmed by the CPU using the AHB bus. Results can be transferred by DMA or CPU. A trigger can initiate a DMA transfer and an interrupt can notify the availability of the CPU data. These operations can be performed in parallel. The CPU can also poll for end-of-conversion to determine if data is available.

2.8.2 Digital Data System

The following diagram shows the complete digital data system. There are four data channels, of which two are dedicated channels associated with their respective analog channels while the third and fourth can receive data from either analog channel. This allows the analog channel to feed alternate analog measurements from two different signal sources to the two data channels with appropriate configuration for those measurements. It also facilitates diagnosis by allowing either analog channel to be used to measure the same signals.

Parameters for the alternate digital channel, especially compensation values, must be programmed to appropriate values corresponding to the analog channel being measured. The AGC function is described in the next section.

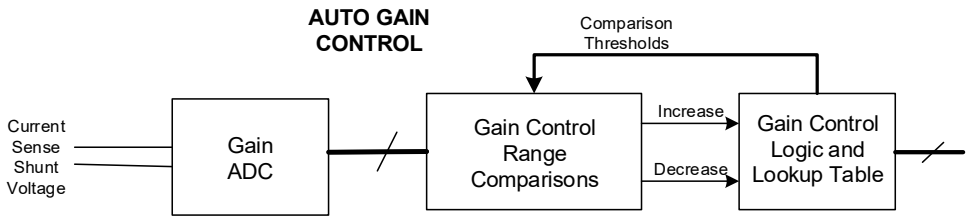
Figure 2-11. Digital Channel Data System



2.8.3 Current Channel Automatic Gain Control

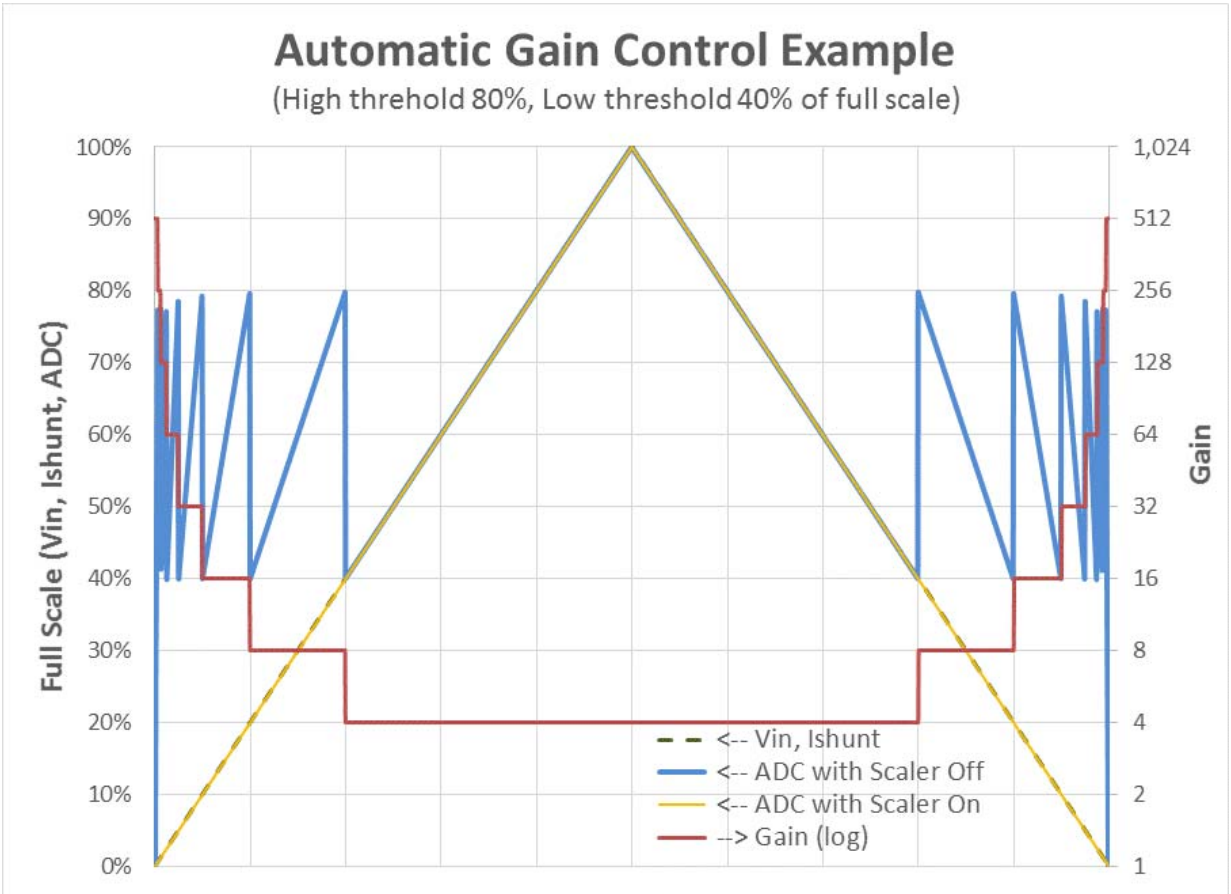
The current channel includes an automatic gain control (AGC) mechanism shown in the block diagram below. This functions by measuring the analog channel input voltage with an ADC and increasing or decreasing gain when programmable thresholds are reached. The output of the gain control comparators is used by a look-up table to set scaler, PGA, and modulator gain settings. To minimize input referred noise, it is advisable to configure the gain table to increase PGA gain before increasing modulator gain.

Figure 2-12. AUTO GAIN CONTROL



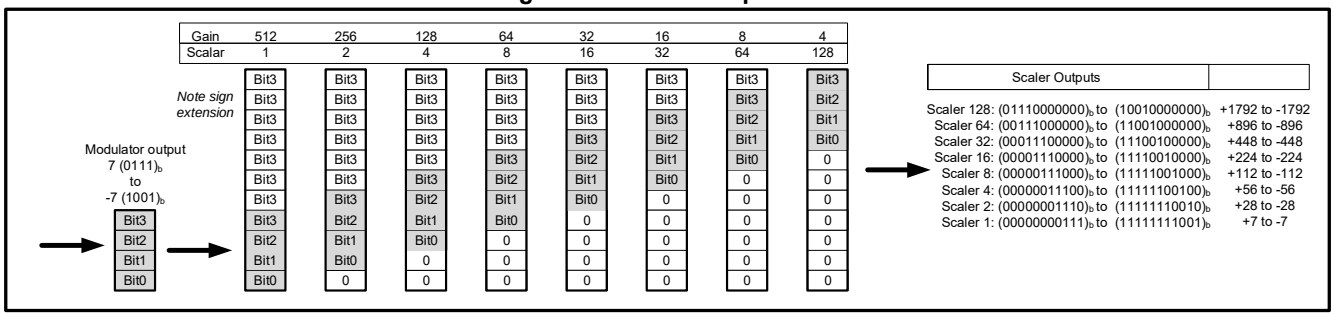
Following is an example of the AGC with current going from 0% to 100% of full scale (3000A). The table shows full-scale amperes, resolution, and scaler values for gains from 4-512. As described in the previous sections, the scaler is used to normalize results so the LSB always has the same weight (0.715 mA) which is accomplished by multiplying the modulator by the scaler value; the scaler value is the same as 512/Gain.

Figure 2-13. AUTOMATIC GAIN CONTROL Example



The following diagram illustrates scaler operation. In this example, a 4-bit modulator input from ±7 is scaled by 1 to 128. For example, when scaled by 128, ±7 becomes ±7*128 (= ±1792).

Figure 2-14. Scaler Operation



The AGC can be configured to increase or decrease gain by factors of 2 or more. Large steps can track large current changes faster by reducing the number of gain changes needed for tracking.

2.8.4 Temperature Sensor

Temperature measurements are performed by measuring the difference in base-emitter voltage (VBE) of PNP bipolar transistors at two different current densities - temperature is directly proportional to the voltage difference. The principle of operation is:

$VBE = nkT/q*\ln(I/I_S)$;	(1) VBE voltage at a given current and temperature
$dVBE = nkT/q*\ln(M*I/I_S) - nkT/q*\ln(I/I_S) = nkT*\ln(M)$;	(2) Difference in VBE at two different current densities (current ratio "M")
$T(°K) = dVBE*q/(nk*\ln(M))$	(3) Temperature as a function of dVBE

Where VBE is the base-emitter diode voltage, dVBE is the difference in diode voltage at two different current densities (the ratio of current density is M), n is the base-emitter diode ideality factor, k is Boltzman's constant, q is the charge of an electron, I is the diode current, and I_S is the diode saturation current.

Note that I_S cancels as does the magnitude of I; n, k, and ln(M) are constants, which produce a nominal voltage of 179 µV/°K with M=8.

Temperature is calculated from dVBE using a polynomial with factory-supplied calibration coefficients to compensate for errors and drift in n and M, which can vary slightly with temperature and temperature-related package stress. Boltzman constant k and electron charge q are physical constants which do not drift.

Two independent current reference sources are available to diagnose current reference malfunctions by comparing results using the two independent references. Similar redundancy is provided by changing transistor current density either by changing the magnitude of the current source or the size of the transistor.

Temperature measurement is usually performed with an interrupt routine, which can either be software or timer triggered.

2.9 High-Voltage Subsystem

The PSoC 4 HV PA high-voltage subsystem includes the following functions:

- An AHB bus interface and control/status registers.
- The V_{BAT} to V_{DDD}/V_{DDA} HV regulator (3.6 to 28-V input, 3.3-V nominal outputs)
- An input attenuator/voltage divider for V_{SENSE} and V_{DIAG} ADC inputs
- A LIN transceiver (physical interface or PHY)

2.9.1 AHB Interface

The AHB includes the control and status registers needed for the HV subsystem.

2.9.1.15 HV Regulator

The high-voltage regulator is always on, supplied by VBAT, and provides V_{DDD} and V_{DDA}. It supplies a nominal output voltage of 3.3 V but may drop as low as 2.7 V when V_{BAT} drops below 4 V.

2.9.1.16 HV Input Attenuator

The HV input attenuator is a voltage divider used on the VSENSE and VDIAG to scale battery voltage to levels compatible with the ADCs, so battery voltages can be measured.

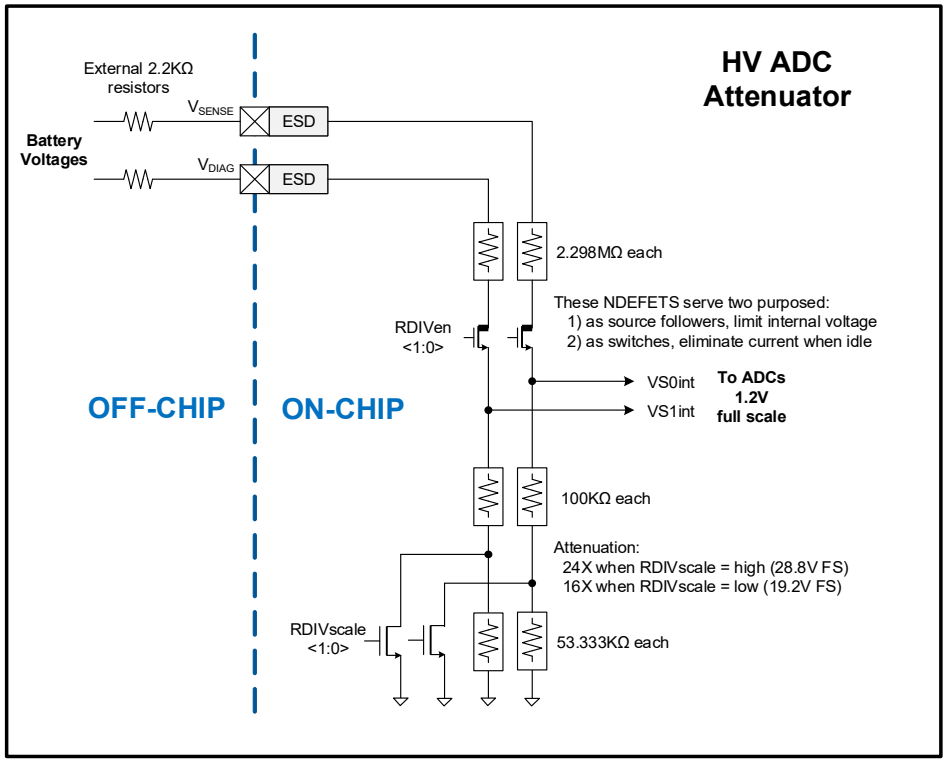
In typical lead-acid battery sensing applications, the V_{SENSE} input is normally connected directly to the battery with a series 2.2-kΩ resistors to measure battery voltage. V_{DIAG} can be used to measure voltage at other locations such as the ECU or other loads where monitoring is desired. It is sometimes used to measure ignition switch voltages such as the run bus (KL15), the start bus (KL50), or the always-on battery bus (KL-30).

The external 2.2-kΩ resistors in series with voltage sources limit current during ESD and transient voltage events. Since the nominal resistance of the on-chip voltage divider is about 2.4 MΩ, the accuracy of the external resistors is not critical since their contribution is only 0.1% of the total divider.

The voltage divider slightly loads the source being measured with the 2.4-MΩ resistor. A small current from source to ground flows through the divider (for example, 6 µA when measuring a 12-V source). The voltage divider can be switched off using the RDIVen control bits.

The RDIVscale control bits select whether the voltage divider input-to-output ratio is 24 or 16. Since the ADC full scale input voltage is 1.2 V, the 24X ratio corresponds to 28.8-V full scale and 16X ratio corresponds to 19.2-V full scale. Voltage divider matching error results in a gain error, which can be corrected with gain correction in the ADC.

Figure 2-17. HV DC Attenuator



2.9.1.17 LIN Transceiver

The LIN transceiver meets the requirements of LIN standard 2.2A and is downward compatible with the LIN 2.0. Data rates of 10 kBps and 20 kBps are supported. A non-LIN fast slew rates mode is available providing 100 kBps data rates for fast downloads for factory and field flash program updates using the LIN pin.

The LIN transceiver is guaranteed not to block the LIN bus with a dominant bit when the VBAT voltage is below the minimum LIN supply voltage (7V, VBAT_LIN, LIN 2.2A Parameter 10) and may continue to operate below that voltage but communication is not guaranteed. The LIN transceiver is inhibited if VCCD is not valid to prevent erroneous control signals from interference with the LIN bus A timer is also present clocked by the low-speed clock system which disables the LIN if the bus is dominant for too long. The timer can generate an interrupt if the LIN bus wakeup signal (LIN bus in dominant state for 250 µs to 5 ms) is detected. LIN compliance testing is facilitated by making the transceiver data signals available on GPIO pins (LIN_RX, LIN_TX) as are the serial control block UART signals are also available (UART_RX, UART_TX).

The LIN transceiver has an open drain output and digital receiver connected to the LIN pin which connects to the LIN bus. The bus has pullups to VBAT with total pullup resistance between 500 Ω and 1 kΩ. A series diode between VBAT and the pull-ups prevents the bus from powering VBAT. The diode and pull-up resistor are usually located at or near the LIN master. The transceiver has a weak slave resistor (nominally 30 kΩ) on-chip and the driver can be configured to provide a weak, normal, or fast pull-down. Both the pull-up and weak pull-down can be used for diagnostics without disturbing LIN bus communications.

The pull-up resistor and ESD networks prevent parasitic current paths if VBAT or ground become disconnected. The LIN driver will withstand differences of ±1 V if shorted to another ground and if continuously shorted to another ground or VBAT will not be permanently damaged. The LIN transceiver complies with Q100-2/IEC6100-4-2 ESD and ISO 7637 capacitively coupled transient pulses. Heating of LIN driver in normal operation does not affect measurement accuracy.

Figure 2-18. LIN Transceiver

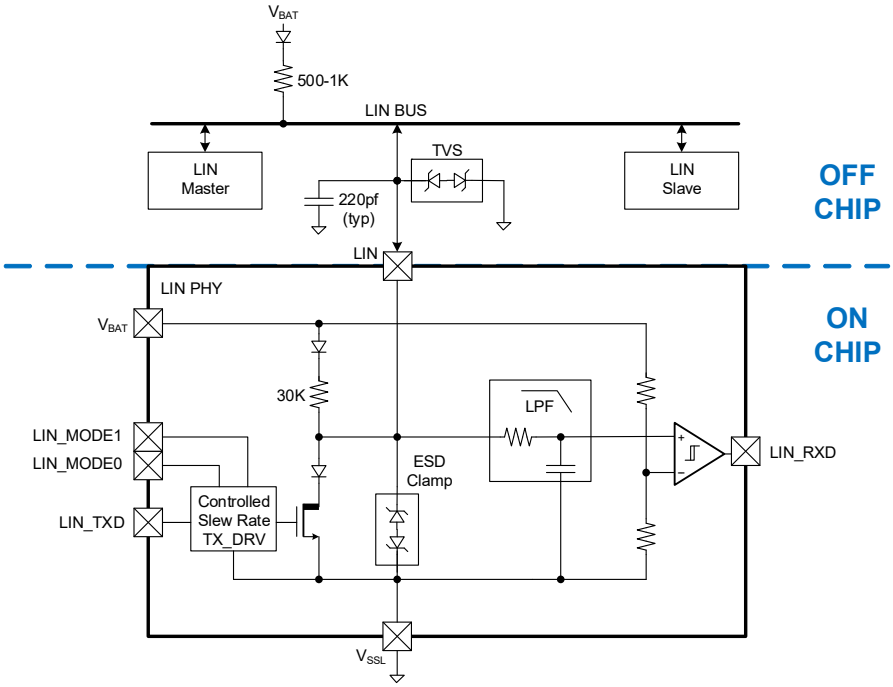


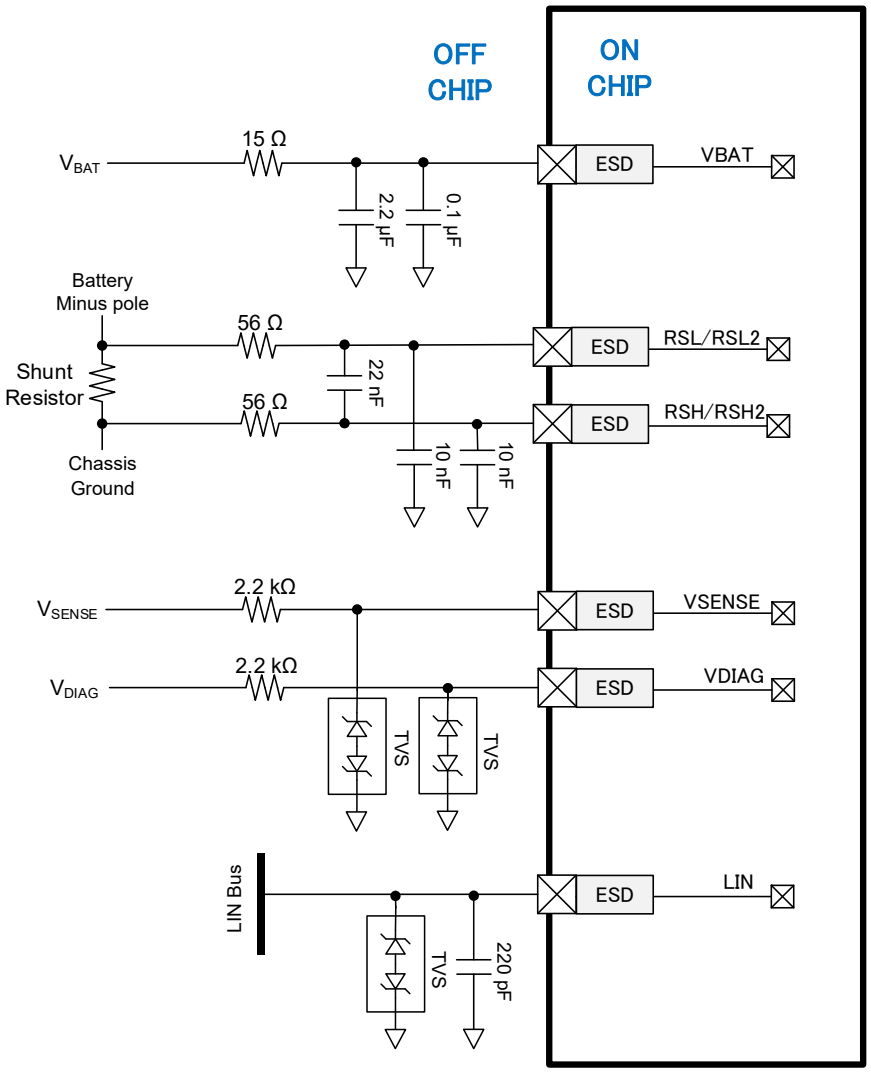
Table 2-1. LIN Transceiver Truth Table

LIN Transceiver Function	LIN_MODE1	LIN_MODE0	DRIVER			Slave Pull-up
			Slew Control	LIN_TXD=1	LIN_TXD=0	
Fast Mode (non-LIN)	1	1	No	Z (rec)	Low (dom)	On
Normal/Enabled	1	0	Yes	Z (rec)	Low (dom)	On
Weak (diagnosis)	0	1	No	Z (rec)	Low (weak)	On*
Disabled	0	0	No	Z (rec)	Z	Off
rec - recessive; dom - dominant; Z - driver off; For LIN_TXD and LIN_RXD recessive=1, dominant=0						
* In weak (diagnosis) mode, slave pull-up is on when LIN_TXD=1, Off when LIN_TXD=0						

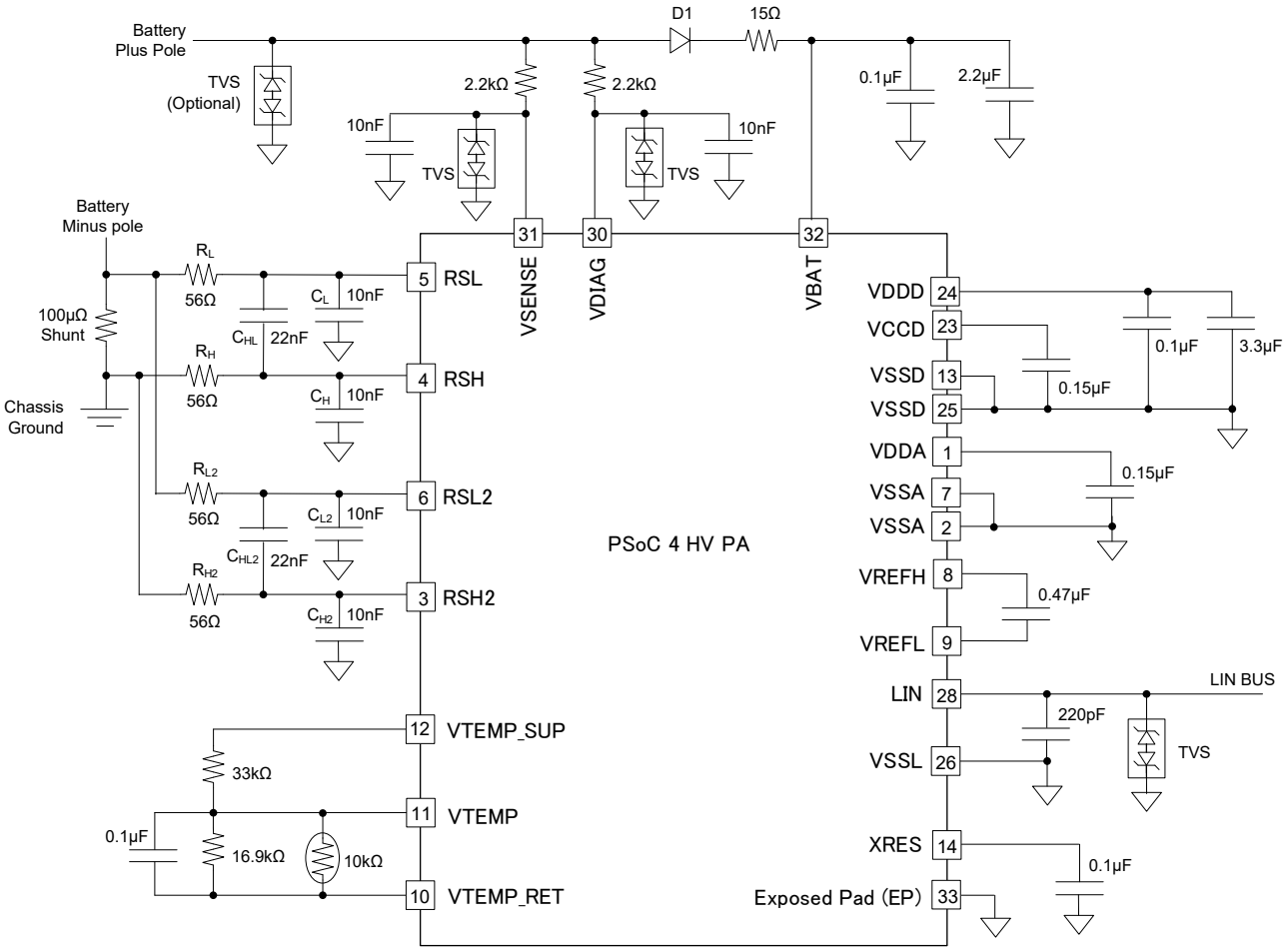
2.10 ESD Protection

PSoC 4 HV PA requires sufficient protection to withstand the high voltage ESD on specific pins. The ESD on LIN, VBAT, VSENSE , VDIAG, RSH, RSL, RSH2, and RSL2 is rated at ±8 kV (SIDA2), and is required to protected as shown in Figure 2-19.

Figure 2-19. ESD Protection



3. Sample Application Schematic



* R_L, R_H, C_{HL}, C_H, C_L, and R_{L2}, R_{H2}, C_{HL2}, C_{H2}, C_{L2} selection for best EMC performance.
* RSH2, RSL2 and VDIAG pins are for redundant measurements – based on configuration.
* Module GND connected to Battery Minus or Chassis Ground – based on configuration.

4. Pinouts

The following table provides the pin list for PSoC HV PA for the 32-pin QFN package.

Table 4-1. 32-QFN Pin Description

32-QFN		32-QFN	
Pin	**Name**	**Pin**	**Name**
1	VDDA	17	P0.5
2	VSSA	18	P0.4
3	RSH2	19	P0.3
4	RSH	20	P0.2
5	RSL	21	P0.1
6	RSL2	22	P0.0
7	VSSA	23	VCCD
8	VREFH	24	VDDD
9	VREFL	25	VSSD
10	VTEMP_RET (P1.2)	26	VSSL
11	VTEMP (P1.1)	27	NC
12	VTEMP_SUP (P1.0)	28	LIN
13	VSSD	29	NC
14	XRES	30	VDIAG
15	P0.7	31	VSENSE
16	P0.6	32	VBAT

Descriptions of the Power pins are as follows:

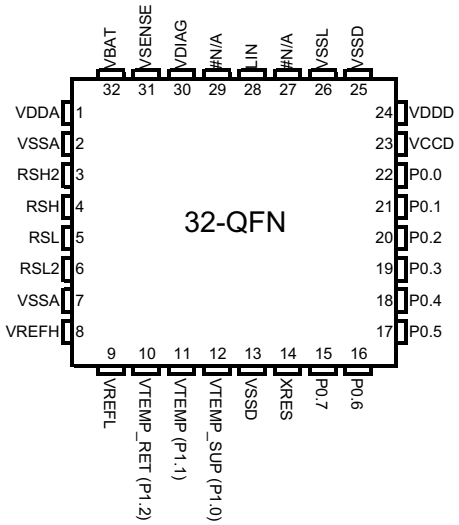
VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Power supply for the core (LV Logic) (1.8 V ±5%)

Figure 4-1. Pin Assignment



4.1 Alternate Pin Functions

Each port pin can be assigned to one of multiple functions; it can, for example, be an analog I/O or a digital peripheral function. The pin assignments are shown in the following table.

Table 4-2. Alternate Pin Functions

Name	Analog	ACTIVE				DEEP SLEEP		
		ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2
P0.0	amuxbus_a/amuxbus_b	tcpwm.tr_in[0]	lin.lin_rx[0]	scb.uart_rx:1	tcpwm.line[0]	scb.spi_clk		scb.i2c_scl
P0.1	amuxbus_a/amuxbus_b	tcpwm.tr_in[1]	lin.lin_tx[0]	scb.uart_tx:1	tcpwm.line_compl[0]	scb.spi_mosi		scb.i2c_sda
P0.2	amuxbus_a/amuxbus_b	tcpwm.tr_in[2]	lin.lin_en[0]		tcpwm.line[1]	scb.spi_miso		
P0.3	amuxbus_a/amuxbus_b	tcpwm.tr_in[3]			tcpwm.line_compl[1]	scb.spi_select0		
P0.4	amuxbus_a/amuxbus_b	peri.virt_in_0			tcpwm.line[2]	scb.spi_select1		cpuss.fault_out[1]
P0.5	amuxbus_a/amuxbus_b	srss.ext_clk			tcpwm.line_compl[2]	scb.spi_select2		cpuss.fault_out[0]
P0.6	amuxbus_a/amuxbus_b	peri.virt_in_1				scb.spi_select3		cpuss.swd_data
P0.7	amuxbus_a/amuxbus_b	peri.virt_in_2						cpuss.swd_clk
VTEMP_RET (P1.2)	pacss.vtemp_ret	peri.virt_in_3	hvss.lin_alt_en		tcpwm.line_compl[3]			
VTEMP (P1.1)	pacss.vtemp		hvss.lin_alt_txd					
VTEMP_SUP (P1.0)	pacss.vtemp_sup		hvss.lin_alt_rxd		tcpwm.line[3]			
VirtLinEn[1]			lin.lin_en[1]					
VirtLinTxd[1]			lin.lin_tx[1]	scb.uart_tx				
VirtLinRxd[1]			lin.lin_rx[1]	scb.uart_rx				

Note
1. Internal connections to the integrated LIN PHY.

5. Electrical Specifications

5.1 Absolute Maximum Ratings

Within the maximum ratings, no damage shall occur. Parametric and functionality may deviate from specifications. All analog voltages are relative to V_{SSA} and all digital voltages are relative to V_{SSD}. A negative current if flowing out of a pin, and positive current into a pin.

Table 5-1. Absolute Maximum Ratings

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDA1	V_{ESDHBM}	V_{HBM} ESD on all pins	±2000	–	–	V	
SIDA2	V_{ESDHV}	ESD on LIN, V_{BAT}, V_{SENSE}, V_{DIAG}, RSH, RSL, RSH2, RSL2	±8000	–	–	V	As per ISO10605 With required external protection as per the guidelines in the ESD Protection section
SIDA3	$V_{ESDCDMCOR}$	CDM ESD on Corner Pins	±750	–	–	V	
SIDA4	V_{ESDCDM}	CDM ESD on non-corner pins	±500	–	–	V	
SIDA5	V_{BAT}	Supply voltage V_{BAT}[2]	–0.3	–	42	V	
SIDA6	V_{SHV}	V_{SENSE}/V_{DIAG} ADC sense voltage[2]	–0.3	–	42	V	
SIDA7	V_{SHV}	V_{SENSE}/V_{DIAG} ADC sense voltage[2]	–40	–	42	V	With external 2.2-kΩ resistor
SIDA8	I_{SH}	V_{SENSE}/V_{DIAG} current[2]	–20	–	1	mA	Forced externally
SIDA9	I_{CS}	R_{SH}/R_{SL}/R_{SH2}/R_{SL2} current[2]	–1	–	1	mA	Forced externally
SIDA10	V_{LIN}	LIN pin voltage[2]	–27	–	42	V	
SIDA11	I_{LIN}	LIN pin current[2]	–	–	200	mA	
SIDA12	V_{GPIO}	GPIO pin input voltage	–0.5	–	V_{DDD} +0.5	V	
SIDA13	V_{DDA}, V_{DDD}	V_{DDA}, V_{DDD} supply voltage	–0.3	–	4.7	V	
SIDA13A	I_{BAT}	V_{BAT} supply current[3]	–	–	160	mA	
SIDA13B	$I_{BATABSDC}$	V_{BAT} supply current, long-term average	–	–	40	mA	
SIDA14	V_{CCD}	VCC core supply voltage	–0.3	–	1.95	V	
SIDA16	I_{GPIO}	Current per GPIO pin	–20	–	20	mA	
SIDA17	V_{SLV}	RSHx, RSLx, VTEMP	–0.3	–	VDDA +0.3		
SIDA18	T_A	Ambient temperature	–40	–	125	°C	
SIDA19	T_S	Storage temperature	–55	–	125	°C	
SIDA20	T_J	Junction temperature	–40	–	150	°C	
SIDA21		Life time	15	–	–	Years	
SIDA22		Storage time	5	–	–	Years	T_A = 55 °C, 85% r.H.
SIDA23		Storage time	15	–	–	Years	T_A = 40 °C, 80% r.H.
SIDA24	$t_{SCVHVREG}$	Short circuit tolerance time: HVREG	–	–	60	min	V_{BAT}: 3.6 V to 28 V
			–	–	500	ms	V_{BAT}: 28 V to 42 V
SIDA24A	t_{SCLIN}	Short circuit tolerance: LIN	–	–	60	min	V_{BAT}= LIN: 3.6 V to 28 V
			–	–	500	ms	V_{BAT} = LIN: 28 V to 42 V

Notes
2. To prevent damage caused by high-voltage pulses, external protection (that is, series resistor, diode, TVS) may be required. To allow a minimum system level supply voltage of 4.5 V, external protection circuits including reverse protection diodes are designed in a way that guarantees the device minimum functional voltage V_{BAT} of at least 3.6 V.
3. Absolute max current includes inrush / transient current during power-up.

Unless otherwise noted, functionality and parameters are valid over operating voltage and temperature range. All analog voltages are relative to V_{SSA}, all digital voltages are relative to V_{SSD}. A negative current if flowing out of a pin, and positive current into a pin.

Table 5-2. Operating Conditions

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID1	V_{BAT}	Supply voltage VBAT	3.6	–	28	V	
SID2	V_{BAT_LIN}	VBAT range for LIN communications[4]	7	–	28	V	LIN2.2A Parameter 10
SID3	V_{SENSE}	VBAT sense voltage	3.6	–	28	V	
SID4	V_{DIAG}	VDIAG sense voltage	3.6	–	28	V	
SID4A	I_{SENSE}	V_{SENSE}/V_{DIAG} current	–	5	20	µA	
SID5	V_{LIN}	LIN output voltage	6	–	28	V	
SID6	R_{LIN},PU	LIN pull-up resistor	20	30	47	kΩ	
SID7	V_{RSx}	Input range (R_{SH}, R_{SL})	–0.3	–	0.3	V	
SID7A	ICS	RSH/RSL/RSH2/RSL2 Current	–2000	–	20	nA	V_{INADC}: -0.3 to 0.3 V | –40 to +125 °C
SID7B			–200	–	20	nA	V_{INADC}: –0.15 to +0.15 V | –40 to +125 °C
SID7C			–20	–	20	nA	V_{INADC}: –0.075 to +0.075 V | –40 to +125 °C
SID7D			–12	–	12	nA	V_{INADC}: –0.003 to +0.003 V | –40 to +125 °C
SID7E			–2	–	2	nA	V_{INADC}: –0.003 to +0.003 V | –40 to +85 °C
SID8	R_{SENSE}	Shunt current sense resistor	25	100	200	µΩ	
SID9	V_{INADC}	ADC input voltage range	–0.3	–	1.2	V	
SID9A	V_{INGPIO}	GPIO input voltage range (digital)	–0.3	–	V_{DDD}+0.3	V	
SID10	T_A	Ambient temperature range	–40	–	125	°C	
SID11	fCLK	CPU operating frequency	–	–	49.152	MHz	

Note
4. The LIN interface should only be active when the supply voltage is within VBAT_LIN. Outside VBAT_LIN, the LIN module will not interfere with bus communications (will not block the bus with a dominant bit). LIN V2.2A specifications are based on VBAT = 18 V; the AC/DC behavior can change for 18 V < VBAT < 28 V.

5.2 Device-Level Specifications

Unless otherwise noted, functionality and parameters are valid over operating conditions and lifetime (range of functionality). All analog voltages are relative to V_{SSA}, digital voltages are relative to V_{SSD}. A negative current is flowing out of a pin, positive current into a pin.

5.2.1 *Operating Current and Wakeup Times*

Table 5-3. Operating Current and Wakeup Times

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID12	$I_{BAT\_NORM\_24}$	Average supply current in active mode	–	5	10	mA	IMO = 49.152 MHz, HFCLK = IMO/2, CPU Core only
SID12A			–	TBD	TBD	mA	Clocks: IMO = 49.152 MHz HFCLK = IMO/2 SYSCLK = HFCLK PUMP Clock = Disabled TCPWM: 1 counter enabled LIN: 10 kHz, 25% active dominant, 25% active recessive, 50% standby PACSS: Both channels enabled and continuously converting Power settings: Buffer = 78%, PGA = 58%, Modulator = 88%, Sample rate = 8 ksps, FIR enabled, 15 taps MOD_FCHOP = /32 Internal Pump clock sourced from HFCLK CPU: void main() { int i = 1; while(1) { i = i + 1; i = i + 2; i = i + 3; i = i + 4; i = i + 5; }} Designed to provide constant activity + code flash access, not absolute worst case CPU current Prefetch enabled, flash wait states = 1 for 24.576 MHz[5]
SID13	$I_{BAT\_NORM\_48}$	Average supply current in active mode	–	TBD	TBD	mA	IMO = 49.152 MHz, HFCLK = IMO, CPU Core only
SID13A			–	TBD	TBD	mA	Clocks: IMO = 49.152 MHz HFCLK = IMO SYSCLK = HFCLK PUMP Clock = Disabled TCPWM: 1 counter enabled LIN: 10 kHz, 25% active dominant, 25% active recessive, 50% standby PACSS: Both channels enabled and continuously converting Power settings: Buffer = 78%, PGA = 58%, Modulator = 88%, Sample rate = 8 ksps, FIR enabled, 15 taps MOD_FCHOP = /32 Internal Pump clock sourced from HFCLK CPU: void main() { int i = 1; while(1) { i = i + 1; i = i + 2; i = i + 3; i = i + 4; i = i + 5; }} Designed to provide constant activity + code flash access, not absolute worst case CPU current Prefetch enabled, flash wait states = 3 for 49.152 MHz[5]

Note
5. Refer to the TRM for the details on the ACHAN power chopping configuration and pump clock configuration details.

Table 5-3. Operating Current and Wakeup Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID14	I_{BAT_NOCPU}	Average current with CPU in Sleep mode[6]	–	2	–	mA	Peripherals active
SID15[7]	I_{BAT_STOP}	Average supply current in Deep Sleep mode with once-per-second wakeup[8]	–	50	100	µA	Max value @T_A = 25 ºC
SID16[7]	I_{BAT_STOP}	Average supply current in Deep Sleep mode with once-per-second wakeup[8]	–	55	200	µA	At @T_A = 65 ºC
SID17[7]	I_{BAT_SLEEP}	Average current in Deep Sleep mode without periodic wakeup and no periodic calibration[9]	–	20	50	µA	Max value @T_A = 25 ºC
SID18[7]	I_{BAT_SLEEP}	Average current in Deep Sleep mode without periodic wakeup and no periodic calibration[9]	–	25	150	µA	At @T_A = 65 ºC
SID19	I_{BAT_XRES}	Current with XRES low	–	TBD	–	µA	XRES input low
SID20	$t_{STARTUP}$	Start time from reset release	–	–	8	ms	XRES or POR release Includes the ROM boot time and the SWD listen window.
SID21	t_{SLEEP}	Wakeup from Sleep power mode	–	–	6	clocks cycles	
SID22	$t_{DEEPSLEEP}$	Wakeup from Deep Sleep power mode	–	–	35	µs	

5.2.2 Voltage Regulators

Table 5-4. Voltage Regulators

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID23	V_{DDA}	Analog regulator voltage	3	3.3	3.6	V	
SID24	I_{DDA}	Analog regulator current	–	N/A	–		Not to be used off-chip
SID25	V_{DDD}	Digital regulator voltage, V_{BAT} > 4 V	3	3.3	3.6	V	
SID26	V_{DDD}	Digital regulator voltage, 4 V≥ VBAT ≥3.6 V	2.7	–	3.6	V	
SID27	I_{DD}	Digital regulator current	–	–	30	mA	Core, GPIO, & Ext. loads
SID27A	I_{DDGPIO}	Digital regulator current (GPIOs)	–	–	10	mA	For GPIO & Ext. loads
SID28	V_{CCD}	Core regulator voltage	1.75	1.8	1.95	V	
SID29	I_{CC}	Core regulator current	–	N/A	–		Not to be used off-chip

Notes
6. PSoC 4 power mode = sleep, µC powered down, all other high- and low-speed clocks and peripherals active, DMA active, RAM retained.
7. HV Dividers are off.
8. PSoC 4 power mode = deepsleep: µC powered down, high-speed clocks and peripherals off, low-power oscillator and timer active, all RAM and registers except internal µC registers retained. LIN and watchdog timers active. Includes once-per-second wakeup for measurements periodic measurements.
9. Same IBAT_STOP (PSoC 4 Power mode = deepsleep) without cyclic wakeup (no periodic calibration or measurements).

5.2.3 GPIO

Table 5-5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID30	V_{IH}	Input voltage high threshold	0.7*V_{DDD}	–	–	V	CMOS Input
SID31	V_{IL}	Input voltage low threshold	–	–	0.3*V_{DDD}	V	CMOS Input
SID32	V_{IH}	LVTTL input, $V_{DDD} \geq 2.7$ V	2	–	–	V	
SID33	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8	V	
SID34	V_{OH}	Output voltage high level	V_{DDD}-0.45	–	–	V	I_{OH} = –4 mA | $V_{DDD} \geq 3$ V I_{OH} = –1 mA | 2.7 V ≤ V_{DDD} < 3 V
SID35	V_{OL}	Output voltage low level	–	–	0.45	V	I_{OL} = 10 mA | $V_{DDD} \geq$ 2.7 V = 3 mA at 3-V V_{DDD}
SID36	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID37	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID38	I_{IL}	Input leakage current (absolute value)	–	2	–	nA	25 °C, V_{DDD} = 3.0 V
SID38A	I_{IL}	Input leakage current (absolute value)	–	–	1	µA	T_J = 150 °C, V_{DDD} = 3.0 V
SID40	C_{IN}	Input capacitance	–	–	7	pF	
SID41	V_{HYSTTL}	Input hysteresis LVTTL V_{DDD} > 2.7 V	25	40	–	mV	
SID42	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05*V_{DDD}	–	–	V	
SID43	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	100 µA is an absolute value; V_{DDD} + 0.5 = source current, V_{SS} - 0.5 = sink current
SID44	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	10	mA	Sum of GPIO Source or Sink current.

Table 5-6. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID45	t_{RISEF}	Rise time in Fast Strong Mode	1.5	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID46	t_{FALLF}	Fall time in Fast Strong Mode	1.5	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID47	t_{RISES}	Rise time in Slow Strong Mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID48	t_{FALLS}	Fall time in Slow Strong Mode	10	–	60	ns	3.3-V V_{DDD}, Cload = 25 pF
SID49	$f_{GPIOUTF}$	GPIO fOUT; 3.3 V ≤ V_{DDD} ≤ 3.6 V. Fast Strong mode.	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID50	$f_{GPIOUTS}$	GPIO fOUT; 3.3 V ≤ V_{DDD} ≤ 3.6 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID51	f_{GPIOIN}	GPIO input operating frequency;2.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	48	MHz	90/10% V_{IO}

5.2.4 XRES

Table 5-7. XRES DC Specifications[10]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDX1	V_{IH}	Input voltage high threshold	0.7*V_{DDD}	–	–	V	CMOS Input
SIDX2	V_{IL}	Input voltage low threshold	–	–	0.3*V_{DDD}	V	CMOS Input
SIDX3	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	
SIDX4	C_{IN}	Input capacitance	–	–	7	pF	
SIDX5	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by design
SIDX6	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	100 µA is an absolute value; V_{DDD} + 0.5 = source current, V_{SS} - 0.5 = sink current

Table 5-8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDX7	$t_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	
SIDX8	$t_{RESETWAKE}$	Wake-up time from Reset release[10]	–	–	8	ms	

Note
10. Includes the ROM boot time and the SWD listen window.

5.2.5 Clocks

Table 5-9. Internal Oscillators and Clocks

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	f_{IMO}	IMO clock frequency[11]	–	24	49.152	MHz	
SID54	f_{IMO_ACCY1}	IMO frequency variation (not locked to HPOSC)	–2.0	–	2.0	%	
SID55	f_{CPU_ACCY2}	IMO frequency variation (locked to HPOSC)	–1.0	–	1.0	%	
SID56	f_{HPOSC}	Precision 2-MHz reference oscillator	–	2.0	–	MHz	
SID57	f_{HPOSC_ACCY}	Precision 2-MHz reference oscillator	–1.0	–	1.0	%	
SID58	f_{LSO}	Low speed oscillator (PILO)[12]		32	–	kHz	
SID59	f_{LSO_ACCY1}	Accuracy (no periodic calibration)	–5.0	–	5.0	%	
SID60	f_{LSO_ACCY2}	Accuracy (with periodic calibration)[13]	–1.0	–	1.0	%	

Notes
11. F_{IMO} is factory trimmed and is user adjustable between 24 MHz (CY8C412x) and 48 MHz (CY8C414x) in 4-MHz steps. The 48-MHz setting can be boosted to 49.152 MHz using "Special" calibration data stored in SFLASH.
12. The PILO runs in all power modes and is used for low power interval timers and counters.
13. Periodic calibration - locked to HPOSC at least once per second during stop mode. Power required for periodic calibration is included in average stop mode supply current (IBAT_STOP, 100 µA max).

5.3 Analog

5.3.1 LIN Transceiver

Table 5-10. LIN Transceiver Specifications[14]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDL63	I_{BUS_LIM}	LIN output current	40	–	200	mA	Param 12
SIDL64	$I_{BUS\_PAS\_dom}$	Receiver dominant state input leakage (Driver off; V_{BUS}=0 V, V_{BAT}=12 V)	–1	–	1	mA	Param 13
SIDL66	$I_{BUS\_PAS\_rec}$	Receiver recessive state input leakage (Driver off; 7 V<V_{BUS}<18 V, 7 V<V_{BAT}<18 V)	–	–	20	µA	Param 14
SIDL68	$I_{BUS\_NO\_GND}$	Loss of local ground (V_{SS}=V_{BAT} <18 V, 7 V<V_{BUS}<VBAT<18 V)	–1	–	1	mA	Param 15
SIDL70	$I_{BUS\_NO\_BAT}$	Loss of battery power (V_{BAT} disconnected, 7 V<V_{BUS}<18 V)	–	–	100	µA	Param 16
SIDL72	V_{BUSdom}	Receiver dominant state	–	–	0.4	V_{BAT}	Param 17
SIDL73	V_{BUSrec}	Receiver recessive state	0.6	–	–	V_{BAT}	Param 18
SIDL74	V_{BUScnt}	Receiver center voltage	0.475	0.5	0.525	V_{BAT}	Param 19
SIDL75	V_{BUShys}	Receiver hysteresis	–	–	0.175	V_{BAT}	Param 20
SIDL76	V_{OH}	Bus transmitter recessive output voltage	V_{BAT}-2	–	V_{BAT}	V	Not a LIN 2.2A specification
SIDL77	V_{OL}	Bus transmitter dominant output voltage (V_{BAT}= V_{BUS} =7 V)	–	–	1.2	V	RL = 500 Ω (I_{OL}<12 mA)
SIDL79	V_{OL}	Bus transmitter dominant output voltage (V_{BAT} = V_{BUS} =18 V)	–	–	2	V	RL = 500 Ω (IOL<32 mA)
SIDL81	$V_{SerDiode}$	Voltage drop at external series diodes	0.4	0.7	1	V	Param 21
SIDL82	$R_{LIN,PU}$	Internal slave pull-up resistor[15]	20	30	47	kΩ	Param 26 (R_{SLAVE})
SIDL83	$R_{LIN,PD}$	Internal pull-down resistor for diagnosis	20	30	47	kΩ	Not a LIN 2.2A specification
SIDL84	D1	Duty Cycle 1 (20 kBps)	0.396	–	–	–	Param 27 D1 = tBus_rec(min) / (2 x tBit) for baud rate = 20 kBps
SIDL85	D2	Duty Cycle 2 (20 kBps)	–	–	0.581	–	Param 28 D2 = tBus_rec(max) / (2 x tBit) for baud rate = 20 kBps
SIDL86	D3	Duty Cycle 3 (10 kBps)	0.417	–	–	–	Param 29 D3 = tBus_rec(min) / (2 x tBit) for baud rate = 10.4 kBps

Notes
14. LIN V2.2A specifications are based on V_{BAT} = 18 V, the AC/DC behavior can change for 18 V < V_{BAT} < 28 V.
15. LIN V2.2A specifies 20 kΩ ≤ RSLAVE ≤ 60 kΩ. Cypress is specifying a lower maximum R_{SLAVE} value of 47 kΩ.

Table 5-10. LIN Transceiver Specifications[14] *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDL87	D4	Duty Cycle 4 (10 kBps)	–	–	0.59	–	Param 30 D4 = tBus_rec(max) / (2 x tBit) for baud rate = 10.4 kBps
SIDL88	trx_pd	Propagation delay of receiver	–	–	6	µs	Param 31
SIDL89	trx_pd	Symmetry of receiver propagation delay	–2	–	2	µs	Param 32
SIDL90	tr	Rise Time	3.5	–	22.5	µs	1 nf/1 kΩ, 6.8 nf / 660 Ω, 10 nf / 500 Ω
SIDL91	tf	Fall Time	3.5	–	22.5	µs	1 nf/1 kΩ, 6.8 nf/ 660 Ω, 10 nf/500 Ω
SIDL92	d(tr-tf)	Difference between rise time to fall time	–4	–	4	µs	1 nf/1 kΩ, 6.8 nf/ 660 Ω, 10 nf/500 Ω
SIDL93	f_{LIN10K}	Baud rate for LIN 10 kbps mode	–	10	–	kbps	
SIDL94	f_{LIN20K}	Baud rate for LIN 20 kbps mode	–	20	–	kbps	
SIDL95	f_{PROG}	Baud rate for 100 kbps for fast program transfer mode[16]	–	100	–	kbps	LIN2.2A specifications are not applicable in this mode

Per LIN2.2A, comments reference appropriate LIN specification parameters. If no parameter is included in the comment, this parameter is not a requirement of the LIN2.2A specification.

5.3.2 Temperature Channel

Table 5-11. Temperature Channel Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Comment
SID96	T_{RMEAS}	Measurement range	–40	–	125	ºC	
SID97	T_{ACC}	Accuracy including lifetime and temperature drift	–2	–	2	ºC	Includes firmware filtering Alternating VBE measurements are required, refer to the technical reference manual for more details
SID98	T_{RES}	Resolution	–	–	0.1	ºC	
SID99	$f_{TUPDATE}$	Signal update rate output[17]	0.75	8	96	ksps	At decimator Max: only meant for diagnostic modes where multiple samples will be taken. Noise is higher
SID100	N_{ADC},TEMP	Resolution	16	–	–	bits	No missing codes
SID101	V_{TNOISE}	Output referred noise	–	–	0.1	ºC	Diagnostic channel interleaving with voltage channel every 100ms. With firmware filtering

Notes
16. Fast program transfer mode exceeds the 20kB/sec maximum LIN2.2A transfer rate and is not a LIN compliant operating mode. In this mode, LIN Bus specification parameters do not apply. This is mode can be used for factory and field software updates.
17. 8 ksps guaranteed when measuring two different sources with one channel with 16-bit resolution, 96 ksps when continuously measuring one source.
18. First valid decimator output using a 3.072-MHz ADC clock with OSR = 64 and decimator = Sinc3. Digital FIR filtering and averaging may add more delay.

Table 5-11. Temperature Channel Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Comment
SID102	$Latencyt_{MUX}$	Measurement valid delay	-	64.13	64.77	µs	ADC: 3*64 = 192 clock cycles to produce first valid data at sinc3 output. Doesn't include FIR and Rare Reducer (RR) delays T=1/3.07MHz (5 + Channel select delay + 192)*T = 64.13 µs -Typical IMO variation is ±1% when locked to HPOSC (5 + Channel select delay + 192)*T*(1+1%) = 64.77 µs > Max
SID103	V_{TRMEAS}	VTEMP measurement range	0	–	1.2	V	External thermistor ADC input Max = $V_{DDD/3}$
SID103A	ACC_VT	VTEMP accuracy including lifetime and temperature drift	–1	–	1	%	External thermistor ADC input

5.3.3 Diagnostic Channel

Table 5-12. Diagnostic Channel Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID302	NOISE_D	Input referred integrated noise	–	–	45	µVrms	DR = 64, DR2 = 1
SID303	VOFF_D	Input referred offset error	–16	0	16	µV	V_{BAT} < 18 V and T_A < 125 °C
SID304	DNL_D	Differential non-linearity	–0.05	–	0.05	%	
SID305	ACC_D	Accuracy including lifetime and temperature drift	–0.25	TBD	0.25	%	3.6 V < V_{BAT} < 28 V, -40ºC < T_A < 125 ºC

5.3.4 Current Channel

Table 5-13. Current Channel Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID104	I_{RMEAS}	Measurement range (gain=8)	–1500	–	1500	A	For a typical shunt (F7, 100 µΩ) Guaranteed by design
SID105	I_{RMEAS}	Range with gain=512	–23.44	–	23.44	A	Guaranteed by design
SID106	ACC1_I	Accuracy including lifetime and temperature drift	–0.3	TBD	0.3	%	V_{BAT} < 18 V and T_A < 105 °C
SID106A	ACC2_I	Accuracy including lifetime and temperature drift	–0.5	TBD	0.5	%	V_{BAT} > 18 V or T_A > 105 °C
SID107	DNL_V	Differential non-linearity	–0.1	–	0.1	%	
SID108	I_{OFF}	Input referred offset error	–500	0	500	nV	I < 30A and V_{BAT} < 18 V and T_A < 105 ºC
SID109	I_{OFF}	Input referred offset error	–1000	0	1000	nV	I > 30A and V_{BAT} < 18 V and T_A < 105 ºC
SID110	I_{OFF}	Input referred offset error	–2000	0	2000	nV	V_{BAT} > 18 V or Ta>105ºC
SID111	I_{RES1}	Resolution (current measurements)	–	0.715	1	mA	Gain = 512, typical shunt
SID111A	I_{RES1A}	Resolution of accumulated current interrupt	–	0.715	1	mA	Gain = 512, typical shunt
SID112	I_{RES2}	Resolution (voltage measurements)	–	36.6	–	µV	Differential, Gain = 1 ADC Range: –0.3 V to +0.3 V differential

Table 5-13. Current Channel Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID113	I_{NOISE}	Input referred noise	–	–	12	nVrms/√Hz	Gain = 512, equal to 4 mA rms with a 100 µΩ shunt at 1-ksps update rate
SID114	$V_{IN,RSx}$	RSHx, RSLx differential input voltage range	–0.3	–	0.3	V	
SID115	G_{PGA}	Programmable gain	4	–	512	V/V	
SID116	G_{OP}	Fixed gain (voltage mode)	–	1	–	V/V	ADC Range: –1.2 V to +1.2 V differential
SID117	N_{ADC}, CUR	ADC digital channel resolution[19]	23	–	–	bits	No missing codes
SID118	ATT_{IPAS}	Frequency attenuation	0	–	3	dB	@FIPASS=0.1*FIUPDATE, with FIR
SID119	ATT_{ISTOP}	Frequency attenuation	40	–	–	dB	@FIPASS=0.5*FIUPDATE, with FIR
SID120	$f_{IUPDATE}$	Signal update rate output[20]	0.75	8	96	ksps	After decimator, lower rates may be used Max: only meant for diagnostic modes where multiple samples will be taken. Noise is higher
SID121	f_{IAF}	Anti-alias LPF corner frequency	–	30	–	kHz	Guaranteed by design
SID122	R_{SHDIAG}	Shunt disconnect threshold[21]	–	–	10	kΩ	For open circuit detection
SID122A	$R_{SHDIAGA}$		–	–	1	kΩ	V_{SH} limit of ±0.05 V

Notes
19. Decimator output minimum data width is 23-bits to accommodate automatic gain of 4-512 while maintaining LSB with same weight regardless of trim (same mA/LSB); this is accomplished by weighting or shifting modulator output/decimator input by gain.
20. 8 ksps guaranteed when alternately measuring two different sources, up to 96 ksps when continuously measuring one source.
21. The current measurement channel detects disconnect shunt connections by switching internal pull-up resistors to the shunt pins. If the resistance between the RSHx or RSLx to ground is more than 10 kΩ, an open pin fault can be detected. See the functional diagnosis section for more information.

5.3.5 Voltage Channel

Table 5-14. Voltage Channel Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID123	V_{RMEAS}	HV measurement range	0	–	28	V	With HVATTEN = 24
SID124	$V_{RMEASLV}$	LV measurement range	0	–	1.2	V	
SID125	ACC1_V[22]	Accuracy including lifetime and temperature drift	–0.25	TBD	0.25	%	3.6 V < V_{BAT} < 28 V, –40 ºC <T_A< 125 ºC
SID126	ACC2.1_V[22]		–0.15	TBD	0.15	%	11 V < V_{BAT} < 14 V, –40 ºC < T_A < 85 ºC
SID126B	V_{REF1}	Primary high precision reference	–	1.2	–	V	Measured differentially between V_{REFH} and V_{REFL}
		Accuracy including lifetime and temperature drift	–0.15	–	0.15	%	-40 ºC <T_A< 125 ºC
SID126C	V_{REF2}[23]	Secondary reference	–	1.2	–	V	
		Accuracy including lifetime and temperature drift	–2	–	2	%	
SID127	DNL_V	Differential non-linearity	–0.05	–	0.05	%	
SID128	V_{RES}	Resolution	–	0.293	–	mV	0 V to 18-V input range (Rdiv=16)
SID129	V_{RES}	Resolution	–	0.4	–	mV	0 V to 28-V input range (Rdiv=24)
SID130	NOISE_V	Input referred noise	–	–	6	µVrms/√Hz	At 1-ksps update rate
SID131	N_{ADC},V_{OL}	ADC resolution	16	–	–	Bits	No missing codes
SID132	ATT_{VPAS}	Frequency attenuation	0	–	3	dB	@FIPASS=0.1*FIUPDATE, with FIR
SID133	ATT_{VSTOP}	Frequency attenuation	40	–	–	dB	@FIPASS=0.5*FIUPDATE, with FIR
SID134	$f_{VUPDATE}$	Signal update rate output[24]	0.75	8	96	ksps	After decimator, lower rates may be used Max: only meant for diagnostic modes where multiple samples will be taken. Noise is higher
SID135	f_{VAF}	Anti-Alias LPF corner frequency	–	30	–	kHz	For open circuit detection Guaranteed by design

Notes
22. Accuracy includes the effect of leakage current of the 2kohm resistor.
23. Secondary reference with its associated ground can be measured as an input to the ADC (not available on V_{REFH} and V_{REFL}.
24. 8 ksps guaranteed when alternately measuring two different sources with 16-bit resolution, 48 ksps when continuously measuring one source.

Table 5-14. Voltage Channel Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID136	Latency V_{MUX}	Measurement valid delay[25]	–	64.13	64.77	µs	ADC: 3*64 = 192 clock cycles to produce first valid data at sinc3 output. Does not include FIR and Rare Reducer (RR) delays; T = 1/3.07 MHz Typ: (5 + Channel select delay + 192)*T = 64.13 µs Channel select delay = 1, 37 (inter-leaved measurements) Max: IMO variation is ±1% when locked to HPOSC (5 + Channel select delay + 192)*T*(1+1%) = 64.77 µs
SID136A					2200	µs	Includes FIR and Rate Reducer (RR) delays latency = (5 + [(FIR_taps+1)*DR2 + (sinc_order-1)] * DR) / Fos Data rate: 8 ksps DR: Decimation Rate = 64 DR2: Decimation Rate 2 = 6
SID136B	Phasedelay	Phase delay with the current channel	–	–	5	µs	Both channels have FIR enabled, Automatic gain control on current channel
SID137	HV_{ATTEN}	High-voltage divider ratio for V_{SENSE}, V_{DIAG} inputs	–	16	–	V/V	Selectable under program control, includes 2.2-kΩ external resistor
SID137A	HV_{ATTEN}	High-voltage divider ratio for V_{SENSE}, V_{DIAG} inputs	–	24	–	V/V	
SID138	RHV_{ATTEN}	HV resistance to V_{SSA}	–	2.4	–	MΩ	
SID139	IHV_{ATTEN}	HV divider off leakage	–	0	1	µA	V_{SENSE}, V_{DIAG} < 15 V

Note
25. First valid decimator output with a 3.072-MHz ADC clock with OSR=64 and decimator=Sinc3. Digital FIR filtering and averaging may add more latency.

5.4 Digital Peripherals

5.4.1 TCPWM

Table 5-15. TCPWM Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID140	I_{TCPWM1}	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID141	I_{TCPWM2}	Block current consumption at 12 MHz	–	–	155	µA	All modes (TCPWM)
SID142	I_{TCPWM3}	Block current consumption at 49.152 MHz	–	–	650	µA	All modes (TCPWM)
SID143	$f_{TCPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = 49.152 MHz Guaranteed by design
SID144	$t_{TPWMENEXT}$	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Guaranteed by design
SID145	$t_{TPWMEXT}$	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs Guaranteed by design
SID146	t_{CRES}	Counter Resolution	1/Fc	–	–	ns	Minimum time between successive counts Guaranteed by design
SID147	t_{PWMRES}	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output Guaranteed by design
SID148	t_{QRES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Guaranteed by design

5.4.2 LIN

Table 5-16. LIN Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID249	f_{LIN}	Internal clock frequency to the LIN block	–	–	2	MHz	Guaranteed by design
SID250	BR_NOM	Bit rate on the LIN bus	1		20	kbps	
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1		115.2	kbps	

5.4.3 Serial Communication Block

Table 5-17. Fixed I²C DC Specifications[26]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	150		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	2		

Table 5-18. Fixed I²C AC Specifications[26]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	f_{I2C1}	Bit rate	–	–	1	Msps	–

Table 5-19. SPI DC Specifications[26]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560		–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	800		–

Table 5-20. SPI AC Specifications[26]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	f_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	Fc	MHz	Fc max = Fcpu/6. Fcpu maximum = 49.152 MHz

Note
26. Guaranteed by characterization.

Table 5-21. Fixed SPI Master Mode AC Specifications[27]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	t_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	t_{DSI}	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	t_{HMO}	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge

Table 5-22. Fixed SPI Slave Mode AC Specifications[27]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	t_{DMI}	MOSI valid before Sclock capturing edge	30	–	–	ns	–
SID171	t_{DSO}	MISO valid after Sclock driving edge	–	–	48+ 3*T_{SCB}		–
SID171A	t_{DSO_EXT}	MISO valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	t_{HSO}	Previous MISO data hold time	0	–	–		–
SID172A	$t_{SSELSSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns	–

Table 5-23. UART DC Specifications[27]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	60	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	320	µA	–

Table 5-24. UART AC Specifications[27]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	f_{UART}	Bit rate	–	–	1	Mbps	–

5.4.4 SWD Interface

Table 5-25. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	f_SWDCLK1	3.3 V ≤ V_{DDD} ≤ 3.6 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215[28]	t_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[28]	t_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[28]	t_SWDO_VALID	T = 1/f SWDCLK	–	–	1		–
SID217A[28]	t_SWDO_HOLD	T = 1/f SWDCLK	0.5*T	–	–		–

Note
27. Guaranteed by characterization.

5.5 Memory

Table 5-26. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$t_{ROWWRITE}$[29]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$t_{ROWERASE}$[29]	Row erase time	–	–	13		
SID176	$t_{ROWPROGRAM}$[29]	Row program time after erase	–	–	7		
SID178	$t_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35		–
SID180[30]	$t_{DEVPROG}$[29]	Total device program time	–	–	20	Seconds	
SID181[30,31]	f_{END}	Flash endurance	100 K	–	–	Cycles	
SID182	f_{RETQ}	Flash retention. $T_A \leq 105$ °C, 10K P/E cycles, ≤ three years at $T_A \geq 85$ °C	15	–	–	years	Guaranteed by characterization.
SID183	$t_{RESUMESYSCALL}$	Time for non-blocking system calls to be resumed	–	–	25	ms	Non-blocking system calls should be used only for data flash
SID256	tWS48	Number of Wait states at 49.152 MHz	3	–	–		CPU execution from Flash
SID257	tWS36	Number of Wait states at 36 MHz	2	–	–		CPU execution from Flash Guaranteed by design
SID258	tWS24	Number of Wait states at 24.576 MHz	1	–	–		CPU execution from Flash Guaranteed by design
SID259	tWS12	Number of Wait states at 12 MHz	0	–	–		CPU execution from Flash Guaranteed by design

Notes
28. Guaranteed by design.
29. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
30. Guaranteed by characterization.
31. Data flash: 100k cycles per row; Code flash: 100k cycles total

5.6 System Resources

Table 5-27. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V_{IPOR}	POR trip voltage	0.7	–	1.5	V	

Table 5-28. Brown-out Detect (BOD) for V_{DDD}, V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V_{DDD_BOD}	BOD trip voltage for V_{DDD}	2.34	–	2.63	V	
SID190A	V_{CCD_DBOD}	BOD trip voltage for V_{CCD}	1.64	–	1.74		
SID190B	$V_{CCD\_BOD\_DPSLP}$	BOD trip voltage for V_{CCD} in Deep Sleep	1.1	–	1.5		

Table 5-29. Overvoltage Detect (OVD) for V_{DDD}, V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID192	V_{DDD_OVD}	OVD trip voltage for V_{DDD}	3.62	–	3.96	V	
SID192A	V_{CCD_OVD}	OVD trip voltage for V_{CCD}	1.97	–	2.17	V	

6. Ordering Information

The marketing part numbers for the PSoC 4 HV PA devices are listed in the following table.

MPN	Features												Packages	Operating Temp
	Max CPU Speed (MHz)	Code Flash (KB) with ECC	SRAM (KB) with ECC	Data Flash (KB) with ECC	SFlash (KB) for storing constants	16-20 bit Precision ΔΣ ADC	Voltage measurement accuracy	TCPWM Blocks	LIN Blocks	SCB	High-Voltage Subsystem (LDO, LIN PHY)	GPIO	32-QFN (6*6mm)	-40 to +125 °C
CY8C4126LCE-HV403	24.576	64	4	8	1	2	0.25%	4	1	1	Y	8	Y	Y
CY8C4126LCE-HV423	24.576	64	4	8	1	2	0.15%[32]	4	1	1	Y	8	Y	Y
CY8C4127LCE-HV403	24.576	128	8	8	1	2	0.25%	4	1	1	Y	8	Y	Y
CY8C4127LCE-HV423	24.576	128	8	8	1	2	0.15%[32]	4	1	1	Y	8	Y	Y
CY8C4147LCE-HV403	49.152	128	8	8	1	2	0.25%	4	1	1	Y	8	Y	Y
CY8C4147LCE-HV423	49.152	128	8	8	1	2	0.15%[32]	4	1	1	Y	8	Y	Y

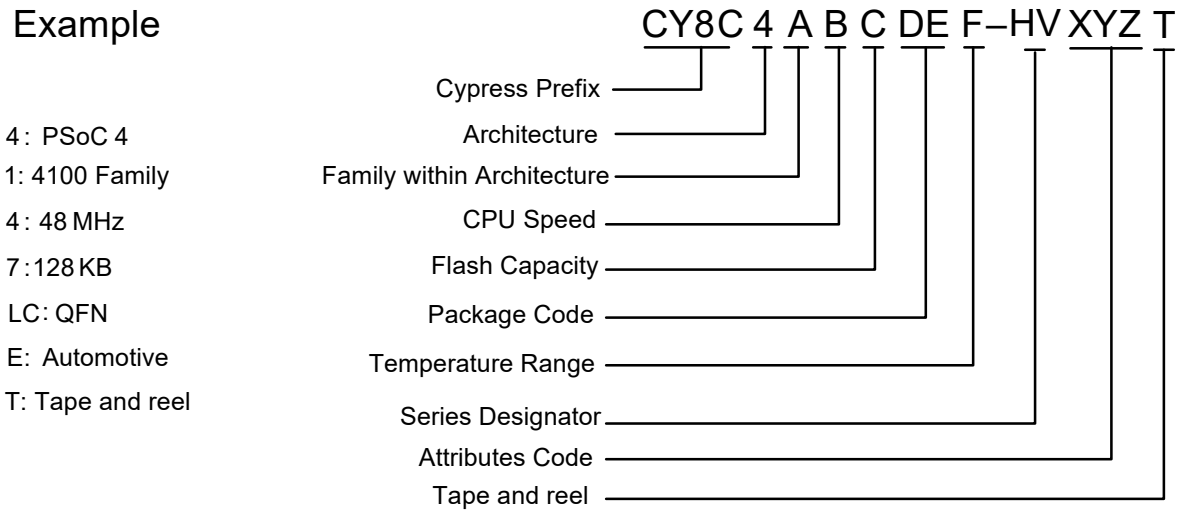
Note
32. 11 V < V_{BAT} < 14 V, -40 °C <T_A < 85 °C.

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	6	64 KB
		7	128 KB
DE	Package Code	LC	QFN with wettable flanks
F	Temperature Range	E	Automotive (-40 °C to +125 °C)
S	Series Designator	HV	PSoC 4 High Voltage Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

Example



7. Packaging

The PSoC 4 HV PA will be offered in a 32-QFN package.

Package dimensions and Cypress drawing numbers are in the following table.

Table 7-1. Package List

Spec ID#	Package	Description	Package Dwg
BID20	32-pin QFN with wettable flanks	6 × 6 × 1-mm height with 0.5-mm pitch	002-29040

Table 7-2. Package Thermal Characteristics

Parameter	Description	Package	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	125	°C
T_J	Operating junction temperature		–40	–	150	°C
T_{JA}	Package θ_{JA} [33]	32-pin QFN	–	–	15.1	°C/Watt
T_{JC}	Package θ_{JC}	32-pin QFN	–	–	1.2	°C/Watt

Table 7-3. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
32-pin QFN	260 °C	30 seconds

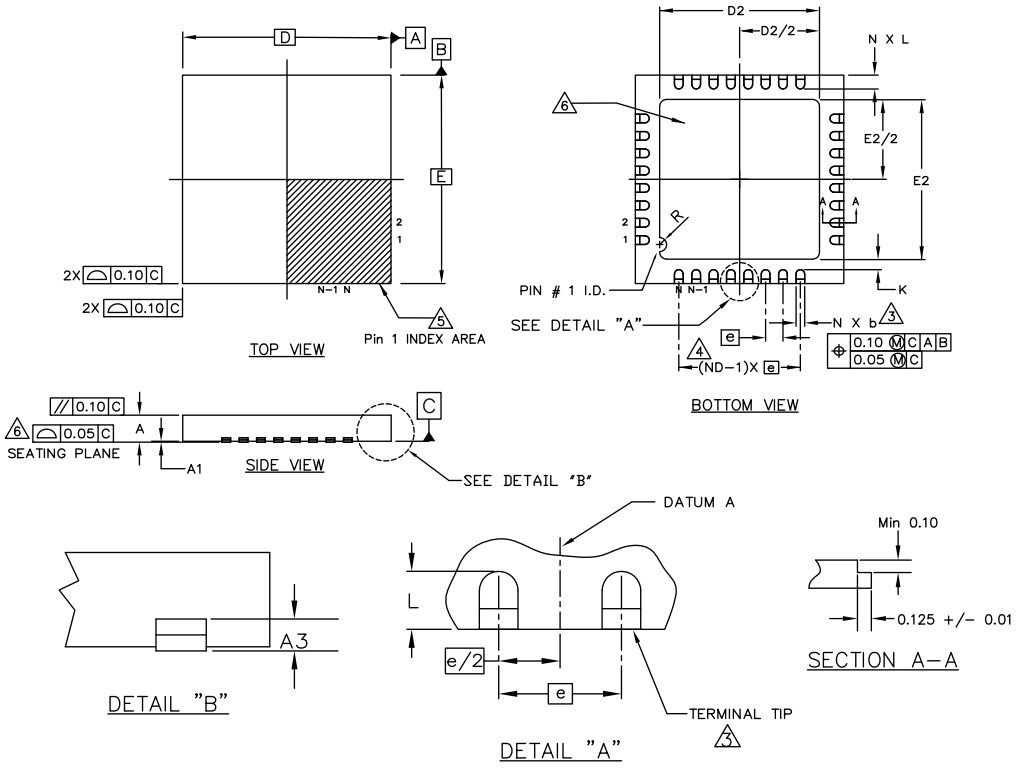
Table 7-4. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
32-pin QFN	MSL 3

Note
33. Four-layered PCB.

7.1 Package Diagram

Figure 7-1. 32-Pin QFN with Wettable Flank (6.0 × 6.0 × 1 mm)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		32	
ND		8	
L	0.35	0.40	0.45
b	0.20	0.25	0.30
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D		6.00 BSC	
E		6.00 BSC	
A	-	-	1.00
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.20 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-29040 *A

8. Acronyms

Table 8-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 8-1. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 8-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 8-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9. Document Conventions

9.1 Units of Measure

Table 9-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC 4 HV Precision Analog 144k Datasheet Document Number: SNPR-491			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6726670	11/07/2019	New datasheet for new device family
*A	6837083	03/24/2020	Changed 'Programmable Analog' to 'Precision Analog'. Added 'Challenge Response functionality'. Lifetime Counter: Changed description with correct values. Updated Watchdog Timers (WDT) Updated Table 2-2, Table 2-3 Added Section 2.4 for LIN Block features. Updated text in Section 2.7. Updated Figure 2-6 Updated all figures in Section 2.8. Fixed typo in dVBE formula ('t' --> 'T') in Section 2.8.4. Updated Pinouts based on planned implementation Updated Packaging based on latest package specification. Updated power system block diagram in Section 2.2. Update bypass capacitor values in Section 2.2. Electrical Specifications: SIDA13A - Added supply current absolute max SID4A - I_{SH}: Added nominal specs for V_{SENSE}/V_{DIAG} current SID7A - I_{CS}: Added nominal specs for $R_{SH}/R_{SL}/R_{SH2}/R_{SL2}$ current SID19 - Added unit 'µA' SID27 - Changed I_{DD} spec to include regulator current including core SID27A - Added I_{DDGPIO} spec to capture regulator current only for GPIOs SID47 - Added unit 'ms' SID48 - Added unit 'ms' SID49 - Changed parameter name from $F_{GPIOUT1}$ to $F_{GPIOUTF}$ (Fast strong mode) SID50 - Changed parameter name from $F_{GPIOUT3}$ to $F_{GPIOUTS}$ (Slow strong mode) SIDL62 - Removed LIN Output voltage spec SIDL76 - Added max for V_{OH} -> LIN Bus transmitted recessive output voltage SIDL83 - Added unit 'kΩ' SIDL84 - Added formula for duty cycle calculation (D1) in 'conditions' SIDL85 - Added formula for duty cycle calculation (D2) in 'conditions' SIDL86 - Added formula for duty cycle calculation (D3) in 'conditions' SIDL87 - Added formula for duty cycle calculation (D4) in 'conditions' SID106 - Added typical value (TBD) for current channel accuracy SID106A - Added typical value (TBD) for current channel accuracy SID112 - Added ADC Range for resolution (under 'conditions') SID122A - Added new spec for Shunt disconnect threshold for a limited V_{SH} SID125 - Added typical value (TBD) for voltage channel accuracy SID126 - Added typical value (TBD) for voltage channel accuracy SID126A - Added typical value (TBD) for voltage channel accuracy SID129 - Added unit 'mV' SID131 - Added 'No missing codes' under 'conditions' SID173 - Removed V_{PE} spec (Erase and Program Voltage) SID249 - Updated max value SIDA13 - Updated max value SID99 - Updated min value SID9 - Updated max value SID.CLK#6 - Updated to SID184. Removed SID214 SID21 - Updated max value SID57 - Added conditions Added spec SID57A (New HPOSC accuracy spec for T_A >105 °C) SID42 - Changed unit from mV to V SID43 - Added conditions

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*A (Cont.)	6837083	03/24/2020	SIDX6 - Added conditions SID166 - Updated spec and conditions Added SID137A SID35 - Updated max value SID45 and SID46 - Updated min value SID170 - Updated min value SID176 - Updated max value Updated XRES DC Specifications[10] and XRES AC Specifications. Updated Power On Reset (PRES), Brown-out Detect (BOD) for VDDD, VCCD, and Overvoltage Detect (OVD) for VDDD, VCCD.
*B	6955769	08/27/2020	Updated Digital Channel Data Path. Updated Figure 2-1 and added Table 2-1. Updated values and conditions for the following spec IDs: SIDA2, SID9, SID12, SID13, SID43, SIDX6, SID99, SID110, SID118, SID119, SID120, SID132, SID133, SID134, SID175. Added SID12A and SID13A. Added footnote for SIDA13A. Removed SID184. Updated ROM to 16 KB in Block Diagram. Updated R1/C1 Max Current Specifications. Updated Alternate Pin Functions Updated footnote 3. Updated Package Thermal Characteristics. Updated Ordering Information.
*C	7122581	04/15/2021	Updated the title to PSoC 4 HV Precision Analog 144k Datasheet. Updated ILO clock source information in Features. Changed VDD references to VDDD. Updated min value for SIDL76. Updated typ and max values for SID122 and SID122A. Updated SID126B and SID126C. Updated conditions for SID139. Added SID178. Updated description for SID258. Parameter names aligned with the internal documentation. System ResourcesAdded Sample Application Schematic. Updated “guaranteed by design” note for the relevant electrical specs. Updated Absolute Maximum Ratings and Operating Current and Wakeup Times: - SID12A, SID13A: Updated conditions - SIDA2: Update pin list for system-level ESD - SIDA24, SIDA24A: New specifications added for defining short circuit tolerance on the HVREG and LIN pins - SID26: Corrected the min Vbat condition
*D			Added footnote for Alternate Pin Functions. Updated Table 2-2. Updated PACSS Measurement/Acquisition System. Updated ESD Protection. Updated Sample Application Schematic. Added footnote for SID15, SID16, SID17, and SID18. Removed conditions for SID54. Updated min and max values for SIDL83. Updated conditions for SID305. Updated conditions for SID112. Updated description for SID213. Updated max value and conditions for SID302. Updated Flash AC Specifications - added new spec SID183.

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