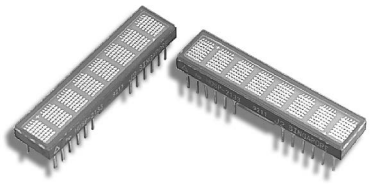
BROADCOM®

Data Sheet

HDSP-2131, HDSP-2132, HDSP-2133, HDSP-2179

Eight-Character 5.0-mm (0.2-in.) Glass/Ceramic Intelligent 5 × 7 Alphanumeric Displays for Military Applications



Description

The Broadcom® HDSP-2131 (yellow), HDSP-2179 (orange), HDSP-2132 (high efficiency red), and HDSP-2133 (green) are eight-digit, 5 × 7 dot matrix, alphanumeric displays. The 5.0-mm (0.2-in.) high characters are packaged in a standard 7.64-mm (0.30-in.) 32-pin DIP. The on-board CMOS IC can decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols may be stored in an on-board RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-213x and HDSP-2179 are designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional 8-bit data bus. These features make the HDSP-213x and HDSP-2179 ideally suited for applications where a hermetic, low power alphanumeric display is required.

Devices

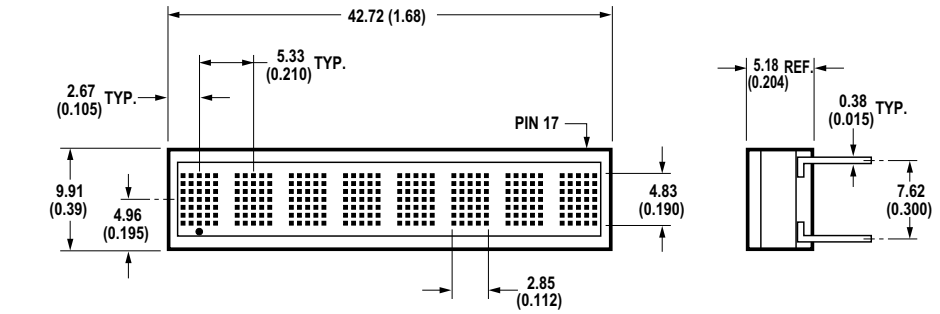
Yellow	High Efficiency Red	High Performance Green	Orange
HDSP-2131	HDSP-2132	HDSP-2133	HDSP-2179

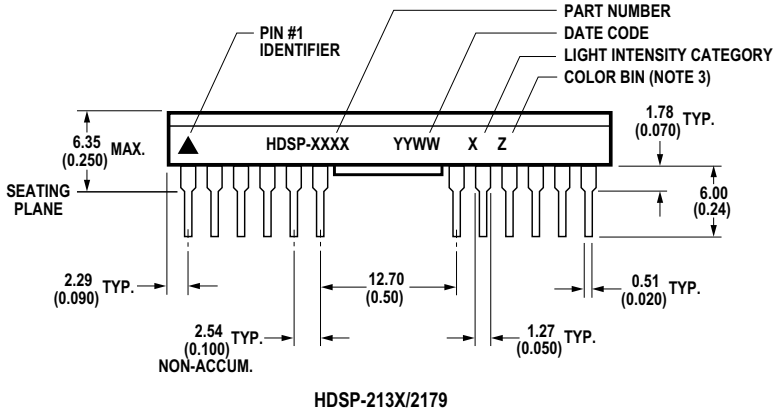
Features

- Wide operating temperature range: –55°C to +85°C
- Smart alphanumeric display
  - On-board CMOS IC
  - Built-in RAM
  - ASCII decoder
  - LED drive circuitry
- 128 ASCII character set
- 16 user-definable characters
- Programmable features:
  - Individual character flashing
  - Full display blinking
  - Multilevel dimming and blanking
  - Self-test
  - Clear function
- Read/write capability
- Full TTL compatibility
- HDSP-2131, HDSP-2133, and HDSP-2179 are usable in night vision lighting applications
- Categorized for luminous intensity
- HDSP-2131 and HDSP-2133 are categorized for color
- Excellent ESD protection
- Wave solderable
- X-Y stackable
- RoHS compliant

CAUTION! Observe standard CMOS handling precautions with the HDSP-2131, HDSP-2132, HDSP-2133, and HDSP-2179.

Package Dimensions





HDSP-213X/2179

PIN #	FUNCTION	PIN #	FUNCTION
1	CLS	17	GND (SUPPLY)
2	CLK	18	GND (LOGIC)
3	$\overline{WR}$	19	D4
4	$\overline{CE}$	20	D5
5	$\overline{RST}$	21	D6
6	$\overline{RD}$	22	D7
7	NO PIN	23	NO PIN
8	NO PIN	24	NO PIN
9	NO PIN	25	NO PIN
10	NO PIN	26	NO PIN
11	D0	27	$\overline{FL}$
12	D1	28	A0
13	D2	29	A1
14	D3	30	A2
15	NC	31	A3
16	V_{DD}	32	A4

NOTES:
1. ALL DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE IS± 0.30 mm (0.015 INCH).
3. FOR GREEN AND YELLOW DEVICES ONLY.
4. LEADS ARE COPPER ALLOY, SOLDER DIPPED.

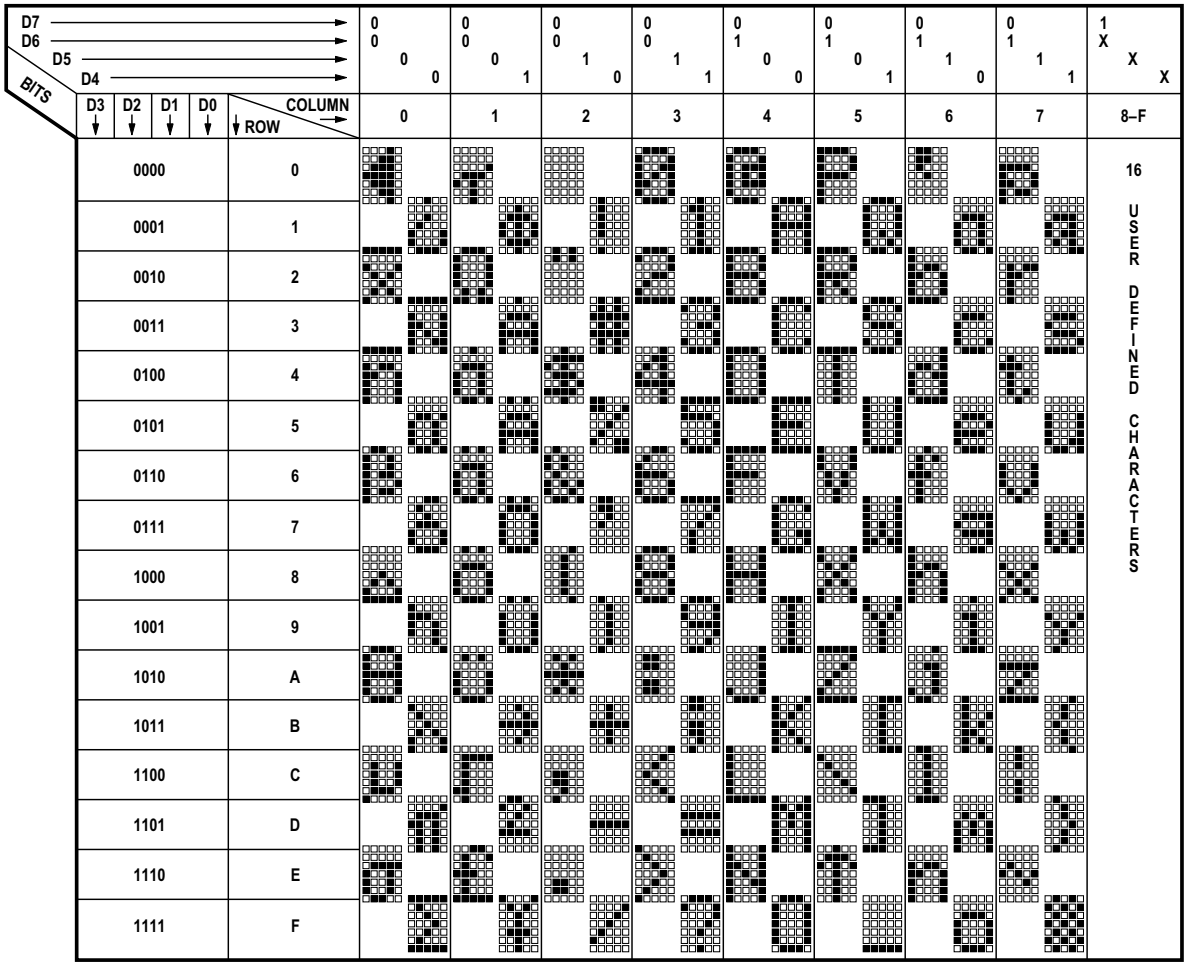
Absolute Maximum Ratings

Parameter	Values
Supply Voltage, V_{DD} to Ground[a]	–0.3V to 7.0V
Operating Voltage, V_{DD} to Ground[b]	5.5V
Input Voltage, Any Pin to Ground	–0.3V to V_{DD} + 0.3V
Free Air Operating Temperature Range, T_A	–55°C to +85°C
Storage Temperature, T_S	–55°C to +100°C
CMOS IC Junction Temperature, T_J (IC)	+150°C
Soldering Temperature (1.59 mm [0.063 in.] below Body) Solder Dipping Wave Soldering	 260°C for 5 seconds 250°C for 3 seconds
ESD Protection at 1.5 kΩ, 100 pF	V_Z = 4 kV (each pin)

a. Maximum voltage is with no LEDs illuminated.

b. 20 dots ON in all locations at full brightness.

Character Set



Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical Characteristics over Operating Temperature Range

4.5V < V_{DD} < 5.5V (unless otherwise specified).

Parameter	Symbol	Min.	25°C Typ.[a]	25°C Max.[a]	Max.[b]	Units	Test Conditions
Input Leakage (Input without Pullup)	I_I	–10.0	—	—	+10.0	µA	V_{IN} = 0 to V_{DD}, pins CLK, D_0 to D_7, A_0 to A_4
Input Current (Input with Pullup)	I_{IP}	–30.0	11	18	30	µA	V_{IN} = 0 to V_{DD}, pins $\overline{RST}$, $\overline{CLS}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	I_{DD} (BLK)	—	0.5	1.5	2.0	mA	V_{IN} = V_{DD}
I_{DD} 8 digits 12 Dots/Character[c]	I_{DD}(V)	—	200	255	330	mA	"V" on in all 8 locations
I_{DD} 8 digits 20 Dots/Character[c]	I_{DD}(#)	—	300	370	430	mA	"#" on in all 8 locations
Input Voltage High	V_{IH}	2.0	—	—	V_{DD} + 0.3V	V	V_{DD} = 5.5V
Input Voltage Low	V_{IL}	GND – 0.3V	—	—	0.8	V	V_{DD} = 4.5V
Output Voltage High	V_{OH}	2.4	—	—		V	V_{DD} = 4.5V, I_{OH} = –40 µA
Output Voltage Low D_0 to D_7	V_{OL}	—	—	—	0.4	V	V_{DD} = 4.5V, I_{OL} = 1.6 mA
Output Voltage Low CLK		—	—	—	0.4	V	V_{DD} = 4.5V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-Pin	$R\theta_{J\text{-}PIN}$	—	11	—		°C/W	

a. V_{DD} = 5.0V.

b. Maximum I_{DD} occurs at –55°C.

c. Average I_{DD} is measured at full brightness. See Table 2 for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 × Average I_{DD} (#).

Optical Characteristics at 25°C[1]

V_{DD} = 5.0V at full brightness.

High Efficiency Red HDSP-2132

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}	—	635	nm
Dominant Wavelength	λ_d	—	626	nm

Orange HDSP-2179

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}	—	600	nm
Dominant Wavelength	λ_d	—	602	nm

Yellow HDSP-2131

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}	—	583	nm
Dominant Wavelength	λ_d	—	585	nm

High Performance Green HDSP-2133

Description	Symbol	Minimum	Typical	Units
Luminous Intensity Character Average (#)	I_V	2.5	7.5	mcd
Peak Wavelength	λ_{PEAK}	—	568	nm
Dominant Wavelength	λ_d	—	574	nm

1. Refers to the initial case temperature of the device immediately prior to the light measurement.

AC Timing Characteristics over Temperature Range

V_{DD} = 4.5V to 5.5V unless otherwise specified.

Reference Number	Symbol	Description	Min.[a]	Units
1	t_{ACC}	Display Access Time		ns
		Write	210	
		Read	230	
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[b, c]		ns
		Write	140	
		Read	160	
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of[a, b]		ns
		Write	140	
		Read	160	
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal[b, c]	0	ns
8	t_W	Write Active Time[b, c]	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
—	t_{RC}	Reset Active Time[d]	300	ns

a. Worst case values occur at an IC junction temperature of 150°C.

b. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.

c. Changing the logic levels of the Address lines when CE = "0" may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.

d. The display must not be accessed until after three clock pulses (110 µs minimum using the internal refresh clock) after the rising edge of the reset line.

AC Timing Characteristics Over Temperature Range

V_{DD} = 4.5V to 5.5V unless otherwise specified.

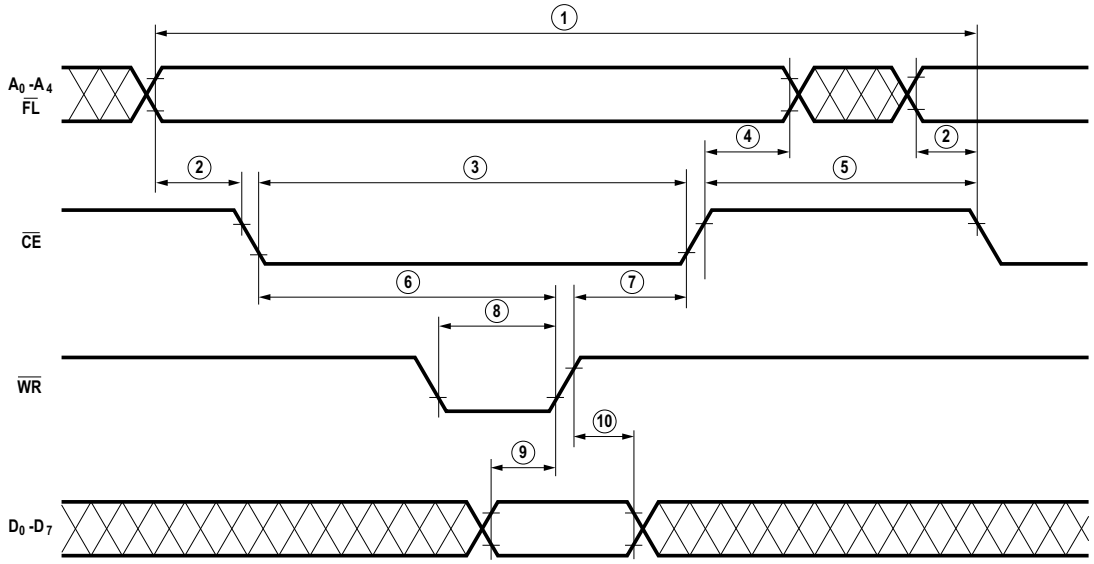
Symbol	Description	25°C Typical	Minimum	Units
F_{OSC}	Oscillator Frequency	57	28	kHz
F_{RF}[a]	Display Refresh Rate	256	128	Hz
F_{FL}[b]	Character Flash Rate	2	1	Hz
t_{ST}[c]	Self Test Cycle Time	4.6	9.2	Sec

a. $F_{RF} = F_{OSC}/224$

b. $F_{FL} = F_{OSC}/28,672$

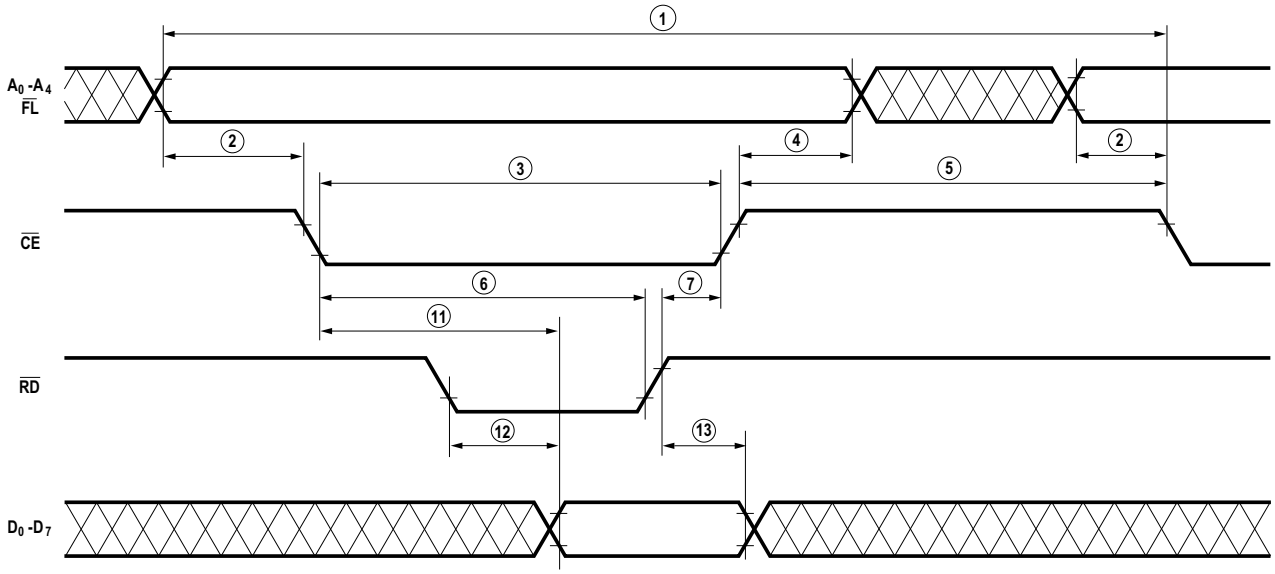
c. $t_{ST} = 262,144/F_{OSC}$

Write Cycle Timing Diagram



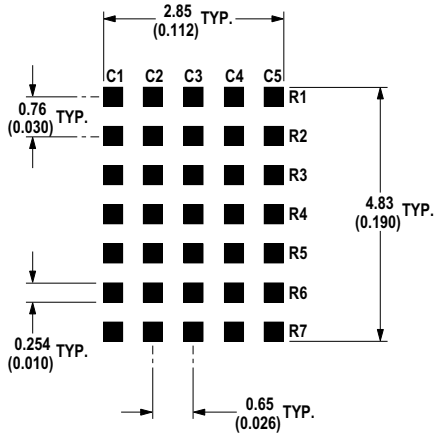
INPUT PULSE LEVELS: 0.6 V to 2.4 V

Read Cycle Timing Diagram



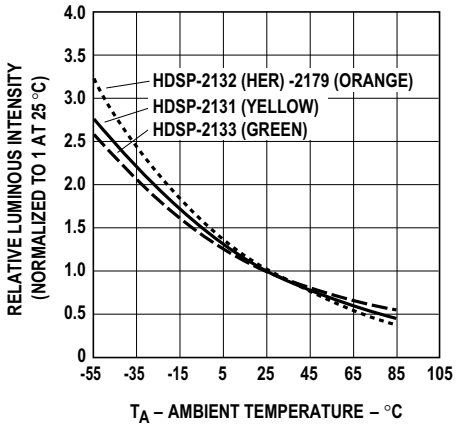
INPUT PULSE LEVELS: 0.6 V to 2.4 V
OUTPUT REFERENCE LEVELS: 0.6 V to 2.2 V
OUTPUT LOADING = 1 TTL LOAD AND 100 pF

Character Font



NOTE: NOT TO SCALE

Relative Luminous Intensity vs. Temperature



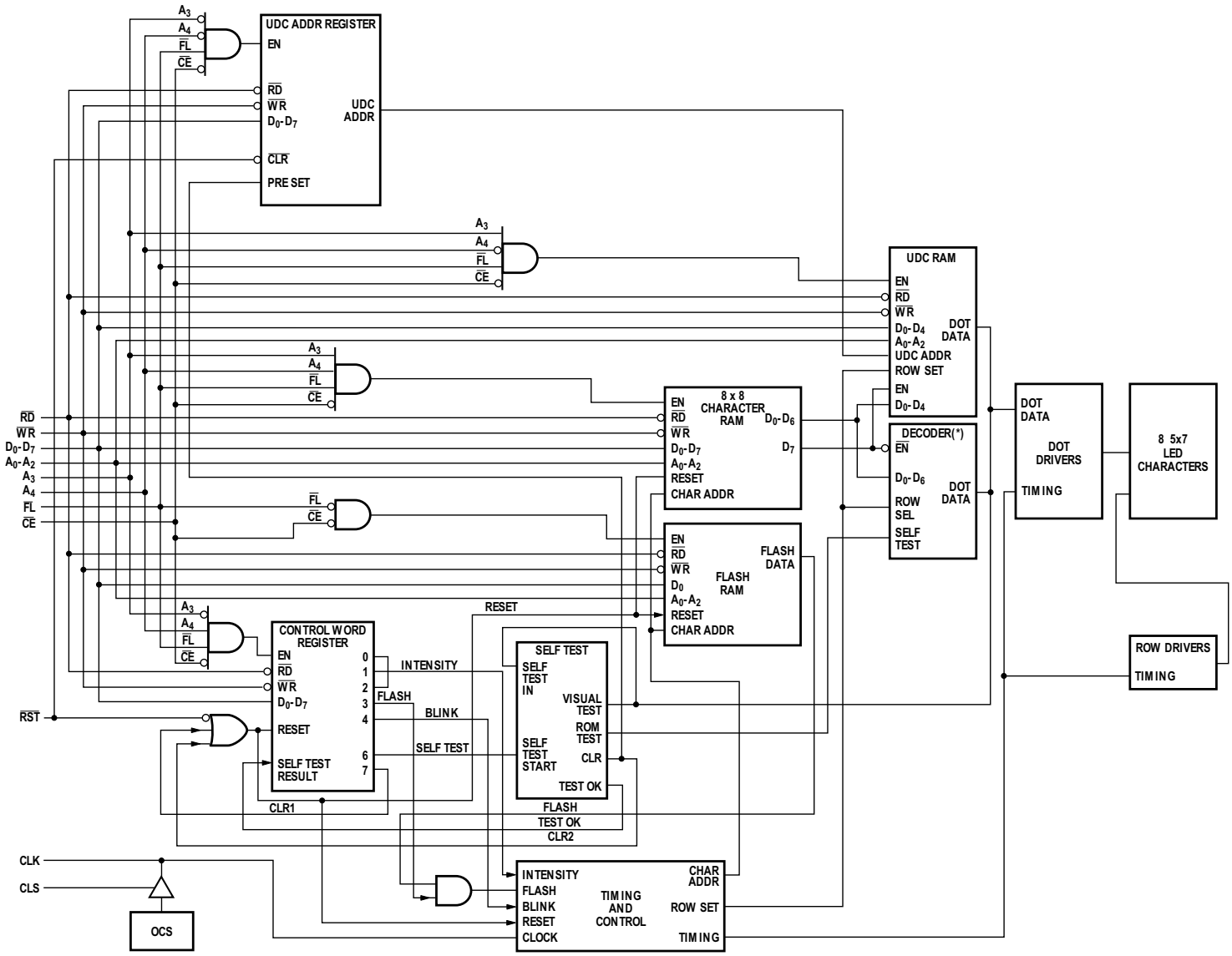
Electrical Description

Pin Function	Description
RESET ($\overline{RST}$, Pin 5)	Reset initializes the display.
FLASH ($\overline{FL}$, Pin 27)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3 to A_4.
ADDRESS INPUTS (A_0 to A_4, Pins 28 to 32)	Each location in memory has a distinct address. Address inputs (A_0 to A_2) select a specific location in the Character RAM, the Flash RAM, or a particular row in the UDC (User-Defined Character) RAM. A_3 to A_4 select which section of memory is accessed. See Table 1 for the logic levels needed to access each section of memory.
CLOCK SELECT (CLS, Pin 1)	This input select s either an internal (CLS = 1) or external (CLS = 0) clock source.
CLOCK INPUT/OUTPUT (CLK, Pin 2)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, Pin 3)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, Pin 4)	This input must be at a logic low to read data from or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, Pin 6)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D_0 to D_7, Pins 11 to 14, 19 to 22)	The data bus reads from or writes to the display.
$GND_{(SUPPLY)}$ (Pin 17)	This is the analog ground for the LED drivers.
$GND_{(LOGIC)}$ (Pin 18)	This is the digital round for internal logic.
$V_{DD(POWER)}$ (Pin 16)	This is the positive power supply input.

Table 1: Logic Levels to Access Memory

$\overline{FL}$	A_4	A_3	Section of Memory	A_2 A_1 A_0
0	X	X	Flash RAM	Character Address
1	0	0	UDC Address register	Don't Care
1	0	1	UDC RAM	Row Address
1	1	0	Control Word register	Don't Care
1	1	1	Character RAM	Character Address

Figure 1: HDSP-213x/HDSP-2179 Internal Block Diagram



Display Internal Block Diagram

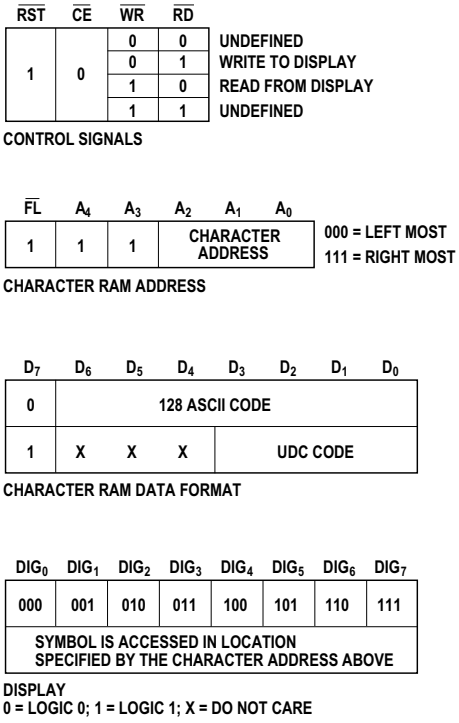
Figure 1 shows the internal block diagram of the HDSP-213x/HDSP-2179 display. The CMOS IC consists of an 8-byte Character RAM, an 8-bit Flash RAM, a 128-character ASCII decoder, a 16-character UDC RAM, a UDC Address register, a Control Word register, and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 × 7 dot matrix characters. The major user accessible portions of the display are listed below.

Character RAM	This RAM stores either ASCII character data or a UDC RAM address.
Flash RAM	This is a 1 × 8 RAM which stores Flash data.
User-Defined Character RAM (UDC RAM)	This RAM stores the dot pattern for custom characters.
User-Defined Character Address register (UDC Address register)	This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
Control Word register	This register allows the user to adjust the display brightness, flash individual characters, blink, self test, or clear the display.

Character RAM

Figure 2 shows the logic levels needed to access the HDSP-213x/HDSP-2179 Character RAM. During a normal access, the $\overline{CE}$ = "0" and either $\overline{RD}$ = "0" or $\overline{WR}$ = "0". However, erroneous data may be written into the Character RAM if the address lines are unstable when $\overline{CE}$ = "0" regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A_0 to A_2 select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D7 differentiates between an ASCII character and a UDC RAM address. D_7 = 0 enables the ASCII decoder and D_7 = 1 enables the UDC RAM. D_0 to D_6 are used to input ASCII data and D_0 to D_3 are used to input a UDC address.

Figure 2: Logic Levels to Access the Character RAM



UDC RAM and UDC Address Register

Figure 3 shows the logic levels needed to access the UDC RAM and the UDC Address register. The UDC Address register is 8 bits wide. The lower four bits (D_0 to D_3) select one of the 16 UDC locations. The upper four bits (D_4 to D_7) are not used. When the UDC address has been stored in the UDC Address register, the UDC RAM can be accessed.

To completely specify a 5 × 7 character requires eight write cycles. One cycle stores the UDC RAM address in the UDC Address register. Seven cycles store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 4 shows the organization of a UDC character assuming the symbol to be stored is an "F." A_0 to A_2 select the row to be accessed, and D_0 to D_4 transmit the row dot data. The upper three bits (D_5 to D_7) are ignored. D_0 (least significant bit) corresponds to the right most column of the 5×7 matrix and D_4 (most significant bit) corresponds to the left most column of the 5 × 7 matrix.

Figure 3: Logic Levels to Access a UDC Character

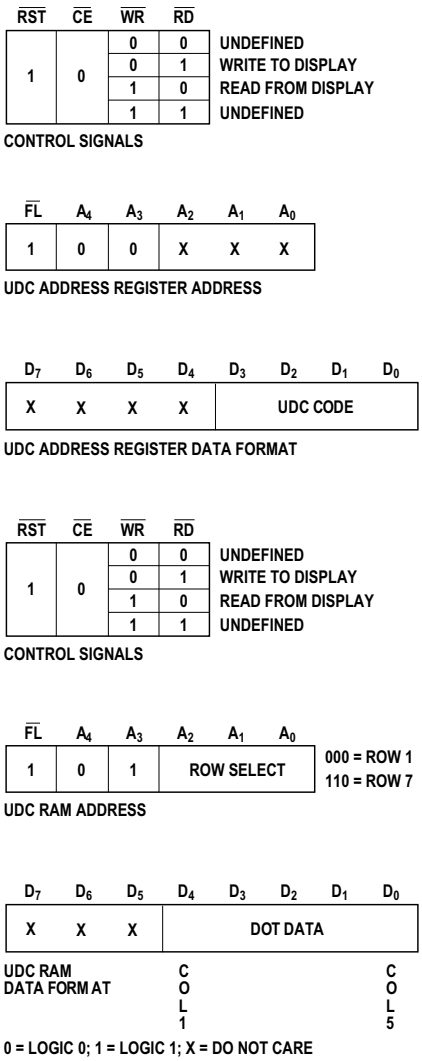
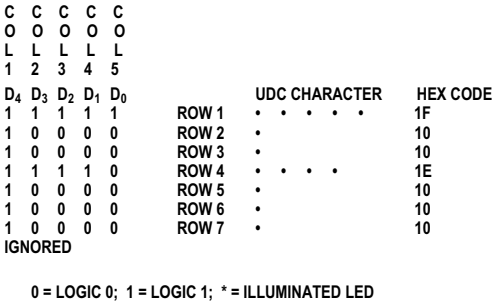


Figure 4: Data to Load "F" into the UDC RAM

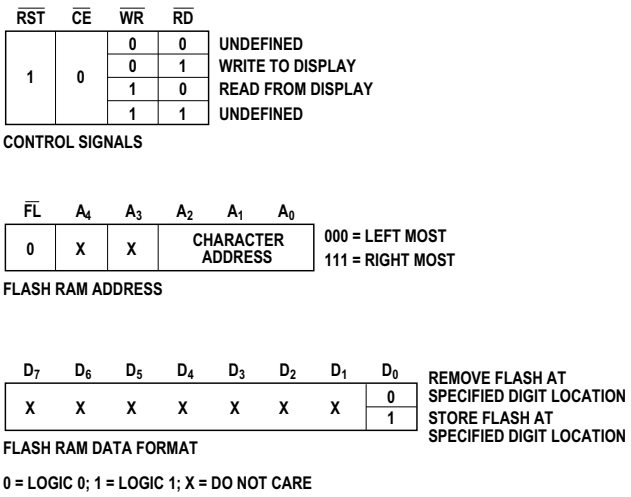


Flash RAM

Figure 5 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input selects the Flash RAM. Address lines A_3 to A_4 are ignored. Address lines A_0 to A_2 select the location in the Flash RAM to store the attribute. D_0 stores or removes the flash attribute. D_0 = "1" stores the attribute, and D_0 = "0" removes the attribute.

When the attribute is enabled through bit 3 of the Control Word and a "1" is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the flash rate can be calculated by dividing the clock frequency by 28,672.

Figure 5: Logic Levels to Access the Flash RAM



Control Word Register

Figure 6 shows how to access the Control Word register. This is an eight bit register that performs five functions. They are brightness control, Flash RAM control, blinking, self-test and clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

Brightness (Bits 0 to 2)

Bits 0 to 2 of the Control Word adjust the brightness of the display. Bits 0 to 2 are interpreted as a three bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0 to 2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 2.

Figure 6: Logic Levels to Access the Control Word Register

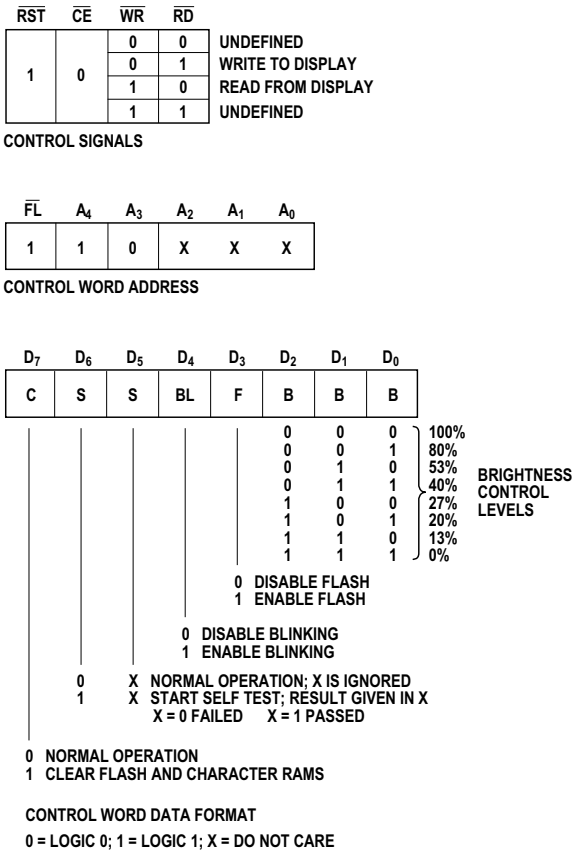


Table 2: Current Requirements at Different Brightness Levels

Symbol	D_2	D_1	D_0	% Brightness	25°C Typ.	Units
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a "1," the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a "1," the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by driving the clock frequency by 28,672. If the flash enable bit of the Control Word is a "0," the content of the Flash RAM is ignored. To use this function with multiple display systems, see Display Reset.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a "1", all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. This function will override the Flash function when it is active. To use this function with multiple display systems see Display Reset.

Self-Test Function (Bits 5, 6)

Bit 6 of the Control Word register initiates the self-test function. Results of the internal self-test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = "1" indicates a passed self test, and bit 5 = "0" indicates a failed self-test.

Setting bit 6 to a logic 1 will start the self-test function. The built-in self-test function of the IC consists of two internal routines that exercise major portions of the IC and illuminates all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to "1." The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self-test function, the display must not be accessed. The time needed to execute the self test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 kHz, then the time to execute the self-test function frequency is equal to (262,144/58,000) = 4.5-second duration.

At the end of the self-test function, the Character RAM is loaded with blanks, the Control Word register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address register is set to all ones.

Clear Function (Bit 7)

Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a “1” will start the clear function. Three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a "0." The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display and the Flash RAM will be loaded with "0"s. The UDC RAM, UDC Address register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 7 shows the logic levels needed to reset the display. The display should be reset on power- up. The external reset clears the Character RAM, Flash RAM, and Control Word and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 µs minimum using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word register are loaded with all "0"s. The UDC RAM and UDC Address register are unaffected. All displays that operate with the same clock source must be simultaneously reset to synchronize the flashing and blinking functions.

Figure 7: Logic Levels to Reset the Display

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4 -A_0	D_7 -D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF $\overline{RST}$, $\overline{CE}$, AND $\overline{WR}$ ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

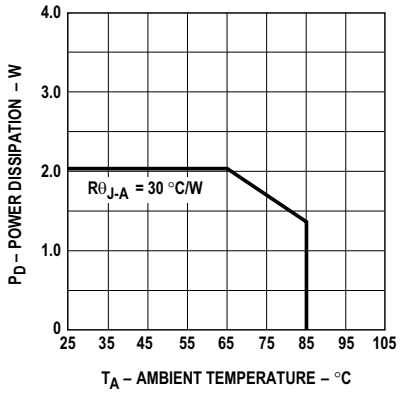
Mechanical and Electrical Considerations

The HDSP-213x/HDSP-2179 is a 32-pin dual-inline package with 24 external pins, that can be stacked horizontally and vertically to create arrays of any size. The HDSP-213x/HDSP-2179 is designed to operate continuously from –55° to +85°C with a maximum of 20 dots ON per character. Illuminating all 35 dots at full brightness is not recommended.

The HDSP-213x/HDSP-2179 is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a ceramic substrate. A glass window is placed over the ceramic substrate creating an air gap over the LED wire bonds. A second glass window creates an air gap over the CMOS IC. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering and visual inspection of the IC.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results, use standard CMOS handling precautions. Prior to use, the HDSP-213X should be stored in antistatic packages or conductive material. During assembly, a grounded conductive work area should be used and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided because they are prone to static charge buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{DD} (V_{IN} > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, connect unused inputs either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display. Transient input voltages should be eliminated.

Figure 8: Maximum Power Dissipation vs. Ambient Temperature Derating Based on T_{JMAX} = 125°C



Thermal Considerations

The HDSP-213x/HDSP-2179 has been designed to provide a low thermal resistance path from the CMOS IC to the 24 package pins. This heat is then typically conducted through the traces of the user's printed circuit board to free air. For most applications, no additional heatsinking is required.

The maximum operating IC junction temperature is 150°C. The maximum IC junction temperature can be calculated using the following equation:

$$T_J(IC)\ MAX = T_A + (P_D MAX)\ (R\theta_{J\text{-}PIN} + R\theta_{PIN\text{-}A})$$

Where

$P_D MAX = (V_{DD} MAX) \times (I_{DD} MAX)$

$I_{DD}MAX$ = 370 mA with 20 dots ON in eight character locations at 25°C ambient. This value is from the Electrical Characteristics table.

$P_D MAX = (5.5V) \times (0.370A)$

$= 2.04W$

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnects between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground that can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from –0.3V to +0.3V with respect to the logic ground. Voltage below –0.3V can cause all dots to be on. Voltage above +0.3V can cause dimming and dot mismatch.

ESD Susceptibility

These displays have ESD susceptibility ratings of CLASS 3 per DOD-STD-1686 and CLASS B per MIL-STD-883C.

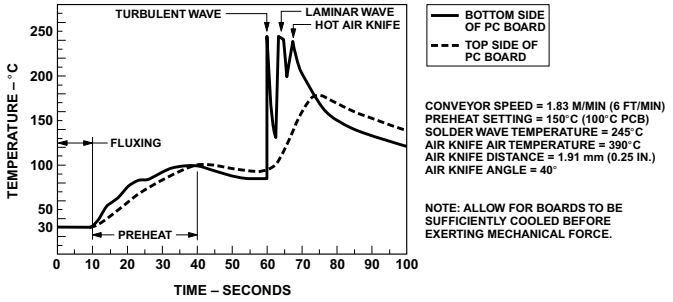
Soldering and Post Solder Cleaning Instructions for the HDSP-213x/HDSP-2179

The HDSP-213x/HDSP-2179 may be hand soldered or wave soldered with lead-free solder. When hand soldering, use an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and dwell in the wave should be set between 1½ to 3 seconds for optimum soldering. The preheat temperature should not exceed 105°C (221°F) as measured on the solder side of the PC board.

Proper handling is imperative to avoid excessive thermal stresses to component when heated. Therefore, the solder PCB must be allowed to cool to room temperature, 25°C, before handling.

For further information on soldering and post solder cleaning, refer to Application Note 1027, *Soldering LED Components*.

Figure 9: Recommended Wave Soldering Profile for Lead-Free Smart Display



Contrast Enhancement

When used with the proper contrast enhancement filters, the HDSP-213x/HDSP-2179 series displays are readable daylight ambients. Refer to Application Note 1029, *Luminous Contrast and Sunlight Readability of the HDSP-235x Series Alphanumeric Displays for Military Applications*, for information on contrast enhancement for daylight ambients. Refer to Application Note 1015, *Contrast Enhancement Techniques for LED Displays*, for information on contrast enhancement in moderate ambients.

Night Vision Lighting

When used with the proper NVG/DV filters, the HDSP-2131, HDSP-2179, and HDSP-2133 may be used in night vision lighting applications. The HDSP-2131 (yellow) and HDSP-2179 (orange) displays are used as master caution and warning indicators. The HDSP-2133 (high performance green) displays are used for general instrumentation. For a list of NVG/DV filters and a discussion on night vision lighting technology, refer to Application Note 1030, *LED*

Displays and Indicators and Night Vision Imaging System Lighting. An external dimming circuit must be used to dim these displays to night vision lighting levels to meet NVIS radiance requirements. Refer to AN 1039, *Dimming HDSP-213x Displays to Meet Night Vision Lighting Levels*.

Intensity Bin Limits

Bin	Intensity Range (mcd)	
	Min.	Max.
G	2.50	4.00
H	3.41	6.01
I	5.12	9.01
J	7.68	13.52
K	11.52	20.28

NOTE: Test conditions as specified in the Optical Characteristics table.

Color Bin Limits

Color	Bin	Color Range (nm)	
		Min.	Max.
Green	1	576.0	580.0
	2	573.0	577.0
	3	570.0	574.0
	4	567.0	571.5
Yellow	3	581.5	585.0
	4	584.0	587.5
	5	586.5	590.0
	6	589.0	592.5

NOTE: Test conditions as specified in the Optical Characteristics table.

Option Code Definition

HDSP-213x- x y z xx

Color Bin Range Identifier	
A	Color Bin 2 or 3
B	Color Bin 4 or 5
C	Color Bin 5 or 6
D	Color Bin 3 or 4
Iv bin Range Identifier	
x	Minimum Iv bin
y	Maximum Iv bin

Packing Information

Products are packed in blister packs as illustrated in Figure 10. Each blister pack contains a maximum 10 units.

Figure 10: Blister Pack for HDSP-213x/2179