SC1104A/B
Simple, Synchronous Voltage Mode PWM Controller

Description

The SC1104A/B is a versatile voltage-mode PWM controller designed for use in single ended DC/DC power supply applications. A simple, fixed frequency high efficiency buck regulator can be implemented using the SC1104A/B with a minimum of external components. Internal level shift and drive circuitry eliminates the need for an expensive P-channel, high-side switch. The small device footprint allows for compact circuit design.

SC1104A/B features include temperature compensated voltage reference, triangle wave oscillator, current limit comparator and an externally compensated error amplifier. Current limit is implemented by sensing the voltage drop across the top FET's $R_{DS(ON)}$.

The SC1104 operates at fixed frequencies of 300kHz(A) or 600kHz(B) providing an optimum compromise between efficiency, external component size, and cost. 600kHz switching frequency is reserved for the SC1104B, $+5V_{CC}$ operation only.

SC1104A/B has a thermal protection circuit, which is activated if the junction temperature exceeds 150°C.

Features

- Up to +14V input, 300kHz operation (SC1104A)
- Up to +7V input, 600kHz operation (SC1104B)
- High efficiency (>90%)
- 1% Reference voltage accuracy
- Hiccup mode over current protection
- Robust output drive
- $R_{DS(ON)}$ Current sensing
- Industrial temperature range
- 8-Lead SOIC package. Pb-free package available, fully WEEE and RoHS compliant

Applications

- Termination supplies
- Low cost microprocessor supplies
- Peripheral card supplies
- Industrial power supplies
- High density DC/DC conversion

Typical Application Circuit

Typical Distributed Power Supply

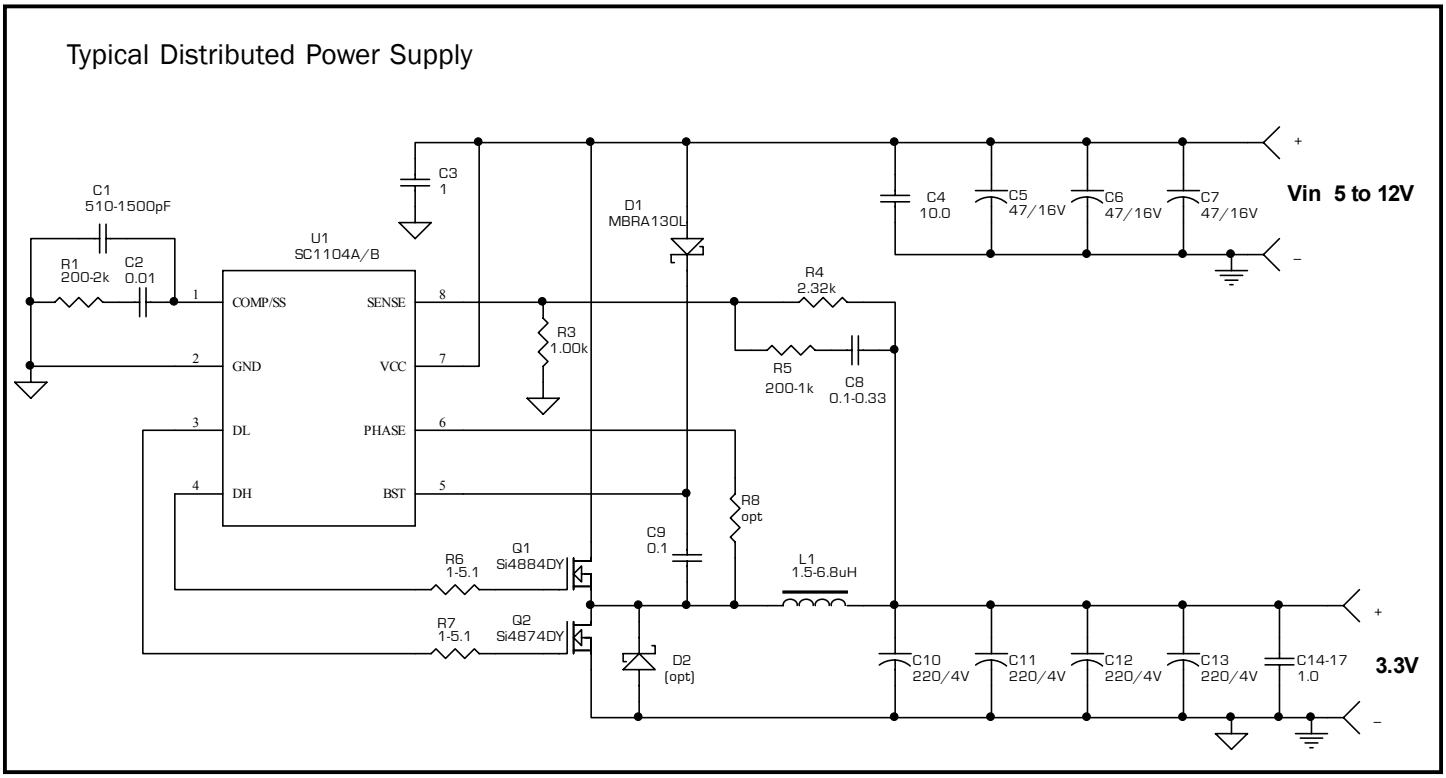


Figure 1

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
V_{CC} to GND		+20	V
BST to PHASE		+20	V
PHASE to GND		-0.5 to +20	V
COMP/SS to GND		+7	V
SENSE to GND		+7	V
Thermal Resistance Junction to Case	θ_{JC}	40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	160	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{Lead}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, $T_J = T_A$ = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, $T_J = T_A$ = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}	F_{SW} = 300kHz (nom.), SC1104A	4.5		14	V
	V_{CC}	F_{SW} = 600kHz (nom.), SC1104B	4.5		7	
Supply Current	I_{CC}	$V_{COMP} \leq 0.4V$		11	14	mA
Error Amplifier						
E/A Transconductance(1)	g_m			12		mS
Open Loop DC Gain(1)	A_O			42		dB
Bandwidth - 3dB(1)	F_{BW}			400		kHz
Input Bias Current	I_{FB}			1	3	µA
Output Sink Current	I_{SIK}	$V_{SENSE} \geq 1.1V$; V_{COMP} = 1.5V	0.65	0.7		mA
Source Current	I_{SC}	$V_{SENSE} \geq 0.9V$; V_{COMP} = 1.5V	0.95	1.1		
Oscillator						
Switching Frequency	F_{OSC}	V_{CC} = 12V ± 0.6V	255	300	345	kHz
		V_{CC} = 5V ± 0.25V	510	600	690	

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, $T_J = T_A$ = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, $T_J = T_A$ = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Ramp Peak Voltage(1)	V_{P-K}	4.75V ≤ V_{CC} ≤ 12.6V		2.0		V
Ramp Valley Voltage(1)	V_V	4.75V ≤ V_{CC} ≤ 12.6V		1.0		V
Maximum Duty Cycle(2)	dc_{MAX}	V_{CC} = 12V (300kHz, SC1104A)	90	95		%
		V_{CC} = 5V (600kHz, SC1104B)	85	90		
MOSFET Drivers						
DH Sink/Source Current SC1104A	I_{DH}	d.c. < 2%, t_{PW} < 100µs V_{GS} = 4.5V (src)	0.6	0.8		A
DL Sink/Source Current SC1104A	I_{DL}	V_{GS} = 2.5V (snk)	0.6	0.7		
DH Sink/Source Current SC1104B	I_{DH}	d.c. < 2%, t_{PW} < 100µs V_{GS} = 4.5V (src)	0.45	0.6		A
DL Sink/Source Current SC1104B	I_{DL}	V_{GS} = 2.5V (snk)	0.45	0.6		
DH Rise/Fall Time	tr, tf	C_L = 3000pF, See Fig. 2		50		ns
DL Rise/Fall Time	tr, tf	C_L = 4000pF, See Fig. 2		50		
Dead Time	t_{dt}	See Fig. 2		80		ns
DH Minimum Off Time	t_{OFF}	4.75V ≤ Vcc ≤ 12.6V		160		
Reference Section						
Reference Voltage	V_{REF}	4.75V ≤ Vcc ≤ 12.6V	0.990	1.000	1.010	V
Temp Variance	ΔV_{REF}	0 < T_J < +70°C	-1		1	%
		-40 < T_J < +85°C	-1.5		1.5	
Long Term Stability		T_J = 125°C, 1000 hrs.			5	mV
Current Limit						
Trip Voltage	V_{TRIP}	4.75V < Vcc < 12.6V V_{trp} = Vcc - V_{PHASE}	180	200	220	mV
Soft-Start/Enable						
SS Source Current	I_{SRC}	V_{COMP} < 2.5V	0.5		1.8	µA
SS Sink Current	I_{SNK}	V_{COMP} > 0.5V	0.5		1.8	µA
Enable Input Threshold			1.00		1.35	V
Enable Input Current		V_{COMP} = 0.8V			2	mA

Electrical Characteristics

Unless specified: **A:** V_{CC} = 12 ± 0.6V, V_{BST} = 23 ± 1V, V_{OUT} = 3.3V, T_J = T_A = 25°C. **B:** V_{CC} = 5 ± 0.25V, V_{BST} = 12 ± 0.6V, V_{OUT} = 2.0V, T_J = T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under Voltage Lockout						
UVLO Threshold	V_{th}	-40 < T_J < 85°C	3.9	4.15	4.5	V
Thermal Shutdown						
Over Temperature Trip Point(2)	T_{OTP}		140		160	°C

Notes:
(1) Guaranteed by design.
(2) Not tested, by characterization.

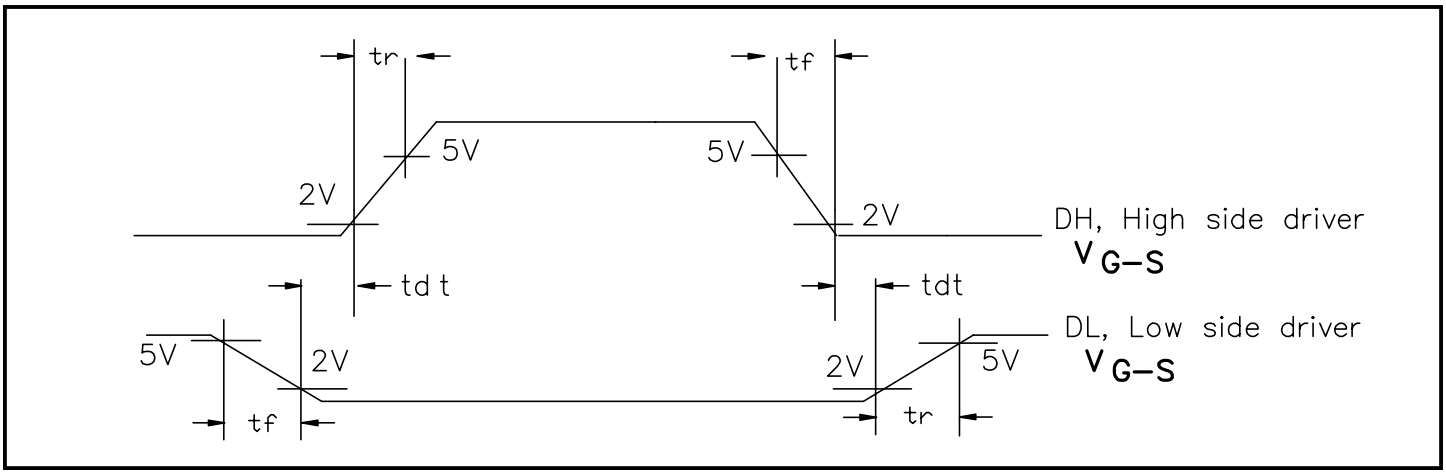


Figure 2

Block Diagram

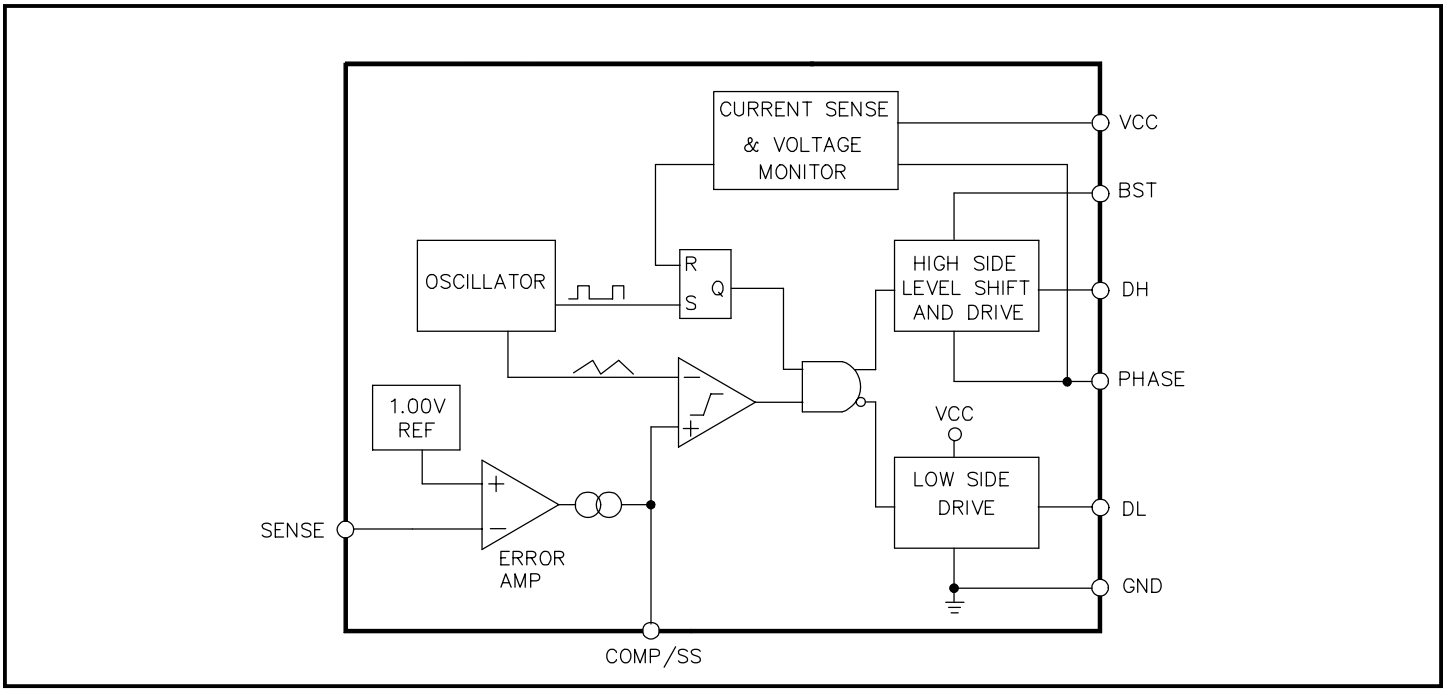
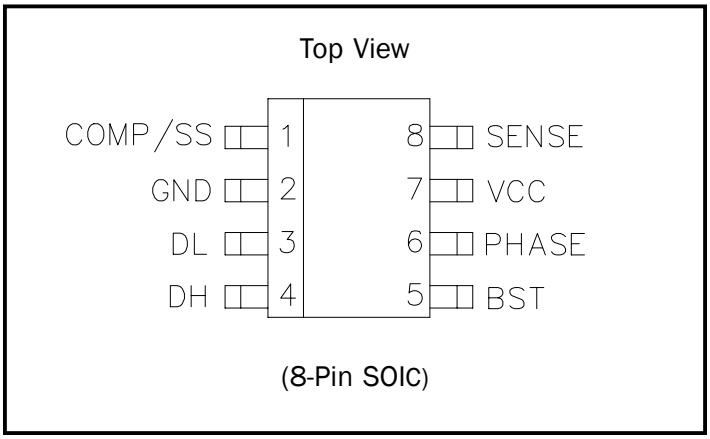


Figure 3

Pin Configuration



(8-Pin SOIC)

Ordering Information

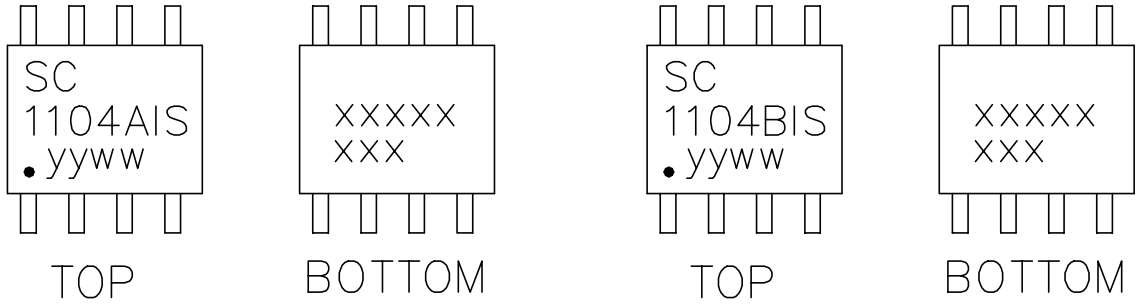
Device (2)	Package	Temp Range (T_J)
SC1104XISTR (1)	SOIC-8	-40° to 125°C
SC1104XISTRT (1)(3)		
SC1104XEVB	Evaluation Board	

Notes:
(1) In place of "X": A = 300kHz, V_{CC} = 5V to 12V.
B = 600kHz, V_{CC} = 5V.
(2) Only available in tape and reel packaging. A reel contains 2500 devices.
(3) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	COMP/SS	Error amplifier output. Compensation, soft start/enable.
2	GND	Ground.
3	DL	Low side driver output
4	DH	High side driver output
5	BST	Bootstrap, high side driver.
6	PHASE	Input from the phase node between the MOSFETs.
7	VCC	Chip bias supply voltage.
8	SENSE	Output voltage sense input.

Marking Information



yyww = Date Code (Example: 0012)
xxxxxxx = Semtech Lot No. (Example: E90101-1)

Theory of Operation

Synchronous Buck Converter

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The inverting input of the error amplifier receives its voltage from the SENSE pin. The non-inverting input of the error amplifier is connected to an internal 1V reference.

The error amplifier output is connected to the COMPensation pin. The error amplifier generates a current proportional to (Vsense – 1V), which is the COMP pin output current (Transconductance ~ 12mS). The voltage on the COMP pin is the integral of the error amplifier current. The COMP voltage is the non-inverting input to the PWM comparator and controls the duty cycle of the MOSFET drivers. The size of capacitor Ccomp controls the stability and transient response of the regulator. The larger the capacitor, the slower the COMP voltage changes, and the slower the duty cycle changes.

The inverting input voltage of the PWM comparator is the triangular output of the oscillator.

When the oscillator output voltage drops below the COMP voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET. After a short delay ("dead time"), DH is pulled high, turning on the high-side FET. When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and after a dead time delay, DL is pulled high, turning on the low-side FET. The dead time delay is determined by a monostable on the chip.

The triangle wave minimum is about 1V, and the maximum is about 2V. Thus, if Vcomp = 0.9V, high side duty cycle is the minimum (~0%) , but if Vcomp is 2.0V, duty cycle is at maximum (~90%).The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 300kHz (SC1104A) or 600kHz (SC1104B).

Figure 1 shows a 3.3V output converter. If the Vout <3.3V, then the SENSE voltage < 1V. In this case the error amplifier will be sourcing current into the COMP pin so that COMP voltage and duty cycle will gradually increase. If Vout > 3.3V, the error amplifier will sink current and reduce the COMP voltage, so that duty cycle will decrease.

The circuit will be in steady state when Vout =3.3V , Vsense = 1V, Icomp = 0 . The COMP voltage and duty cycle depend on Vin.

Under Voltage Lockout

The under voltage lockout circuit of the SC1104A/B assures that both high-side and low-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.2V typ.

$R_{DS(ON)}$ Current Limiting

In case of a short circuit or overload, the high-side (HS) FET will conduct large currents. To prevent damage, in this situation, large currents will generate a fault condition and begin a soft start cycle.

While the HS driver is on, the phase voltage is compared to the Vcc pin voltage. If the phase voltage is 200mV lower than Vcc, a fault is latched and the soft start cycle begins.

The voltages are compared during the middle of the HS pulse, to prevent transients from affecting the accuracy.

The sampling of the voltage across the top FET occurs after a time delay t_{DELAY} = 100ns_typ from the time the DH is pulled high. This delay prevents the measurement to be effected by ringing on the leading edge of the phase node pulse. The duration of the sampling is t_{SAMPLE} = 100ns_typ. It is being disabled at very low duty cycle when t_{ON} < 300ns_typ. This feature allows for the orderly start-up during the inrush of the current charging output capacitor and the fault free operation with extremely high input/output voltage ratio, e.g., V_{IN} = 12V and V_{OUT} = 1V.

The over-current comparator (OC) is only active if the phase node is > 3.3V. This means that in the case of power source being < 3V the OC will be disabled even though the rest of the circuitry is completely functional. SC1104 still can be used for stepping down, e.g. 2.8V to 2.5V, 2V, 1.8V, etc.

Theory of Operation (Cont.)

When choosing OC trip point one should consider the Tempco of the MOSFETs Rds_on and SC1104's Vtrip. Also, any ringing on the Vcc and Phase nodes due to parasitic L and C will have some effect on the OC Vtrip.

Example:

Iout_nom = 6A; assume I_max = 125% • Iout_nom = 7.5A

Rds_on = 0.014Ω; assume Rds_on_max ≈ 150% • Rds_on = 0.02Ω

Voc = 7.5A • 0.02Ω = 150mV.

This proves that MOSFETs with R_{DS_ON} = 0.014Ω @ 25°C is the right choice.

Soft Start

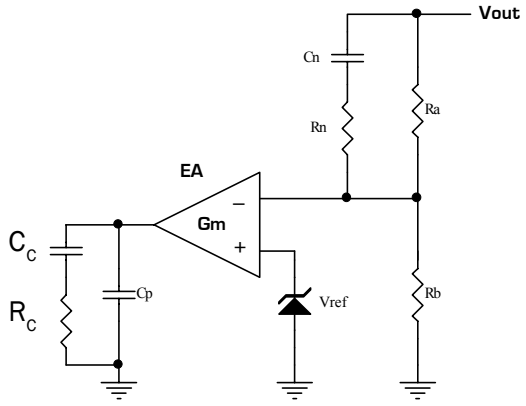
The soft start (or hiccup) circuitry is activated when a fault occurs. Faults occur for three reasons:

1) Under voltage (V_{CC} < 4.2V)
2) Over temperature (die temperature > 150°C)
3) Over current in high side FET.

All faults are handled the same way. Both DH and DL are forced low. The error amplifier is turned off, but a 2µA current flows into the comp pin (soft start current). The sink current reduces the Comp voltage down to 0.6V over a period of a few milliseconds. When Vcomp ~ 0.6V, the fault is cleared and the DL goes high. Also, the soft start current changes polarity and begins to increase the voltage on the Comp capacitor. The DH remains low, because Vcomp is less than the lowest excursion of the oscillator ramp (1.0V). After a few ms, the Vcomp increases to about 1.0V and the DH will start to switch. The duty cycle will gradually increase, and Vsns will increase. When Vsns ~ 1.00V, the error amplifier turns on again. The circuit has now reached its operating point. If a fault occurs during the soft start, the cycle will begin again (drivers low, Vcomp decreasing down to 0.6V).

Closing the Loop

In order to have a stable closed loop system with optimum transient response one should make sure that open-loop frequency response has an adequate Gain & Phase margins. The Bode plot of log. Gain vs Freq. and Phase vs Freq. provide the necessary means for the circuit evaluation. Loop stability defined by compensation networks around transconductance error amplifier (EA) and output divider, see below and output capacitor Cout and inductor Lout.



Typical transconductance error amplifier

The inductor and output capacitor form a "double pole" at the frequency:

$$f_{LC} = \frac{1}{2 \bullet \prod \bullet \sqrt{Lo \bullet Co}}$$

The ESR of the output capacitor and the output capacitor value create a "zero" at the frequency.

$$f_{ESR} = \frac{1}{2 \bullet \prod \bullet ESR \bullet Co}$$

The "zero" and "pole" from the EA compensation network are:

$$f_Z = \frac{1}{2 \bullet \prod \bullet Rc \bullet Cc} \qquad f_P = \frac{1}{2 \bullet \prod \bullet Rc \bullet Cp}$$

The additional "lead" network R_A, C_N, R_N can be used to improve phase margin in case when output capacitors with extra-low ESR are used and there is a need to compensate for "high quality" output Lo, Co filter.

Theory of Operation (Cont.)

$$f_{NET} = \frac{1}{2 \bullet \prod \bullet Ra \bullet Cn}$$

Value for the resistor R_N should be 1/10 of the output divider upper resistor R_A.

Example.
Switching frequency f_{SW} = 300kHz
Output capacitance C_{OUT} = 3 x 330µF
Output capacitor ESR = 45mΩ/each
Output inductance L_{OUT} = 4.7µH
Input voltage V_{IN} = 12V
Output voltage V_{OUT} = 3.3V

Let's choose crossover frequency
$f_{CO} = 1/20 \bullet f_{SW}$ = 15kHz

The compensation values used in this example are based on the following criteria:

$f_Z = f_{LC}$; $f_{NET} = 1/10 \bullet f_{LC}$; $f_P = 10 \bullet f_{CO}$ = 150kHz

Therefore,

$$f_{LC} = \frac{1}{2 \bullet \prod \bullet \sqrt{4.7\mu H \bullet 990\mu F}} = 2.33kHz$$

$$f_{ESR} = \frac{1}{2 \bullet \prod \bullet 0.015 \bullet 990\mu F} = 10.72kHz$$

Since, the EA can sink/source about 1mA, let's choose Rc = 680Ω, then

$$C_C = \frac{1}{2 \bullet \prod \bullet Fz \bullet Rc} = 0.1\mu F$$

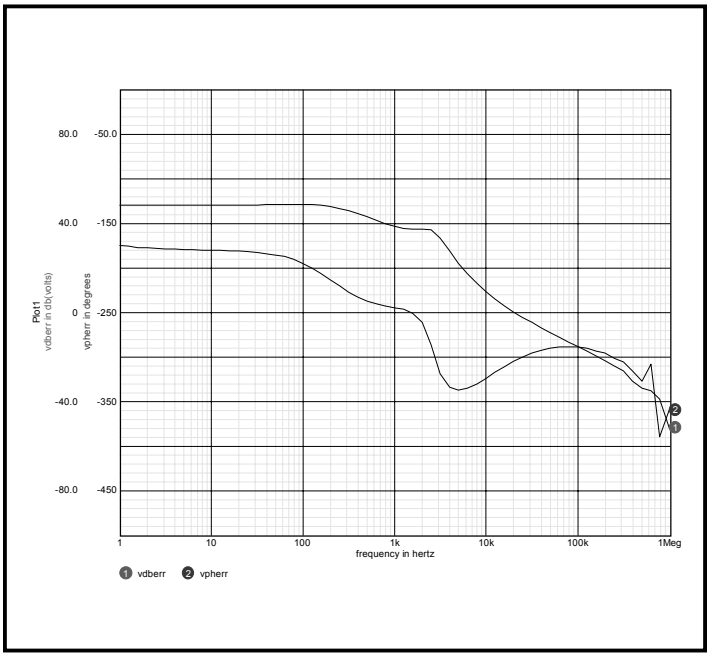
$$C_P = \frac{1}{2 \bullet \prod \bullet Fp \bullet Rc} = 1500pF$$

Assuming the output divider lower resistor R_B = 1k, then for V_{OUT} = 3.3V the R_A = 2.32k.

$$C_N = \frac{1}{2 \bullet \prod \bullet f_{NET} \bullet Ra} = 0.3\mu F$$

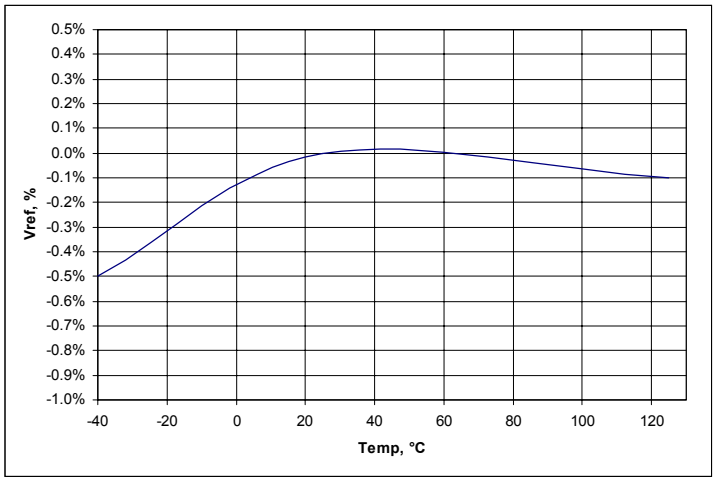
At the closed-loop crossover frequency f_{CO}, the attenuation due to the L_O, C_O filter and the output resistor divider R_A, R_B is compensated by the gain of the PWM modulator and the gain of the transconductance error amplifier ($Gm_{EA} \bullet Z_{COMP}$).

Shown below is a typical Bode plot of the open-loop frequency response of SC1104 based buck converter.

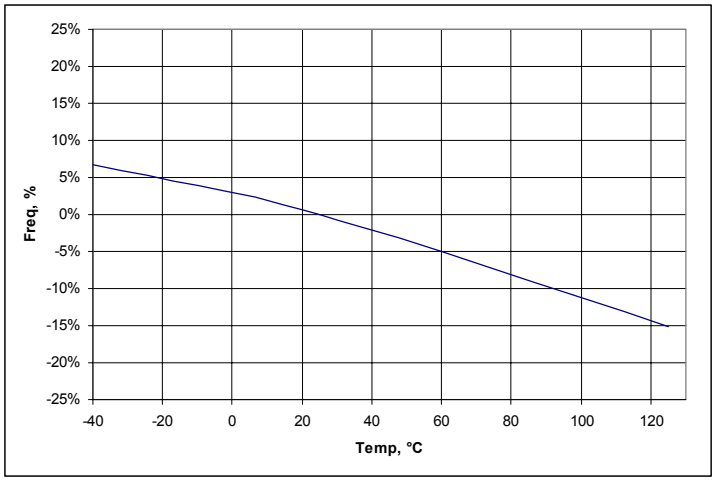


Typical Characteristics

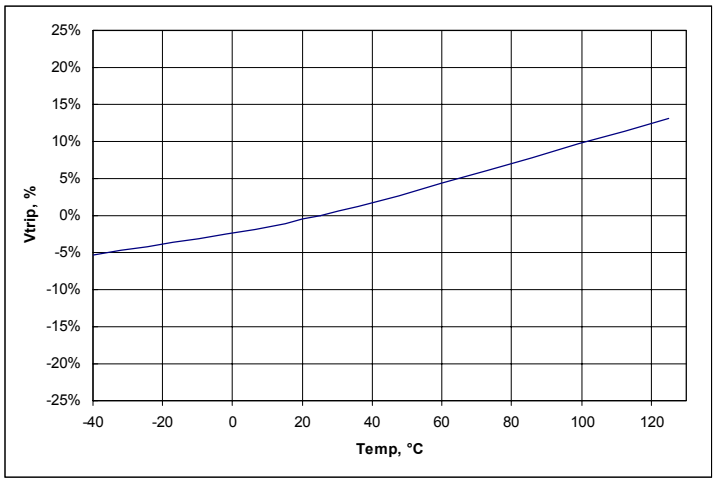
Reference Voltage vs. Temp



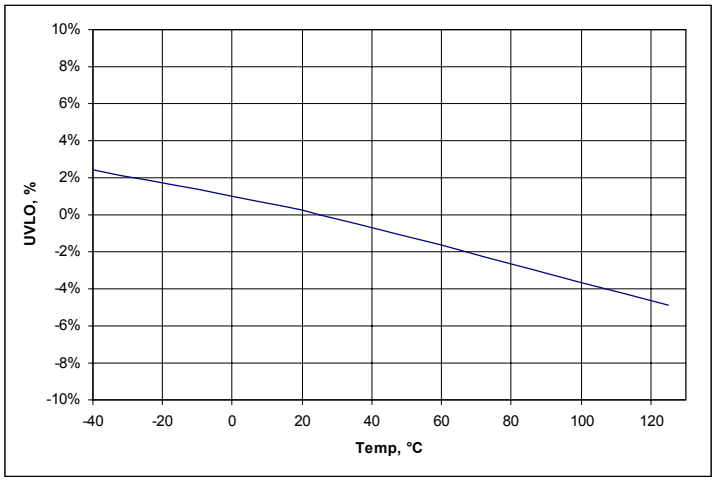
Switching Frequency vs. Temp



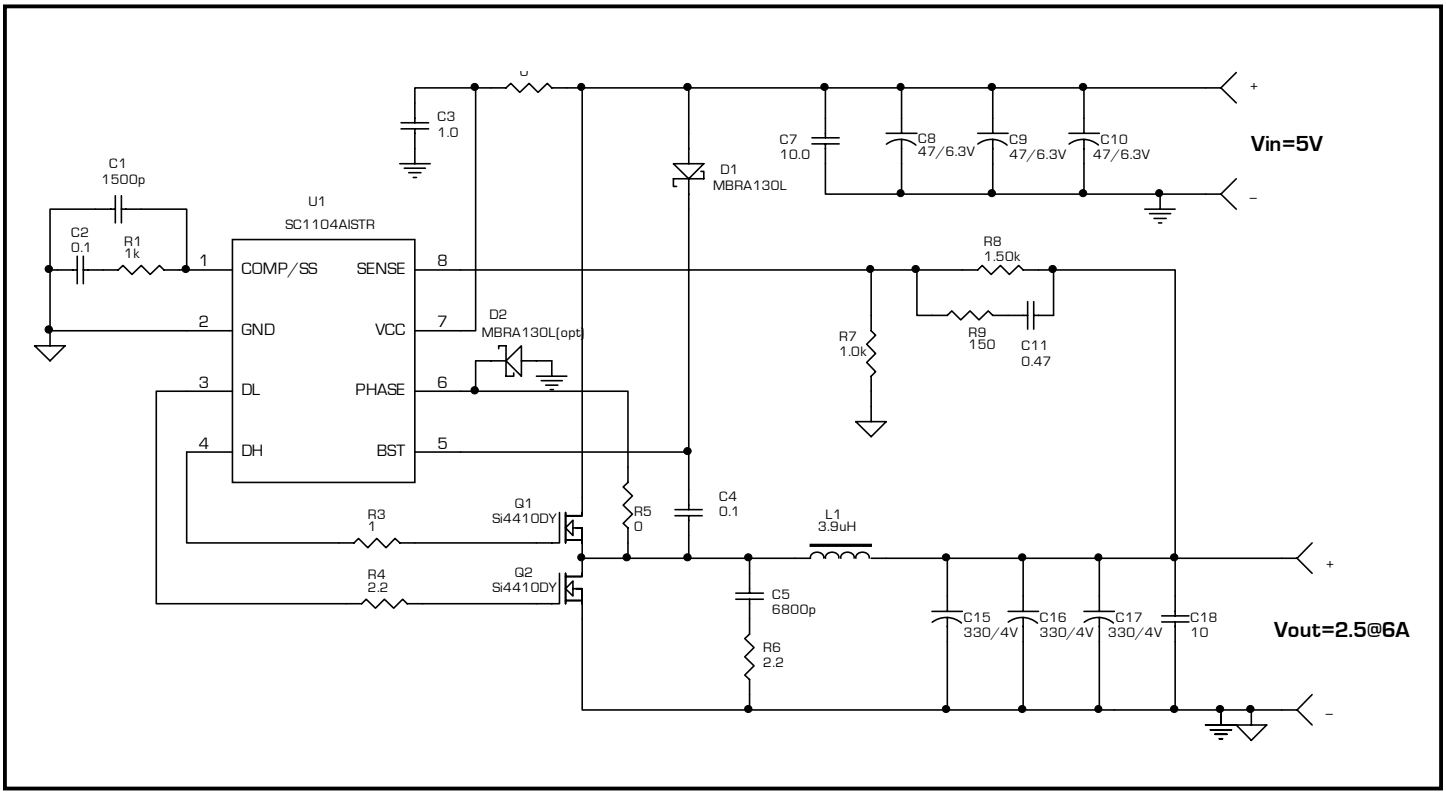
Trip Voltage vs. Temp



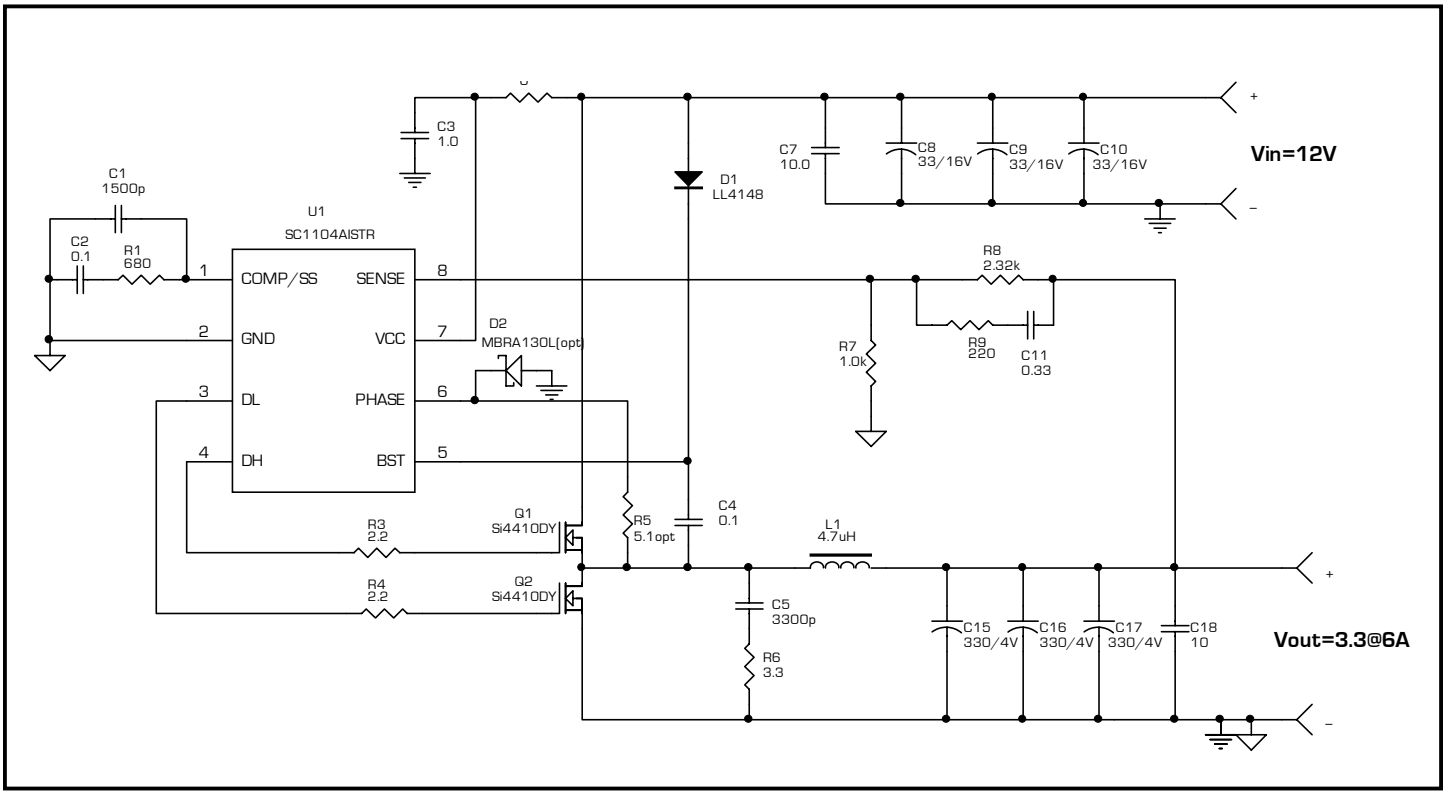
Under Voltage Lockout vs. Temp



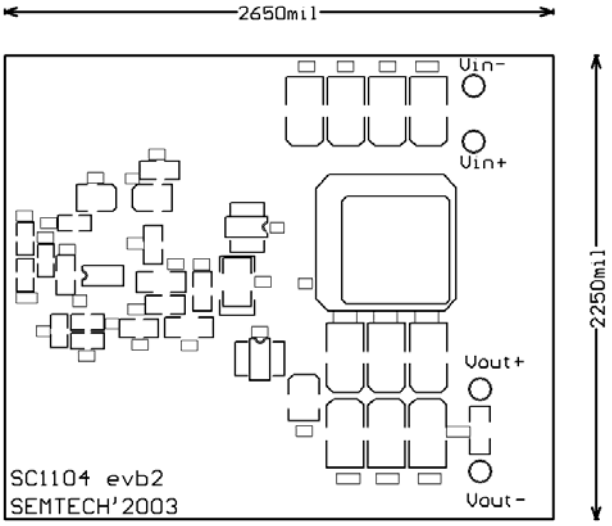
Evaluation Board Schematic - V_{IN} = 5V



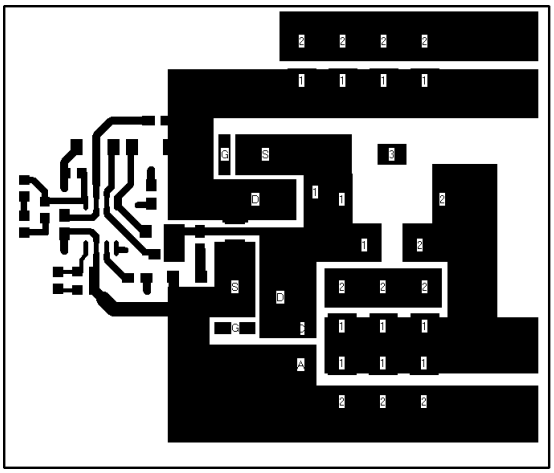
Evaluation Board Schematic - V_{IN} = 12V



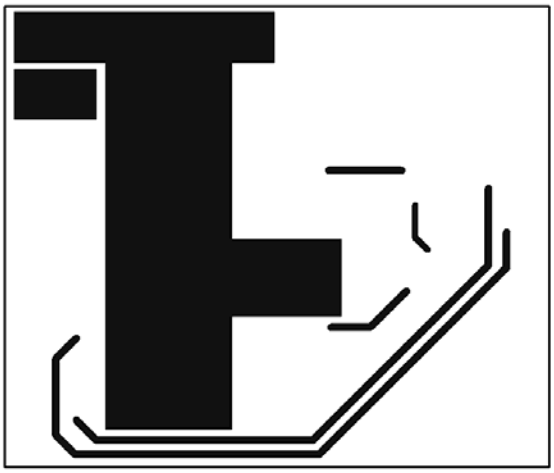
Evaluation PC Board



Top View

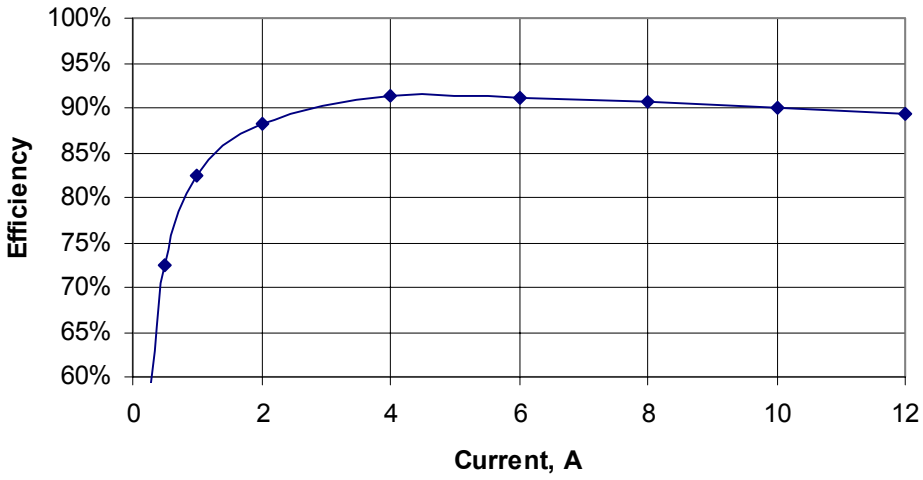


Top Layer

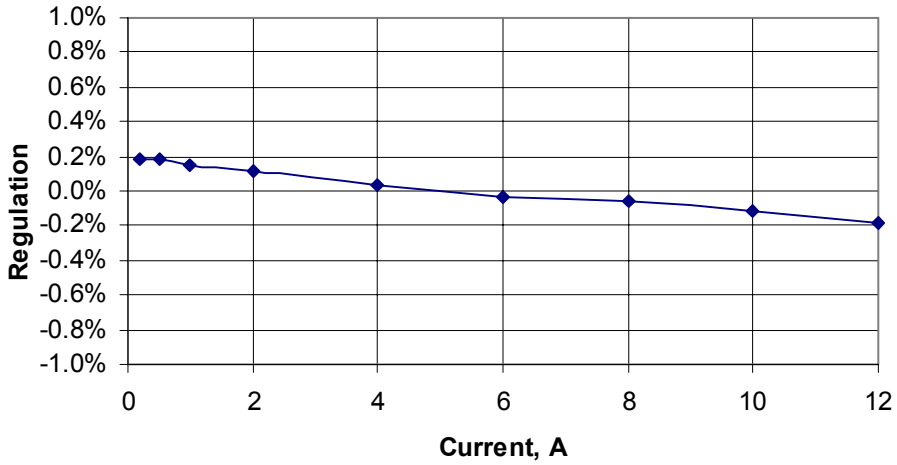


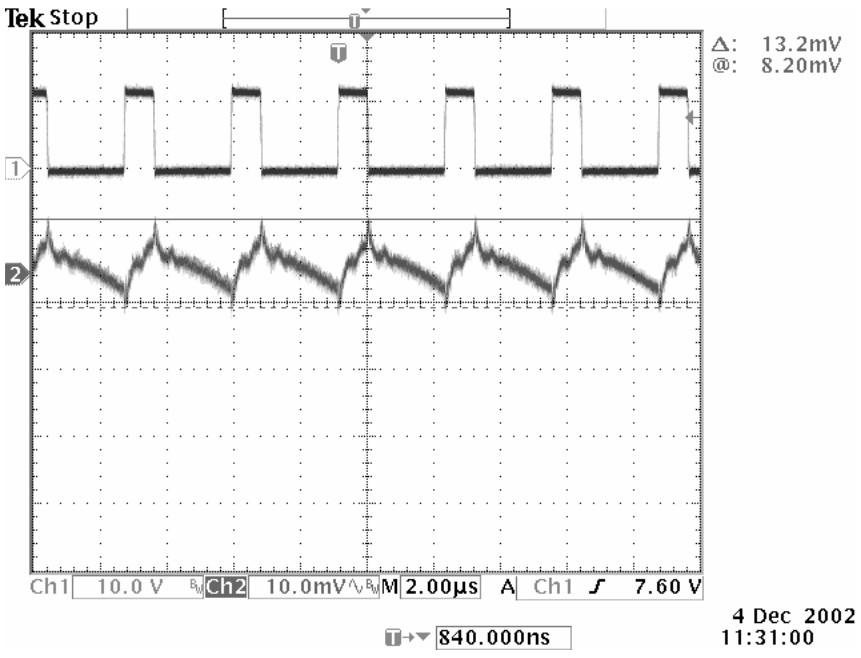
Bottom Layer

Typical Characteristics

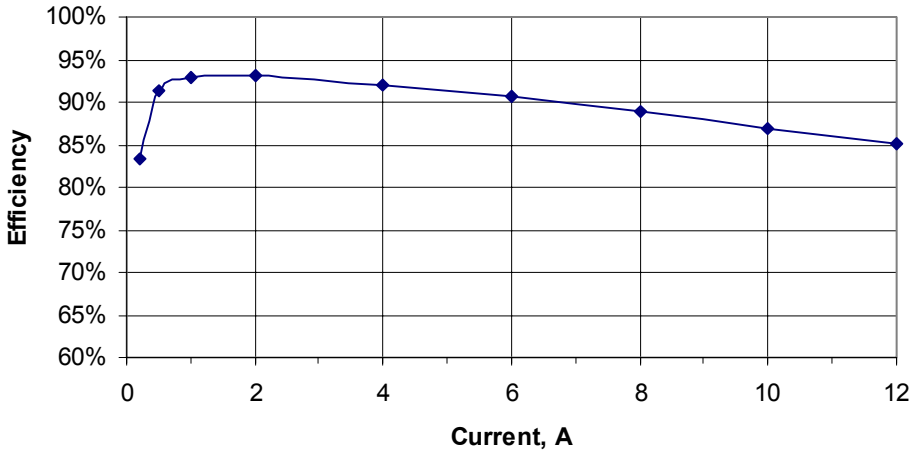


12V = Vin
3.3V = Vout
12A = Iout

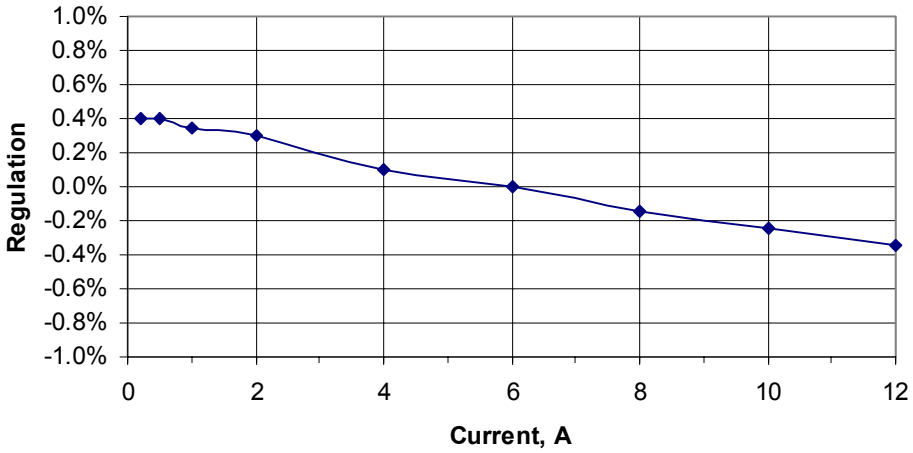


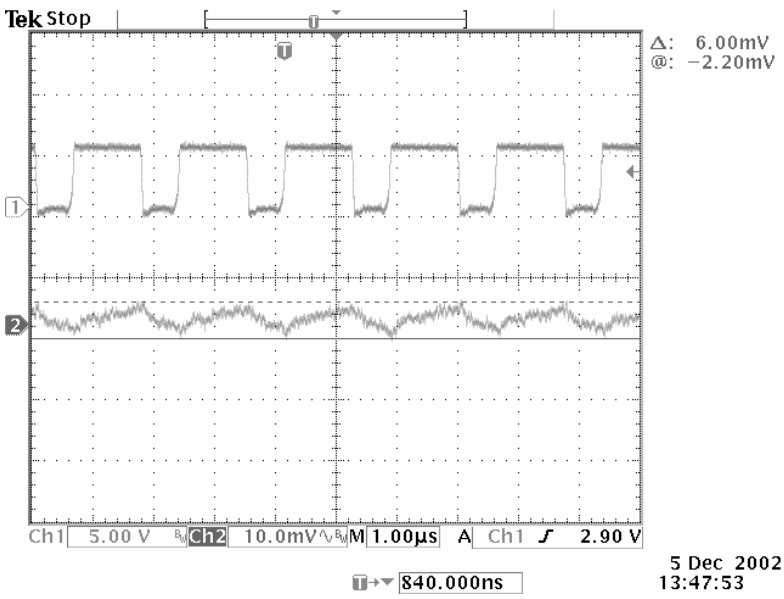


Typical Characteristics (Cont.)

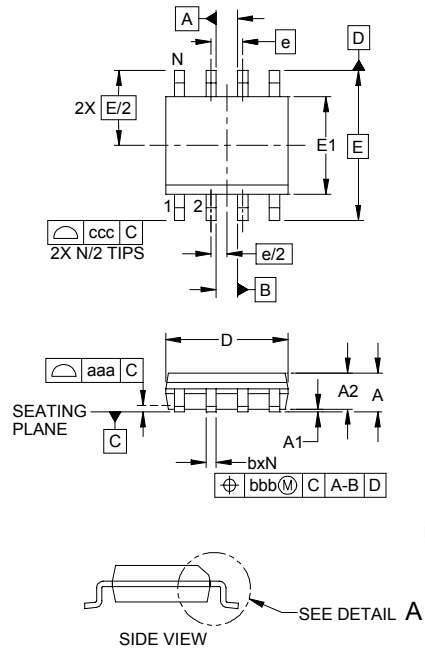


5V = Vin
2V = Vout
12A = Iout





Outline Drawing - SOIC - 8

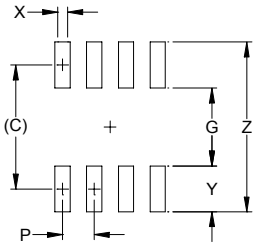


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Minimum Land Pattern - SOIC - 8



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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