

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	R_{DS(on)}	4.4 mΩ
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Current	122 A	Q_G (TYP)	40.5 nC
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Feature

- $R_{DS(ON)} < 4.4 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- $R_{DS(ON)} < 6.5 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 25 \text{ A}$
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

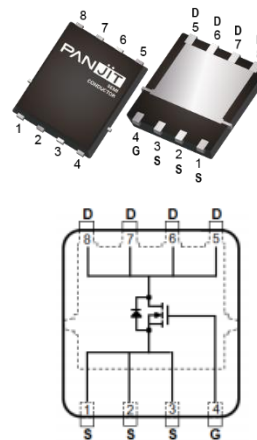
Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.08 grams

Application

- SR solutions of PD Charger, Brick Power, 48V DC/DC converter

DFN5060-8L



Top side view

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 3)	$T_C = 25^\circ\text{C}$	I_D	122	A
	$T_C = 100^\circ\text{C}$		77	
Pulsed Drain Current	$T_C = 25^\circ\text{C}$	I_{DM}	488	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	50	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	318	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	125	W
	$T_C = 100^\circ\text{C}$		50	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$

Thermal Characteristics

PARAMETER		SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=270\text{ }\mu\text{A}$	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	3.8	4.4	m Ω
		$V_{GS}=6\text{ V}, I_D=25\text{ A}$	-	5.0	6.5	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{ V}$	-	-	± 100	nA
Transfer characteristics (Note 1)	g_{fs}	$V_{DS}=10\text{ V}, I_D=50\text{ A}$	-	105	-	S
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=50\text{ V}, I_D=50\text{ A},$ $V_{GS}=10\text{ V}$	-	40.5	53	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Gate Plateau Voltage	$V_{plateau}$		-	5	-	V
Input Capacitance	C_{iss}	$V_{DS}=50\text{ V}, V_{GS}=0\text{ V},$ $f=250\text{ kHz}$	-	3010	3910	pF
Output Capacitance	C_{oss}		-	1080	1400	
Reverse Transfer Capacitance	C_{rss}		-	14	-	
Output Charge	Q_{oss}	$V_{DS}=50\text{ V}, V_{GS}=0\text{ V}$	-	85	110	nC
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=50\text{ V}, I_D=50\text{ A},$ $V_{GS}=10\text{ V}, R_G=6.0\text{ }\Omega$ (Note 2)	-	11	-	ns
Rise Time	t_r		-	6	-	
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	
Fall Time	t_f		-	8	-	
Gate Resistance	R_g	$f=1.0\text{ MHz}$	-	0.8	1.6	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	$I_S=50\text{ A}, V_{GS}=0\text{ V}$	-	0.9	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F=50\text{ A}, V_{DD}=50\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$	-	85	-	nC
Reverse Recovery Time	T_{rr}		-	56	-	ns

NOTES :

1. Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of $L = 1.0\text{ mH}$, $I_{AS} = 25.2\text{ A}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 50\text{ A}$ in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

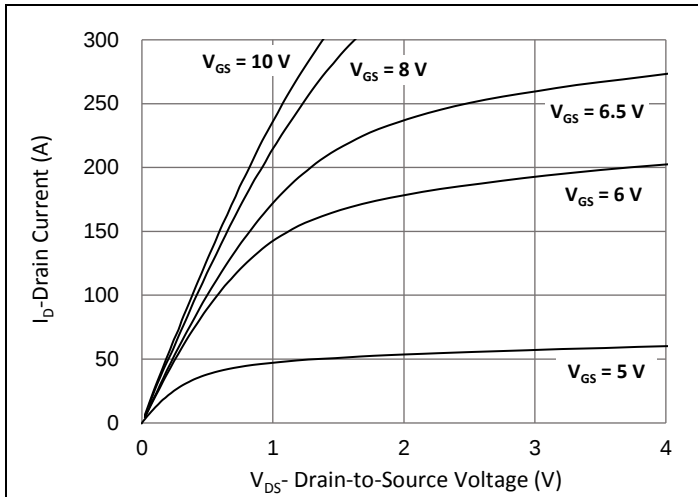


Fig.1 Output Characteristics

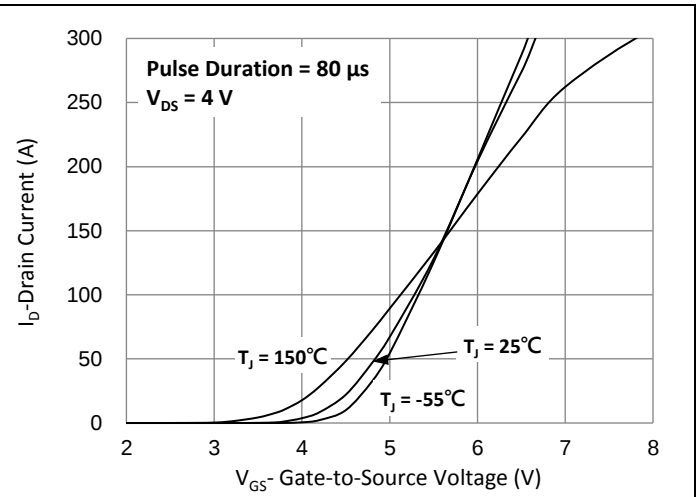


Fig.2 Transfer Characteristics

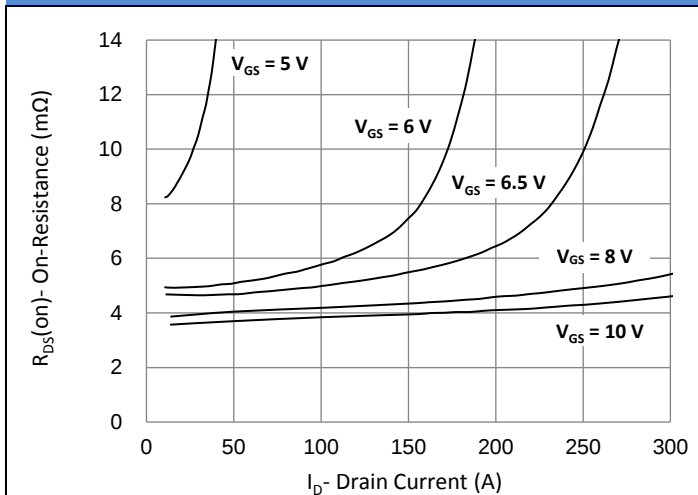


Fig.3 On-Resistance vs. Drain Current

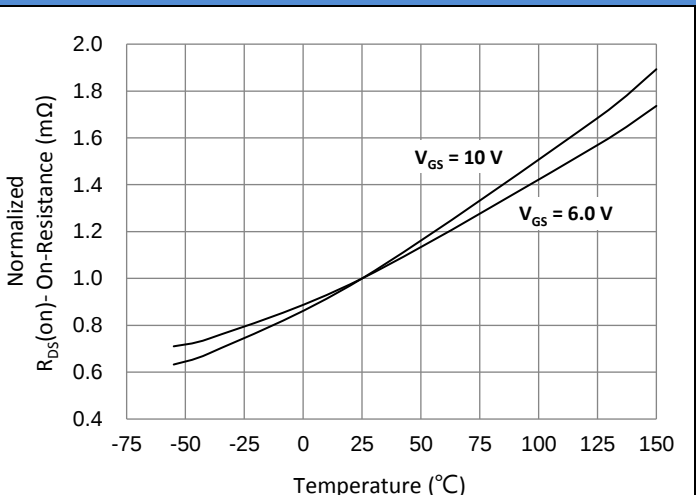


Fig.4 On-Resistance vs. Junction temperature

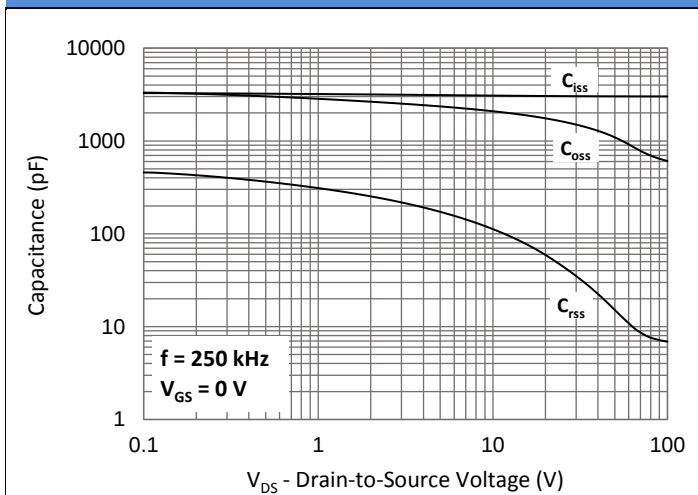


Fig.5 Capacitance vs. Drain-Source Voltage

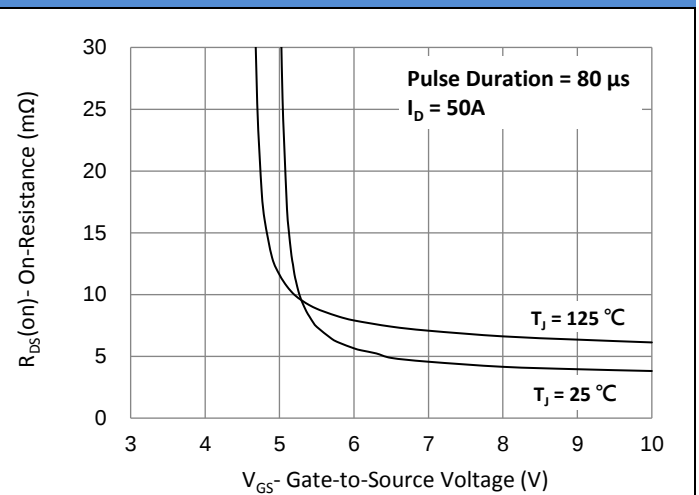


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

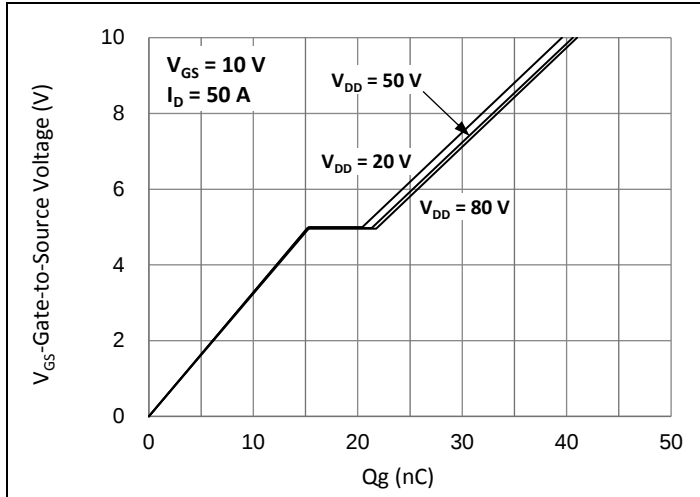


Fig.7 Gate-Charge Characteristics

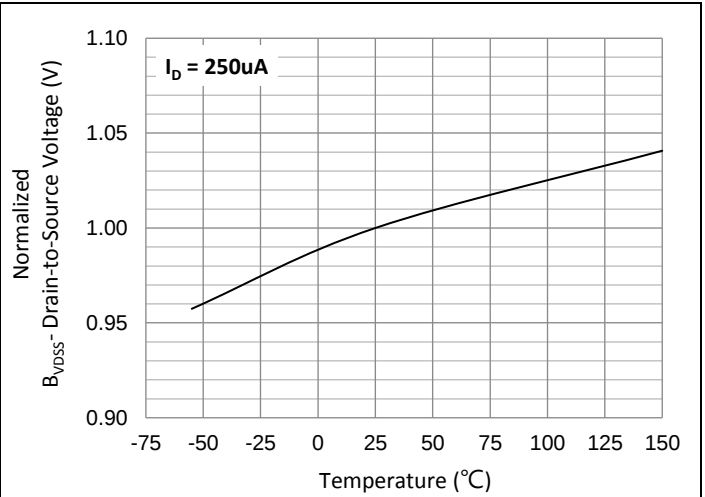


Fig.8 Breakdown Voltage Variation vs. Temperature

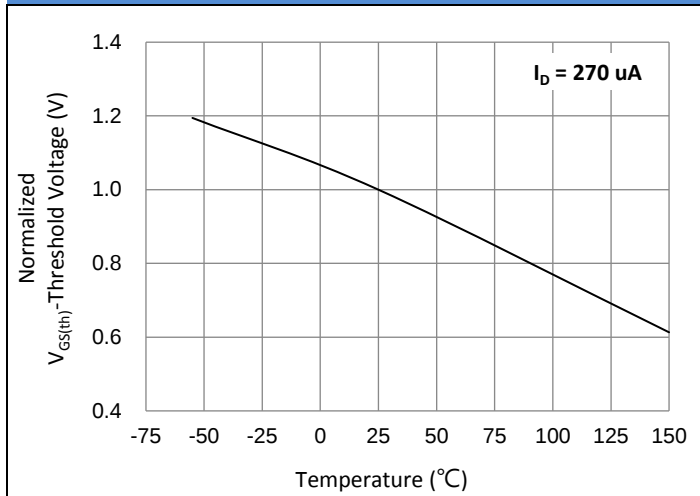


Fig.9 Threshold Voltage Variation with Temperature

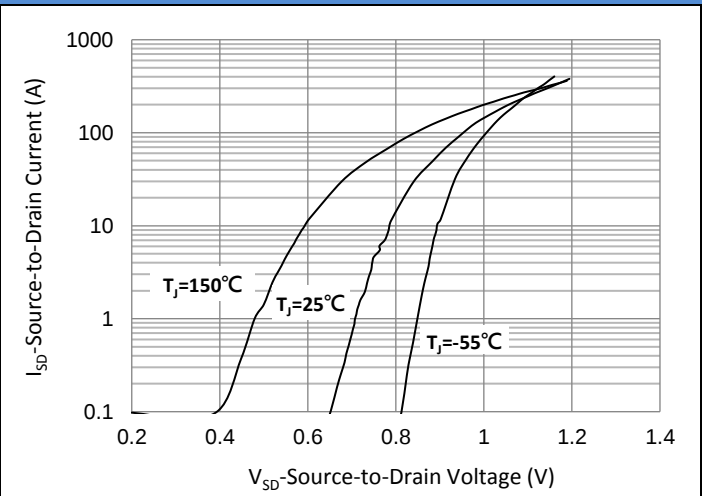


Fig.10 Source-Drain Diode Forward Voltage

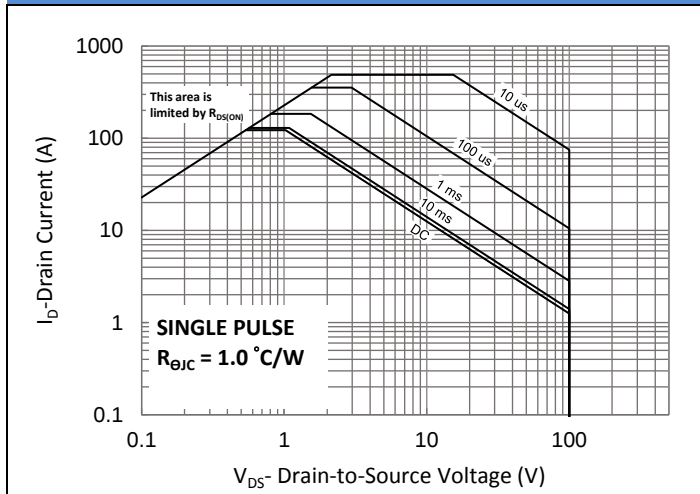


Fig.11 Maximum Safe Operating Area

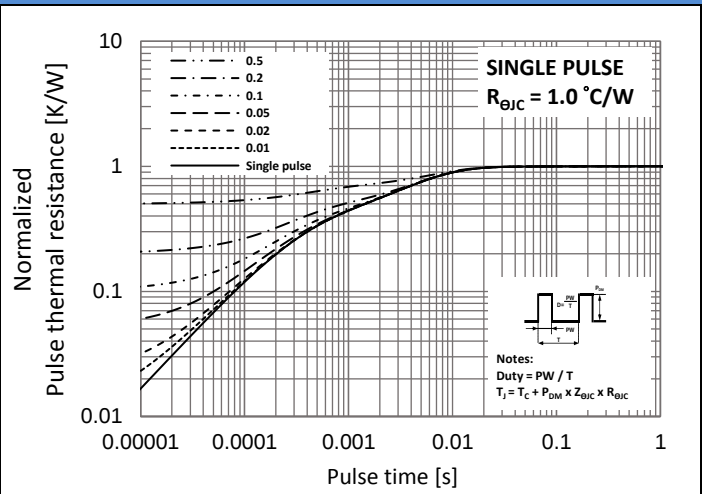


Fig.12 Normalized Transient Thermal Impedance

TYPICAL CHARACTERISTIC CURVES

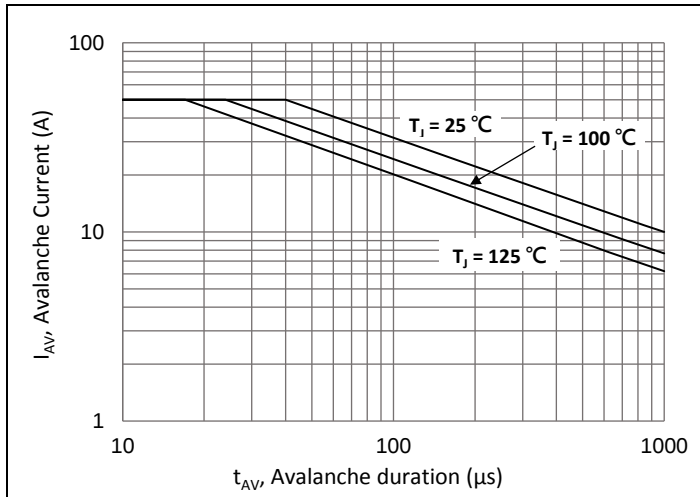


Fig.13 Avalanche Characteristics

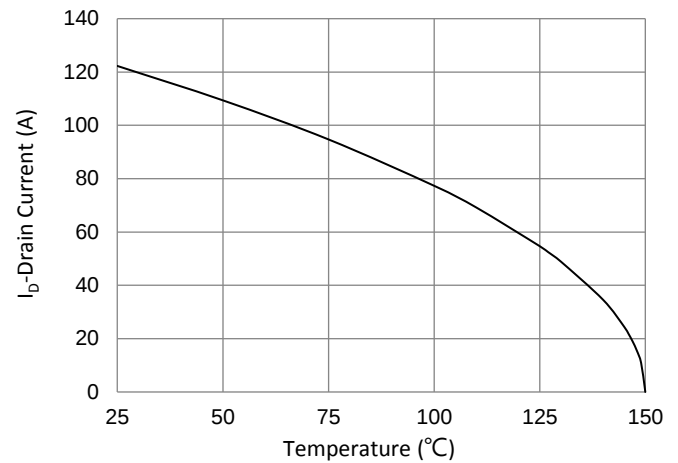
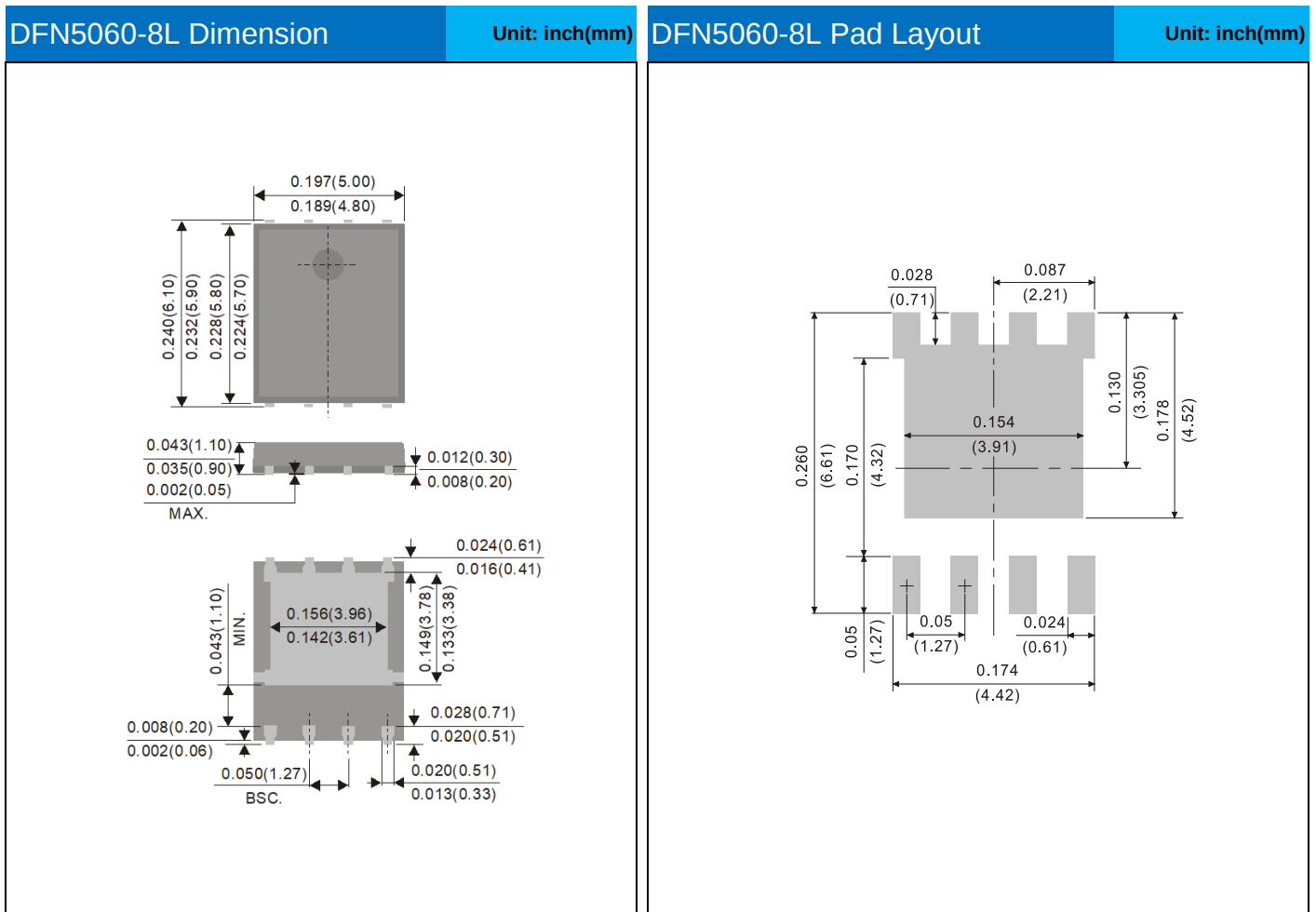


Fig.14 Drain Current vs. Case Temperature

Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PSMQC040N10NS2	DFN5060-8L	3000pcs / 13" reel	040N10NS

Packaging Information & Mounting Pad Layout



Marking Diagram

PJ	Y = Year Code
040N10NS	W = Week Code (A~Z)
YWLL x	LL = Lot Code (00~99)
	x = Production Line Code

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