MOSFET - Power, Single, **N-Channel** 60 V, 10.7 mΩ, 50 A

NVMFS5C673N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C673NWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	٧
Gate-to-Source Voltage			V _{GS}	±20	٧
Continuous Drain	Steady State	T _C = 25°C	I _D	50	Α
Current R _{θJC} (Notes 1, 3)		T _C = 100°C		35	
Power Dissipation		T _C = 25°C	P_{D}	46	W
R _{θJC} (Note 1)		T _C = 100°C		23	
Continuous Drain		T _A = 25°C	I _D	14	Α
Current R _{θJA} (Notes 1, 2, 3)	Steady	T _A = 100°C		10	
Power Dissipation	State	T _A = 25°C	P_{D}	3.6	W
R _{θJA} (Notes 1 & 2)		T _A = 100°C		1.8	
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	290	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			I _S	52	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 2 A)			E _{AS}	81	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	3.2	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	42	

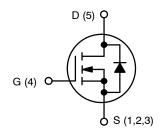
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



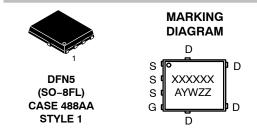
ON Semiconductor®

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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	10.7 m Ω @ 10 V	50 A



N-CHANNEL MOSFET



XXXXXX = 5C673N

(NVMFS5C673N) or

673NWF

(NVMFS5C673NWF)

= Assembly Location

= Year

W = Work Week = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				-	-	-
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				29		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V, T_{J} = 25^{\circ}C$				10	
		V _{DS} = 60 V	T _J = 125°C			250	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 35 \mu A$		2.0		4.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-8.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 7 A		8.9	10.7	mΩ
Forward Transconductance	9 _{FS}	V _{DS} = 15 V, I _E	_O = 25 A		37		S
Gate Resistance	R _G	T _A = 25°C			1.2		Ω
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 30 V			680		pF
Output Capacitance	C _{OSS}				465		
Reverse Transfer Capacitance	C _{RSS}				6.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 7 A			9.6		nC
Threshold Gate Charge	Q _{G(TH)}				2.3		
Gate-to-Source Charge	Q _{GS}				3.6		
Gate-to-Drain Charge	Q_{GD}				0.9		
Plateau Voltage	V _{GP}				4.6		V
SWITCHING CHARACTERISTICS (Note 5	i)						
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 10 V, V_{DS} = 48 V, I_{D} = 7 A, R_{G} = 2.5 Ω			8.4		- ns
Rise Time	t _r				1.9		
Turn-Off Delay Time	t _{d(OFF)}				12.5		
Fall Time	t _f				2.8		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.82	1.2	
	$I_S = 7 \text{ A}$ $T_J = 125^{\circ}\text{C}$			0.67		-	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0$ V, $dls/dt = 100$ A/ μ s, $l_S = 3$ A			32		
Charge Time	ta				16		ns
Discharge Time	t _b				16		
Reverse Recovery Charge	Q_{RR}				22		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

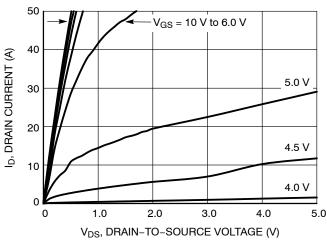


Figure 1. On-Region Characteristics

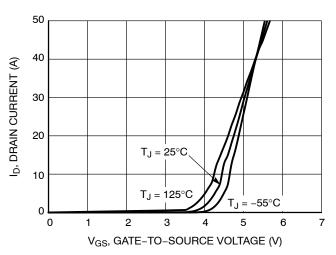


Figure 2. Transfer Characteristics

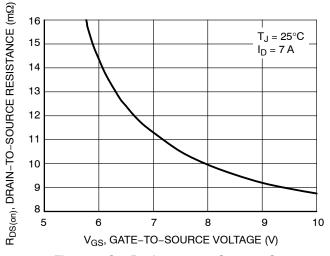


Figure 3. On–Resistance vs. Gate–to–Source Voltage

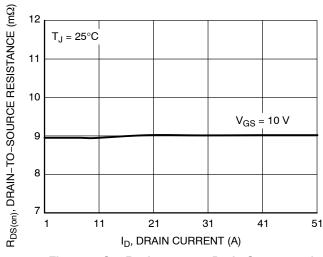


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

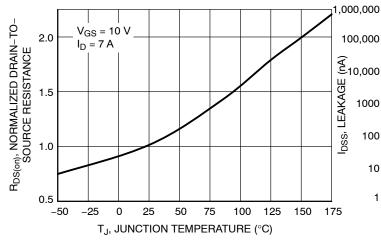


Figure 5. On–Resistance Variation with Temperature

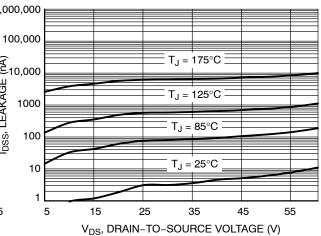


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

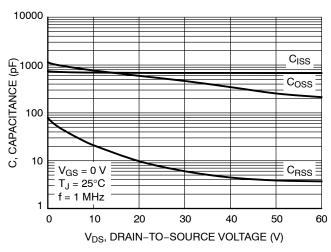


Figure 7. Capacitance Variation

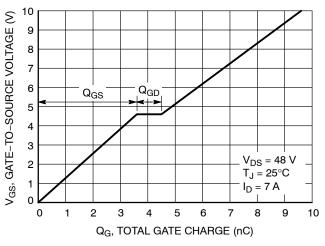


Figure 8. Gate-to-Source vs. Total Charge

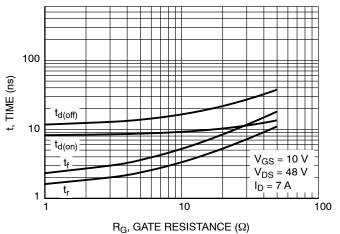


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

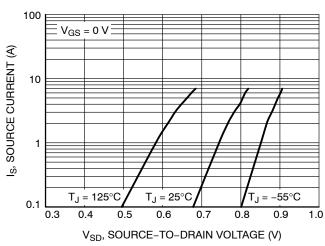


Figure 10. Diode Forward Voltage vs. Current

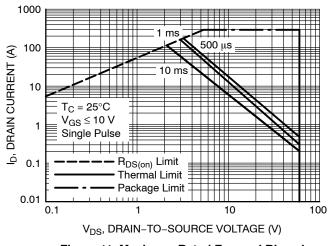


Figure 11. Maximum Rated Forward Biased Safe Operating Area

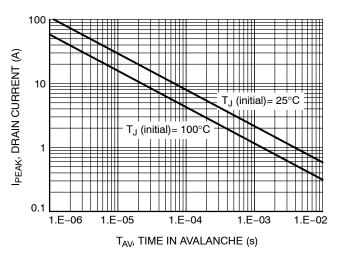


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

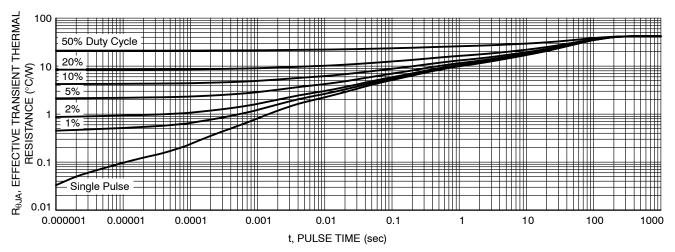


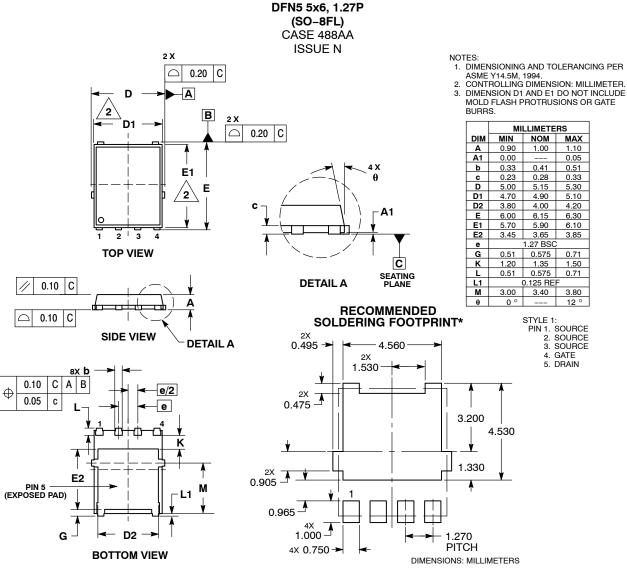
Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C673NT1G	5C673N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NWFT1G	673NWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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