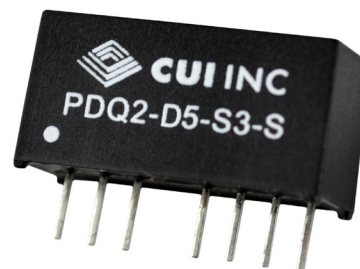


SERIES: PDQ2-S | DESCRIPTION: DC-DC CONVERTER
FEATURES

- up to 2 W isolated output
- industry standard SIP-8 package
- nominal input voltages: 5, 12, 24, 48 Vdc
- 2:1 input range
- single/dual regulated output
- 1,500 Vdc isolation voltage
- remote on/off control
- -40 to 100°C
- efficiency up to 84%
- EN 62368
- designed to meet UL 62368


MODEL

	input voltage		output voltage	output current		output power	ripple & noise ¹		efficiency
	typ (Vdc)	range (Vdc)		min (mA)	max (mA)		max (mVp-p)	typ (%)	
PDQ2-D5-S3-S	5	4.5~9	3.3	0	500	1.65	75	73	
PDQ2-D5-S5-S	5	4.5~9	5	0	400	2	75	76	
PDQ2-D5-S12-S	5	4.5~9	12	0	167	2	75	80	
PDQ2-D5-S15-S	5	4.5~9	15	0	134	2	75	80	
PDQ2-D5-D5-S	5	4.5~9	±5	0	±200	2	75	77	
PDQ2-D5-D12-S	5	4.5~9	±12	0	±83	2	75	79	
PDQ2-D5-D15-S	5	4.5~9	±15	0	±67	2	75	80	
PDQ2-D12-S3-S	12	9~18	3.3	0	500	1.65	75	76	
PDQ2-D12-S5-S	12	9~18	5	0	400	2	75	79	
PDQ2-D12-S12-S	12	9~18	12	0	167	2	75	82	
PDQ2-D12-S15-S	12	9~18	15	0	134	2	75	83	
PDQ2-D12-D5-S	12	9~18	±5	0	±200	2	75	79	
PDQ2-D12-D12-S	12	9~18	±12	0	±83	2	75	82	
PDQ2-D12-D15-S	12	9~18	±15	0	±67	2	75	83	
PDQ2-D24-S3-S	24	18~36	3.3	0	500	1.65	75	76	
PDQ2-D24-S5-S	24	18~36	5	0	400	2	75	79	
PDQ2-D24-S12-S	24	18~36	12	0	167	2	75	82	
PDQ2-D24-S15-S	24	18~36	15	0	134	2	75	83	
PDQ2-D24-D5-S	24	18~36	±5	0	±200	2	75	79	
PDQ2-D24-D12-S	24	18~36	±12	0	±83	2	75	81	
PDQ2-D24-D15-S	24	18~36	±15	0	±67	2	75	84	
PDQ2-D48-S3-S	48	36~75	3.3	0	500	1.65	75	74	
PDQ2-D48-S5-S	48	36~75	5	0	400	2	75	79	
PDQ2-D48-S12-S	48	36~75	12	0	167	2	75	82	
PDQ2-D48-S15-S	48	36~75	15	0	134	2	75	84	

Notes: 1. At full load, nominal input, 20 MHz bandwidth oscilloscope.

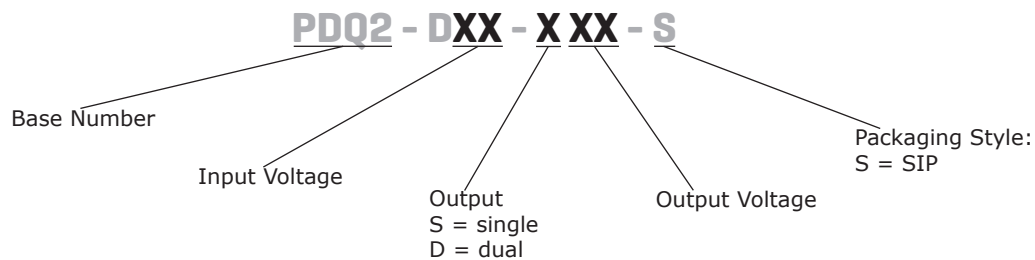
2. All specifications are measured at Ta=25°C, nominal input voltage, and rated output load unless otherwise specified.

MODEL

	input voltage		output voltage	output current		output power	ripple & noise ¹	efficiency
	typ (Vdc)	range (Vdc)	(Vdc)	min (mA)	max (mA)	max (W)	max (mVp-p)	typ (%)
PDQ2-D48-D5-S	48	36~75	±5	0	±200	2	75	78
PDQ2-D48-D12-S	48	36~75	±12	0	±83	2	75	82
PDQ2-D48-D15-S	48	36~75	±15	0	±67	2	75	84

Notes: 1. At full load, nominal input, 20 MHz bandwidth oscilloscope.
2. All specifications are measured at Ta=25°C, nominal input voltage, and rated output load unless otherwise specified.

PART NUMBER KEY



INPUT

parameter	conditions/description	min	typ	max	units
operating input voltage	5 Vdc input models	4.5	5	9	Vdc
	12 Vdc input models	9	12	18	Vdc
	24 Vdc input models	18	24	36	Vdc
	48 Vdc input models	36	48	75	Vdc
surge voltage	for maximum of 100 ms				
	5 Vdc input models			15	Vdc
	12 Vdc input models			25	Vdc
	24 Vdc input models			50	Vdc
current	5 Vdc input models		580		mA
	12 Vdc input models		280		mA
	24 Vdc input models		140		mA
	48 Vdc input models		70		mA
under voltage shutdown	5 Vdc input models, power up			4.2	Vdc
	5 Vdc input models, power down	3			Vdc
	12 Vdc input models, power up			7.3	Vdc
	12 Vdc input models, power down	5.8			Vdc
	24 Vdc input models, power up			15.5	Vdc
	24 Vdc input models, power down	12			Vdc
	48 Vdc input models, power up			31	Vdc
	48 Vdc input models, power down	24			Vdc
remote on/off ³	turn on (<0.8 Vdc or open circuit) turn off (4~15 Vdc)				
filter	capacitive				
input reverse polarity protection	no				
input fuse	1 A time delay fuse for 5 Vdc input models (recommended) 0.5 A time delay fuse for 12 Vdc input models (recommended) 0.25 A time delay fuse for 24 & 48 Vdc input models (recommended)				

Notes: 3. CMOS or open collector TTL, reference to -Vin.

OUTPUT

parameter	conditions/description	min	typ	max	units
maximum capacitive load	3.3 Vdc output models			500	μF
	5 Vdc output models			400	μF
	12 Vdc output models			167	μF
	15 Vdc output models			134	μF
	±5 Vdc output models			200	μF
	±12 Vdc output models			83	μF
	±15 Vdc output models			67	μF
voltage accuracy				±1.5	%
line regulation	from high line to low line			±0.5	%
load regulation	from 100% load to minimum load			±0.5	%
	single output models			±1	%
voltage balance	dual output models			±1	%
cross regulation ¹	load cross variation 25%/100% (dual output models)			±5	%
turn-on delay time, from input	from Vin, min to 10% Vo		1		ms
turn-on delay time, from on/off control	from Von/off to 10% Vo		1		ms
rise time	from 10% Vo to 90% Vo		2.5		ms
switching frequency	at nominal Vin, full load	100			kHz
dynamic load response	25% step load change		± 6		%
	error band (Vout) recovery time			500	μs
temperature coefficient			±0.03		%/°C

Note: 1. For asymmetric loading, both outputs must be at least 25% load.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
over current protection		120			%
short circuit protection	continuous, automatic recovery				

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	input to output for 1 minute	1,500			Vdc
isolation resistance	input to output	1,000			MΩ
isolation capacitance	input to output		500		pF
safety approvals	62368-1: EN designed to meet 62368-1: UL				
conducted emissions	EN 55022 Class A & Class B (external circuit required, see Figure 3)				
MTBF	as per MIL-HDBK-217F, full load, GB, 25°C		2,500,000		hours
RoHS	2011/65/EU				

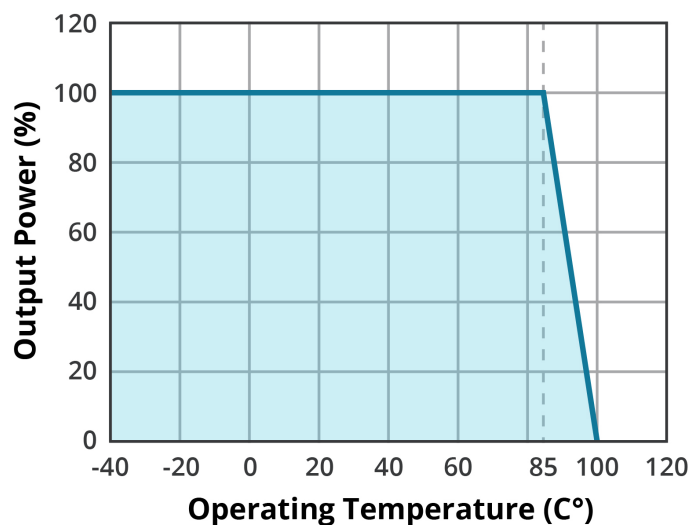
ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		100	°C
storage temperature		-55		125	°C
operating humidity	non-condensing			95	%

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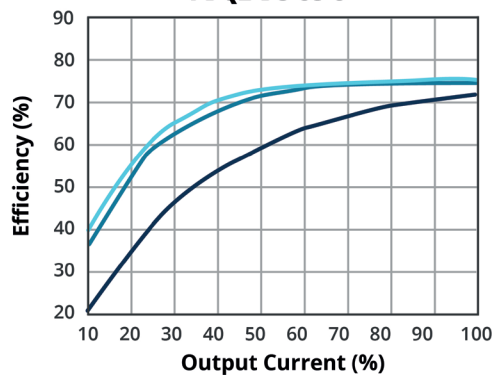
DERATING CURVE

TEMPERATURE DERATING CURVE



EFFICIENCY CURVES

EFFICIENCY VS OUTPUT LOAD
PDQ2-D5-S3-S



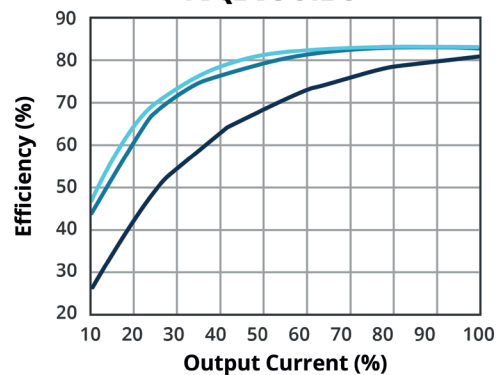
Key

4.5 Vdc

5 Vdc

9 Vdc

EFFICIENCY VS OUTPUT LOAD
PDQ2-D5-S12-S



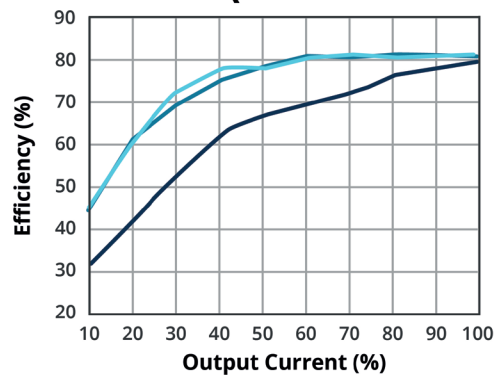
Key

4.5 Vdc

5 Vdc

9 Vdc

EFFICIENCY VS OUTPUT LOAD
PDQ2-D5-S15-S



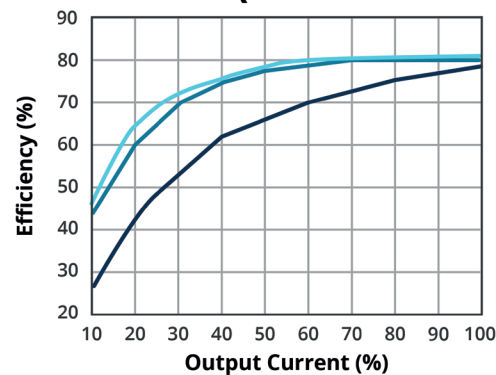
Key

4.5 Vdc

5 Vdc

9 Vdc

EFFICIENCY VS OUTPUT LOAD
PDQ2-D5-D5-S



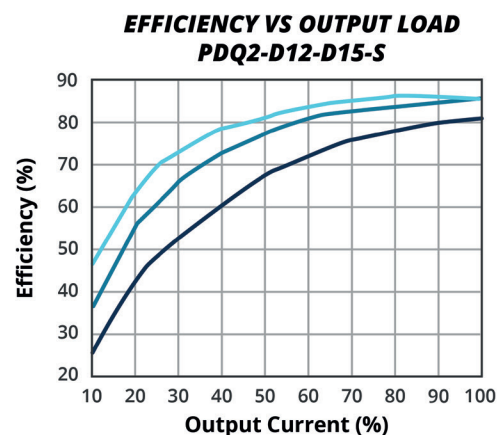
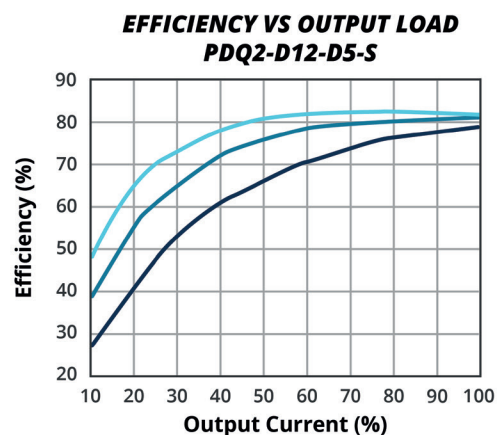
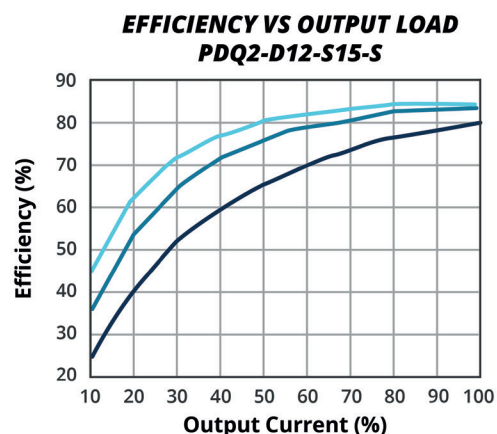
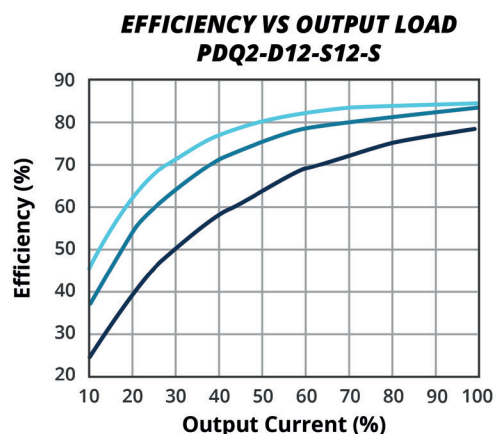
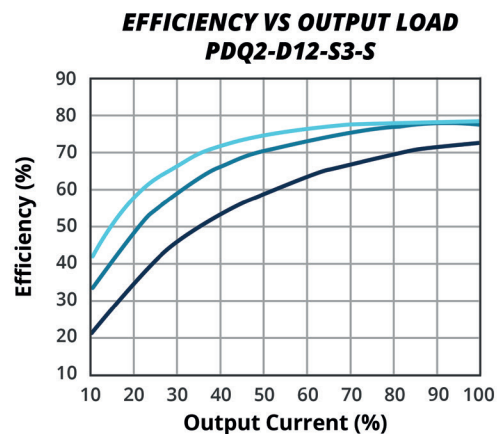
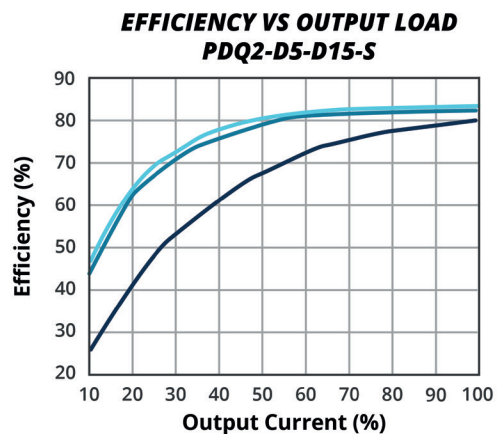
Key

4.5 Vdc

5 Vdc

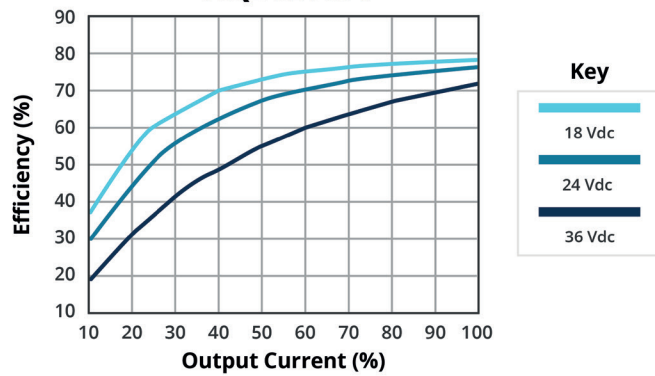
9 Vdc

EFFICIENCY CURVES (CONTINUED)

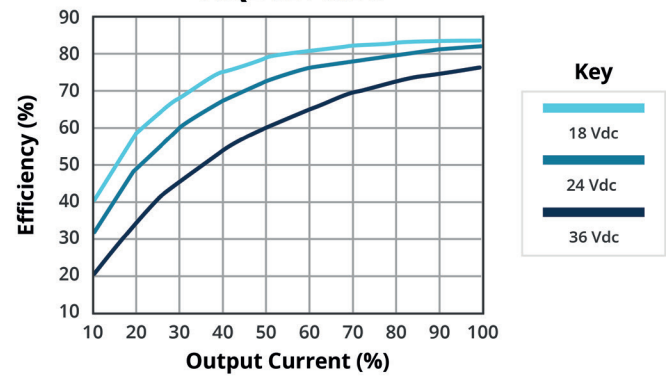


EFFICIENCY CURVES (CONTINUED)

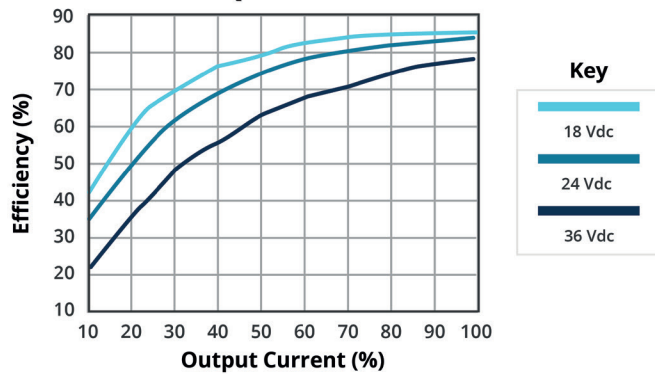
EFFICIENCY VS OUTPUT LOAD
PDQ2-D24-S3-S



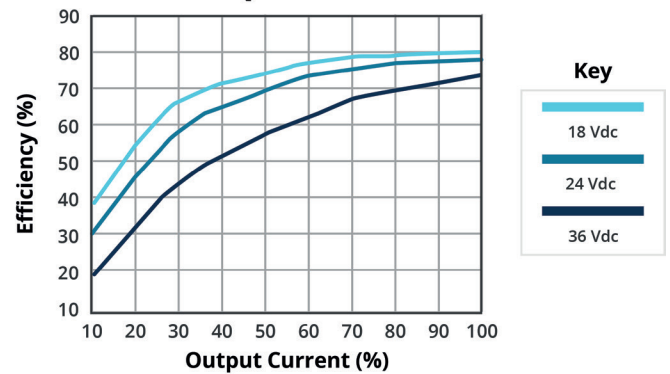
EFFICIENCY VS OUTPUT LOAD
PDQ2-D24-S12-S



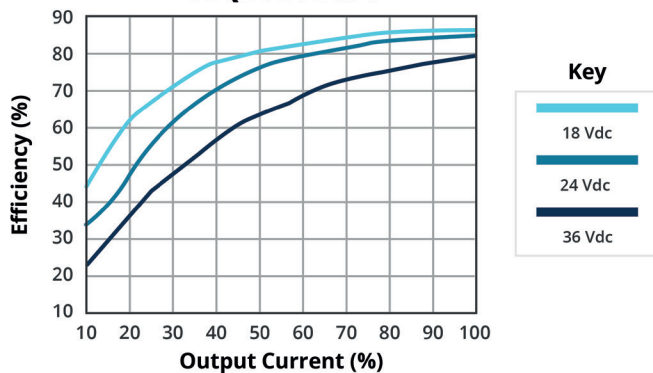
EFFICIENCY VS OUTPUT LOAD
PDQ2-D24-S15-S



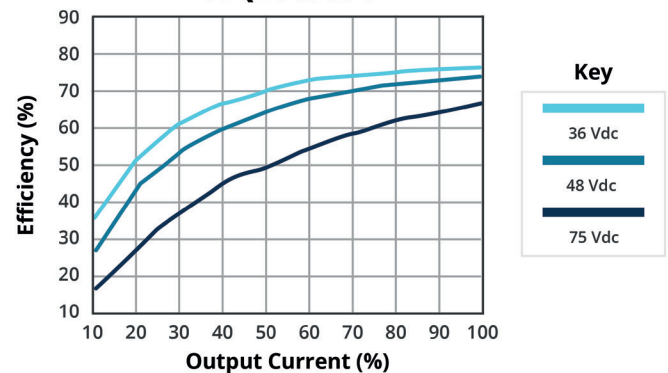
EFFICIENCY VS OUTPUT LOAD
PDQ2-D24-D5-S



EFFICIENCY VS OUTPUT LOAD
PDQ2-D24-D15-S

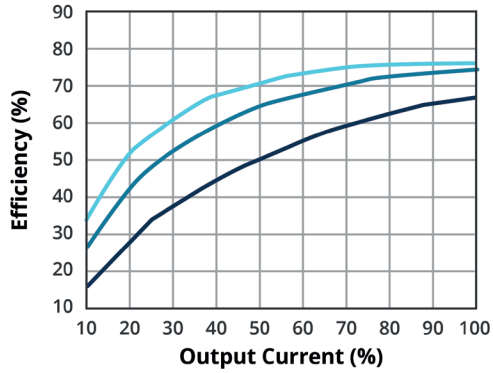


EFFICIENCY VS OUTPUT LOAD
PDQ2-D48-S3-S

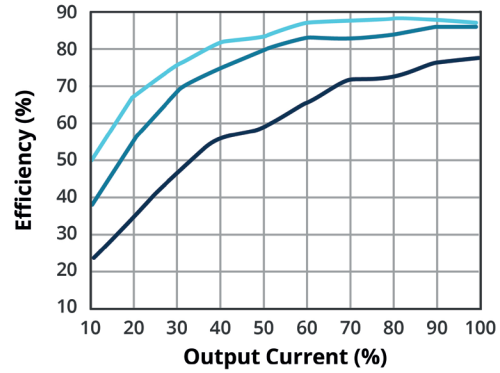


EFFICIENCY CURVES (CONTINUED)

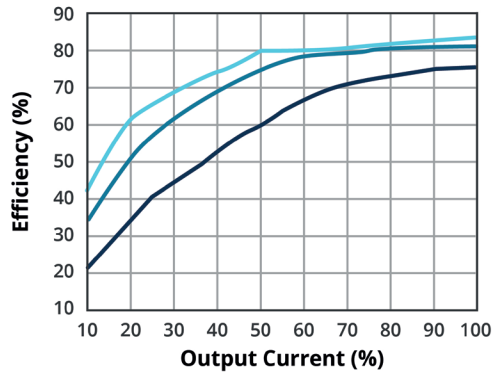
**EFFICIENCY VS OUTPUT LOAD
PDQ2-S48-S12-S**



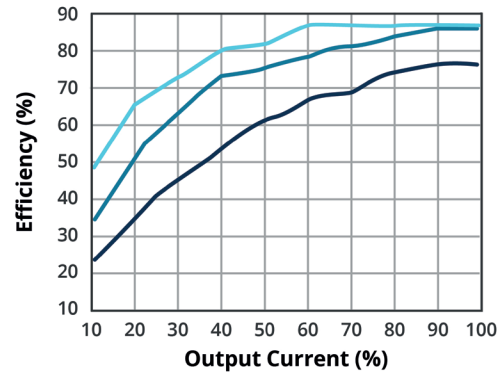
**EFFICIENCY VS OUTPUT LOAD
PDQ2-D48-S15-S**



**EFFICIENCY VS OUTPUT LOAD
PDQ2-S48-D5-S**



**EFFICIENCY VS OUTPUT LOAD
PDQ2-D48-D15-S**



TEST CONFIGURATIONS

Input Ripple Current & Output Noise

Figure 1 Measuring Input Ripple Current

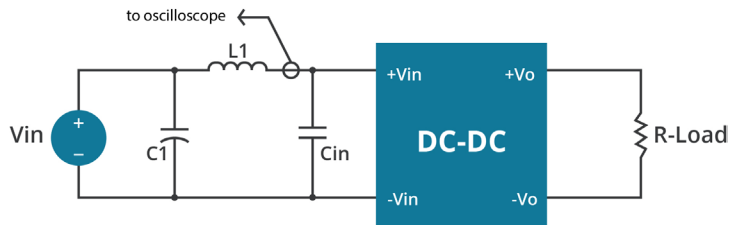


Figure 2 Measuring Output Ripple And Noise

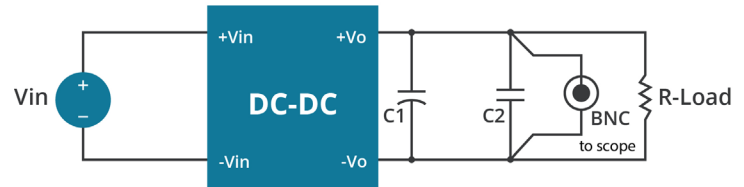


Table 1

L1	12 μ H
C1	NC
Cin	33 μ F ESR<0.7 Ω at 100 kHz

Table 2

C1	NC
C2	NC

EMC RECOMMENDED CIRCUIT

Test Condition

Input Voltage: Nominal

Output Load: Full Load

Figure 3 Conducted Emissions Test Circuit

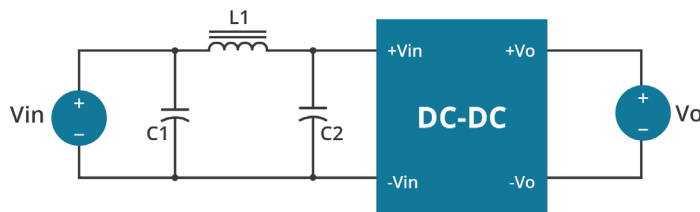


Table 3

EN55022 Class A Recommended External Circuit Components			
Input Voltage (Vdc)	C1 ¹	C2	L1
5	10 μ F / 16 V	NC	2.2 μ H
12	2.2 μ F / 25 V	NC	12 μ H
24	4.7 μ F / 50 V	NC	12 μ H
48	1 μ F / 100 V	NC	68 μ H

Notes: 1. Ceramic Capacitor

Table 4

EN55022 Class B Recommended External Circuit Components			
Input Voltage (Vdc)	C1 ¹	C2	L1
5	10 μ F / 25 V	NC	10 μ H
12	2.2 μ F / 25 V	NC	33 μ H
24	6.8 μ F / 50 V	NC	33 μ H
48	2.2 μ F / 100 V	NC	150 μ H

Notes: 1. Ceramic Capacitor

REVISION HISTORY

rev.	description	date
1.0	initial release	07/26/2016
1.01	safeties updated	02/04/2021
1.02	safeties updated	05/25/2021
1.03	derating curve, efficiency curves and circuit figures updated	07/12/2021
1.04	safeties updated	05/26/2022

The revision history provided is for informational purposes only and is believed to be accurate.



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