

# Si858x Data Sheet

## Integrated Isolated RS-485 Transceivers

The Si858x products are devices that combine robust fully compliant RS-485 transceivers with signal isolation. These devices are ideal for industrial automation applications that require isolated interfaces for FieldBus systems that form a communication network for connecting sensors, actuators, and controllers.

These devices are ideal for isolating nodes on FieldBuses based on the RS-485 standard such as ProfiBus or ModBus. These transmission lines can be susceptible to electrical noise transients especially in harsh environments such as a factory floor, or in sensitive environments such as process control or data acquisition. Isolation provides a means of protection from such transients and noise that could corrupt signal integrity.

These isolated transceivers can operate with a 3.3 V or 5.0 V nominal power supply and have robust bus fault tolerance of up-to  $\pm 30$  V for protecting against harmful transients in the noisy environment where such systems are often utilized. The bus pins are also protected up to 15 kV HBM ESD. Product options are available for half duplex and full duplex mode in industry standard footprints and incorporate slew rate controlled drivers with 1 Mbps data rate capability for reducing the EMI profile or options for high data rate up to 10 Mbps with no slew rate control implemented. These products also offer safety and protection features such as receiver fail-safe and thermal protection.

These devices utilize Skyworks' proprietary silicon isolation technology, supporting up to 5 kVRMS (for 1 minute) isolation voltage per UL 1577. This technology enables high CMTI ( $>60$  kV/ $\mu$ s), low propagation delays and skew, reduced variation with temperature, and age and tight part-to-part matching.

### Industrial Applications

- Industrial automation systems
- Isolated switch mode supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

### Safety Approval

- UL 1577 recognized
  - Up to 5000 V<sub>RMS</sub> for 1 minute
- CSA certification conformity
  - IEC 62368-1 (reinforced insulation)

### KEY FEATURES

- Compliance to TIA/EIA-485-A (RS-485), EN 50170 (ProfiBus)
- Industry standard footprint and logic operation
- Signaling rates of up to 10 Mbps
- HBM 15 kV bus pin ESD ratings
- Common mode voltage supported for operation:  $-7$  V to  $+12$  V
- Bus fault protection:  $\pm 30$  V
- Thermal shutdown protection
- VDD1: 3.0 to 5.5 V
- VDD2: 3.3 V or 5.0 V
- 50 ns typical driver propagation delay
- 5 kV isolation UL 1577, CSA, and CQC certified
- CMTI of 100 kV/ $\mu$ s (min)
- Unit loading: Up to 256 transceivers on a bus at 5 V, 128 at 3.3 V
- T<sub>A</sub>:  $-40$  to  $+125$  °C
- JEDEC-qualified
- WB SOIC-16 RoHS-compliant package

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## 1. Ordering Guide

**Table 1.1. Ordering Guide**

See [Top Marking](#) for product name decoder.

Ordering Part Number (OPN)	RS-485 Configuration	Nodes	Slew Rate Control	Data Rate (Mbps)	VDD2 (V)	Isolation Rating (kVrms)
Si85853D-IS	Half Duplex	64	Yes	1	5.0	5.0
Si85833D-IS	Half Duplex	64	Yes	1	3.3	5.0
Si85855D-IS	Half Duplex	256	No	10	5.0	5.0
Si85835D-IS	Half Duplex	256	No	10	3.3	5.0
Si85856D-IS	Half Duplex with isolated Tx_EN pin	256	No	10	5.0	5.0
Si85836D-IS	Half Duplex with isolated Tx_EN pin	256	No	10	3.3	5.0
Si85857D-IS	Full Duplex	64	Yes	1	5.0	5.0
Si85837D-IS	Full Duplex	64	Yes	1	3.3	5.0
Si85858D-IS	Full Duplex	256	No	10	5.0	5.0
Si85838D-IS	Full Duplex	256	No	10	3.3	5.0

**Note:**

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. The temperature ranges is –40 to +125 °C.

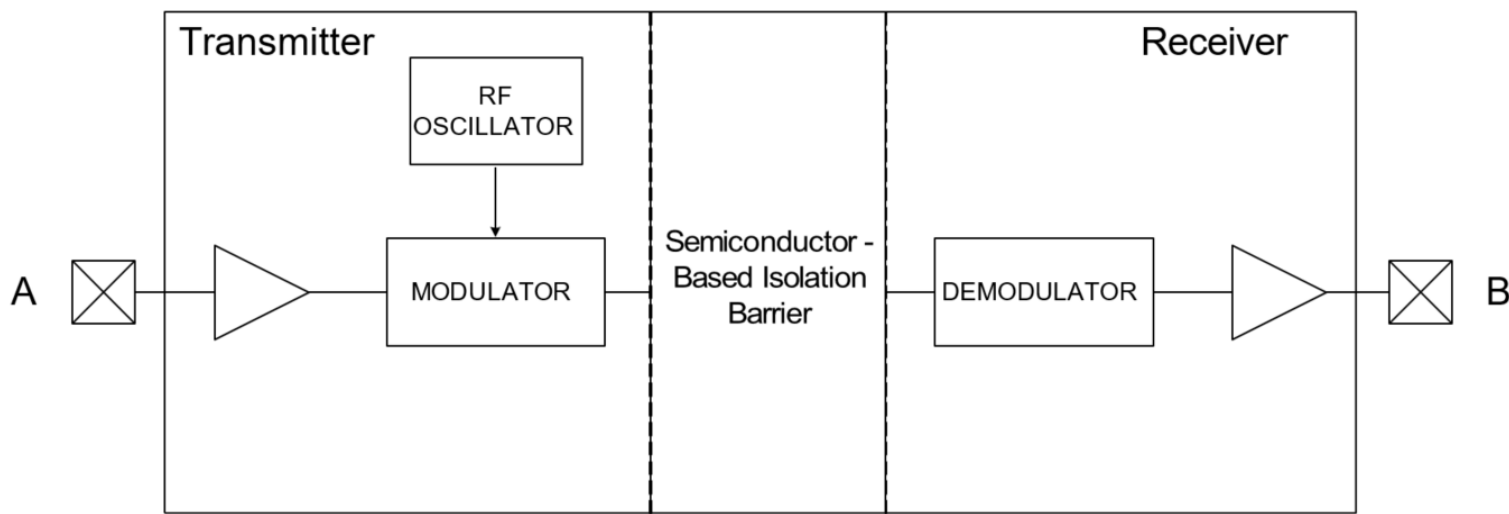
## 2. Functional Description

### 2.1 Theory of Operation

The Si858x family of products is capable of transmitting and receiving RS-485 signals from one power domain to an isolated domain with up to 5.0 kVrms of isolation. In addition, these products include a completely integrated RS-485 transceiver.

### 2.2 Digital Isolation

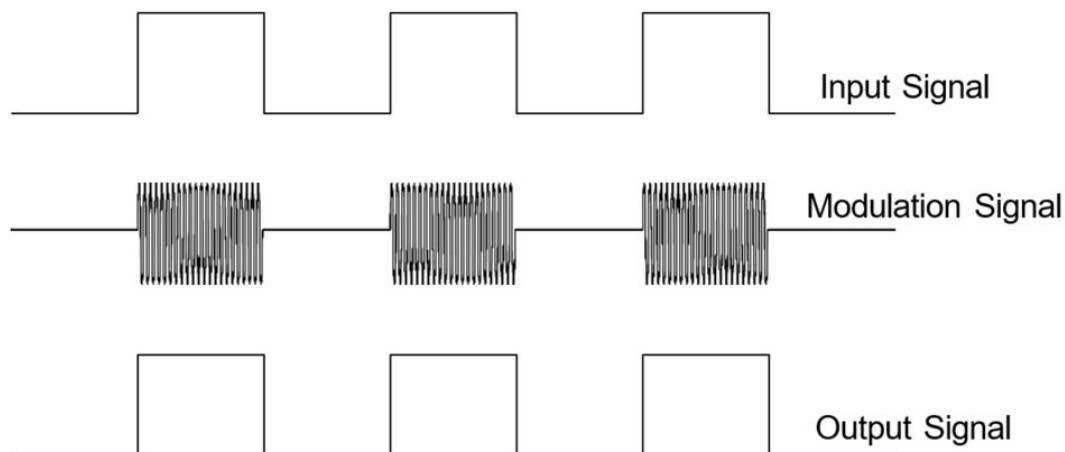
The operation of an Si858x digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si858x channel is shown in the following figure.



**Figure 2.1. Simplified Si858x Channel Diagram**

A channel consists of an RF transmitter and RF receiver separated by a silicon dioxide capacitive isolation barrier. In the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the following figure for more details.

**Figure 2.2. Modulation Scheme**

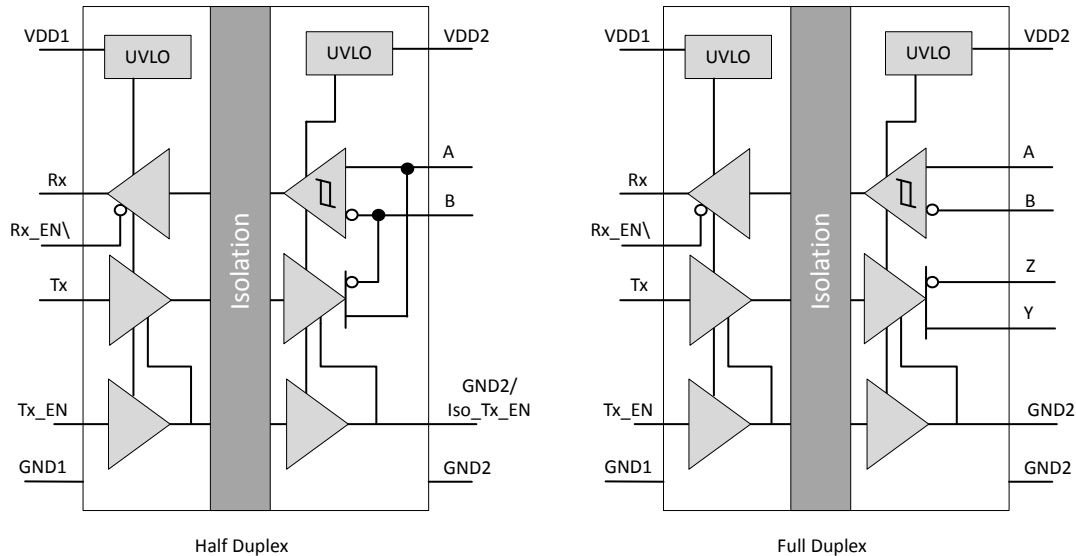


### 2.3 RS-485 Signaling

These isolated transceivers are compliant to the TIA/EIA-485 standard. They are available in full duplex as well as half duplex configurations.

For the driver operation, when VDD1 and VDD2 are both powered up and the driver enabled (Tx\_EN pin is high), a logic high on driver input pin Tx produces a corresponding logic high on the isolated driver output bus pin Y (pin A for half duplex) and a logic low on pin Z (pin B for half duplex). A logic low on the Tx pin will invert the outputs. Thus, the differential output voltage on the bus, defined as  $VOD = VY/A - VB/Z$ , is positive when Tx is high and negative when Tx is low. The Tx\_EN pin is active high with a pull-up resistor internally, driving it low will disable the driver function and the bus pins will be high impedance.

The receiver enable is active low with an internal pull-down resistor. Leaving it open or driving it low enables the receiver while driving it high will disable it. With the receiver enabled, a differential input (defined as  $VID = VA-VB$ ) greater than the input threshold of the receiver produces a logic high on the receiver output pin Rx. A differential input that is lower than the receiver threshold will produce a logic low.



**Figure 2.3. Isolated Transceiver Block Diagram**

### 3. Device Operation

**Table 3.1. Si858x Driver Operation**

Input TX <sup>1</sup>	Enable TX_EN <sup>1</sup>	VDD1 <sup>2, 3</sup>	VDD2 <sup>2, 3</sup>	Output ISO_TX_EN <sup>1</sup>	Output Y or A <sup>1</sup>	Output Z or B <sup>1</sup>
H	H	P	P	H	H	L
L	H	P	P	H	L	H
X	L	P	P	L	Hi-Z	Hi-Z
X	OPEN	P	P	L	Hi-Z	Hi-Z
OPEN	H	P	P	H	L	H
X <sup>4</sup>	X	UP <sup>5</sup>	P	L	Hi-Z	Hi-Z
X	X	P	UP <sup>6</sup>	UD	UD	UD
X	X	UP	UP	UD	UD	UD

**Note:**

1. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance, UD = undetermined.
2. VDD1 and VDD2 are the logic and transceiver side power supplies.
3. “Powered” state (P) is defined as > 2.5 V, “Unpowered” state (UP) is defined as VDD = 0 V.
4. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
5. For reliability reasons, it is highly recommended that the power supply (VDD1 or VDD2) not be powered down while TX\_EN is asserted high or while it is in the transition to disable state.
6. When VDD2 is UP, ISO\_Tx\_EN pin may still follow the TX\_EN state. It is recommended that while VDD2 is in the UP state, the status of ISO\_TX\_EN be ignored.

**Table 3.2. Si858x Receiver Operation**

Differential Input VID = VIA – VIB <sup>1</sup>	Enable RX_EN <sup>2</sup>	VDD1 <sup>3, 4</sup>	VDD2 <sup>3, 4</sup>	Output RX <sup>2</sup>
VID ≥ –10mV	L or OPEN	P	P	H
–200 mV < VID < –10 mV	L or OPEN	P	P	UD
VID ≤ –200 mV	L or OPEN	P	P	L
X	H	P	P	Hi-Z
OPEN	L	P	P	H
SHORT	L	P	P	H
IDLE (terminated)	L	P	P	H
X	X <sup>5</sup>	UP	P	UD
X	L or open	P	UP	H
X	H	P	UP	Hi-Z

**Note:**

1. Open = transceiver disconnected from bus, Short = bus shorted, Idle = bus not actively driven.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance, UD = undetermined.
3. VDD1 and VDD2 are the logic and transceiver side power supplies.
4. “Powered” state (P) is defined as > 2.5 V, “Unpowered” state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.

## 4. Electrical Specifications

**Table 4.1. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature <sup>1</sup>	T <sub>A</sub>	–40	25	125	°C
Logic Supply Voltage	VDD1	2.5	—	5.5	V
Transceiver Supply Voltage	VDD2	3.135 4.75	3.3 5.0	3.465 5.25	V
Voltage on Bus Pin A, B, Y, Z	V <sub>CM</sub>	–7	—	12	V
High Level Input voltage on Tx, TX_EN, Rx_EN\	V <sub>IH</sub>	0.7 x VDD1			V
Low Level Input Voltage	V <sub>IL</sub>	—	—	0.3 x VDD1	V
Differential Input Voltage	V <sub>ID</sub>	–5	—	10	V
Differential Load Resistance	R <sub>D</sub>	54			Ω
Driver Output Current	I <sub>OD</sub>	–60		60	mA
Receiver Output Current	I <sub>OR</sub>	–4		4	mA

**Note:**

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

**Table 4.2. Electrical Characteristics**

Typical specs at 25 °C, with VDD1 = VDD2 = 5.0 V, unless specified, –40 °C to 125 °C ambient temperature.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Supply Current							
Supply Current, VDD1	IDD1	VDD1 = 3.3 V	Tx_EN = 0	—			mA
			Tx_EN = 1 , 1 Mbps	—			
			Tx_EN = 1 , 10 Mbps	—			
		VDD1 = 5.0 V	Tx_EN = 0	—			
			Tx_EN = 1 , 1 Mbps	—	3.7	5.2	
			Tx_EN = 1 , 10 Mbps	—	19	24	
Supply Current, VDD2	IDD2	VDD2 = 3.3 V	Tx_EN = 0	—	19.5		
			Tx_EN = 1 , 1 Mbps	—	58		
			Tx_EN = 1 , 10 Mbps	—	69		
		VDD2 = 5.0 V	Tx_EN = 0	—	19.5		mA
			Tx_EN = 1 , 1 Mbps	—	72	79	
			Tx_EN = 1 , 10 Mbps		92	110	mA
Driver							

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Differential Output Voltage Steady State	VOD(SS)	RLOAD = 54 $\Omega$	Figure 4.1 Measurement for Driver Differential Voltage, VOD with Load on page 11	1.5	—	VDD2	V
Change in Differential Output Steady State	Delta VOD(SS)	RLOAD = 54 $\Omega$	Figure 4.1 Measurement for Driver Differential Voltage, VOD with Load on page 11	-200.0	—	200.0	mV
Open Circuit Differential Output Voltage	VOD	No load	Figure 4.2 Measurement for Driver Differential Voltage VOD, No Load on page 11	1.5	—	VDD2	V
Differential Output Voltage Under/Overshoot	VOD(RING)	RLOAD = 54 $\Omega$	Figure 4.1 Measurement for Driver Differential Voltage, VOD with Load on page 11	—	—	10%*VOD	V
Common Mode Output Voltage Steady State	VOC(SS)	VDD2 = 3.3 V RLOAD = 54 $\Omega$	Figure 4.3 Measurement for Driver Common Mode Voltage VOC on page 12	2	2.1	3	V
Common Mode Output Voltage Steady State	VOC(SS)	VDD2 = 5.0 V RLOAD = 54 $\Omega$	Figure 4.3 Measurement for Driver Common-Mode Voltage VOC on page 12				
Change in Common Mode Output Voltage Steady State	Delta VOC(SS)	VDD2 = 5.0 V RLOAD = 54 $\Omega$	Figure 4.3 Measurement for Driver Common-Mode Voltage VOC on page 12	-200	—	200	mV
Peak-to-Peak Common Mode Output Voltage	VOC(PP)	VDD2 = 5.0 V RLOAD = 54 $\Omega$	Figure 4.3 Measurement for Driver Common-Mode Voltage VOC on page 12	—	500	-	mV
Short Circuit Steady State Output Current	IOS(SS)	Tx_EN = 1	VOS = -7 to +12 V, Tx = 0 Figure 4.1 Measurement for Driver Differential Voltage, VOD with Load on page 11	-250	—	+250	mA

**Receiver**

Positive Going Differential Input Threshold Voltage	VIT+	IO = -8 mA		-85-	-75	-66	mV
Negative Going Differential Input Threshold Voltage	VIT-	IO = 8 mA		-137	-135	-123	mV
Input Hysteresis Voltage	V(HYS)			49	50	63	mV
Differential Input Capacitance	CID	Test signal is 1.5 MHz sine wave with 1 Vpp magnitude, CID measured across A and B (or Y and Z)		—	7	10	pF
Single Ended Input Resistance	RA, RB		Figure 4.2 Measurement for Driver Differential Voltage VOD, No Load on page 11	96	127	223	k $\Omega$
Differential Input Resistance	RID		“	191	311	439	k $\Omega$

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Input Resistance Matching			“	-0.3		0.3	%
High Level Output Voltage: RX	VOH	VID = 200 mV	VDD1 = 5.0 V, IOH = -4 mA	VDD1-0.4	—	—	V
			VDD1 = 5.0 V IOH = -20 uA	VDD1-0.1	—	—	V
Low Level Output Voltage: RX	VOL	VID = -200 mV	VDD1 = 5.0 V, IOL = 4 mA	—	—	0.4	V
			VDD1 = 5.0 V, IOL = 20 uA	—	—	0.1	V
Bus Input Current	IA, IB	VI = -12 to 12 V		-200	—	200	uA
Other IO							
Low Level Input Current: TX, TX_EN, RX_EN, STB				—	—	15	uA
High Level Input Current: TX, TX_EN, RX_EN, STB				-15	—	—	uA
Input Leakage, Low or High for V5_EN							
Input Voltage Hysteresis	VI(HYS)					150	mV
Switching Characteristics							
Maximum Data rate				—	—	10	Mbps
Driver							
Propagation Delay	tpLH, tpHL	VDD2 = 5.0 V, RL = 54 Ω, CL = 50 pF, 50% to 50% <a href="#">Figure 4.4 Measurement for Driver Timing Chracteristics on page 12</a>		33	37	42	ns
Differential Signal Rise/Fall Time	tr, tf	A-B: VDD2 = 5.0 V, R L= 54 Ω. CL = 50 pF, 10% to 90% <a href="#">Figure 4.4 Measurement for Driver Timing Chracteristics on page 12</a>		30	34	38	ns
Pulse Skew (tpHL-tpLH)	tpsk	VDD2 = 5.0 V, RL = 54 Ω, CL = 50 pF, 50% to 50%		—	2	5	ns
Driver Enable/Disable Delay Time	tp(A/BZH), tp(A/BZL), tp(A/BHZ), tp(A/BLZ)	50% TX_EN=0,1 to 50% A,B transition <a href="#">Figure 4.7 Enable/Disable Delay Measurements on page 13</a>		—	40	108	ns
CMTI				60	100	—	kV/uS
Receiver							
Propagation Delay	tpLH, tpHL	VDD2 = 5.0 V <a href="#">Figure 4.5 Measurement for Receiver Output and Timing Characteristics on page 12</a>		—	38	43	ns
Pulse Skew (tpHL-tpLH)	tpsk						
Rx Output Rise/Fall Time	tr, tf	VDD1 = 5.0 V, CL = 15 pF, 10% to 90%		—	3.7	4	ns
Receiver Enable/Disable Delay Time	tp(ZH), tp(ZL), tp(HZ), tp(LZ)	VDD1,2 = 5.0 V, CL = 15 pF		—	2	12	ns

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Delay from VDD2 Power Loss to RX=1				—	—	6	uS
<b>Protection</b>							
VDD1 Undervoltage Threshold	VDD <sub>UV+</sub>			1.9	2.2	2.4	V
VDD Undervoltage Threshold	VDD <sub>UV-</sub>	V <sub>DD1</sub> rising		1.8	2.1	2.3	V
VDD1 Undervoltage Hysteresis				50	70	95	mV
VDD2 Undervoltage Threshold (5.0 V VDD2)	VDD2 <sub>UV+</sub>	V <sub>DD1</sub> rising		3.8	4.2	4.4	V
VDD2 Undervoltage Threshold (5.0 V VDD2)	VDD2 <sub>UV-</sub>	V <sub>DD2</sub> falling		3.8	4.1	4.4	V
VDD2 Undervoltage Hysteresis (5.0 V VDD2)				130	135	140	mV
VDD2 Undervoltage Threshold (3.3 V VDD2)	VDD2 <sub>UV+</sub>	V <sub>DD1</sub> rising		2.2	2.3	2.5	V
VDD2 Undervoltage Threshold (3.3 V VDD2)	VDD2 <sub>UV-</sub>	V <sub>DD2</sub> falling		2.2	4.1	2.5	V
VDD2 Undervoltage Hysteresis				63	65	68	mV

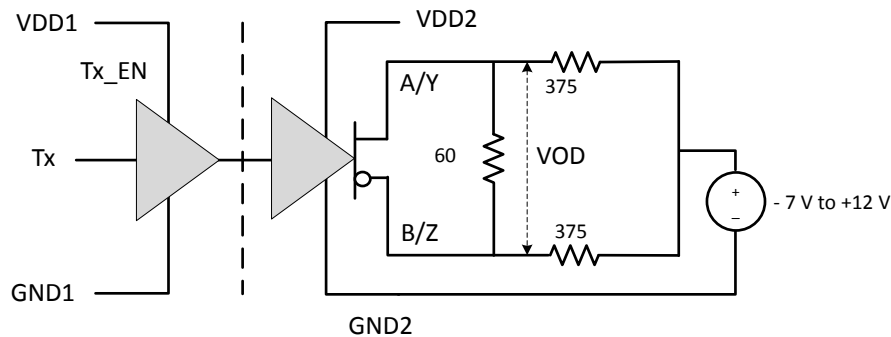


Figure 4.1. Measurement for Driver Differential Voltage, VOD with Load

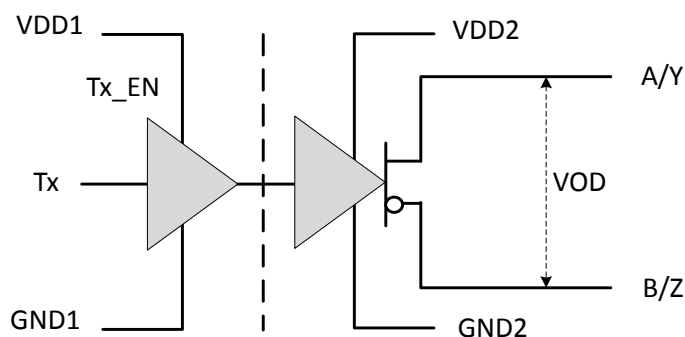


Figure 4.2. Measurement for Driver Differential Voltage VOD, No Load

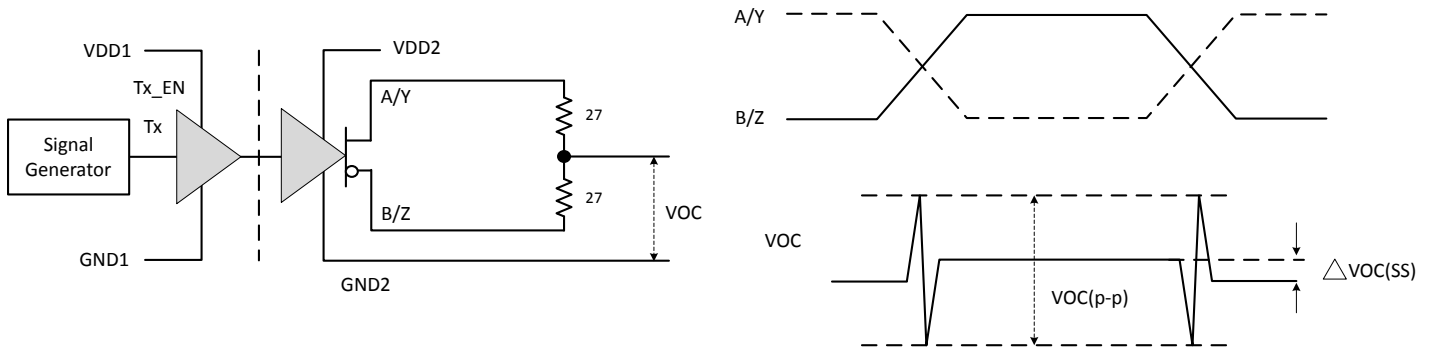


Figure 4.3. Measurement for Driver Common-Mode Voltage  $V_{OC}$

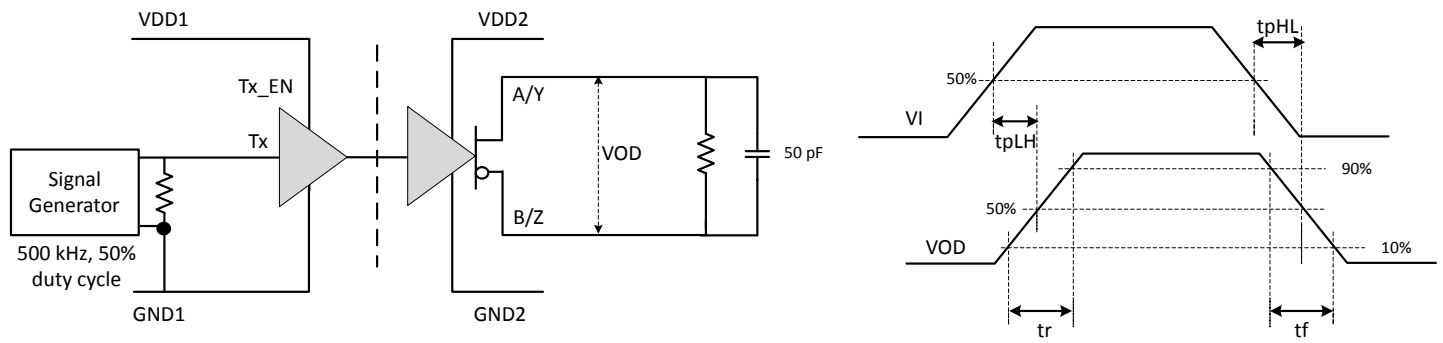


Figure 4.4. Measurement for Driver Timing Characteristics

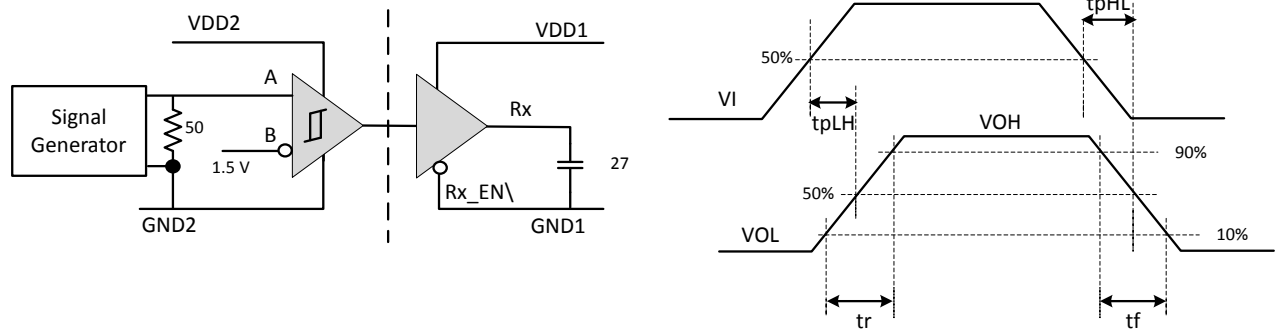


Figure 4.5. Measurement for Receiver Output and Timing Characteristics

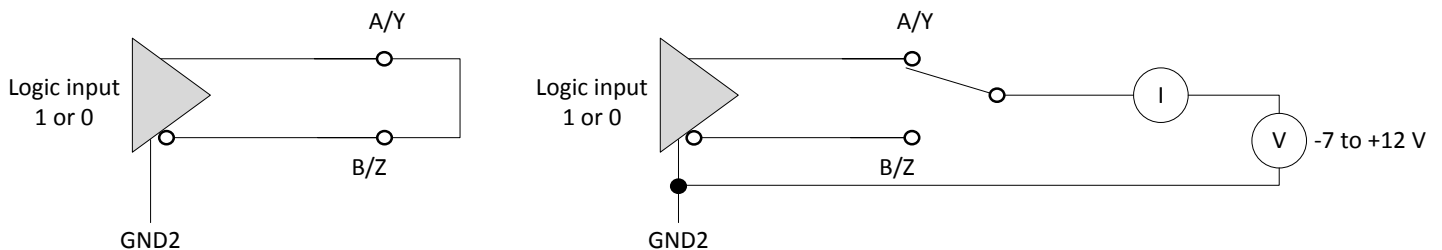
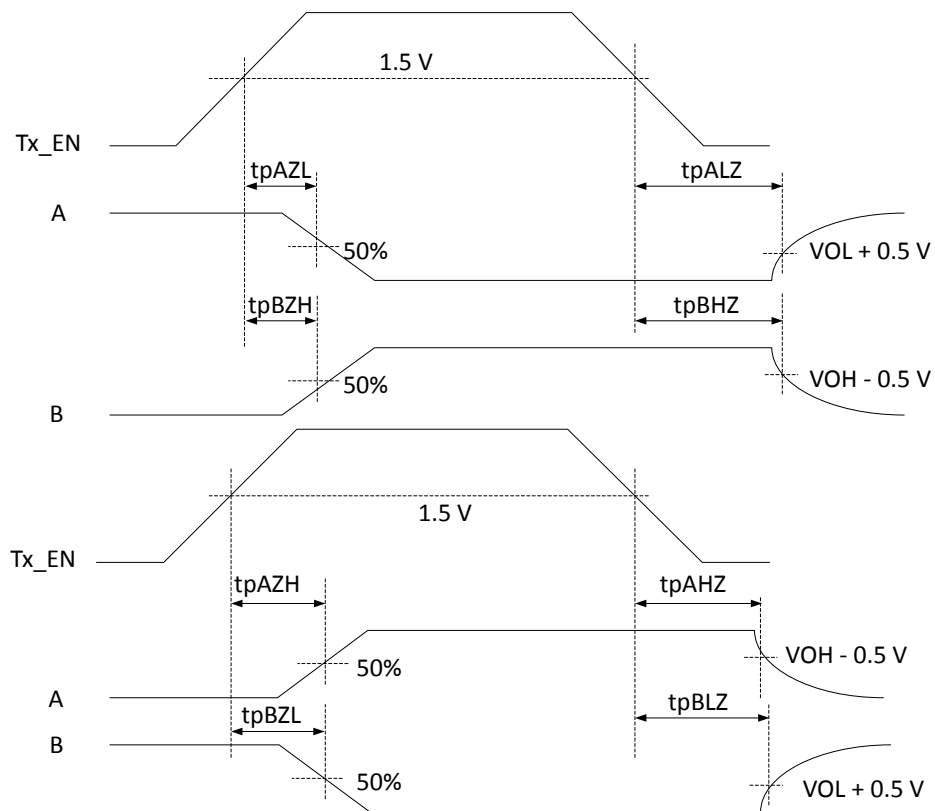


Figure 4.6. Short Circuit Current Measurement



**Figure 4.7. Enable/Disable Delay Measurements**

## Typical Performance Characteristics

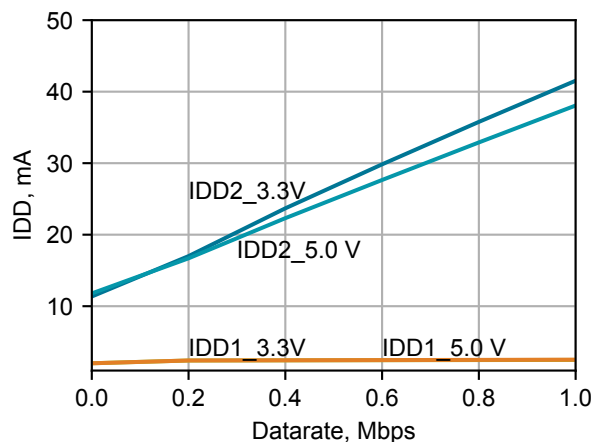


Figure 4.8. Si858x3/7 Supply Current vs. Data Rate, No Load

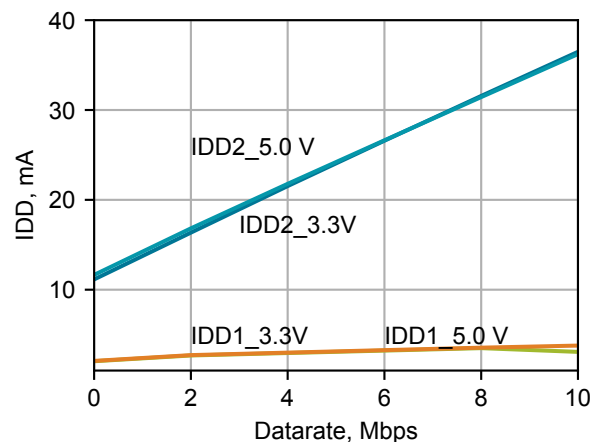


Figure 4.9. Si858x5/6/8 Supply Current vs. Data Rate, No Load

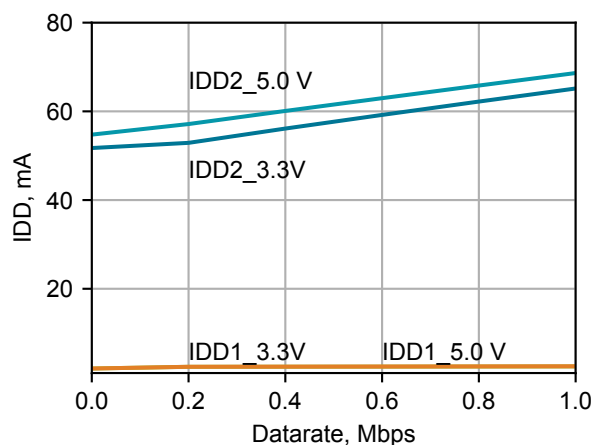


Figure 4.10. Si858x3/7 Supply Current vs. Data Rate, 54 Ω, 50 pF Load

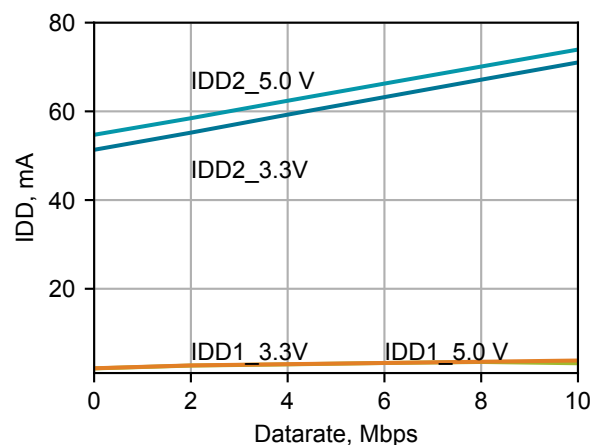


Figure 4.11. Si858x5/6/8 Supply Current vs. Data Rate, 54 Ω, 50 pF Load

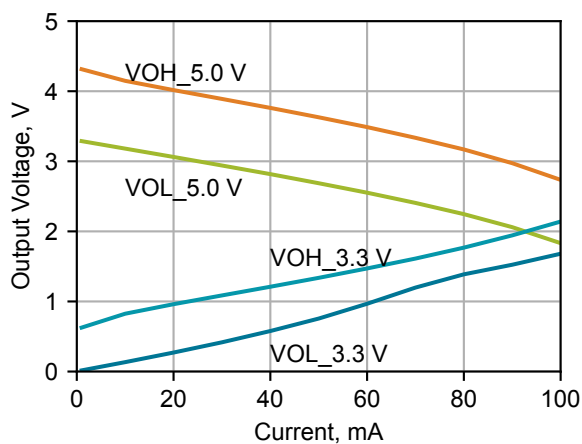


Figure 4.12. Driver Output Voltage vs. Current

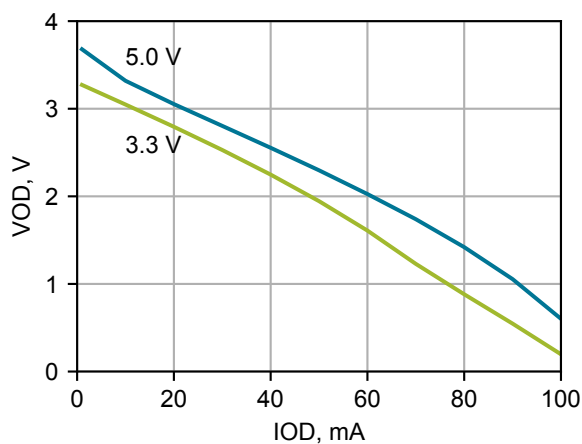


Figure 4.13. Driver Differential Output Voltage vs. Current

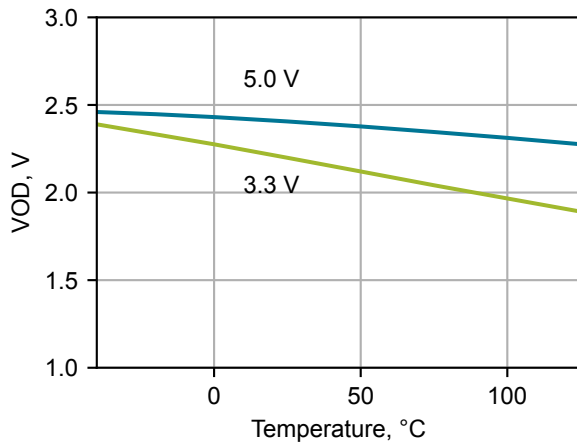


Figure 4.14. Driver Differential Output Voltage vs. Temperature

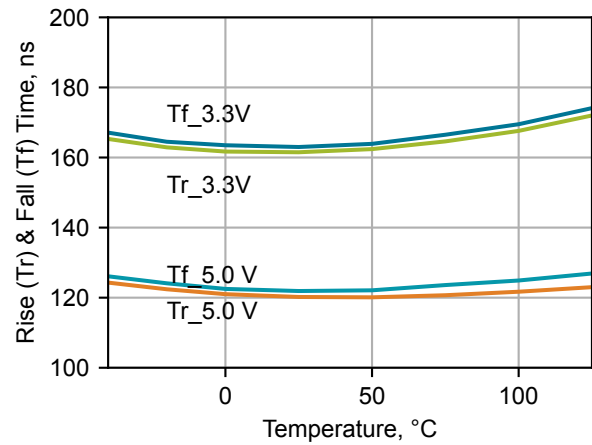


Figure 4.15. Si858x3/7 Driver Rise/Fall Time vs. Temperature

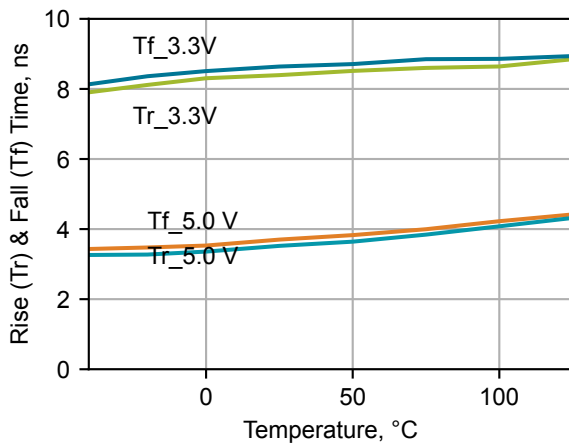


Figure 4.16. Si858x5/6/8 Driver Rise/Fall Time vs. Temperature

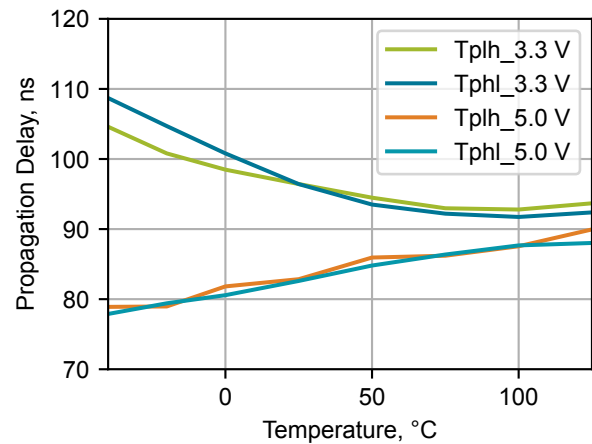


Figure 4.17. Si858x3/7 Driver Propagation Delay vs. Temperature

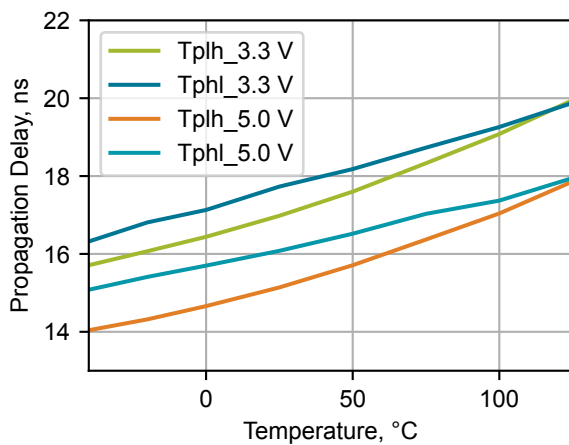


Figure 4.18. Si858x5/6/8 Driver Propagation Delay vs. Temperature

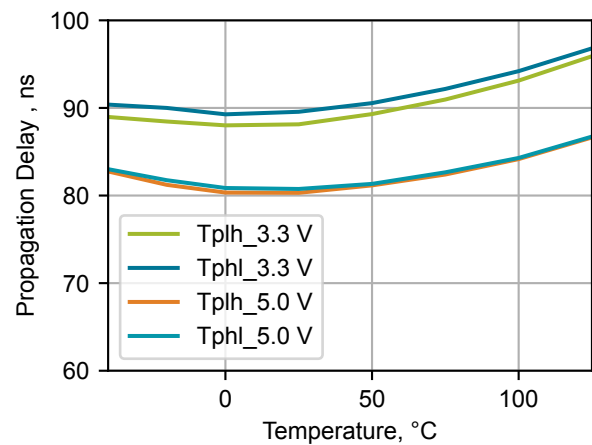


Figure 4.19. Receiver Propagation Delay vs. Temperature

**Table 4.3. Regulatory Information<sup>1</sup>**

<b>CSA</b>
The Si858x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 1000 V <sub>RMS</sub> basic insulation working voltage.
60601-1: Up to 250 V <sub>RMS</sub> working voltage and 2 MOPP (Means of Patient Protection).
<b>VDE</b>
The Si858x is certified under VDE. For more details, see File 5006301.
IEC60747-17: Up to 2121 V <sub>peak</sub> for reinforced insulation working voltage.
62368-1: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 1000 V <sub>RMS</sub> basic insulation working voltage.
<b>UL</b>
The Si858x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV <sub>RMS</sub> , V <sub>ISO</sub> isolation voltage for basic protection.
<b>CQC</b>
The Si858x is certified under GB4943.1-2011.
Rated up to 250 V <sub>RMS</sub> reinforced insulation working voltage at 5000 meters tropical climate.
<b>Note:</b>
1. Regulatory Certifications apply to >2.5 kV <sub>RMS</sub> rated devices which are production tested to 3.0 kV <sub>RMS</sub> for 1 sec. Regulatory Certifications apply to 3.75 kV <sub>RMS</sub> rated devices which are production tested to 4.5 kV <sub>RMS</sub> for 1 sec. Regulatory Certifications apply to 6.0 kV <sub>RMS</sub> rated devices which are production tested to 7.2 kV <sub>RMS</sub> for 1 sec. For more information, see Section 1. <a href="#">Ordering Guide</a> .

**Table 4.4. Insulation and Safety-Related Specifications**

Parameter	Symbol	Test Condition	Value WB SOIC-16	Unit
Nominal External Air Gap (Clearance)	CLR		8.0	mm
Nominal External Tracking (Creepage)	CRP		8.0	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	V <sub>RMS</sub>
Erosion Depth	ED		0.019	mm
Resistance (Input-Output) <sup>1</sup>	RIO	Test voltage = 500 V	10 <sup>12</sup>	Ω
Capacitance (Input-Output) <sup>1</sup>	CIO	f = 1 MHz	2.0	pF
Input Capacitance <sup>2</sup>	CI		4.0	pF
<b>Note:</b>				
1. To determine resistance and capacitance, the Si858x is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.				
2. Measured from input pin to ground.				

**Table 4.5. IEC 60664-1 Ratings**

Parameter	Test Condition	Specification WB SOIC-16
Basic Isolation Group	Material Group	I
Installation Classification	RateMains Voltages < 150 V <sub>RMS</sub>	I-IV
	RateMains Voltages < 300 V <sub>RMS</sub>	I-IV
	RateMains Voltages < 400 V <sub>RMS</sub>	I-III
	RateMains Voltages < 600 V <sub>RMS</sub>	I-III

**Table 4.6. IEC 60747-17 Insulation Characteristics for Si858x <sup>1</sup>**

Parameter	Symbol	Test Condition	Characteristic WB SOIC-16	Unit
Maximum Working Isolation Voltage	V <sub>IOWM</sub>		1500	V <sub>RMS</sub>
Maximum Repetitive Isolation Voltage	V <sub>IORM</sub>	Method b1 (V <sub>IORM</sub> x 1.875 = V <sub>PR</sub> , 100% Production Test, t <sub>m</sub> = 1 sec, Partial Dis- charge < 5 pC)	2121	V <sub>peak</sub>
Input to Output Test Voltage	V <sub>PR</sub>	Method b1 (V <sub>IORM</sub> x 1.875 = V <sub>PR</sub> , 100% Production Test, t <sub>m</sub> = 1 sec, Partial Discharge < 5 pC)	3977	V <sub>peak</sub>
Maximum Transient Isolation Voltage	V <sub>IOTM</sub>	t = 60 s	8000	V <sub>peak</sub>
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>	Tested with 10400 V <sub>peak</sub> and 1.2 μs/50 μs profile	8000	V <sub>peak</sub>
Maximum Impulse Voltage	V <sub>IOSM</sub>	Tested with 8000 V <sub>peak</sub> and 1.2 μs/50 μs profile	8000	V <sub>peak</sub>
Pollution Degree		DIN VDE 0110	2	
Insulation Resistance	R <sub>S</sub>	TAMB = T <sub>S</sub> , V <sub>IO</sub> = 500 V	>10 <sup>9</sup>	Ω

**Note:**

1. Maintenance of the safety data is ensured by protective circuits. The Si858x provides a climate classification of 40/125/21.

**Table 4.7. IEC Safety Limiting Values<sup>1</sup>**

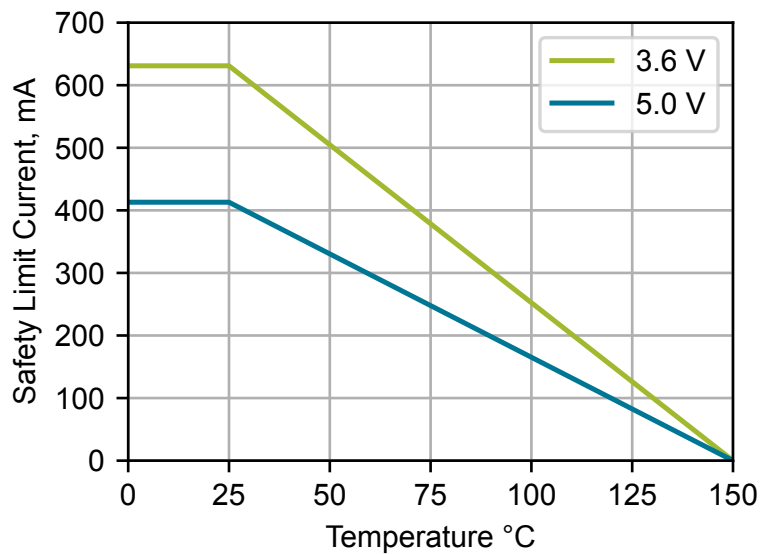
Parameter	Symbol	Test Condition	WB SOIC-16	Unit
Safety temperature	$T_S$		150	°C
Safety input current	$I_S$	$\theta_{JA} = 55\text{ °C/W}$ (WB SOIC-16), $V_{DDA} = 5.5\text{ V}$ , $T_J = 150\text{ °C}$ , $T_A = 25\text{ °C}$	413	mA
Device power dissipation	$P_D$		2.27	W

**Note:**

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in [Figure 4.20 WB SOIC-16 Thermal Derating Curve \(Dependence of Safety Limiting Current\)](#) on page 18.

**Table 4.8. Thermal Characteristics**

Parameter	Symbol	WB SOIC-16	Unit
IC junction-to-air thermal resistance	$\theta_{JA}$	55	°C/W

**Figure 4.20. WB SOIC-16 Thermal Derating Curve (Dependence of Safety Limiting Current)**

**Table 4.9. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Min	Max	Unit
Storage temperature	T <sub>STG</sub>	–65	+150	°C
Junction temperature	T <sub>J</sub>	—	+150	°C
Input supply voltage	VDD1, VDD2	–0.6	6.0	V
Voltage on any digital pin with respect to ground, Tx, TX_EN, Rx, RX_EN, V5_EN	V <sub>IN</sub>	–0.5	VDD + 0.5	V
Bus fault protection		–30	30	V
Voltage on bus pin with respect to ground	VOC	–60	60	V
Receiver output current	IO		10	mA
Lead solder temperature (10 s)		—	260	°C
ESD per JEDEC	HBM, bus pins only		15	kV
	CDM, bus pins only		2	kV
	HBM, all other pins		4	kV
	CDM, all other pins		1.5	kV
ESD per AEC-Q100	HBM	—	4	kV
	CDM	—	500	V
Maximum isolation (input-to-output, 1 sec)		—	6000	VRMS

**Note:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5. Pinout Diagrams

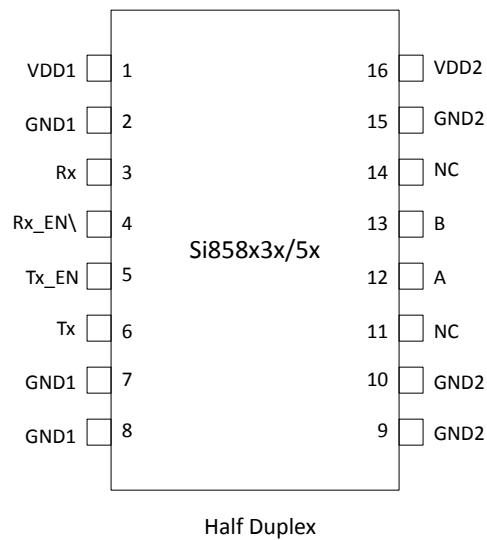


Figure 5.1. Pinout Diagram for Half Duplex Transceivers

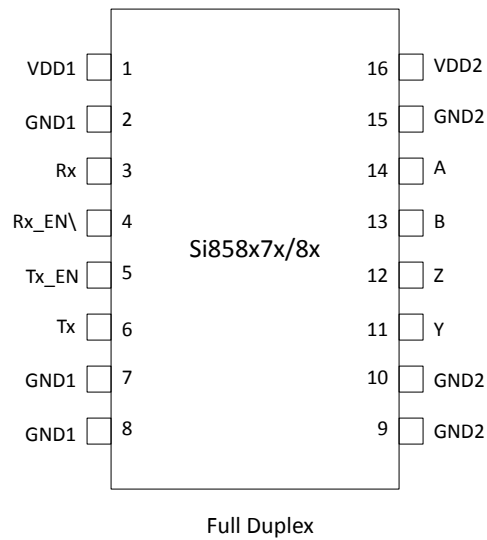


Figure 5.2. Pinout Diagram for Full Duplex Transceivers

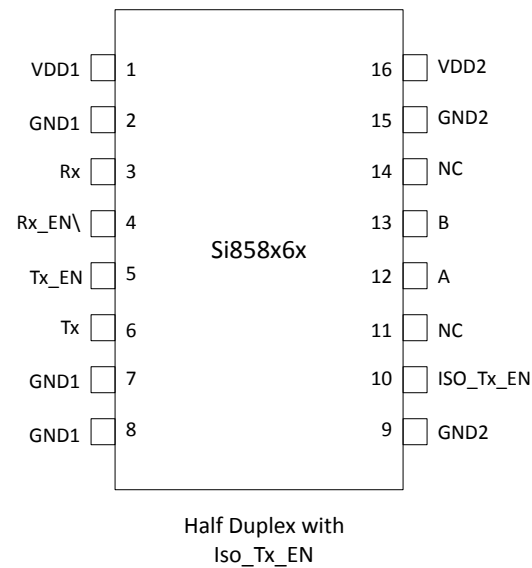


Figure 5.3. Pinout Diagram for Half Duplex with Isolated Tx\_EN

## 6. Pin Descriptions

**Table 6.1. Pin Descriptions**

Pin Name	Description
<b>Logic side</b>	
VDD1	Logic side supply voltage
NC	Not connected
Tx	Driver input
Tx_EN	Driver enable, with internal pull-up resistor. When open or driven high, driver is enabled.
Rx_EN\	Rx enable (active low), with internal pull-down resistor. When open or driven low, the receiver is enabled.
Rx	Receiver output
GND1	Logic side supply ground
<b>Transceiver (bus) side</b>	
GND2	Bus side supply ground
Y, Z	Driver output bus pins for full duplex (Si858x7, Si858x8)
A, B	Receiver input bus pins for full duplex (Si858x7, Si858x8) or driver/receiver bus pins for half duplex (Si858x3, Si858x5, Si858x6)
ISO_Tx_EN	Isolated Tx_EN feedthrough
VDD2	Bus side supply voltage, selectable through V5_EN pin

Technical drawing of a mechanical part, likely a valve or actuator component, showing multiple views and dimensions.

**Views:**

- Top View:** Shows the overall dimensions  $D$  and  $E$ . It includes a central circular feature and a rectangular section with a circle. Dimensions  $E/2$  and  $E1/2$  are indicated. A section line  $A-A$  is shown.
- Front View:** Shows the profile of the component. It includes a circular feature and a rectangular section. Dimensions  $A$ ,  $A1$ , and  $A2$  are indicated. A section line  $B-B$  is shown.
- Side View:** Shows the profile of the component. It includes a circular feature and a rectangular section. Dimensions  $B$  and  $C$  are indicated. A section line  $C-C$  is shown.
- Detail View (Top Right):** Shows a close-up of the top surface. It includes a circular feature and a rectangular section. Dimensions  $D$  and  $E$  are indicated. A section line  $A-A$  is shown.
- Detail View (Bottom Right):** Shows a close-up of the side surface. It includes a circular feature and a rectangular section. Dimensions  $H$  and  $C$  are indicated. A section line  $B-B$  is shown.

**Dimensions and Callouts:**

- $2X$ : Material specification for the top and front views.
- $16X$ : Material specification for the side view.
- $16X\ b$ : Material specification for the detail view (Top Right).
- $2X\ 8\ TIPS$ : Material specification for the detail view (Bottom Right).
- $A$ ,  $A1$ ,  $A2$ ,  $B$ ,  $C$ ,  $D$ ,  $E$ ,  $E1$ ,  $E1/2$ ,  $L$ ,  $h$ ,  $c$ ,  $e$ : Various dimensions and callouts.
- $SEATING\ PLANE$ : A horizontal line indicating the seating plane of the component.
- $\theta$ : An angle dimension.

### Table 7.1. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	θ°	8°
aaa	—	0.10

Symbol	Millimeters	
	Min	Max
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
4. All dimensions shown are in millimeters (mm) unless otherwise noted.

8. Land Pattern

The following figure illustrates the recommended land pattern details for the Si858x in a WB SOIC-16. The table lists the values for the dimensions shown in the illustration.

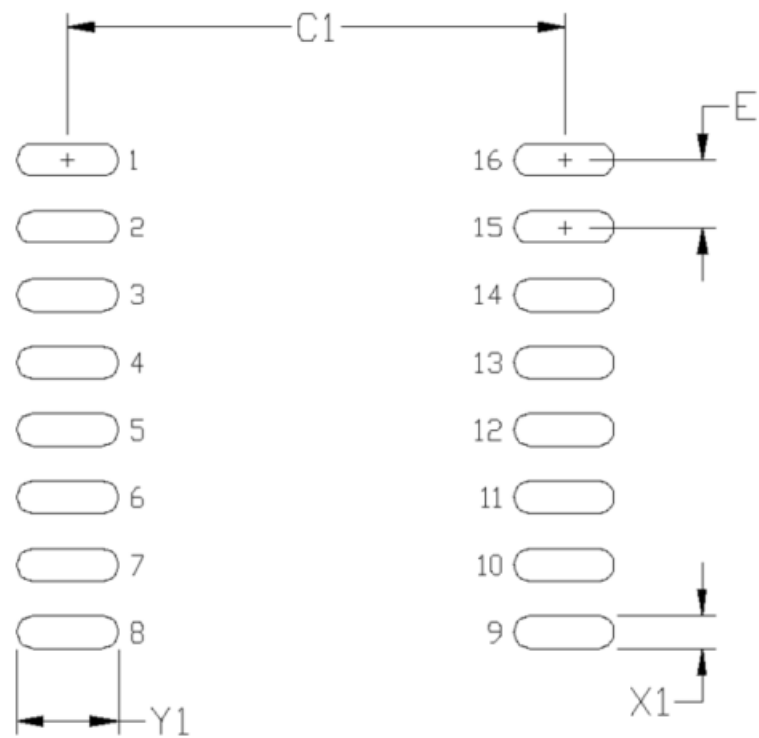


Figure 8.1. WB SOIC-16 PCB Land Pattern

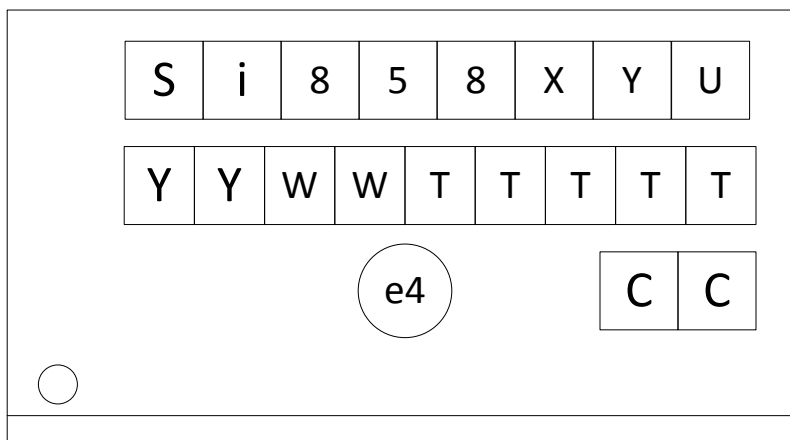
Table 8.1. WB SOIC-16 Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

**Note:**

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 9. Top Marking



**Table 9.1. WB SOIC-16 Top Marking Explanation**

Line 1 Marking:	<p>Base Part Number</p> <p>Ordering Options</p> <p>(See Ordering Guide for more information).</p>	<p>Si858 = Isolated RS-485 Transceiver</p> <p>X = VDD2 nominal supply voltage:</p> <ul style="list-style-type: none"> <li>• 3 = 3.3 V</li> <li>• 5 = 5.0 V</li> </ul> <p>Y = Transceiver type:</p> <ul style="list-style-type: none"> <li>• 3 = 1 Mbps half duplex</li> <li>• 5 = 10 Mbps half duplex</li> <li>• 6 = 10 Mbps half duplex with isolated Tx_EN pin</li> <li>• 7 = 1 Mbps full duplex</li> <li>• 8 = 10 Mbps full duplex</li> </ul> <p>U = Isolation rating:</p> <ul style="list-style-type: none"> <li>• D = 5.0 kV</li> </ul>
Line 2 Marking:	<p>YY = Year</p> <p>WW = Workweek</p>	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTT = Mfg Code	Manufacturing code from assembly purchase order form.
Line 3 Marking:	<p>Circle = 1.5 mm Diameter</p> <p>(Center-Justified)</p>	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

## 10. Revision History

### Revision 0.2

May, 2022

- Initial release.

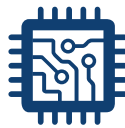


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