

## 3A, Ultra-Low Dropout Voltage Regulator

### General Description

The RT9059A is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a VIN as low as 1V and VDD voltage 3V with programmable output voltage as low as 0.8V. The RT9059A features ultra-low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shutdown. The RT9059A provides excellent regulation over variations in line, load and temperature. The RT9059A provides a power good signal to indicate if the voltage level of  $V_O$  reaches 90% of its rating value.

### Ordering Information

RT9059A□□

- Package Type  
QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System  
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

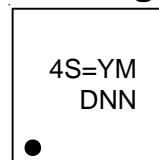
### Features

- Output Current up to 3A
- High Accuracy ADJ Voltage 1.5%
- Dropout Voltage 350mV @ 3A Typically
- VOUT Power Good Signal
- VOUT Pull Low Resistance when Disable
- Current-Limit Protection
- Thermal Shutdown Protection
- RoHS Compliant and Halogen Free

### Applications

- Notebook PC Applications
- Motherboard Applications

### Marking Information

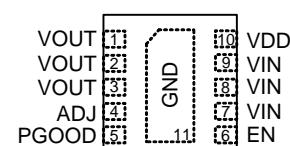


4S= : Product Code

YMDNN : Date Code

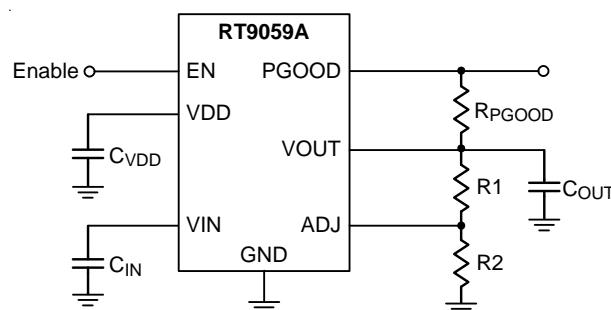
### Pin Configuration

(TOP VIEW)



WDFN-10L 3x3

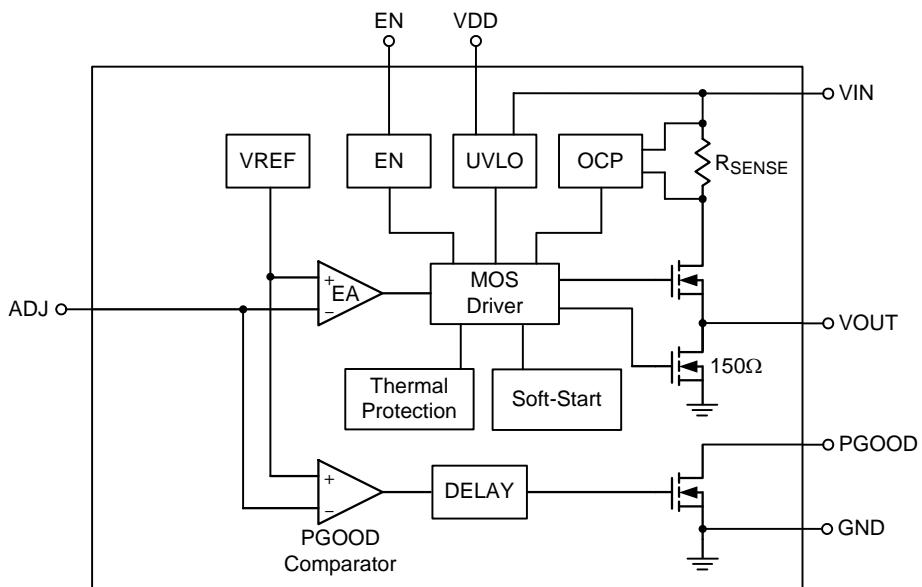
### Simplified Application Circuit



## Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2, 3	VOUT	Output voltage.
4	ADJ	Output voltage setting. $VOUT = V_{REF} \times (R1 + R2) / R2$ .
5	PGOOD	Power good open-drain output.
6	EN	Enable control input.
7, 8, 9	VIN	Supply voltage input.
10	VDD	Supply voltage of control circuit.
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

## Functional Block Diagram



## Operation

The RT9059A is a high performance positive voltage regulator designed for use in very low input voltage and very low dropout voltage with high output current up to 3A.

### Output Transistor

The RT9059A includes a built-in low dropout N-MOSFET output transistor for low input voltage and high output current applications.

### Error Amplifier

The Error Amplifier compares output feedback voltage from an internal feedback voltage divider or from ADJ pin to an internal reference voltage and controls the N-MOSFET gate voltage to maintain output voltage regulation.

### Soft-Start

The RT9059A provides soft-start function to prevent large in-rush current during power on period.

### Current Limit and Over-Temperature Protection

The RT9059A provides a current limit function to prevent damage during output over-load or short-circuit conditions. The output current is detected by an internal sensing transistor.

The RT9059A also equips Over-Temperature Protection (OTP) function. When the internal junction temperature exceeds 160°C, OTP function will turn off the N-MOSFET. Once the junction temperature cools down below 90°C, the RT9059A will resume operation automatically.

**Absolute Maximum Ratings** (Note 1)

- Supply Input Voltage, VIN to GND
 

DC	–0.3V to 6V
< 10ms	–0.3V to 7V
- Control Voltage, VDD to GND
 

DC	–0.3V to 6V
< 10ms	–0.3V to 7V
- Output Voltage, VOUT ----- –0.3V to 6V
- Chip Enable Voltage, EN ----- –0.3V to 6V
- Adjust Voltage, ADJ ----- –0.3V to 6V
- Power Good Voltage, V<sub>PGOOD</sub> ----- –0.3V to 6V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C
 

WDFN-10L 3x3	3.04W
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- Package Thermal Resistance (Note 2)
 

WDFN-10L 3x3, θ <sub>JA</sub>	32.8°C/W
WDFN-10L 3x3, θ <sub>JC</sub>	5.9°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- –65°C to 150°C
- ESD Susceptibility (Note 3)
 

HBM (Human Body Model)	2kV
MM (Machine Model)	200V

**Recommended Operating Conditions** (Note 4)

- Supply Input Voltage, VIN ----- 1V to 5V
- Control Voltage, VDD (V<sub>DD</sub> > V<sub>OUT</sub> + 1.5V) ----- 3V to 5.5V
- Junction Temperature Range ----- –40°C to 125°C
- Ambient Temperature Range ----- –40°C to 85°C

**Electrical Characteristics**(V<sub>DD</sub> = 5V, C<sub>IN</sub> = C<sub>OUT</sub> = 10μF, C<sub>VDD</sub> = 1μF, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Operation Range	V <sub>DD</sub>		3	--	5.5	V
VDD POR Threshold	V <sub>POR_VDD</sub>	V <sub>DD</sub> rising	2.4	2.7	3	V
VDD POR Falling Hysteresis	ΔV <sub>POR_VDD</sub>	V <sub>DD</sub> falling	0.15	0.2	--	V
Input Voltage Range	V <sub>IN</sub>		1	--	5.5	V
VIN POR Threshold	V <sub>POR_VIN</sub>	V <sub>IN</sub> rising	0.7	0.8	0.9	V
VIN POR Falling Hysteresis	ΔV <sub>POR_VIN</sub>	V <sub>IN</sub> falling	0.15	0.2	0.25	V
Quiescent Current	I <sub>Q</sub>	EN On, no load	--	0.6	1.2	mA
Reference Voltage	V <sub>REF</sub>		0.788	0.8	0.812	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy			-1.5	--	1.5	%
V <sub>OUT</sub> Load Regulation	$\Delta V_{LOAD}$	$I_{OUT} = 1\text{mA to } 3\text{A}$ , $V_{IN} = V_{OUT} + 1\text{V}$	--	0.5	1	%
OUT Line Regulation	$\Delta V_{LINE}$	$V_{DD} = 3.6\text{V to } 5.5\text{V}$ , $V_{IN} = V_{OUT} + 1\text{V to } 5\text{V}$ , $I_{OUT} = 1\text{mA}$	--	0.2	0.6	%
Dropout Voltage	$V_{DROP}$	$I_{OUT} = 2\text{A}$	--	250	350	mV
		$I_{OUT} = 3\text{A}$	--	350	450	
Current Limit	$I_{LIM}$	$V_{IN} = 3.6\text{V}$	3.1	3.6	4.2	A
Short Circuit Current	$I_{SC}$	$V_{OUT} < 0.2\text{V}$	1	1.4	1.8	A
V <sub>OUT</sub> Pull Low Resistance	$R_{PULL}$	$V_{EN} = 0\text{V}$	--	150	--	$\Omega$
Thermal Shutdown Temperature	$T_{SD}$		--	160	--	$^{\circ}\text{C}$
Thermal Shutdown Recovery Temperature	$T_{SDR}$		--	90	--	$^{\circ}\text{C}$
PGOOD Rising Threshold	$V_{TH\_PGOOD}$	$V_{OUT}$ rising	--	90	--	%
PGOOD Hysteresis	$\Delta V_{TH\_PGOOD}$	$V_{OUT}$ falling	--	10	--	%
PGOOD Delay Time			0.2	1	1.5	ms
PGOOD Sink Capability	$V_{PGOOD}$	$I_{SINK} = 10\text{mA}$	--	0.2	0.4	V
EN Input Voltage	Logic-High	$V_{IH}$	1.2	--	--	V
	Logic-Low	$V_{IL}$	--	--	0.4	
EN Delay Time			0.3	0.85	1.4	ms
EN Pin Bias Current	$I_{EN}$	$V_{EN} = 0\text{V}$	--	12	--	$\mu\text{A}$
V <sub>DD</sub> Pin Shutdown Current	$I_{SHDN\_VDD}$	$V_{EN} = 0\text{V}$	--	15	30	$\mu\text{A}$
V <sub>IN</sub> Pin Shutdown Current	$I_{SHDN\_VIN}$	$V_{EN} = 0\text{V}$ , $V_{IN} = 5\text{V}$	--	--	1	$\mu\text{A}$
Inrush Current	$I_{INRUSH}$	$V_{OUT} = 1.8\text{V}$ , $C_{OUT} = 10\mu\text{F}$ , $I_{LOAD} = 1\text{A}$	--	0.5	--	A
Soft-Start Time	$t_{SS}$		1.9	2.8	3.75	ms

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

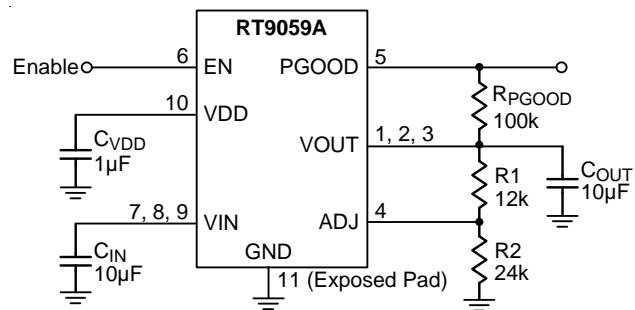
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^{\circ}\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

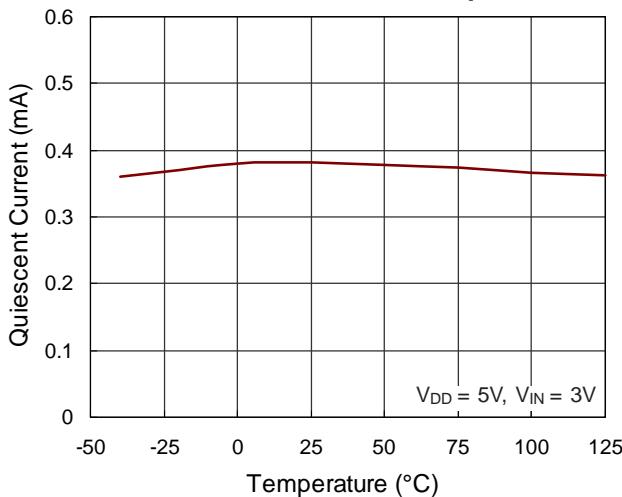


$$V_{OUT} = 0.8 \times (R1 + R2) / R2$$

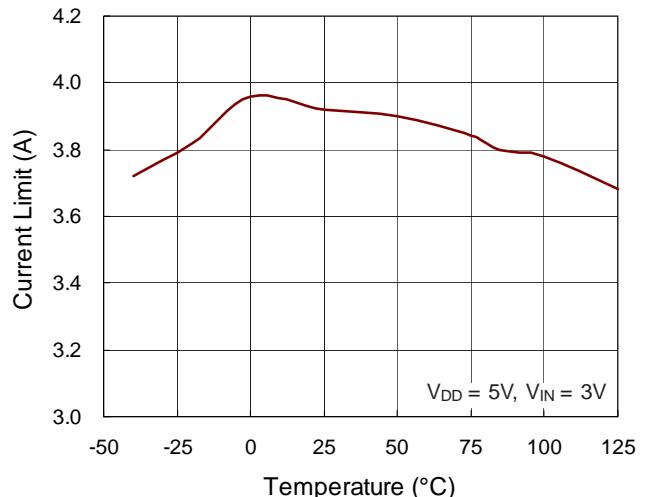
Figure 1. Adjustable Voltage Regulator

## Typical Operating Characteristics

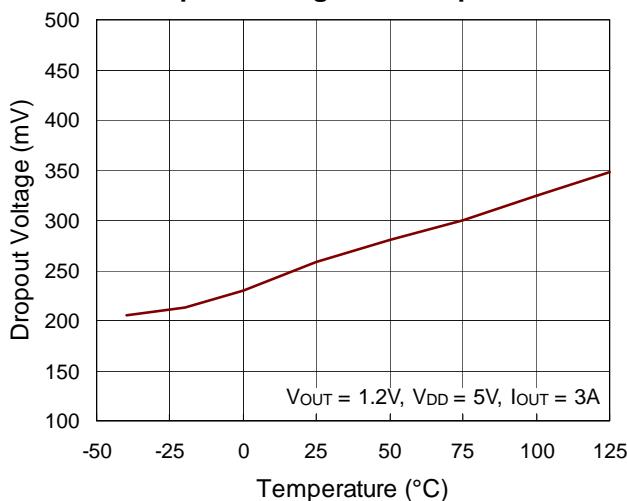
Quiescent Current vs. Temperature



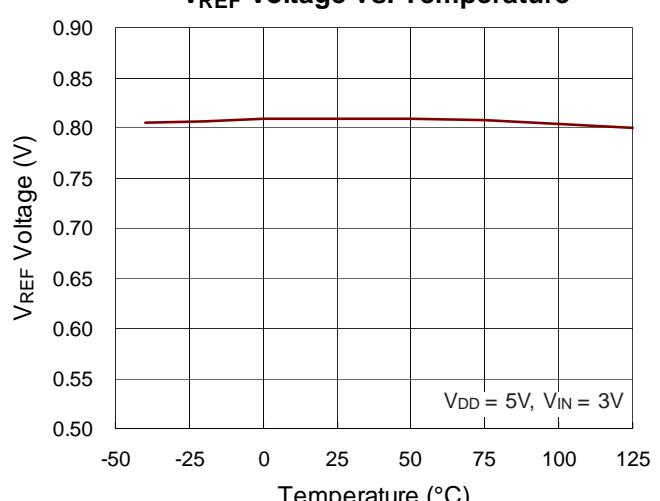
Current Limit vs. Temperature



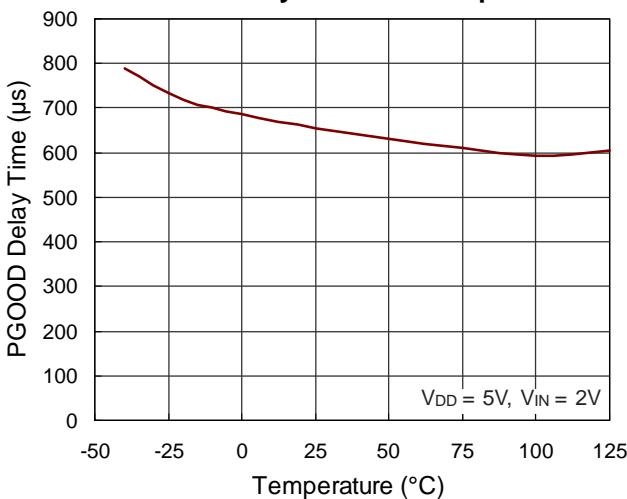
Dropout Voltage vs. Temperature



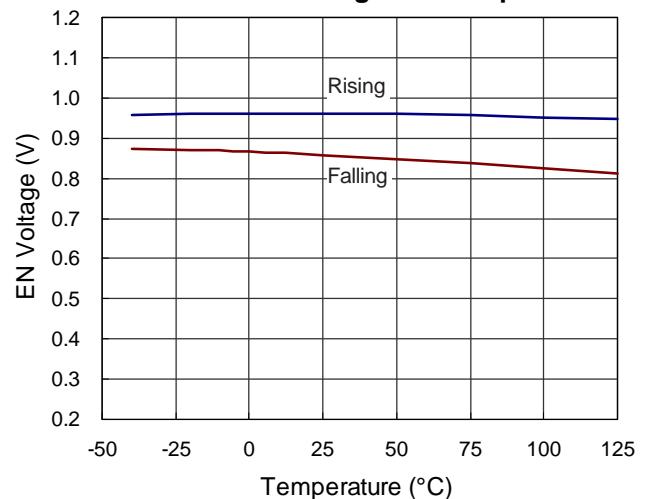
$V_{REF}$  Voltage vs. Temperature

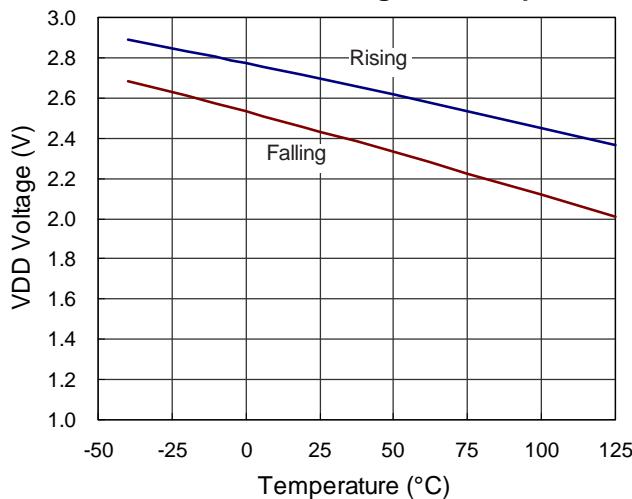
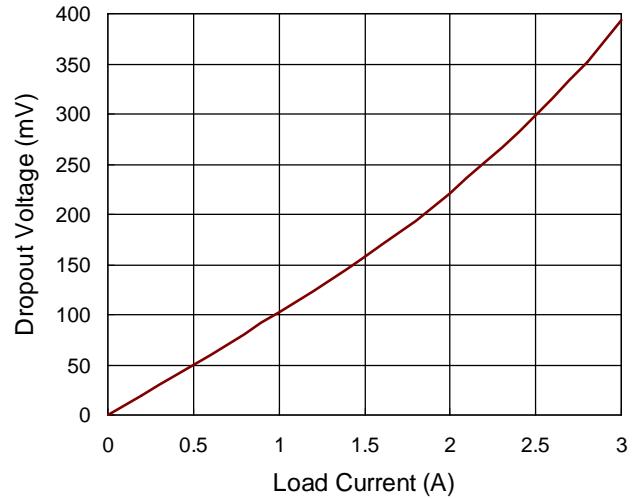
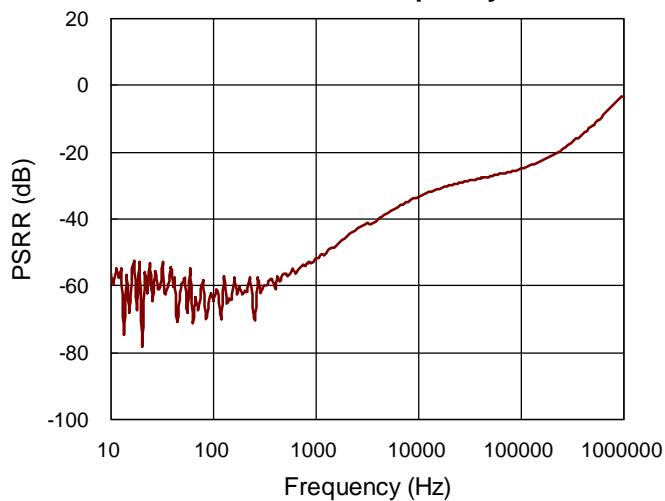
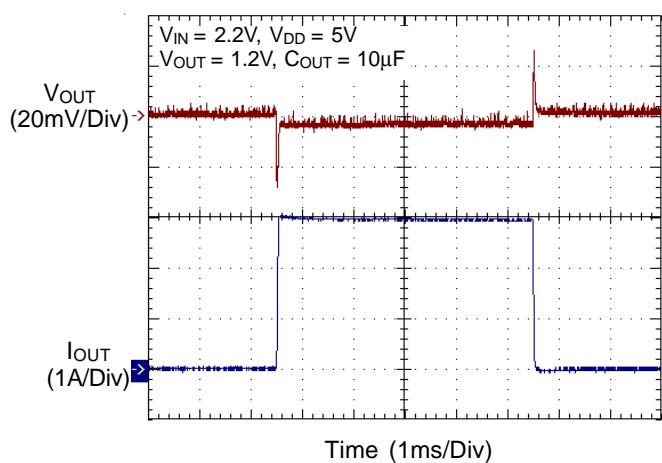
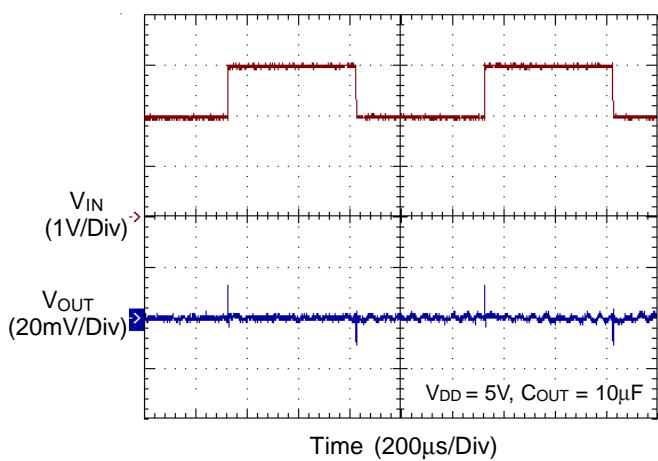
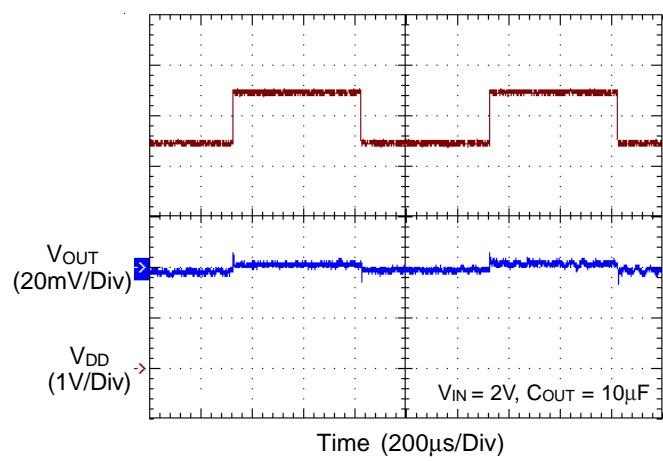


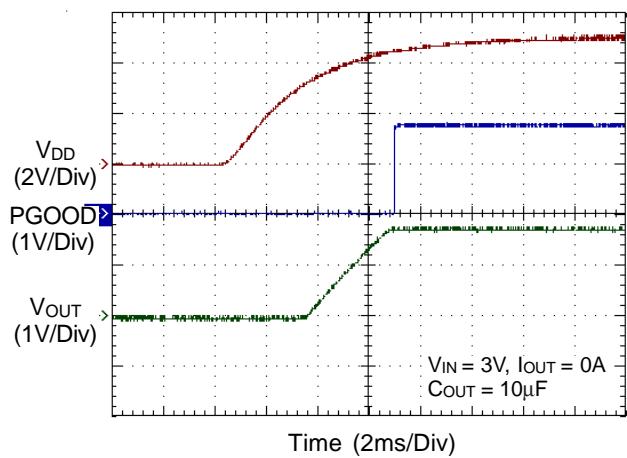
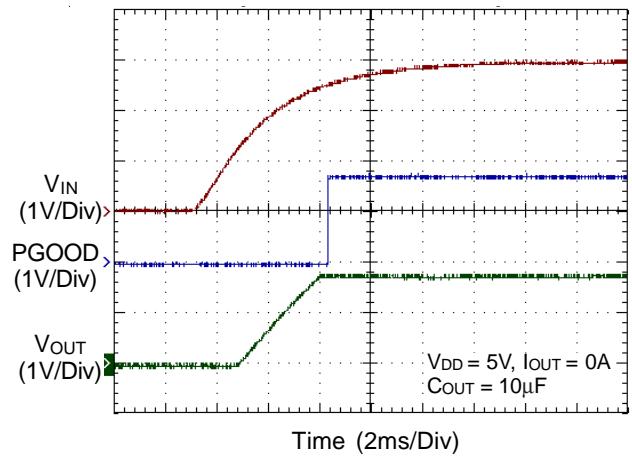
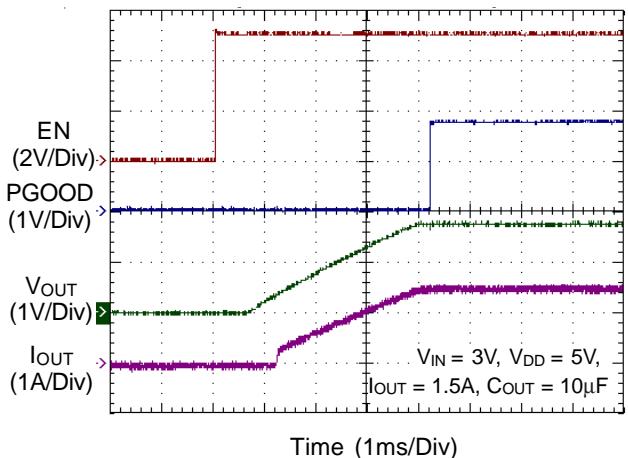
PGOOD Delay Time vs. Temperature



EN Threshold Voltage vs. Temperature



**VDD POR Threshold Voltage vs. Temperature****Dropout Voltage vs. Load Current****PSRR vs. Frequency****Load Transient Response** **$V_{IN}$  Line Transient Response** **$V_{DD}$  Line Transient Response**

**Start Up from  $V_{DD}$** **Start Up from  $V_{IN}$** **Start Up from Enable and PGOOD Delay**

## Applications Information

### Adjustable Mode Operation

The output voltage of RT9059A is adjustable from 0.8V to VIN by external voltage divider resistors as shown in Typical Application Circuit (Figure 1). The value of resistors R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation :

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right)$$

where  $V_{REF}$  is the reference voltage (0.8V typical).

### Enable

The RT9059A goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 1µA typical. The RT9059A goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, please notice the RT9059A internal initial logic level. For the RT9059A, the EN pin function pulls high level internally. So the regulator will be turned on when EN pin is floating.

### Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10µF input capacitor or greater located as close as possible to the IC is recommended.

### Output Capacitor

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs applications. The RT9059A is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a at least 10µF ceramic capacitor on the RT9059A output ensures stability. The RT9059A still works well with output capacitor of other types due to the wide stable ESR range. Figure 5 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located no more than 0.5 inch from the VOUT pin of the RT9059A and returned to a clean analog ground.

### Region of Stable $C_{OUT}$ ESR vs. Output Current

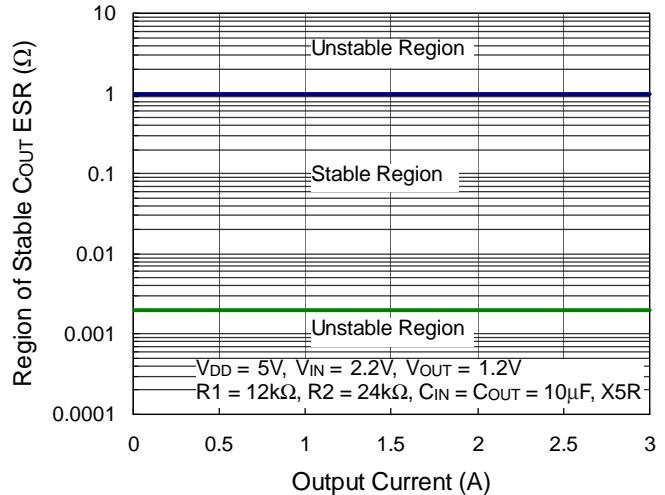


Figure 2. Region of Stable  $C_{OUT}$  ESR vs. Output Current

### Current Limit

The RT9059A contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimum limiting the output current to 3.1A typical. When the output voltage is less than 0.2V, the short circuit current protection starts the current fold back function and maintains the loading current at maximum 1.8A. The output can be shorted to ground indefinitely without damaging the part.

### Power Good

The power good function is an open-drain output. Connect a 100kΩ pull-up resistor to  $V_{OUT}$  to obtain an output voltage. The PGOOD pin will output high immediately after the output voltage arrives 90% of normal output voltage.

### Thermal Shutdown Protection

Thermal protection limits power dissipation to prevent the IC from overheat. When the operation junction temperature exceeds 160°C, the over-temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For WDFN-10L 3x3 package, the thermal resistance,  $\theta_{JA}$ , is 32.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (32.8^\circ\text{C/W}) = 3.04\text{W} \text{ for WDFN-10L 3x3 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

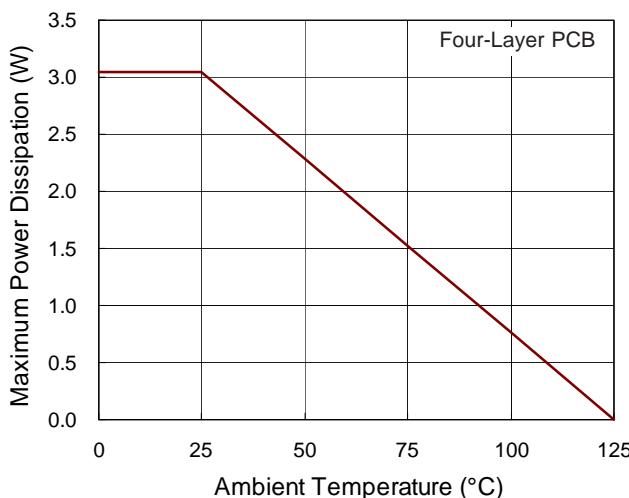
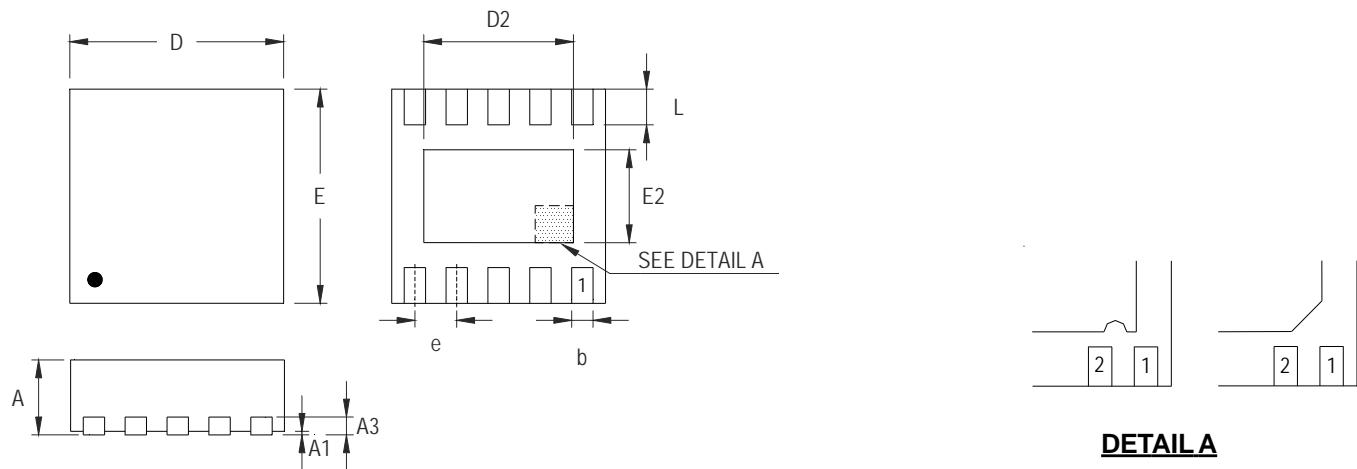


Figure 3. Derating Curve of Maximum Power Dissipation

## Outline Dimension

**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

**W-Type 10L DFN 3x3 Package****Richtek Technology Corporation**14F, No. 8, Tai Yuen 1<sup>st</sup> Street, Chupei City

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Tel: (8863)5526789

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