

MSKSEMI 美森科

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

MSTPS7A20xxPDQNR

Product specification

GENERAL DESCRIPTION

The MSTPS7A20xxPDQNR is a low- I_Q low dropout linear regulator with 300mA driving current. The MSTPS7A20xxPDQNR shows good power dissipation with $<0.1\mu A$ shutdown current and 0.8uA quiescent current of light load for portable devices. The MSTPS7A20xxPDQNR provides 0.8~3.6V output voltage for multiple application and it is with build-in thermal shutdown and current limit protection functions.


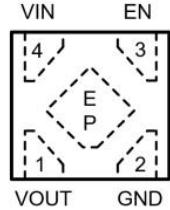
FEATURES

- 0.8uA quiescent current at light load
- $\pm 2\%$ output voltage accuracy
- 1.5~5.5V input range
- 0.8~3.6V output range
- Thermal shutdown protection
- Current limit protection
- RoHS Compliant and Halogen Free


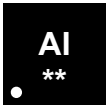
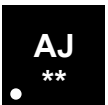
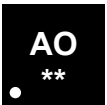



APPLICATIONS

- Cellular and smart phone
- Audio/Video equipment
- Battery-power equipment
- Portable electric devices

Reference News

DFN-4L(1x1)	Pin Configuration
	

MARKING

MSTPS7A2012PDQNR	MSTPS7A2015PDQNR	MSTPS7A2018PDQNR	MSTPS7A2025PDQNR	MSTPS7A2028PDQNR	MSTPS7A2030PDQNR	MSTPS7A2033PDQNR
						

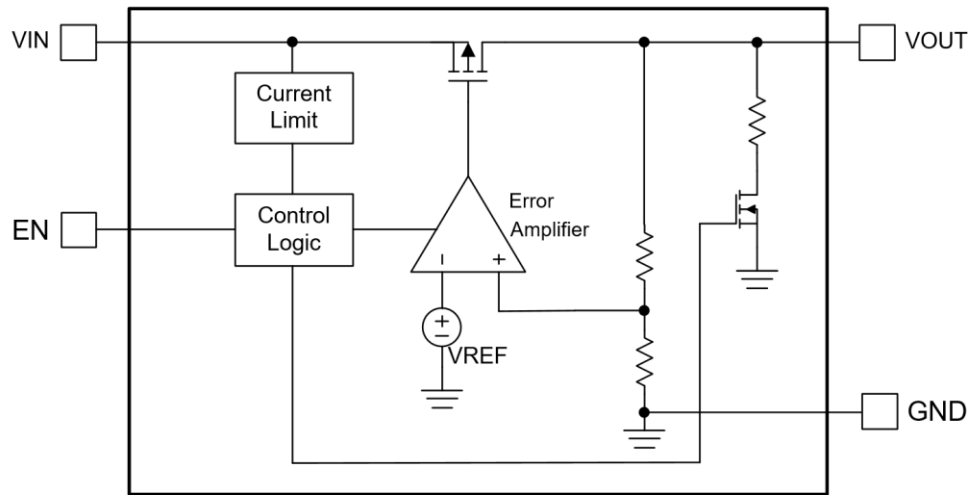
ORDER INFORMATION

P/N	PKG	QTY
MSTPS7A2012PDQNR	DFN-4L(1x1)	10000PCS
MSTPS7A2015PDQNR		
MSTPS7A2018PDQNR		
MSTPS7A2025PDQNR		
MSTPS7A2028PDQNR		
MSTPS7A2030PDQNR		
MSTPS7A2033PDQNR		

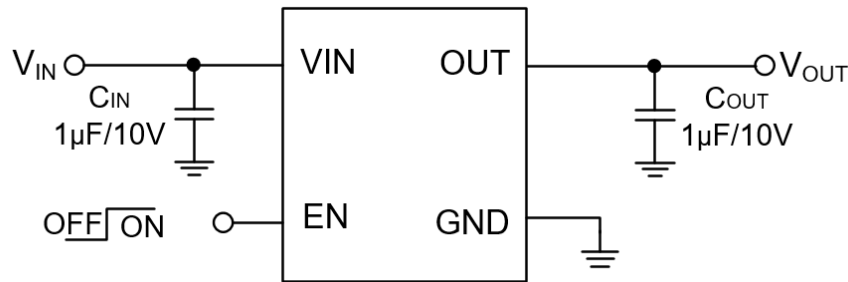
Pin Description

Pin No	Pin Name	Pin Description
DFN-4L(1x1)		
4	VIN	Input of the regulator.
2	GND	Ground.
3	EN	Enable control input, Active High.
--	NC	No Internal Connection.
1	VOUT	Output of the regulator.
EP	Exposed Pad	The exposed pad should be connected to a large ground plane to maximize thermal performance.

Functional Block Diagram



Typical Application Circuit



Absolute Maximum Ratings (Note 1)

VIN	-----	-0.3V to 6.0V
VOUT	-----	-0.3V to 6.0V
EN	-----	-0.3V to 6.0V
VOUT to VIN	-----	-6V to 0.3V
Power Dissipation, PD @ TA = 25°C		
DFN-4L(1x1)	-----	0.4W
Package Thermal Resistance		
DFN-4L(1x1), θJA	-----	250°C/W
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Junction Temperature	-----	150°C
Storage Temperature Range	-----	-55°C to 150°C
ESD Susceptibility		
HBM (Human Body Model)	-----	2kV
CDM (Charged Device Model)	-----	200V

Recommended Operating Conditions

VIN	-----	1.5V to 5.5V
Junction Temperature Range	-----	-40°C to 125°C

Electrical Characteristics

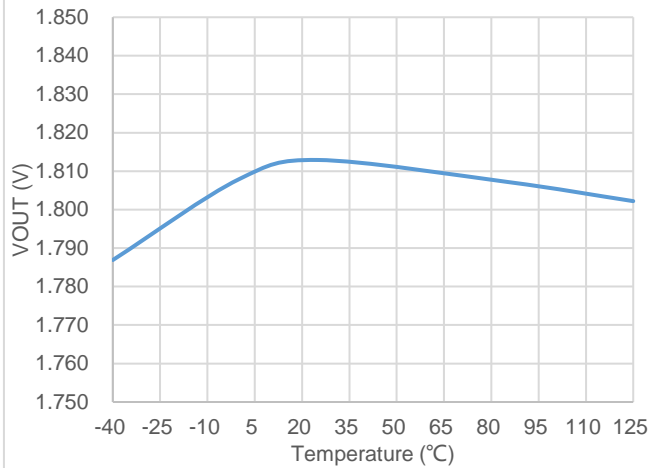
VIN = EN = 5V, CIN=1μF, COUT=1μF, TA=25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	VIN		1.5		5.5	V
Output Voltage Accuracy	VOUT	VIN=VOUT+1V, IOUT=10mA	-2		+2	%
VIN Shut Down Current	ISD	EN=0V			0.1	μA
VIN Quiescent Current	IQ	VIN > VOUT, EN=VIN, no load		0.8	1	μA
Current Limit	ILIMIT	VIN=5V, Load = VOUT*90%		500		mA
Short Current	ISC	VOUT=0V		150		mA
Dropout Voltage (Note 2)	VDROP	VOUT=3.3V, IOUT=200mA		180		mV
		VOUT=2.8V, IOUT=200mA		200		
		VOUT=1.8V, IOUT=200mA		280		
		VOUT=1.2V, IOUT=200mA		420		
Line Regulation	ΔVLINE	VIN=VOUT+0.5V to 5.5V IOUT=20mA		5		mV
Load Regulation	ΔVLOAD	IOUT=1mA to 300mA		20		mV
Enable High Voltage	VENH		1.5			V
Enable Low Voltage	VENL				0.4	V
Power Supply Rejection Rate	PSRR	f=100Hz and IOUT=10mA		66		dB
		f=1kHz and IOUT=10mA		50		
Output Noise Voltage	eNO	10Hz to 100kHz and COUT=1uF		80		μVRMS
Output Discharge Resistance	Rdischg			60		Ω
Thermal Shutdown Threshold	TSD			165		°C
Thermal Shutdown Hysteresis	ΔTSD			20		°C

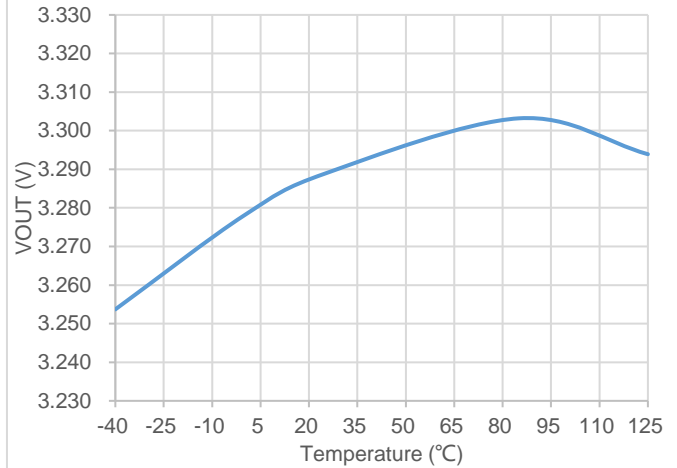
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. The dropout voltage is defined as VIN – VOUT, when VOUT is 95% of the normal value of VOUT.

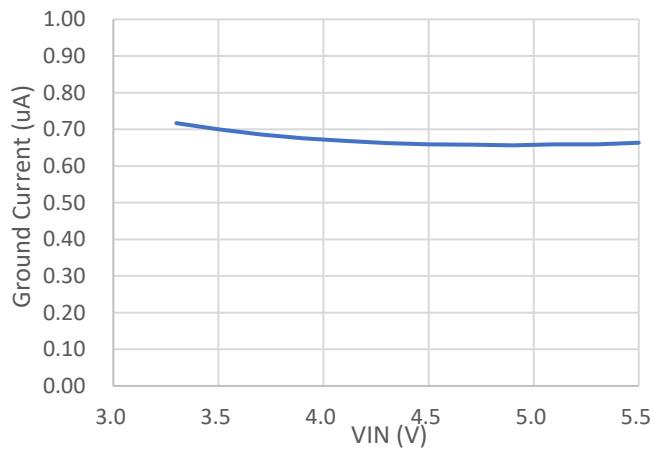
Typical Operating Characteristics



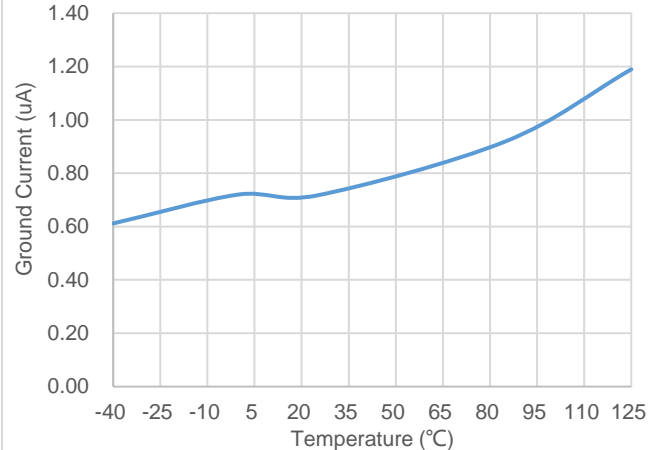
Output Voltage vs Temperature
VIN = 2.8V, VOUT = 1.8V, IOUT = 20mA



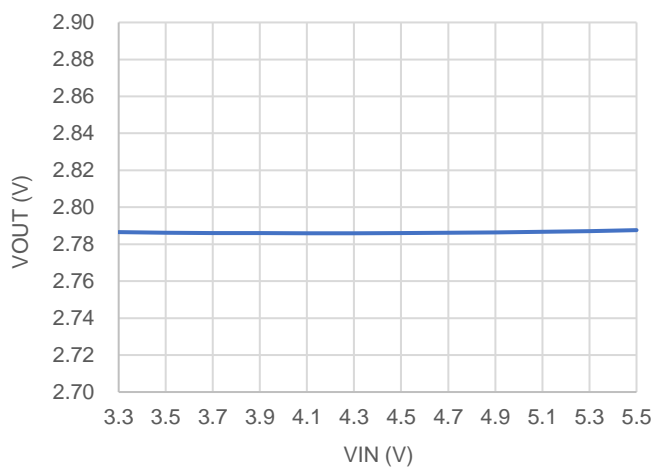
Output Voltage vs Temperature
VIN = 4.3V, VOUT = 3.3V, IOUT = 20mA



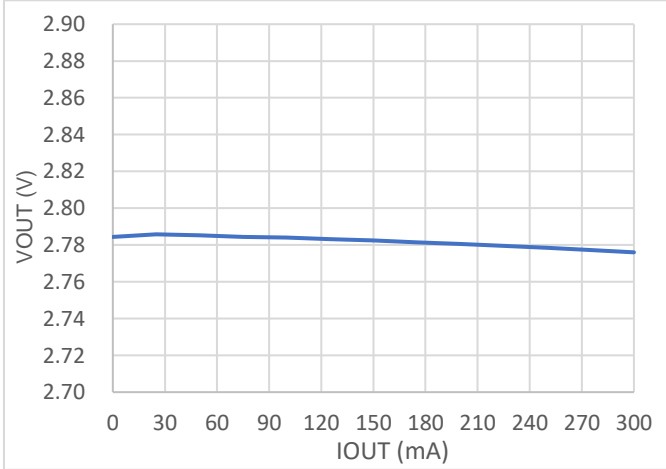
Ground Current vs Input Voltage
VOUT = 2.8V, no load



Ground Current vs Temperature
VIN = 3.3V, VOUT = 2.8V, no load

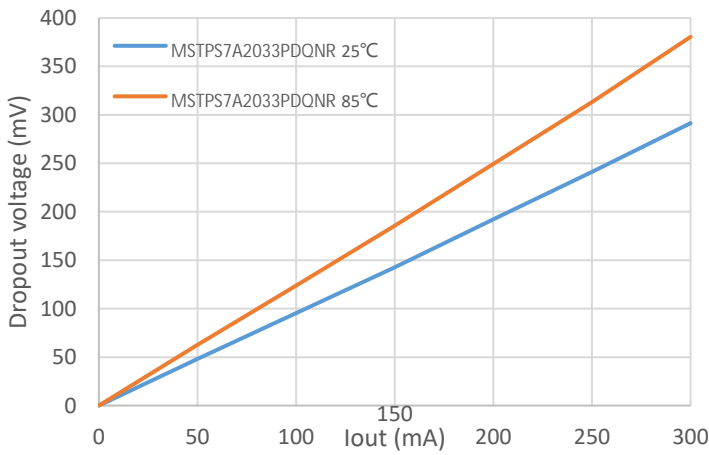


Output Voltage vs Input Voltage
VOUT = 2.8V, IOUT = 20mA

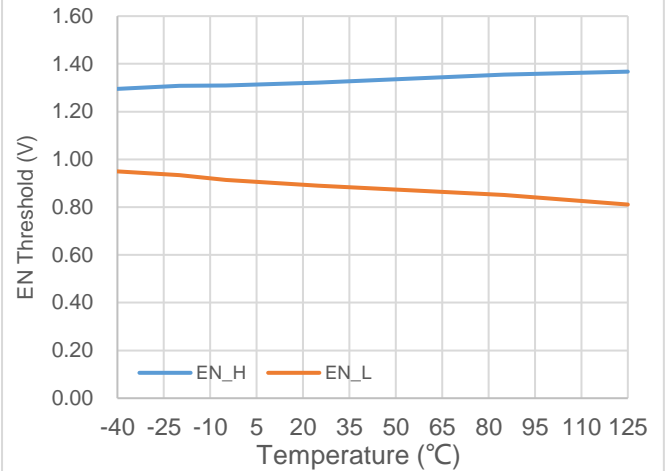


Output Voltage vs Output Current
VIN = 3.6V, VOUT = 2.8V

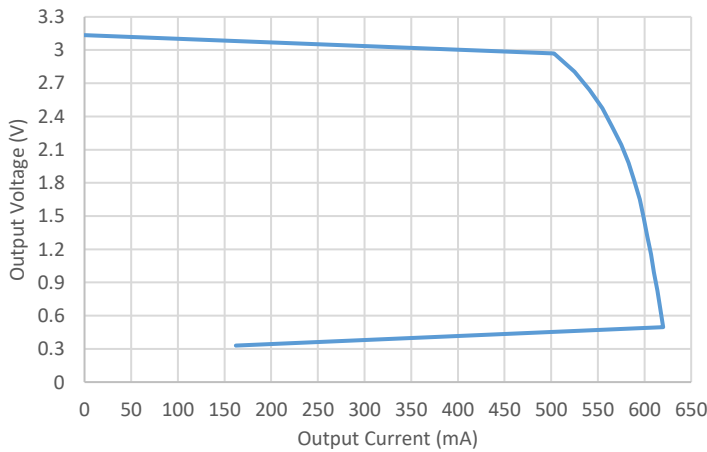
Typical Operating Characteristics(continued)



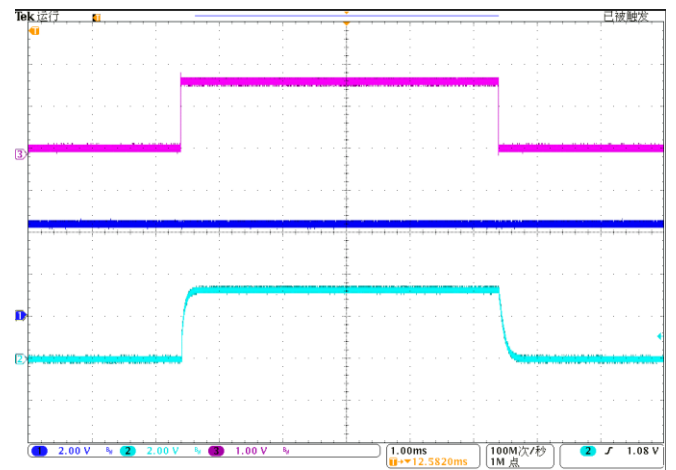
Dropout Voltage vs Output Current
VOUT = 3.3V



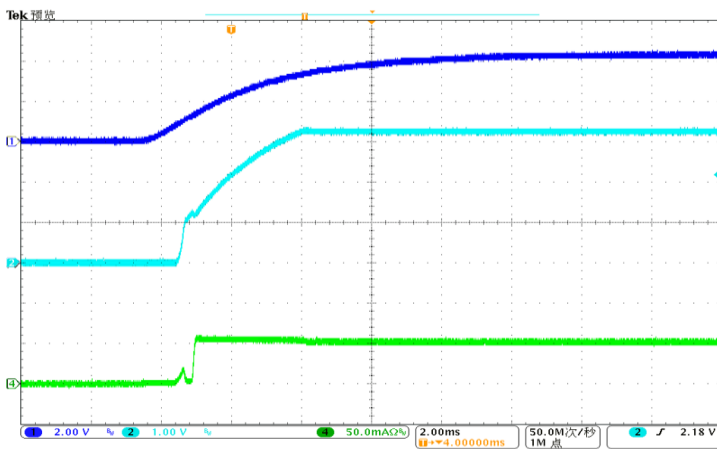
EN Threshold vs Temperature
VIN = 3.3V, VOUT = 2.8V



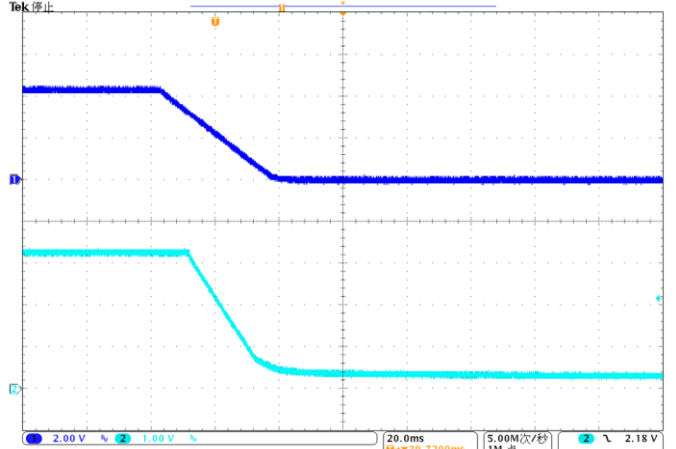
Output Voltage VS Output Current
VIN = 5V, VOUT = 3.3V



ON/OFF by EN (CH1 = VIN, CH2 = VOUT, CH3=EN)
VIN = 4.3V, VOUT = 3.3V

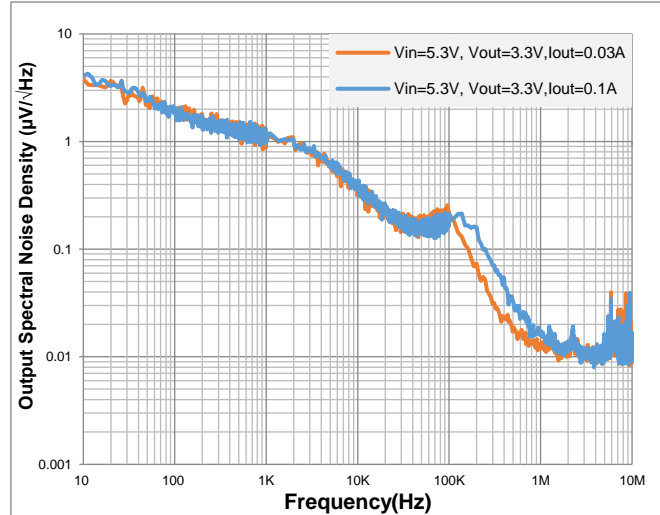
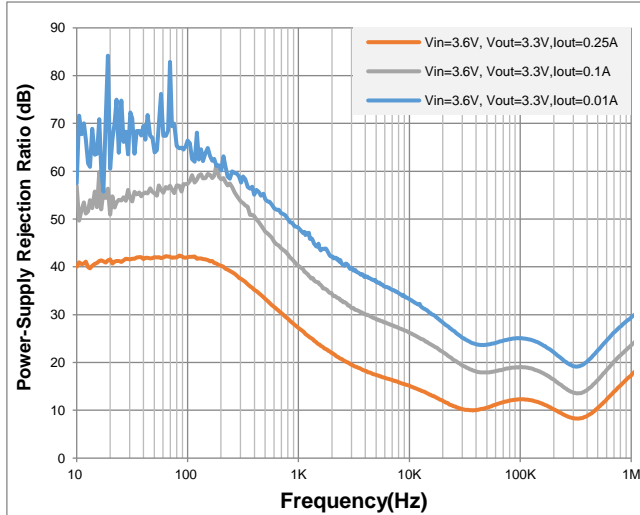
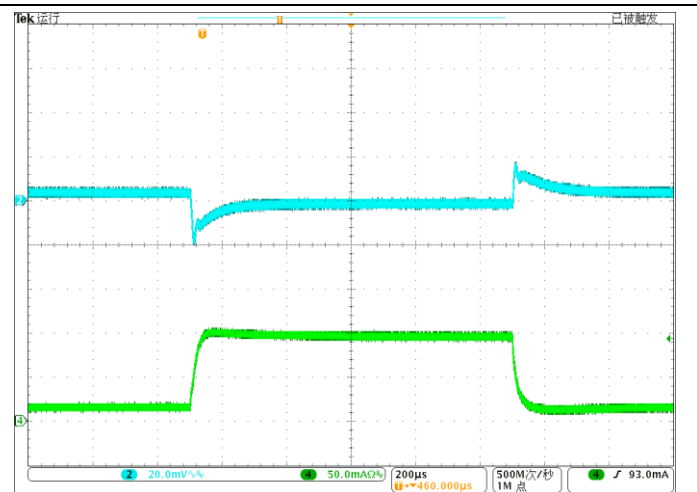
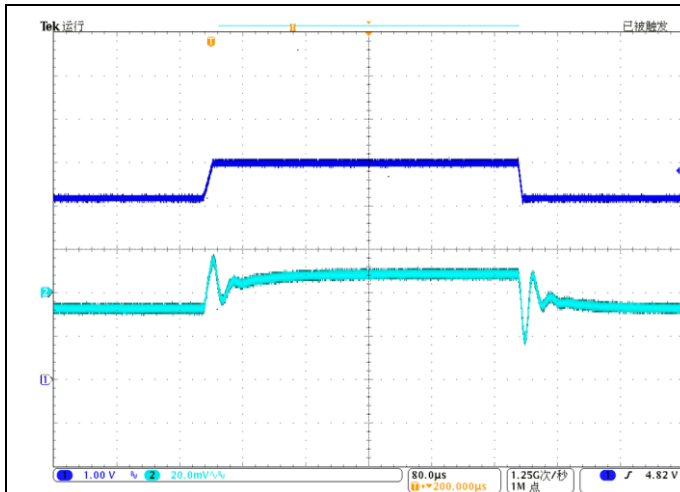


Power ON (CH1 = VIN, CH2 = VOUT, CH3 = IOUT)
VIN = EN, VOUT = 3.3V, IOUT = 50mA



Power OFF (CH1 = VIN, CH2 = VOUT)
VIN = EN, VOUT = 3.3V

Typical Operating Characteristics(continued)



Application Information

Input and Output Capacitor Requirements

The external input and output capacitors of MSTPS7A20xxPDQNR series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Enable Function

The MSTPS7A20xxPDQNR series has an EN pin to turn on or turn off the regulator. When the EN pin is in logic high, the regulator will be turned on. When the EN pin is in logic low, the shutdown current is almost 0μA typical. The EN pin may be directly tied to VIN to keep the part on.

Current Limit

The MSTPS7A20xxPDQNR series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 500mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Auto Discharge Function

The MSTPS7A20xxPDQNR series can discharge the output capacitor. When the VIN ready and EN pin is in logic low, the internal NMOS between VOUT and GND will be turned on. The discharge resistance (Rdischg) is 60Ω (at VIN=5V, typical).

Dropout Voltage

The MSTPS7A20xxPDQNR series use a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout condition.

OTP (Over Temperature Protection)

The over temperature protection function of MSTPS7A20xxPDQNR series will turn off the P-MOSFET when the junction temperature exceeds 165°C (typical). Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

Thermal Considerations

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

$$PD(\text{Max}) = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / (250^{\circ}\text{C/W}) = 0.4\text{W}$$

For SOT-23-5 / DFN1*1 packages.

$$PD(\text{Max}) = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / (330^{\circ}\text{C/W}) = 0.3\text{W}$$

For SOT23-3 package.

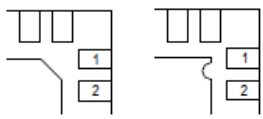
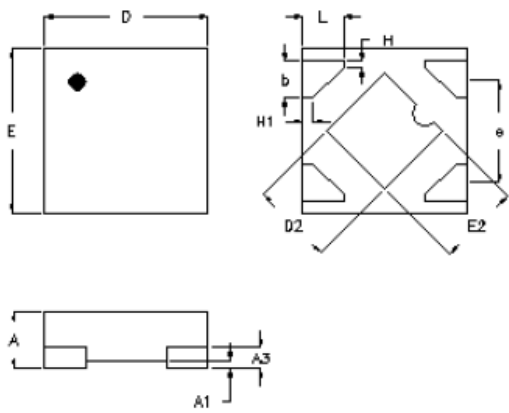
Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the MSTPS7A20xxPDQNR ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

DFN1*1 Package



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specification of any and all MSKSEMI Semiconductor products described or contained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

■ MSKSEMI Semiconductor strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringement of intellectual property rights or other rights of third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the MSKSEMI Semiconductor product that you intend to use.