

# MSKSEMI 美森科

SEMICONDUCTOR



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## MSTPS7A20XXPDBVR

Product specification

## Description

The MSTPS7A20XXPDBVR series is a three-terminal step-down regulator with high precision, low voltage drop and low quiescent. The input voltage range 10V, It can provide large current output capability under extremely small voltage difference conditions and has good regulation rate. It can provide large current output under small voltage difference and has good regulation rate.

The MSTPS7A20XXPDBVR is deliver up to 400mA of output current. high-PSRR linear regulator. The enable pin EN can control the chip to enter standby mode, which greatly reduces the static current consumption. It is particularly suitable for applications with strict requirements on battery life.

The device is protected from short circuit events by the current limit function and from over heating by means of thermal shutdown protection. widely used in audio, video, and communication appliances.

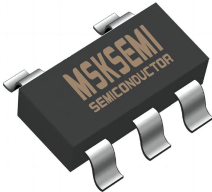
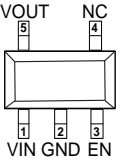
## Features

- Maximum output current 400mA
- Low Voltage Drop 75mV@50mA,  $V_{OUT}=3.3V$
- Low Temperature Coefficient
- Withstanding Voltage 10V
- Quiescent Current 2.0μA@6V
- Output Voltage Accuracy:  $\pm 2\%$
- Output short circuit protection
- Output Current Limit
- High PRSS 76dB @ 1kHz
- Low Output Noise: 70μVRMS @10~100KHz





## Typical Applications

- Battery-powered Equipments
- Communication Equipments
- Audio/Video Equipments
- Smart Battery Packs
- Smoke Detectors
- EV and HEV battery management systems

## Reference News

SOT-23-5	Pin Configuration
	

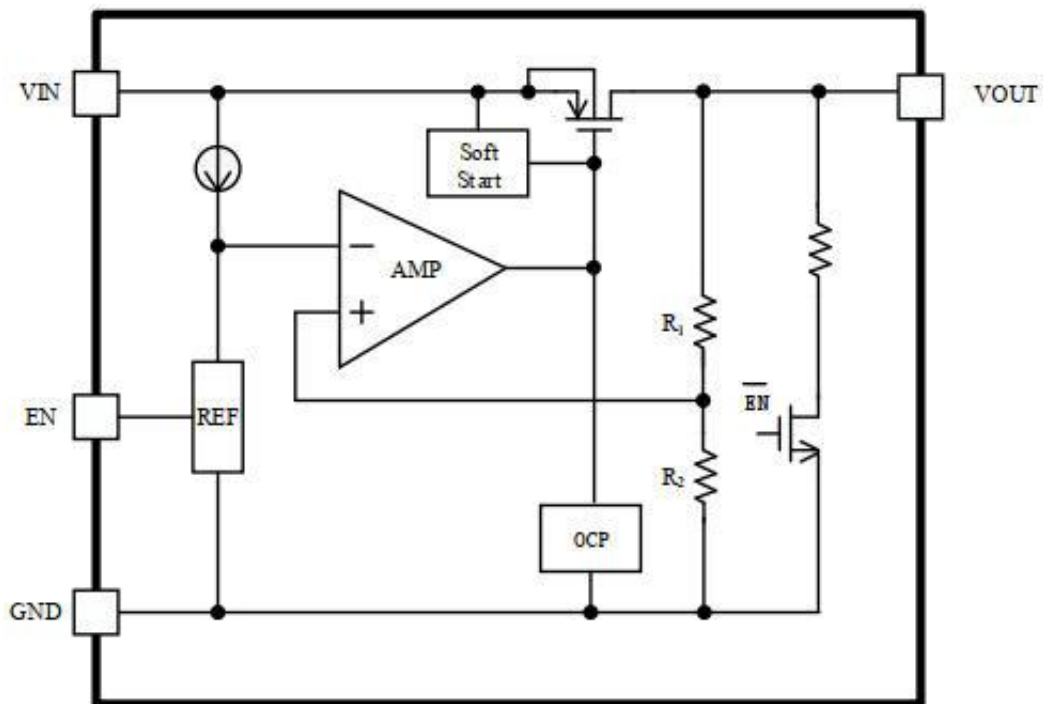
## Marking

MSTPS7A2018PDBVR	MSTPS7A2030PDBVR	MSTPS7A2033PDBVR	MSTPS7A2050PDBVR
			

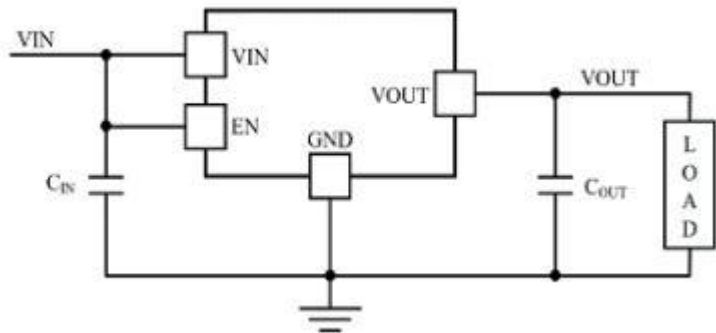
## Pin Description

Pin Number	Name	Functions Description
SOT-23-5		
2	GND	Ground
1	V <sub>IN</sub>	Input
5	V <sub>OUT</sub>	Output
4	NC	No Connect
3	EN	ON/OFF Connect

## Functional Block Diagramf



Typical Application circuit



Note. The input capacitor  $C_{IN}$  is recommended to be at least  $1\mu\text{F}$ ; to ensure the output voltage stability, the output capacitor  $C_{OUT}$  should be a ceramic capacitor of at least  $1\mu\text{F}$ , or an electrolytic capacitor of at least  $2.2\mu\text{F}$ .

Absolute Maximum Ratings

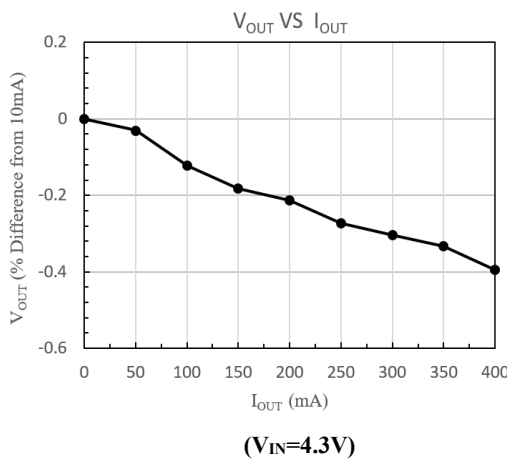
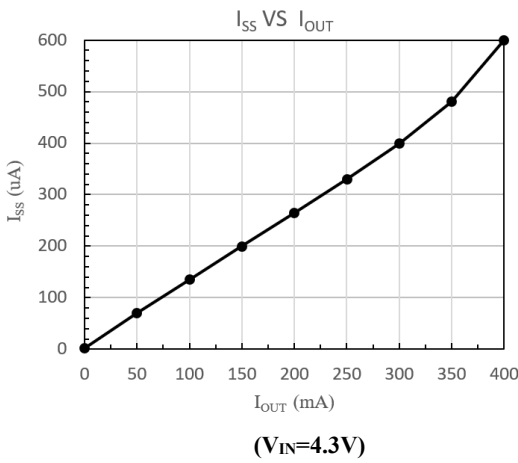
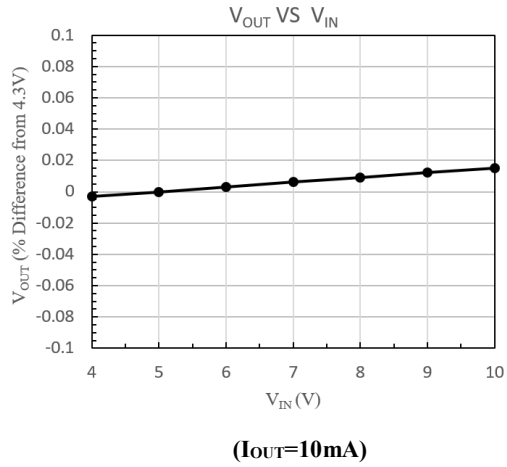
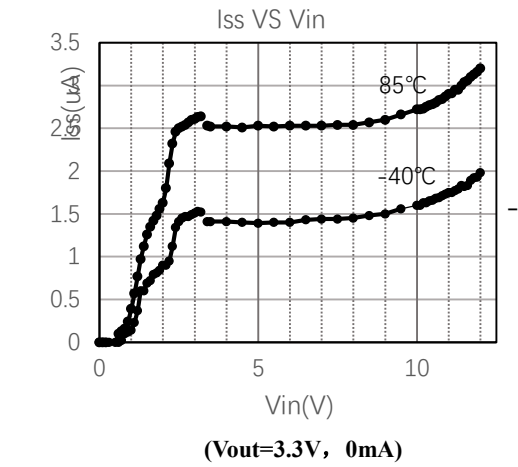
Symbol	Parameter	Value range	Unit
$V_{IN}$	Supply Input Voltage	$-0.3 \sim +12$	V
$I_{OUT}$	Maximum Output Current	450	mA
$T_A$	Operating Free-air Temperature Range	$-40 \sim +85$	$^{\circ}\text{C}$
$T_J$	Maximum Junction Temperature	150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	$-55 \sim +150$	$^{\circ}\text{C}$
$P_d$	Power Dissipation	400	mW

**Note :** Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

**Electrical Characteristics** (unless otherwise noted  $T_A = +25^{\circ}\text{C}$ ,  $C_{IN}=C_{OUT}=1\mu\text{A}$ )

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Voltage	$V_{IN}$			2.2		10	V
Quiescent Current	$I_{SS}$	$V_{IN}=6\text{V}$ , $I_{OUT}=0\text{mA}$			2.0	3	$\mu\text{A}$
		$V_{IN}=10\text{V}$ , $I_{OUT}=0\text{mA}$			2.5	6	
Standby Current	$I_{STB}$	$V_{EN}=0\text{V}$				0.1	$\mu\text{A}$
Voltage Accuracy	$V_{OUT}$	$V_{IN}=V_{OUT}+1\text{V}$ $I_{OUT}=1\text{mA}$		-2		+2	%
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times V_{OUT}$	$V_{OUT}+1\text{V} \leq V_{IN} \leq 6\text{V}$ $I_{OUT}=10\text{mA}$			0.02	0.1	%/V
Load Regulation	$\Delta V_{OUT}$	$V_{IN}=V_{OUT}+1\text{V}$ $1\text{mA} \leq I_{OUT} \leq 200\text{mA}$			0.2	1	%
Temperature Coefficient	$\frac{\Delta V_{OUT}}{\Delta T} \times V_{OUT}$	$I_{OUT}=10\text{mA}$ $-25^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$			$\pm 100$		ppm/ $^{\circ}\text{C}$
Output Current	$I_{OUT}$	$V_{IN}=V_{OUT}+1\text{V}$			400		mA
Voltage Drop	$V_{Drop}$	$I_O=50\text{mA}$	$V_{OUT} \leq 2.0\text{V}$		160		mV
			$2.0 < V_{OUT} \leq 3.0\text{V}$		120		
			$3.0 < V_{OUT} \leq 5.0\text{V}$		75		
Ripple Rejection Rate	PSRR	$V_{IN}=5\text{V}+1V_{p-p}(\text{AC})$ , $f=1\text{KHz}$ $V_{OUT}=3.3\text{V}$ , $I_{OUT}=50\text{mA}$			76		dB
Output noise	$E_n$	BW=10Hz to 100KHz			70		$\mu\text{Vrms}$
EN "High" Voltage	$V_{IH}$	$V_{IN}=5\text{V}$		1.2			V
EN "Low" Voltage	$V_{IL}$	$V_{IN}=5\text{V}$				0.4	V
Discharge Resistor	$R_D$	EN=0V , $V_{OUT}=0.5\text{V}$			500		$\Omega$

Performance Characteristics



## Application Information

### Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is  $1.0\mu\text{F}$ . A ceramic capacitor is recommended with the temperature characteristics of X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place the output capacitor as close as possible to OUT and GND pins.

### Input Capacitor

A  $1\mu\text{F}$  ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

### Current-Limit and Short-Circuit Protection

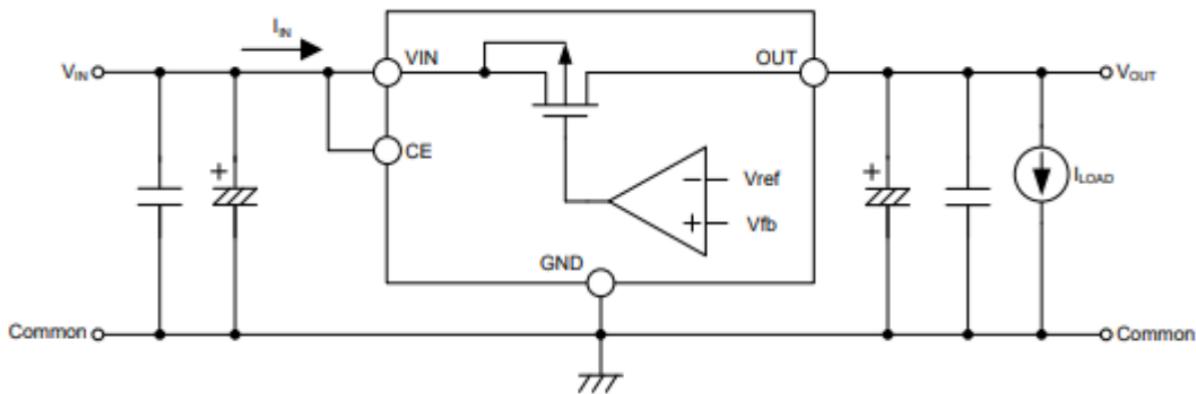
When the output current at VOUT pin is higher than the current-limit threshold or the VOUT pin is directly shorted to GND, current-limit protection will trigger and clamp the output current at a pre-designed level to prevent overcurrent and thermal damage.

### Layout Considerations

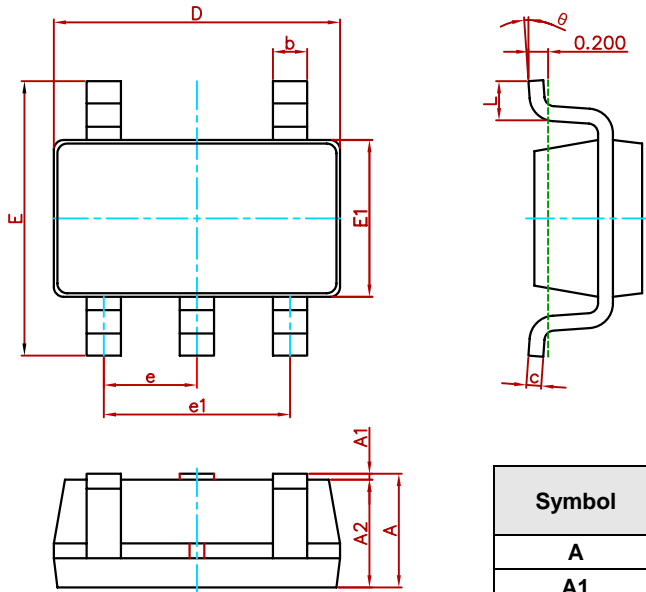
For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from VIN to VOUT, and load circuit.

### Power Estimation

In order to make the chip work within the limit range and maintain a stable output voltage, the power consumption PD of the chip must not exceed the maximum power consumption PD(MAX), that is,  $PD \leq PD(\text{MAX})$ . As can be seen from the figure below, almost all power is generated by the transmission transistor, which is equivalent to connecting a variable resistor in series with the load to keep the output voltage constant. It will generate power consumption in the form of heat energy, and it must be ensured that the chip does not exceed the maximum junction temperature.

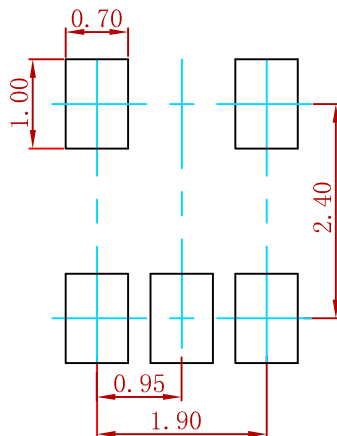


## Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

## Suggested Pad Layout



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.

## Order information

P/N	PKG	QTY
MSTPS7A20XXPDBVR	SOT-23-5	3000



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