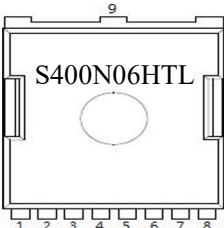


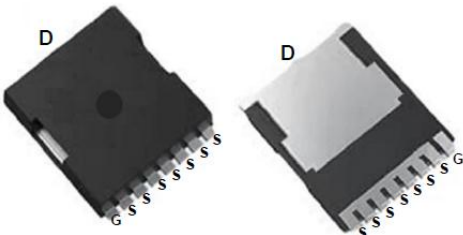
Features ➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low RDS(ON)	Bvdss	Rdson	ID
	60V	1.25mΩ	400A
	Application ➤ DC-DC Converters ➤ Power management functions ➤ Synchronous-rectification applications		



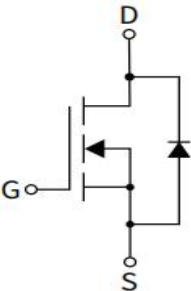
Package



Marking and pin assignment



TOLL-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
S400N06HTL	S400N06HTL	TOLL-8L	2000

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V _{DS}	60	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C =25°C	I _D	400	A
	T _C =100°C	I _D	268	A
Pulsed Drain Current ¹		I _{DM}	1512	A
Power Dissipation	T _C = 25°C	P _D	454.5	W
Single Pulse Avalanche Energy ²		EAS	500	mJ
Junction Temperature		T _J	-55~+175	°C
Storage Temperature		T _{STG}	-55~+175	°C

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ³	R _{θJA}	39	°C/W
Thermal Resistance Junction-Case	R _{θJC}	0.33	°C/W



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS400N06HTL	S400N06HTL	1	9	2,3,4,5,6,7,8	Tape Reel

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	$I_d = 250\mu\text{A}$, $V_{gs} = 0\text{V}$	60	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$, $T_J=100^{\circ}\text{C}$	-	-	100	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2	2.9	4	V
Static Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	1.25	1.55	m Ω
Forward Transconductance ⁴	g_{fs}	$V_{DS}=10\text{V}$, $I_D=20\text{A}$	-	62	-	S
Gate resistance	R_g	$f=1\text{MHz}$	-	2.6	-	Ω
Input Capacitance	C_{iss}	$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	5990	-	pF
Output Capacitance	C_{oss}		-	2257	-	pF
Reverse Transfer Capacitance	C_{rss}		-	86	-	pF
Turn-ON Delay Time	$t_{d(on)}$	$V_{GS}=10\text{V}$, $V_{DD} 30\text{V}$, $R_G=3\Omega$, $I_D=20\text{A}$	-	15.6	-	ns
Rise Time	t_r		-	29	-	ns
Turn-OFF Delay Time	$t_{d(off)}$		-	63	-	ns
Fall Time	t_f		-	51	-	ns
Total Gate Charge	Q_g	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $I_D=20\text{A}$	-	102	-	nC
Gate Source Charge	Q_{gs}		-	24.6	-	nC
Gate Drain Charge	Q_{gd}		-	28.2	-	nC
Body Diode Reverse Recovery Time	t_{rr}	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	80	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	114	-	nC
Maximum Continuous Drain to Source Diode Forward Current	I_S	-	-		400	A
Drain to Source Diode Forward Voltage ⁴	V_{SD}	$V_{GS}=0\text{V}$, $I_S=20\text{A}$	-		1.2	V

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$.
2. The test condition is $V_{DD}=90\text{V}$, $V_{GS}=10\text{V}$, $L=0.4\text{mH}$, $I_{AS}=50\text{A}$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

4. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Typical Characteristics

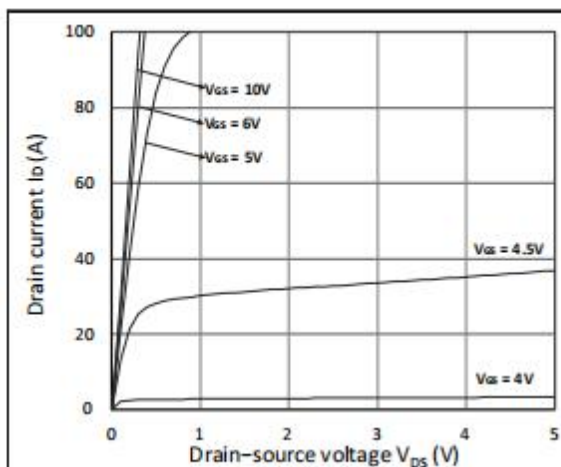


Figure 1. Output Characteristics

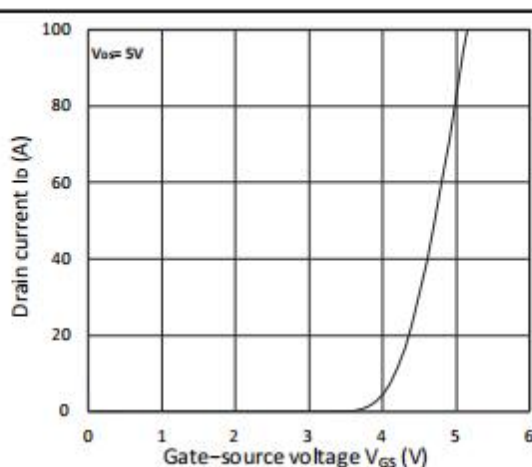


Figure 2. Transfer Characteristics

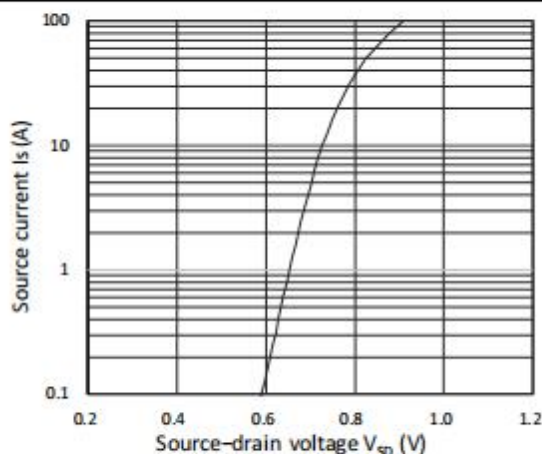


Figure 3. Forward Characteristics of Reverse

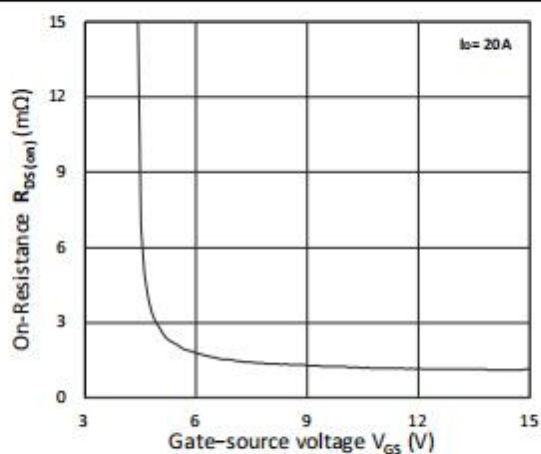


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

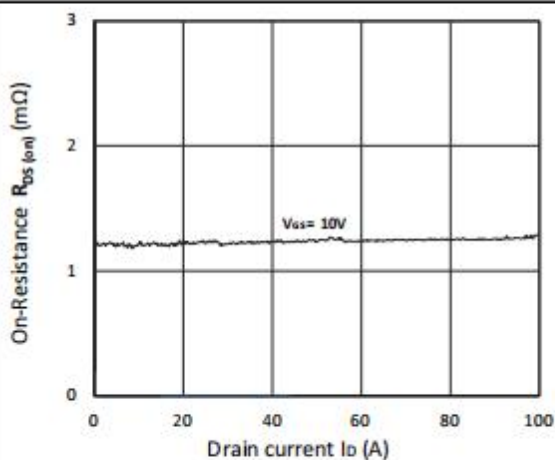


Figure 5. $R_{DS(ON)}$ vs. I_D

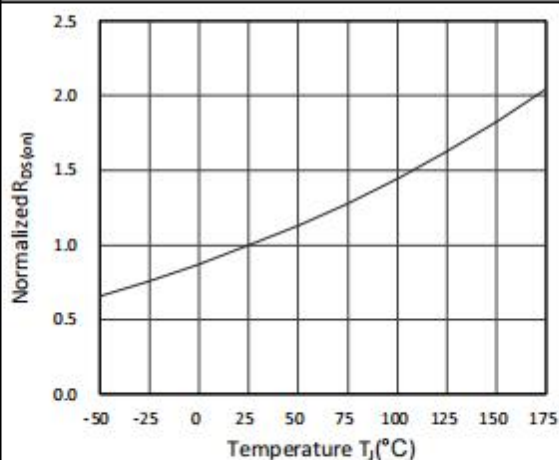


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

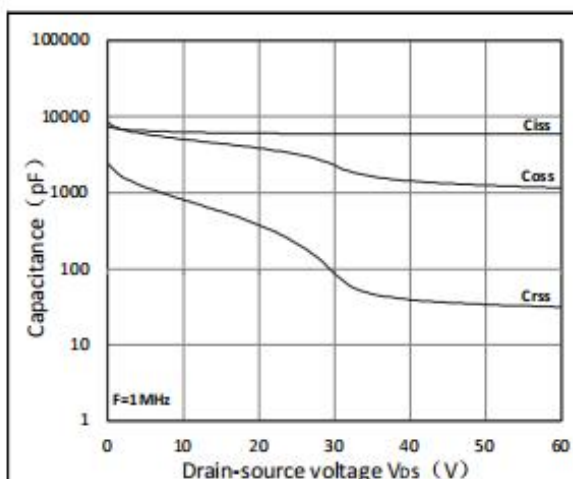


Figure 7. Capacitance Characteristics

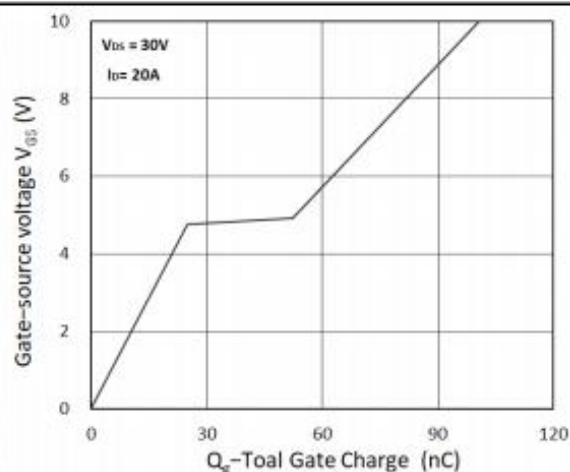


Figure 8. Gate Charge Characteristics

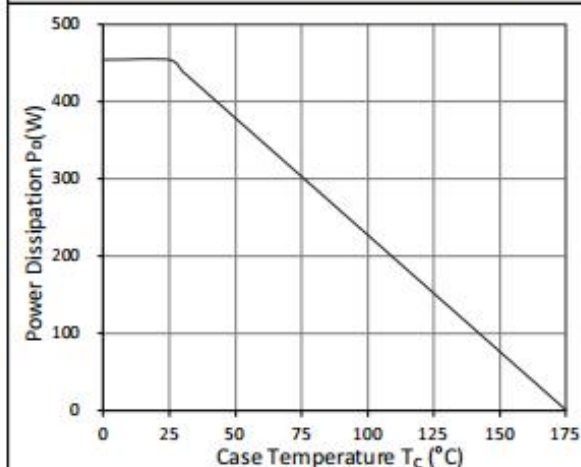


Figure 9. Power Dissipation

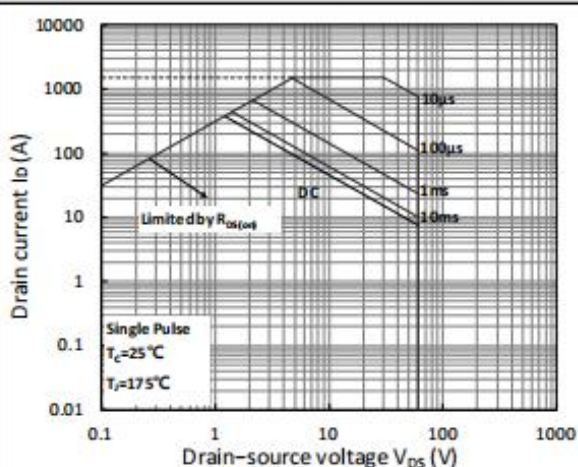


Figure 10. Safe Operating Area

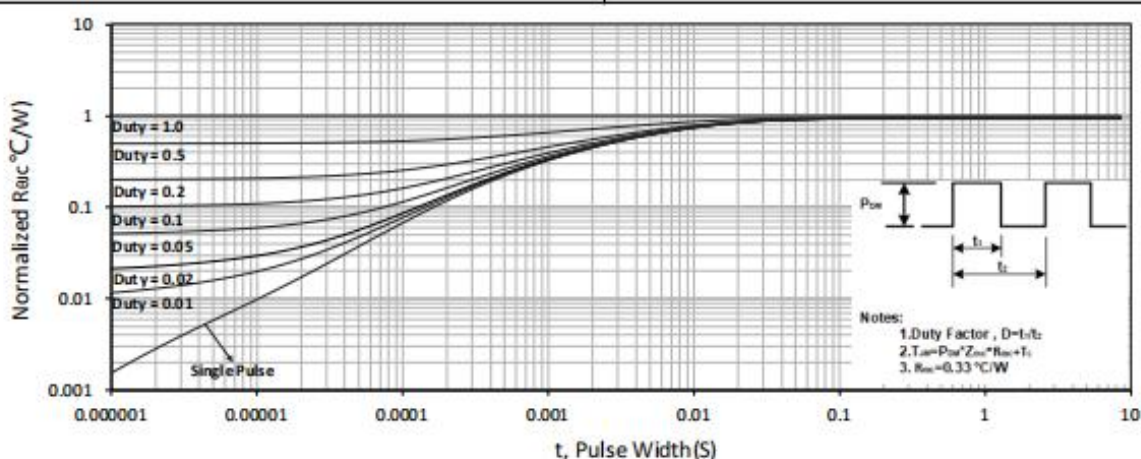


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

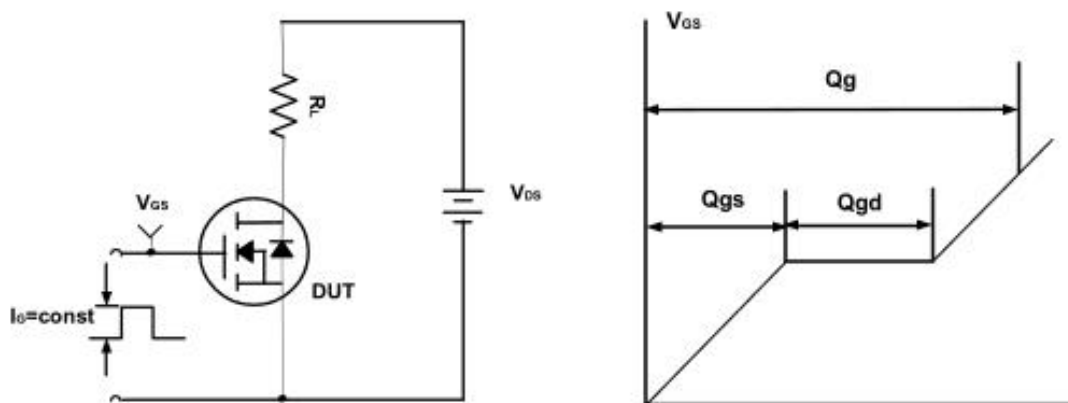


Figure A. Gate Charge Test Circuit & Waveforms

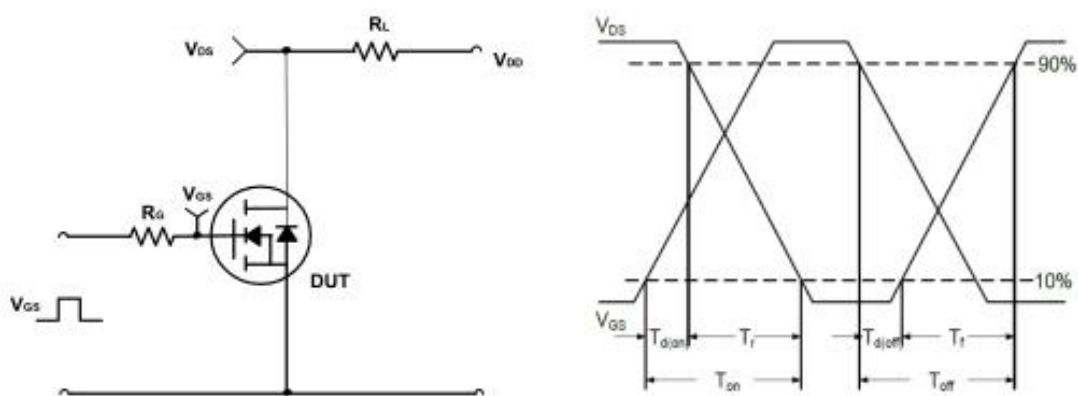


Figure B. Switching Test Circuit & Waveforms

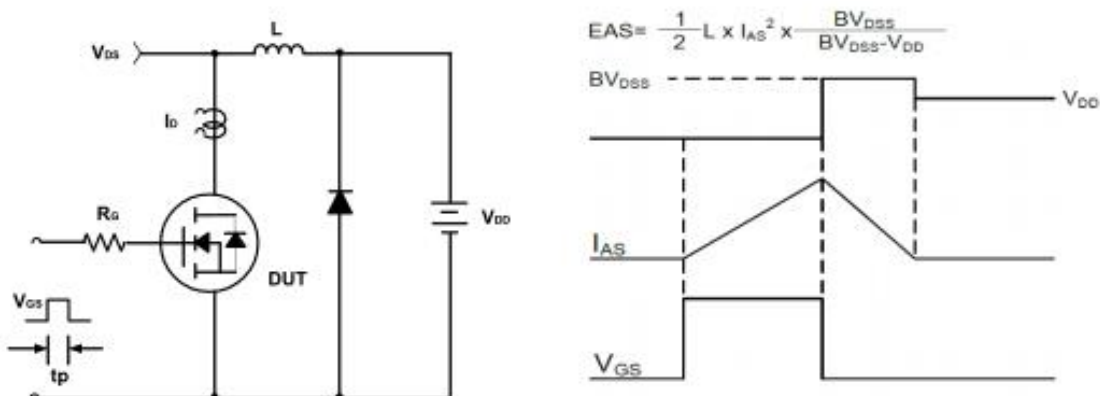
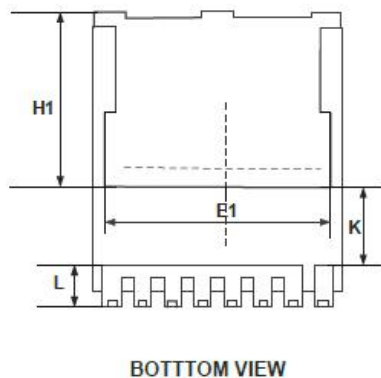
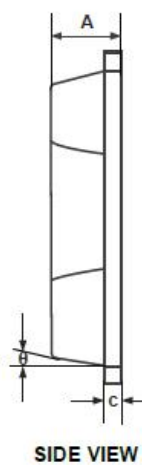
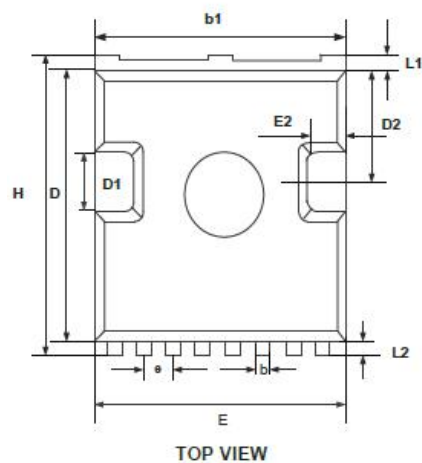


Figure C. Unclamped Inductive Switching Circuit & Waveforms



Package Dimensions TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	



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