1、MT41K256M16HA-CN

(1) Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 (1.5V) SDRAM. When running in 1.5V compatible mode. DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8n-bit-wide, four-clock cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one half-clock-cycle data transfers at the I/O pins.

(2) Features

- VDD = VDDQ = 1.35v (1.283-1.45v)
- VDD = VDDQ = 1.5V±0.075V
  — Supports DDR3L devices to be backward compatible in 1.5V applications
- Differential bidirectional data strobe
- 8 internal banks
- 8n-bit prefetch architecture
- Differential clock inputs(CK, CK#)
- ODT function
- For data, strobe and mask signals
- Programmable CAS (READ) latency(CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency(CWL)
- Fixed burst length (BL) of8 and burst chop (BC) of 4(via the

mode register set [MRS])

- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 105°C

  - 64ms, 8192-cycle refresh up to 85°C
  - 32ms, 8192-cycle refresh at >85°C to 95°C
  - 16ms, 8192-cycle refresh at >95°C to 105°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

(3) Options and Marking

Options		Marking
Configuration	256 Meg x 16	256M16
FBGA package (Pb-free) – x16	96-ball (9mm x 14mm) Type E	HA
	96-ball (7.5mm x 13.5mm) Type N	LY
	96-ball (8mm x 14mm) Type P	TW
Timing-cycle time	938ps @ CL = 14 (DDR3-2133)	-093
	1.07ns @ CL = 13 (DDR3-1866)	-107
	1.25ns @ CL = 11 (DDR3-1600)	-125
Operating temperature	Commercial(0°C≤T_C≤ +95°C)	None
	Industrial (-40°C≤T_C≤ +95°C)	IT
	Automotive (-40°C≤T_C≤ +105°C)	AT

(4) Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-093[1,2]	2133	14-14-14	13.09	13.09	13.09
-107[1]	1866	13-13-13	13.91	13.91	13.91
-125	1600	11-11-11	13.75	13.75	13.75

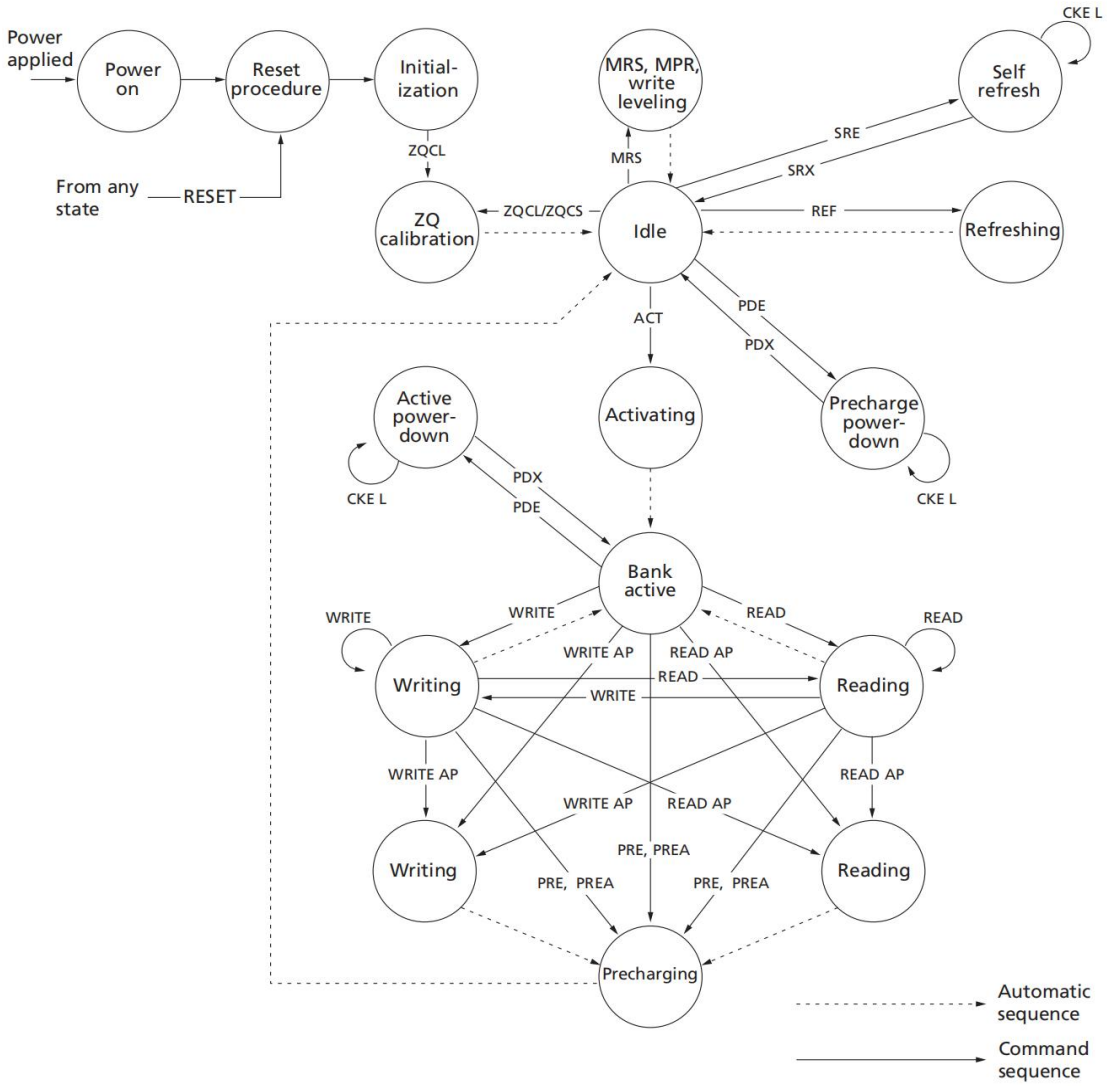
Notes: 1 Backward compatible to 1600,CL = 11(-125)

2 Backward compatible to 1866,CL = 13(-107)

(5) Addressing

Parameter	256 Meg x 16
Configuration	32 Meg x 16 x 8 banks
Refresh count	8K
Row address	32K (A[14:0])
Bank address	8 (BA[2:0])
Column address	1K (A[9:0])
Page size	2KB

(6) State Diagram



ACT=ACTIVATE	PREA= PRECHARGE ALL	SRX=Self refresh exit
MPR=Multipurpose register	READ= RD, RDS4, RDS8	WRITE=WR, WRS4, WRS8
MRS=Mode register set	READ AP =RDAP,RDAPS4, RDAPS8	WRITE AP = WRAP, WRAPS4, WRAPS8
PDE=Power-down entry	REF= REFRESH	ZQCL = ZQ LONG CALIBRATION
PDX=Power-down exit	RESET=START RESET PROCEDURE	ZQCS = ZQ SHORT CALIBRATION
PRE=PRECHARGE	SRE=Self refresh entry	

(7) Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation.The double data rate architecture is an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8n-bit-wide, four-clock cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one half-clock-cycle data transfers at the I/O pins.

The data used for writing is centre aligned. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK, Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to providea self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed -40°C or 95°C. JEDEC specifications require the refresh rate to double when Tc exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when Tc is < 0°C or >95°C.

Automotive Temperature

The Automotive temperature (AT) device requires that the case temperature not exceed -40°C or 105°C. Micron specification requires the refresh rate to 4X when Tc exceeds 95°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when Tc is < 0°C or >95°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as "DQ". DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "DQS" and "CK" found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Row addressing is denoted as A[n:0]. For example 1Gb:n=12(x16); 1Gb:n=13(x4,x8); 2Gb:n=13(x16) and 2Gb:n=14(x4,x8); 4Gb:n=14(x16); and 4Gb:n=15(x4,x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dyamic ODT Special Use Case section.
- Ax16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:

  — Connect UDQS to ground via 1kΩ* resistor.

  — Connect UDQS# to V_{DD} via 1kΩ* resistor.

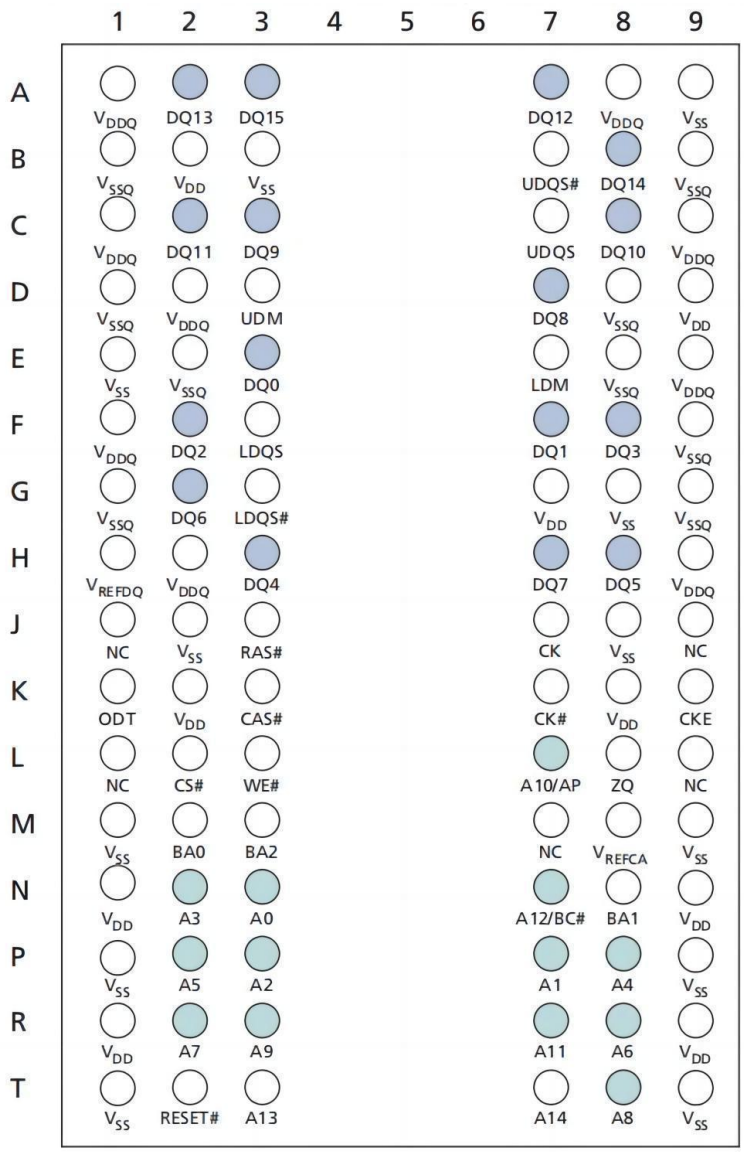
  — Connect UDM to V_{DD} via 1kΩ* resistor.

  — Connect DQ[15:8] individually to either Vss, V_{DD}, or V_{REF} via 1kΩ resistors,* or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

2、Pinout and Description

The lead-in end arrangement shall be as specified in the diagram below.



Pin Arrangement Diagram (Top View)

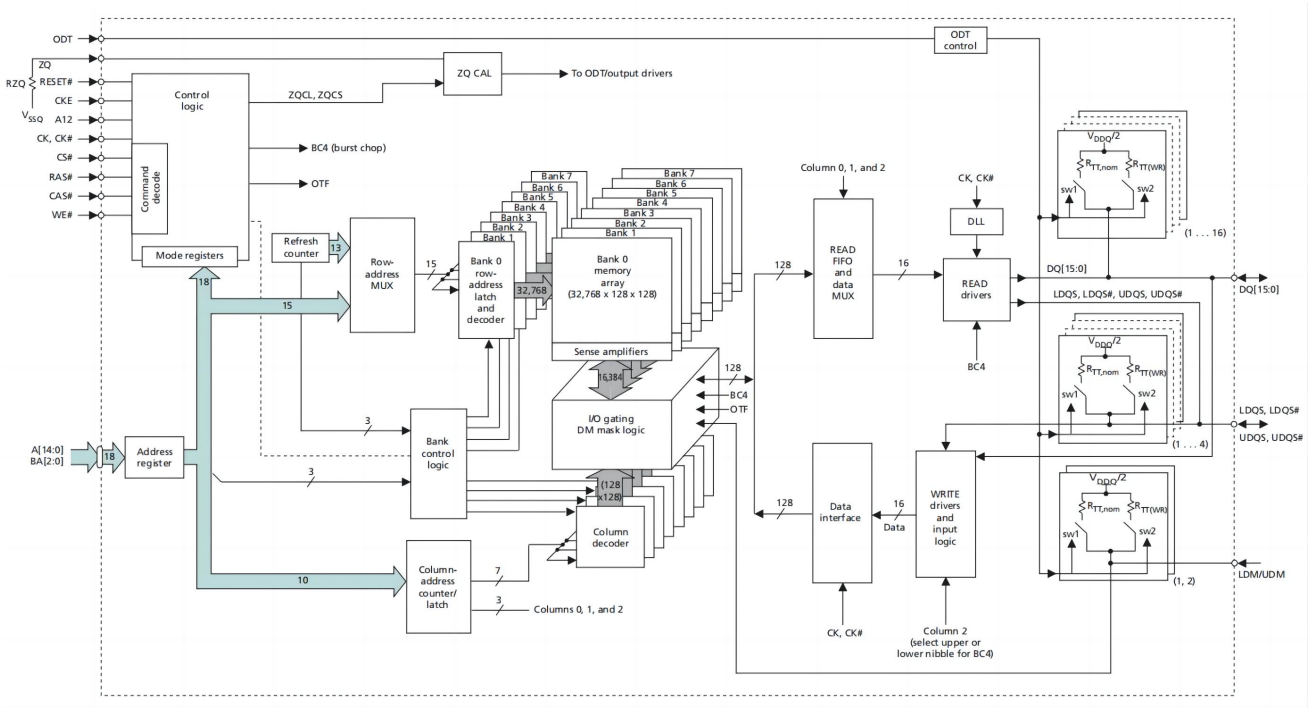
Pin Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 70 (page 117).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.

Pin Descriptions (Continued)

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

3、Functional Block Diagrams



4、Electrical Specifications

Absolute Maximum Ratings					
Symbol	Parameter	Min	Max	Unit	Notes
VDD	VDD supply voltage relative to VSS	-0.4	1.975	V	1
VDDQ	VDD supply voltage relative to VSSQ	-0.4	1.975	V	
VIN、VOUT	Voltage on any pin relative to VSS	-0.4	1.975	V	
TC	Operating case temperature - Commercial	0	95	℃	2,3
	Operating case temperature - Industrial	-40	95		
	Operating case temperature - Automotive	-40	105		
	Operating case temperature - Military	-55	125		
TSTG	Storage temperature	-55	150	℃	

Notes: 1. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6×VDDQ. When VDD 和 VDDQ < 500mV , VREF can be ≤300mV.
2. MAX operating case temperature. TC is measured in the center of the package.
3. Device functionality is not guaranteed if DRAM device exceeds the maximum TC during operation.

Recommended Parameters					
Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	1.28	1.35	1.45	V
VDDQ	I/O Supply voltage	1.28	1.35	1.45	V
Backward compatible to VDD=VDDQ=1.5V±0.075V					

5、 Electrical Characteristics

5.1 Input/Output Capacitance

DDR3L Input/output capacitance

Capacitance Parameters	Sym	DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.4	0.8	1.3	0.8	1.3	pF	
ΔC:CK to CK#	C_{DCK}	0.0	0.15	0.0	0.15	0.0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.4	2.2	1.4	2.1	1.4	2.1	pF	2
Differential I/O:DQS,DQS#,TDQS, TDQS#	C_{IO}	1.4	2.2	1.4	2.1	1.4	2.1	pF	3
ΔC: DQS to DQS#,TDQS, TDQS#	C_{DDQS}	0.0	0.15	0.0	0.15	0.0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	4
Inputs(CTRL,CMD,ADDR)	C_I	0.75	1.2	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	7
ZQ pin capacitance	C_{ZQ}	-	3.0	-	3.0	-	3.0	pF	
Reset pin capacitance	C_{RE}	-	3.0	-	3.0	-	3.0	pF	

Notes：1. V_{DD} = 1.35V (1.283-1.45V)， V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5× V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak.).

2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.

4. C_{DIO} = $C_{IO(DQ)}$ - 0.5 × ($C_{IO(DQS)}$ + $C_{IO(DQS\#)}$)。

5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; A=[n: 0]， BA=[2:0].

6. C_{DI_CTRL}= $C_{I(CTRL)}$-0.5 × ($C_{CK\ (CK)}$ + $C_{CK\ (CK\#)}$)。

7. $C_{DI\_CMD\_ADDR}$ = $C_{I\ (CMD\_ADDR)}$ - 0.5×($C_{CK\ (CK)}$ + $C_{CK\ (CK\#)}$)。

5.2 IDD Specifications and conditions

Within the following IDD measurement tables, the following definitions and conditions are used, unless stated otherwise:

- LOW:$V_{IN} \leq V_{IL(AC)max}$; HIGH:$V_{IN} \geq V_{IH(AC)min}$.
- Midlevel: Inputs are $V_{REF}=V_{DD}/2$.
- R_{ON} set to RZQ/7 (34Ω)。
- $R_{TT,nom}$ set to RZQ/6 (40Ω).
- $R_{TT(WR)}$ set to RZQ/2 (120Ω).
- Q_{OFF} is enabled in MRl.
- ODT is enabled in MRl ($R_{TT,nom}$) and MR2 ($R_{TT(WR)}$).
- TDQS is disabled in MRl.
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$.
- Burst lengths are BL8 fixed.
- AL = 0 (except in I_{DD7}).
- I_{DD} specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- Optional ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Timing Parameters Used for IDD Measurements - Clock Units

I_{DD} Parameter		DDR3L-1600		DDR3L-1866	DDR3L-2133	Unit
		-125E	-125	-107	-093	
		10-10-10	11-11-11	13-13-13	14-14-14	
$^{t}CK(MIN)I_{DD}$		1.25		1.07	0.938	ns
CL I_{DD}		10	11	13	14	CK
$^{t}RCD(MIN)I_{DD}$		10	11	13	14	CK
$^{t}RC(MIN)I_{DD}$		38	39	45	50	CK
$^{t}RAS(MIN)I_{DD}$		28	28	32	36	CK
$^{t}RP(MIN)I_{DD}$		10	11	13	14	CK
^{t}AFT	×16	32	32	33	38	CK
^{t}RRD I_{DD}	×16	6	6	6	7	CK
^{t}RFC	1Gb	88	88	103	118	CK
	2Gb	128	128	150	172	CK
	4Gb	208	208	243	279	CK
	8Gb	280	280	328	375	CK

5.3 Operating IDD Specifications

IDD Maximum Limits for 1.35/1.5V Operation

Speed Bin			DDR3L-1600	DDR3L-1866	DDR3L-2133	Units	Notes
Parameter	Symbol	Width					
Operating current 0:One bank ACTIVATE-to-PRECHARGE	I_{DD0}	×16	110	130	150	mA	1,2
Operating current 1:One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	×16	120	135	155	mA	1,2
Precharge power-down current: Slow exit	I_{DD2P0}	×16	22	22	22	mA	1,2
Precharge power-down current: Fast exit	I_{DD2P1}	×16	45	47	49	mA	1,2
Precharge quiet standby current	I_{DD2Q}	×16	60	65	70	mA	1,2
Precharge standby current	I_{DD2N}	×16	63	68	73	mA	1,2
Precharge standby ODT current	I_{DD2NT}	×16	85	92	98	mA	1,2
Active power-down current	I_{DD3P}	×16	70	80	85	mA	1,2
Active standby current	I_{DD3N}	×16	90	100	105	mA	1,2
Burst read operating current	I_{DD4R}	×16	190	220	240	mA	1,2
Burst write operating current	I_{DD4W}	×16	210	250	280	mA	1,2
Burst refresh current	I_{DD5B}	×16	235	242	250	mA	1,2
Room temperature self refresh	I_{DD6}	×16	25	25	25	mA	1,2,3
Extended temperature self refresh	I_{DD6ET}	×16	28	28	28	mA	2,4
All banks interleaved read current	I_{DD7}	×16	240	270	290	mA	1,2
Reset current	I_{DD8}	×16	23	23	24	mA	1,2

Notes：1. Tc = 85℃; SRT and ASR are disabled.

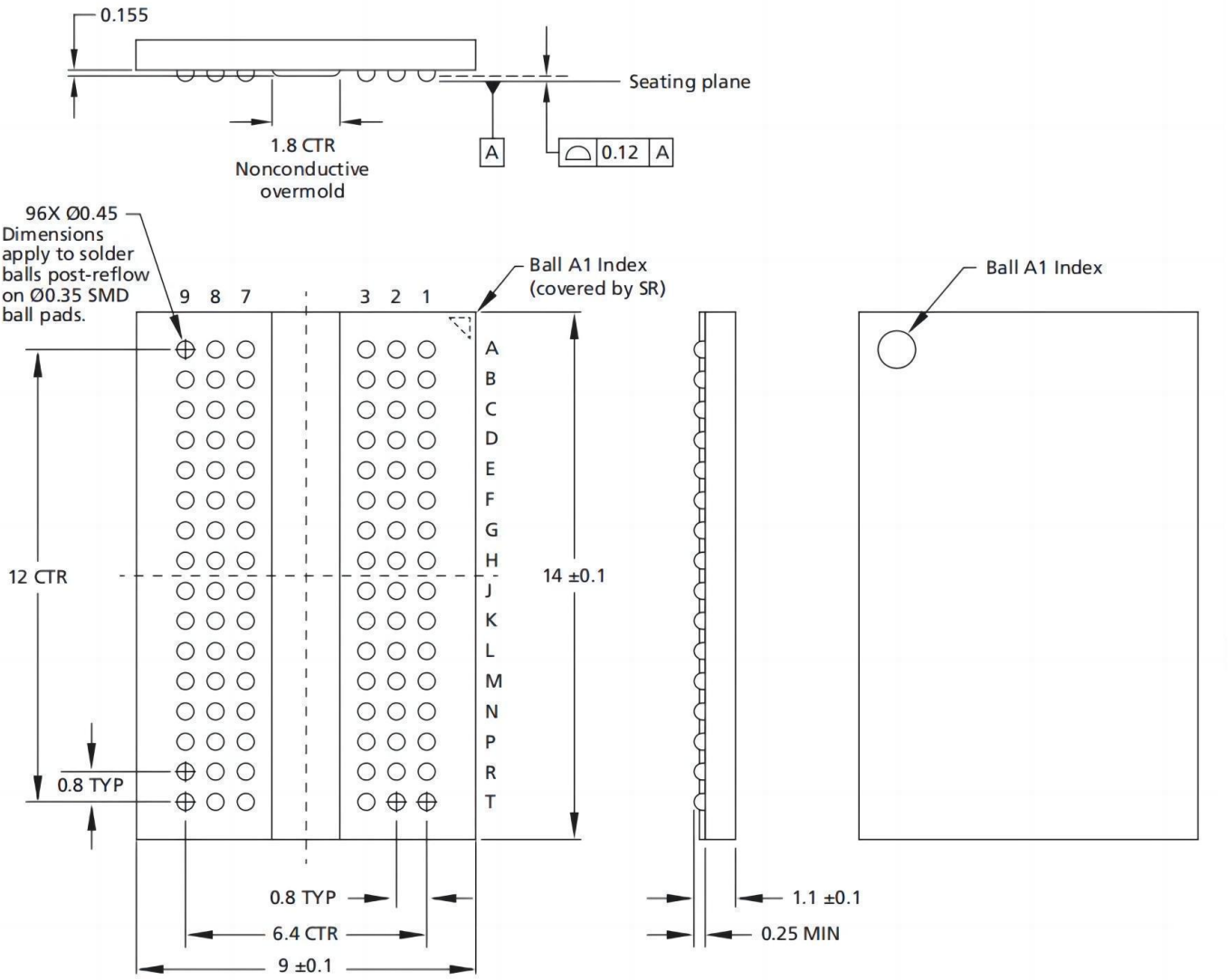
2. Enabling ASR could increase IDDX by up to an additional 2mA.
3. Restricted to T_C(MAX) =85℃.
4. Tc = +85℃； ASR and ODT are disabled: SRT is enabled.
5. When Tc＞+95℃： All IDDX parameters must be derated by 30%.
6. When Tc＞+105℃: All IDDX parameters must be derated by 50%.
7. When Tc＞+105℃: Self-refresh mode is not available.

5.4 DC Operating Conditions

DDR3L 1.35V DC Electrical Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.283	1.35	1.45	V
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V
Input leakage current Any input 0V≤VIN≤VDD, VREF Pin 0V≤VIN≤1.1V (All other pins not under test = 0V)	I_L	-2	-	2	μA
VREF supply leakage current VREFDQ = VDD/2 or VREFCA = VDD/2 (All other pins not under test = 0V)	I_{VREF}	-1	-	1	μA
Output leakage current（DQ off）	I_{OZ}	-5	-	5	μA

6、Package Dimensions



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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