

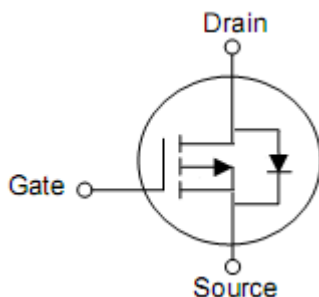
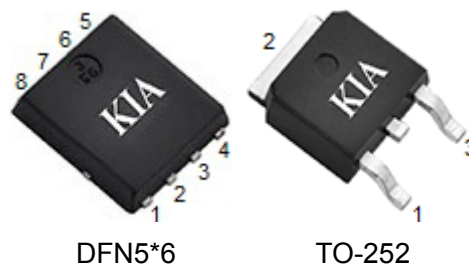
1. Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

2. Applications

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

3. Pin configuration



Pin		Function
DFN5*6	TO-252	
4	1	Gate
5,6,7,8	2	Drain
1,2,3	3	Source

4. Ordering Information

Part Number	Package	Brand
KPY6115A	DFN5*6	KIA
KPD6115A	TO-252	KIA

5. Absolute maximum ratings

T _C =25°C unless otherwise specified				
Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V _{DS}	-150	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current, V _{GS} @ -10V ¹⁾	T _C =25°C	I _D	-10	A
	T _C =100°C	I _D	-6.4	A
Pulsed Drain Current ²⁾		I _{DM}	-40	A
Total Power Dissipation ⁴⁾	T _C =25°C	P _D	89	W
	T _C =100°C	P _D	35	W
Avalanche Energy ³⁾		EAS	30.2	mJ
Avalanche Current		I _{AS}	-11	A
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C

6. Thermal characteristics

Parameter	Symbol	Typ.	Unit
Thermal Resistance, Junction-to-Ambient ¹⁾	R _{θJA}	20	°C/W
Thermal Resistance, Junction-to-Case ¹⁾	R _{θJC}	1.4	°C/W

7. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-150	-	-	V
Drain-Source On-State Resistance ²⁾	R _{DS(ON)}	V _{GS} =-10V, I _D =-5A	-	300	320	mΩ
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =-250uA	-2.0	-	-4.0	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-150V, V _{GS} =0V, T _J =25°C	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Forward Transconductance	g _{fs}	V _{DS} =-5V, I _D =-3A	-	11	-	S
Gate Resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	-	5.7	-	Ω
Input Capacitance	C _{iss}	V _{DS} =-40V, V _{GS} =0V , f=1MHz	-	2109	-	pF
Output Capacitance	C _{oss}		-	513	-	pF
Reverse Transfer Capacitance	C _{rss}		-	408	-	pF
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-10V , I _D =-3A	-	35	-	nC
Gate-Source Charge	Q _{gs}		-	6	-	nC
Gate-Drain Charge	Q _{gd}		-	8.5	-	nC
Turn-On Delay Time	T _{d(on)}	V _{DD} =-50V, V _{GS} =-10V, R _G =3Ω, I _D =-3A	-	28	-	ns
Rise Time	T _r		-	30	-	ns
Turn-Off Delay Time	T _{d(off)}		-	230	-	ns
Fall Time	T _f		-	130	-	ns
Continuous Source Current ^{1),5)}	I _S	V _G =V _D =0V, Force Current	-	-	-10	A
Diode Forward Voltage ²⁾	V _{SD}	V _{GS} =0V, I _S =-5A , T _J =25°C	-	-	-1.2	V
Reverse Recovery Time	t _{rr}	I _F =-5A , T _J =25°C dI/dt=100A/μs,	-	34	-	nS
Reverse Recovery Charge	Q _{rr}		-	32	-	nC

Notes:

1) The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2) The data tested by pulsed, pulse width≤300us, duty cycle ≤2%

3) The EAS data shows Max. rating. The test condition is V_{DD}=-50V, V_{GS}=-10V, L=0.5mH, I_{AS}=-11A

4) The power dissipation is limited by 150°C junction temperature.

5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

9. Typical Characteristics

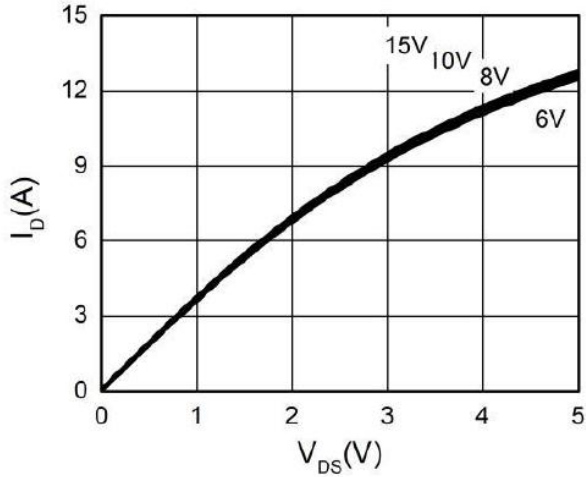


Fig.1 Typical Output Characteristics

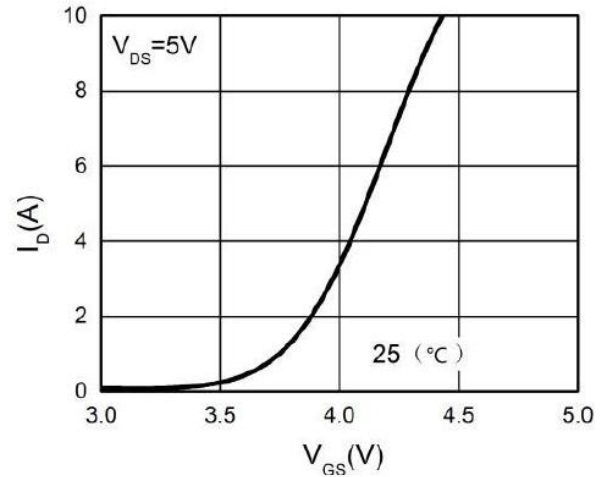


Fig.2 Transfer Characteristics

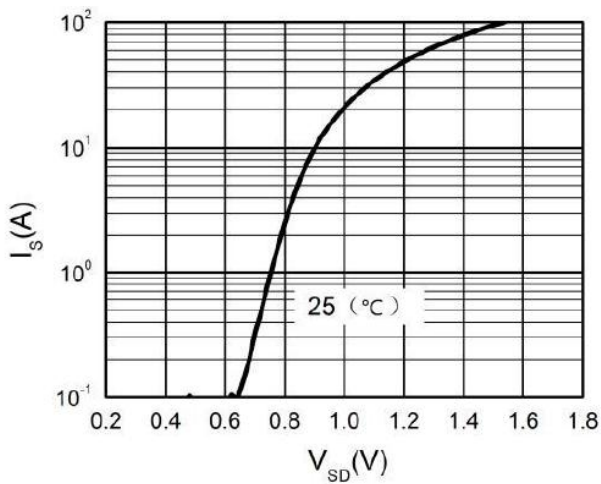


Fig.3 Forward Characteristics Of Reverse

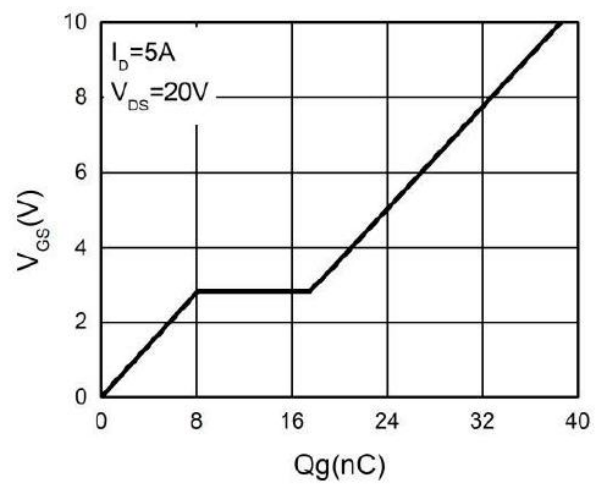


Fig.4 Gate-Charge Characteristics

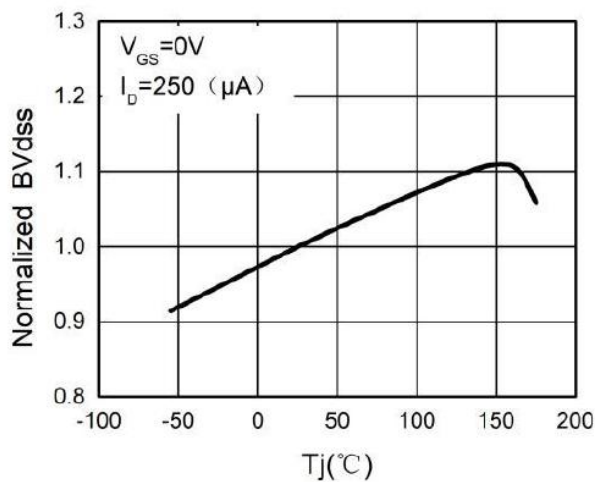


Fig.5 Normalized BV_DS vs. T_J

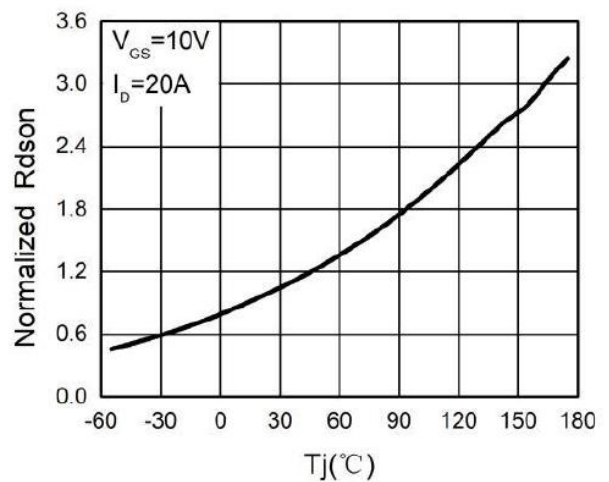


Fig.6 Normalized R_DS(on) vs. T_J

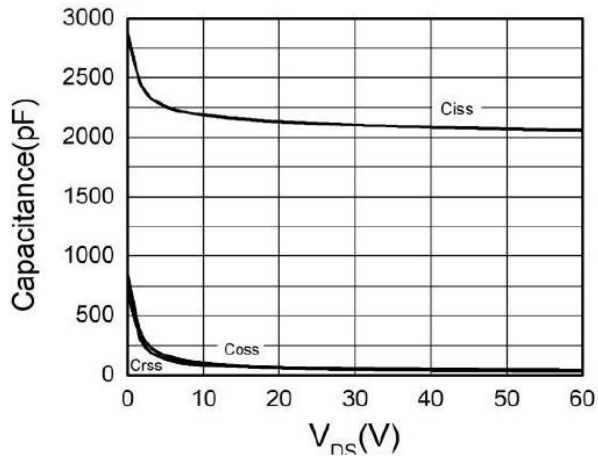


Fig.7 Capacitance

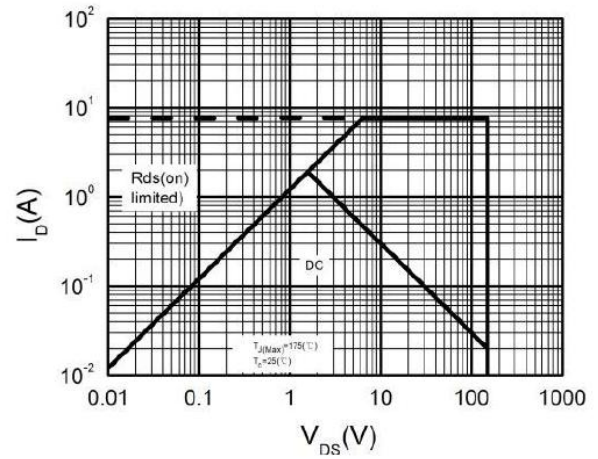


Fig.8 Safe Operating Area

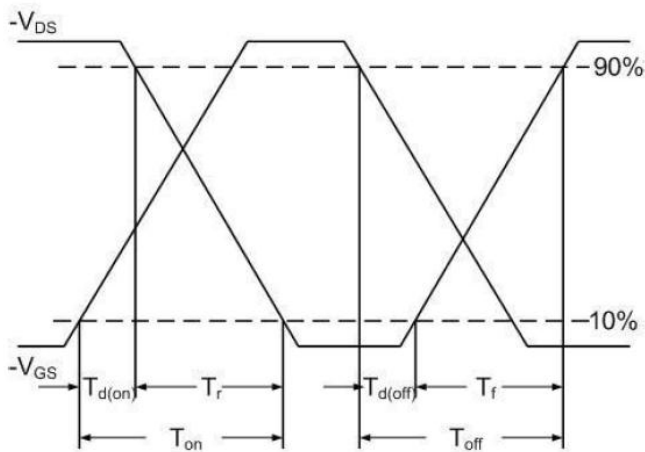


Fig.9 Switching Time Waveform

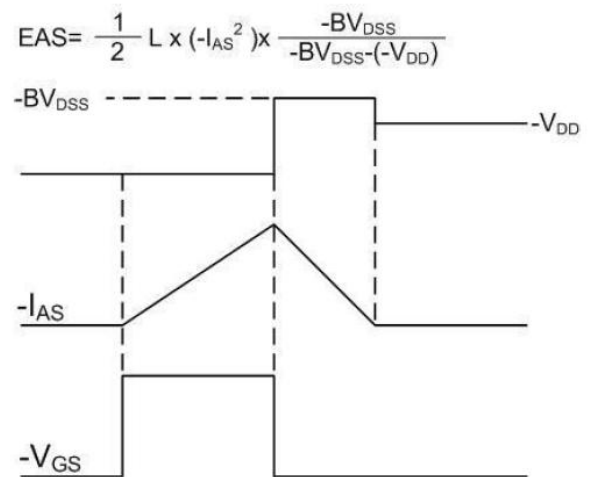


Fig.10 Unclamped Inductive Switching Waveform