FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

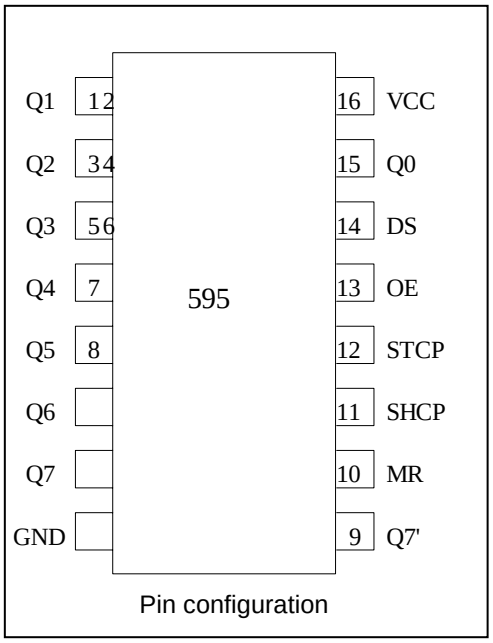
The 74HC595D,118-CN are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The “ 595 ” is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks. Data is shifted on the positive-going transitions of the SHCP input. The data in each register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

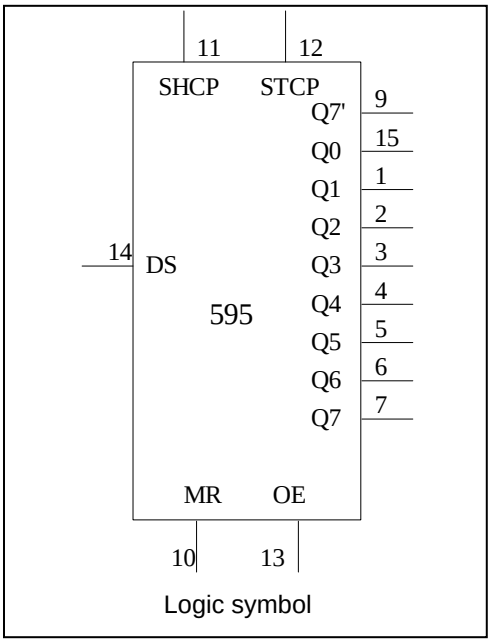
The shift register has a serial input (DS) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

PINNING

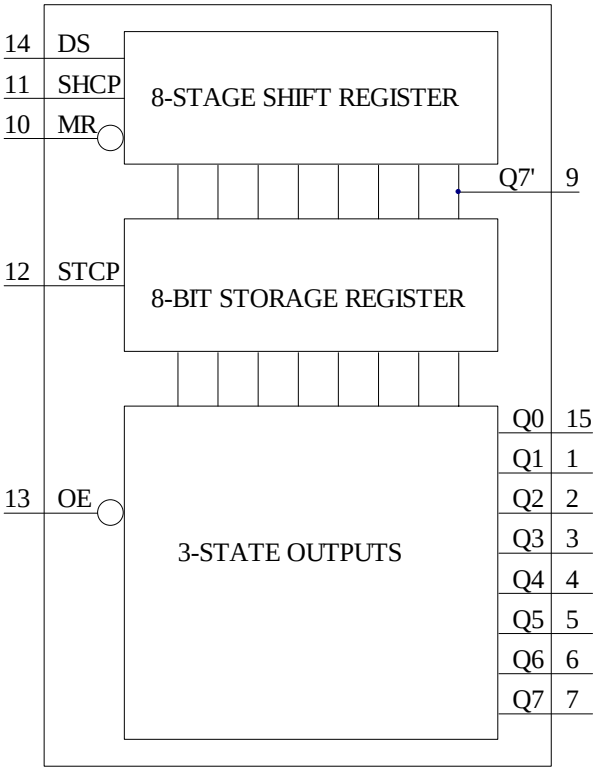
SYMBOL	PIN	DESCRIPTION
Q0 to Q7	15, 1 to 7	parallel data output
GND	8	ground (0 V)
Q7’	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable (active LOW)
DS	14	serial data input
VCC	16	positive supply voltage



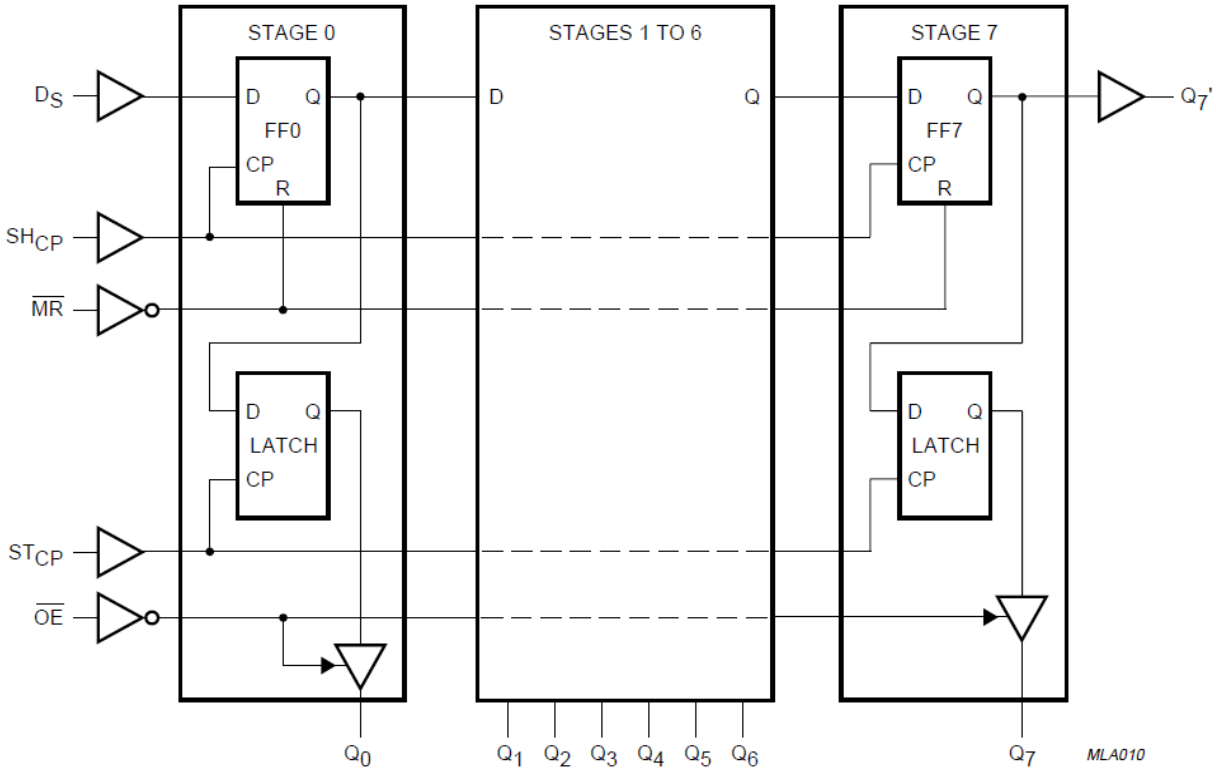
Pin configuration



Logic symbol



Functional diagram



Logic diagram

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTON
SHCP	STCP	OE	MR	DS	Q7’	QN	
X	X	L	L	X	L	NC	a LOW level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6’	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6’) appears on the serial output (Q7’)
X	↑	L	H	X	NC	QN'	contents of shift register stages (internal Qn’) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6’	QN'	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.

Notes

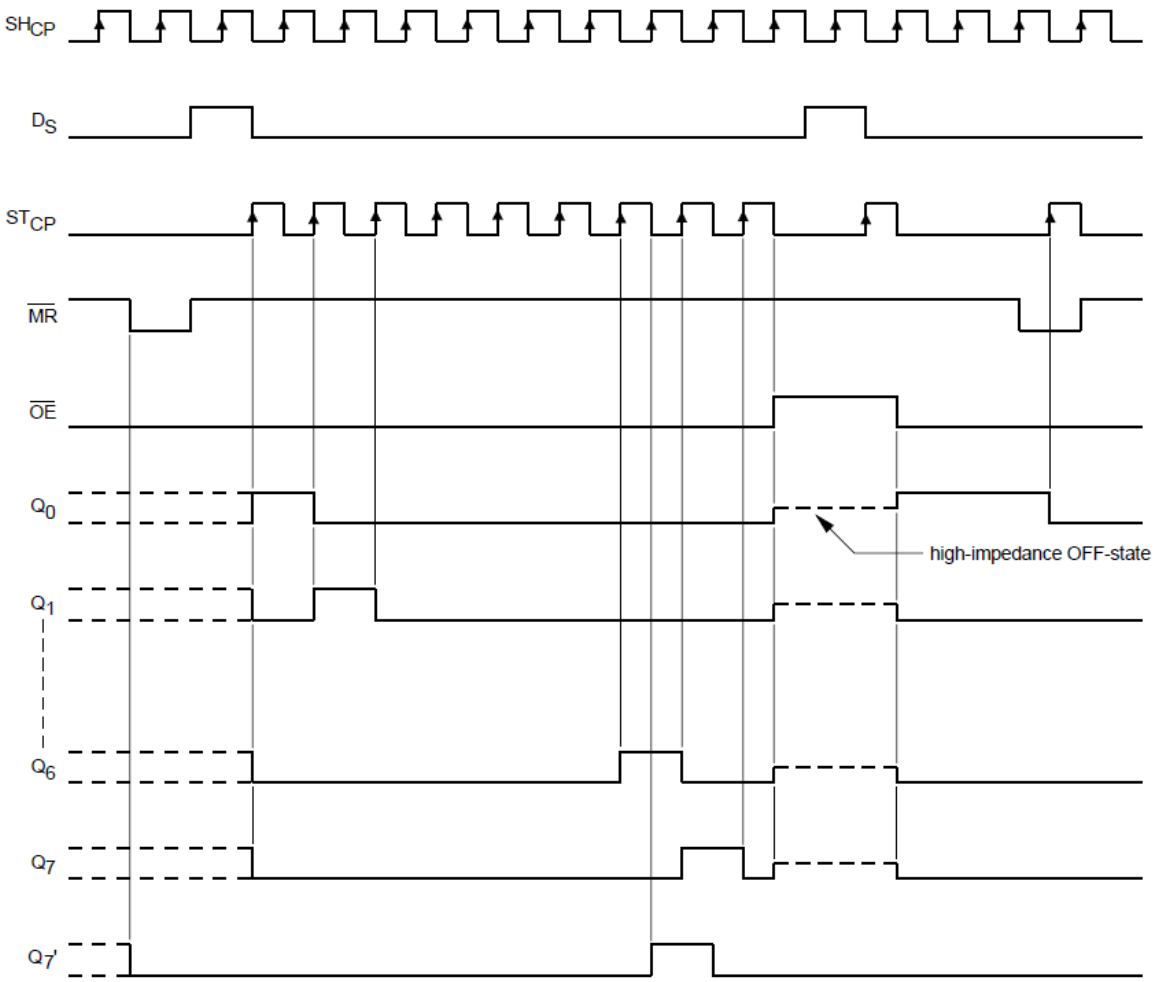
1. H = HIGH voltage level; L = LOW voltage level

↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition

Z = high-impedance OFF-state; NC = no change

X = don’t care.

Timing diagram



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	-0.5 to + 7.0	V
Vin	DC Input Voltage (Referenced to GND)	-0.5 to VCC + 0.5	V
Vout	DC Output Voltage (Referenced to GND)	-0.5 to VCC + 0.5	V
Iin	DC Input Current, per Pin	±20	mA
Iout	DC Output Current, per Pin	±35	mA
ICC	DC Supply Current, VCC and GND Pins	±75	mA
PD	Power Dissipation in Still Air, SOIC Package TSSOP Package	 500 400	mW
mW	Storage Temperature	-65 to + 150	℃
TL	Lead Temperature, 1 mm from Case for 10 Seconds	260	℃

This device contains protectioncircuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit.For proper operation,

Vin and Vout should be constrained to the range GND _ (Vin or Vout) _ VCC. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)	2	6	V
Vin, Vout	DC Input Voltage, Output Voltage(Referenced to GND)	0	VCC	V
TA	Operating Temperature, All Package Types	-20	85	℃
tr, tf	Input Rise and Fall Time VCC = 2.0 V VCC = 4.5 V VCC = 6.0 V	 0 0 0	 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions		VCC (V)	Guaranteed Limit	Unit
VIH	Minimum High-Level Input Voltage	Vout = 0.1 V or VCC - 0.1 V |Iout| ≤20uA		2.0	1.5	V
				3.0	2.1	
				4.5	3.15	
				6.0	4.2	
VIL	Maximum Low-Level Input Voltage	Vout = 0.1 V or VCC - 0.1 V |Iout| ≤20uA		2.0	0.5	V
				3.0	0.9	
				4.5	1.35	
				6.0	1.8	
VOH	Minimum High-Level Output Voltage, Q0 - Q7	Vin = VIH or VIL | Iout| ≤20uA		2.0	1.9	V
				4.5	4.4	
				6.0	5.9	
		Vin = VIH or VIL	|Iout| ≤2.4 mA	3.0	2.34	V
			|Iout| ≤6.0 mA	4.5	3.84	
			|Iout| ≤7.8 mA	6.0	5.34	
VOL	Maximum Low-Level Output Voltage, Q0 - Q7	Vin = VIH or VIL | Iout| ≤20uA		2.0	0.1	V
				4.5	0.1	
				6.0	0.1	
		Vin = VIH or VIL	|Iout| ≤2.4 mA	3.0	0.33	V
			|Iout| ≤6.0 mA	4.5	0.33	
			|Iout| ≤7.8 mA	6.0	0.33	
VOH	Minimum High-Level Output Voltage, Q7'	Vin = VIH or VIL | Iout| ≤20uA		2.0	1.9	V
				4.5	4.4	
				6.0	5.9	

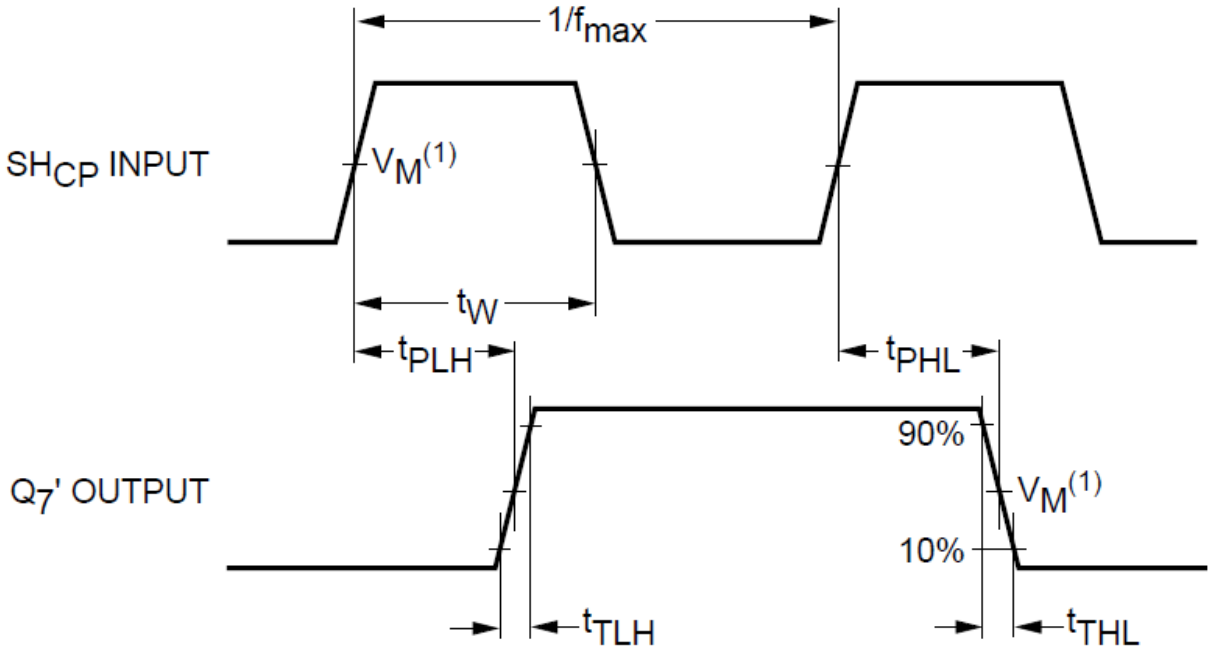
		Vin = VIH or VIL	|Iout|≤2.4 mA	3.0	2.34	V
			|Iout|≤4.0 mA	4.5	3.84	
			|Iout|≤5.2 mA	6.0	5.34	
VOL	Maximum Low-Level Output Voltage, Q7'	Vin = VIH or VIL |Iout|≤20uA		2.0	0.1	V
				4.5	0.1	
				6.0	0.1	
		Vin = VIH or VIL	|Iout|≤2.4 mA	3.0	0.33	V
			|Iout|≤4.0 mA	4.5	0.33	
			|Iout|≤5.2 mA	6.0	0.33	
Iin	Maximum Input Leakage Current	Vin = VCC or GND		6.0	±1.0	uA
IOZ	Maximum Three-State Leakage Current, Q0 – Q7	Output in High-Impedance State Vin = VIL or VIH Vout = VCC or GND		6.0	±2.5	uA
ICC	Maximum Quiescent Supply Current (per Package)	Vin = VCC or GND lout = 0uA		6.0	40	uA

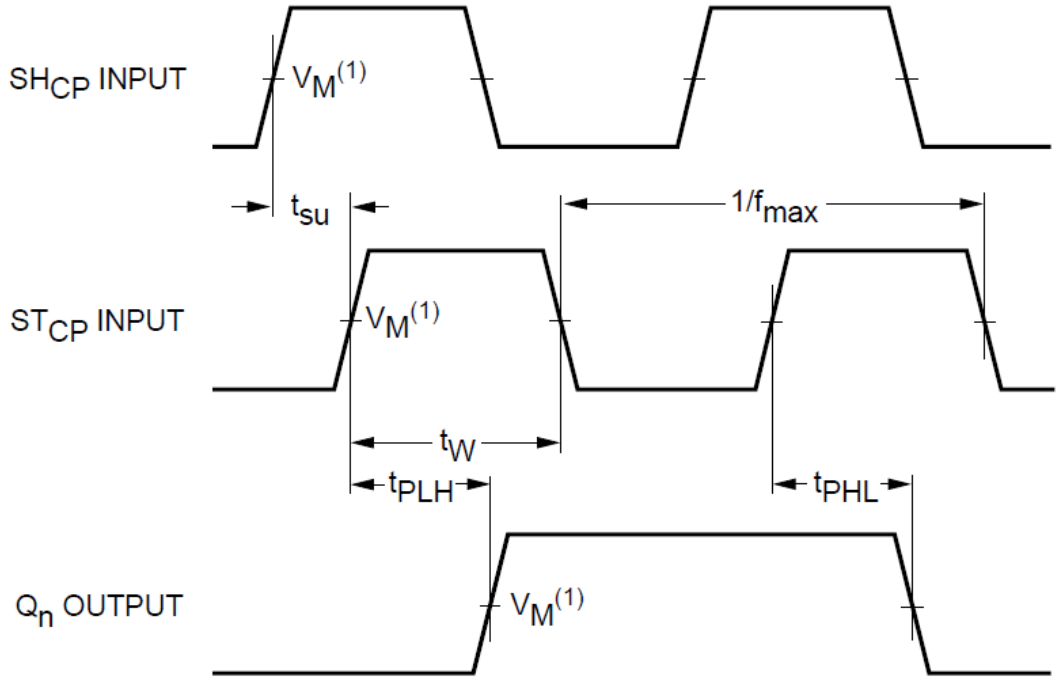
AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6.0 ns)

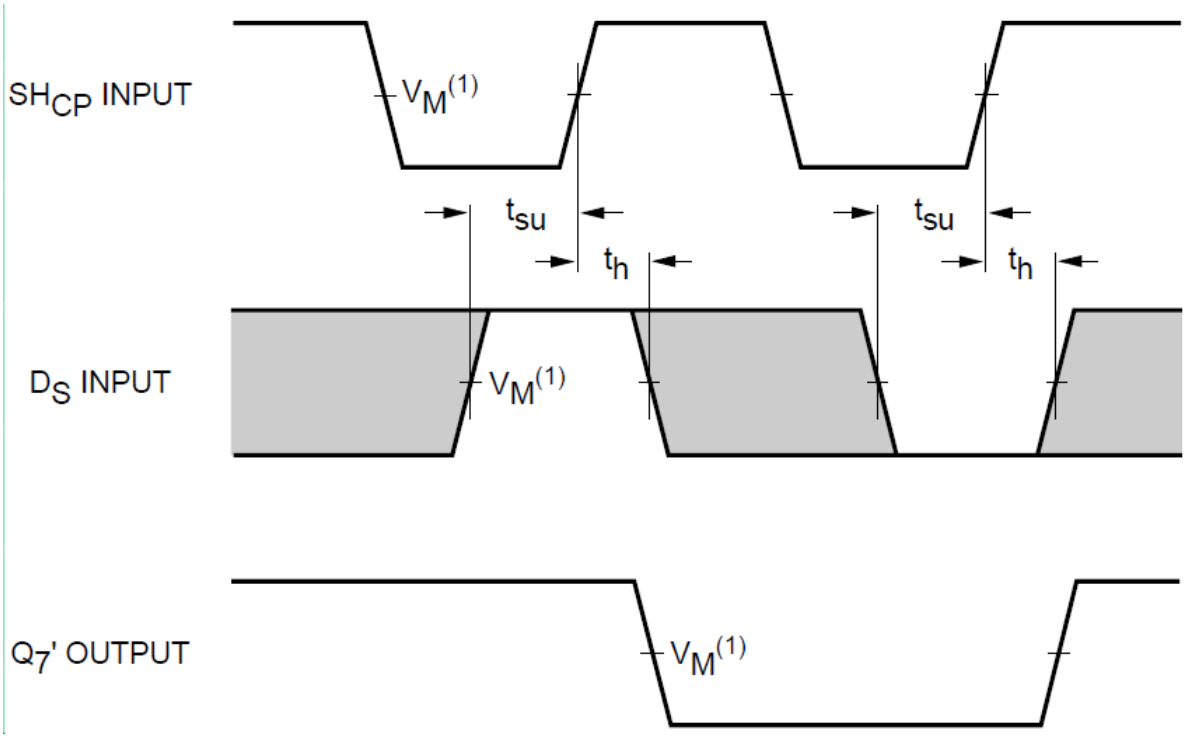
Symbol	Parameter	VCC (V)	Guaranteed Limit	Unit
fmax	Maximum Clock Frequency (50% Duty Cycle)	2.0 3.0 4.5 6.0	2 5 12 14	MHz
tPLH, tPHL	Maximum Propagation Delay, Shift Clock to SQH	2.0 3.0 4.5 6.0	275 225 70 60	ns
tPHL	Maximum Propagation Delay, Reset to Q7'	2.0 3.0 4.5 6.0	280 225 72 62	ns
tPLH, tPHL	Maximum Propagation Delay, Latch Clock to Q0 – Q7	2.0 3.0 4.5 6.0	275 225 70 60	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Q0 – Q7	2.0 3.0 4.5 6.0	290 225 76 68	ns

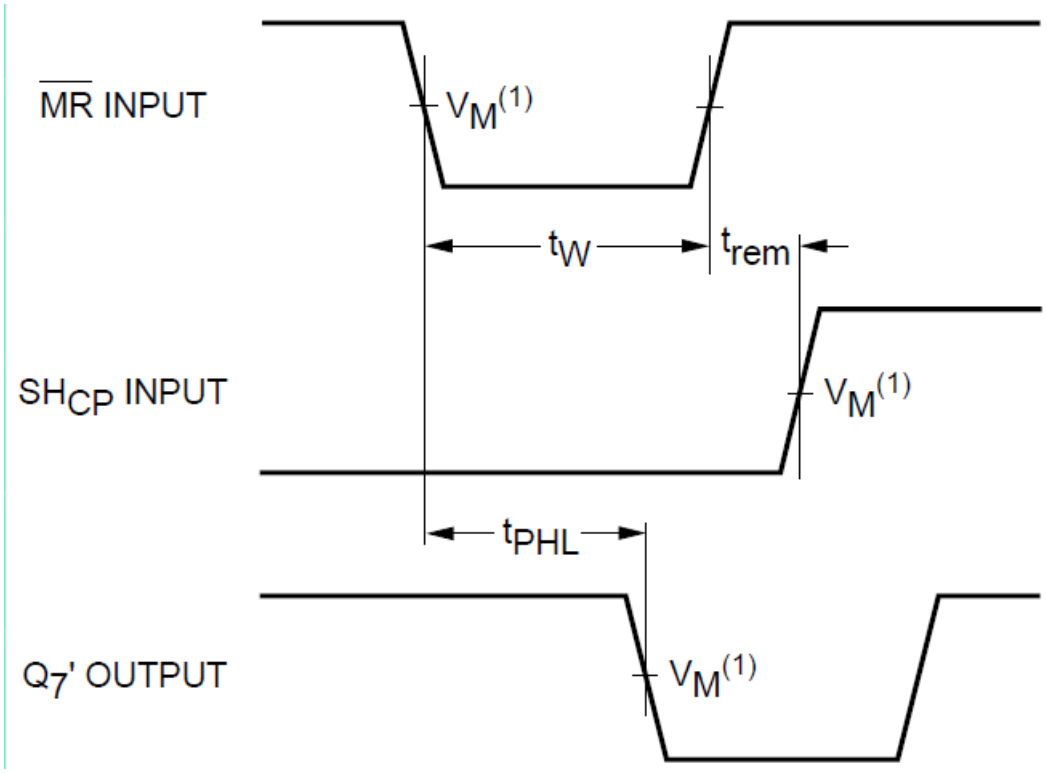
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Q0 – Q7	2.0 3.0 4.5 6.0	270 210 68 58	ns
tTLH, tTHL	Maximum Output Transition Time, Q0 – Q7	2.0 3.0 4.5 6.0	175 54 30 27	ns
tTLH, tTHL	Maximum Output Transition Time, Q7'	2.0 3.0 4.5 6.0	195 65 38 32	ns
Cin	Maximum Input Capacitance		10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q0 – Q7		15	pF

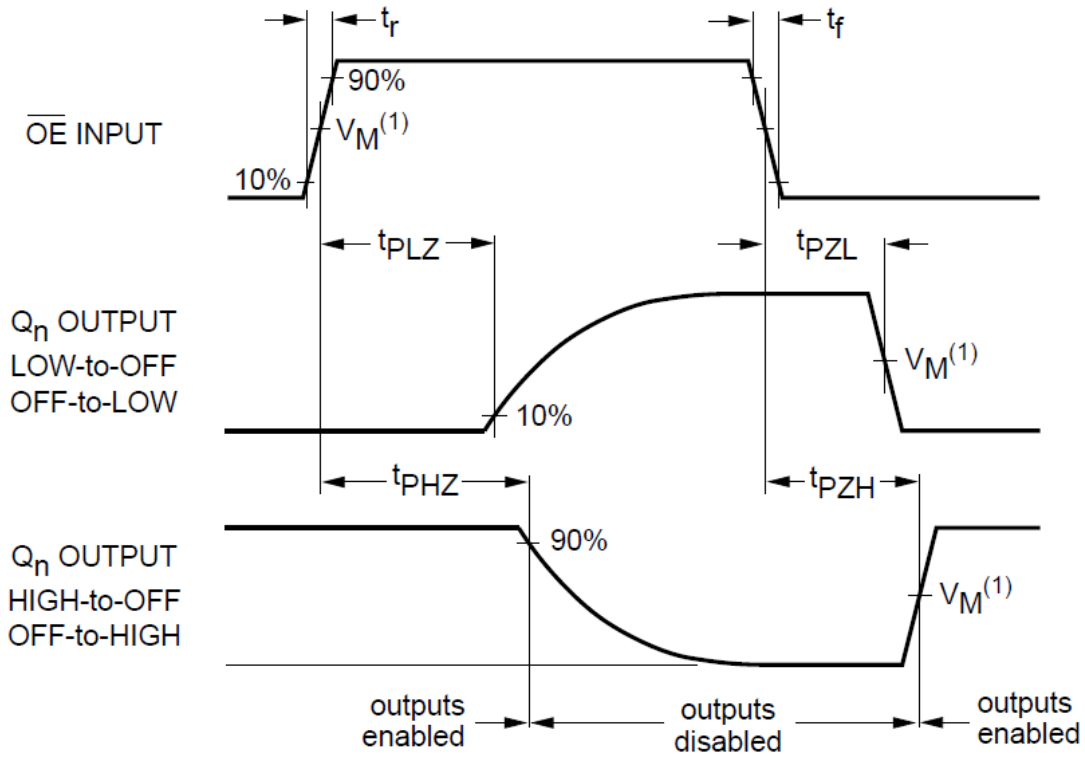
SWITCHING WAVEFORMS



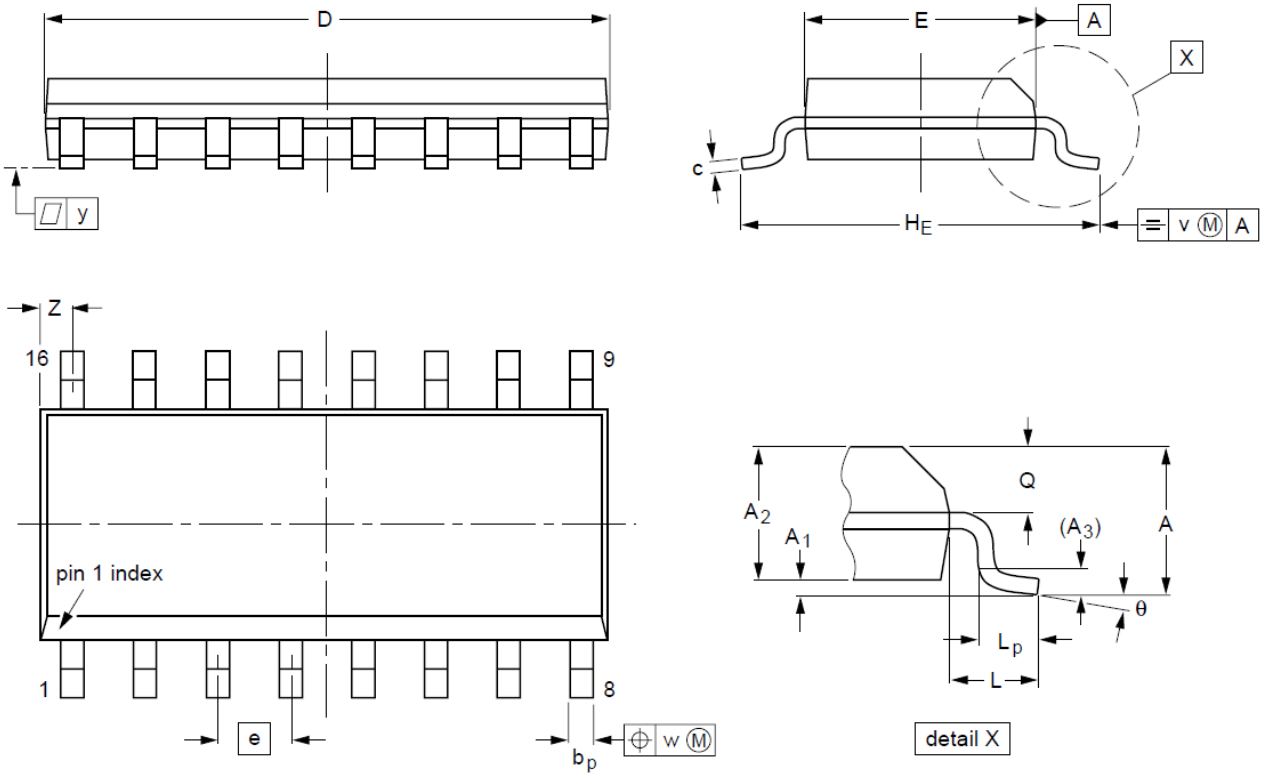

SHCP INPUT
VM(1)
tsu
1/fmax
STCP INPUT
VM(1)
tW
tPLH
tPHL
Qn OUTPUT
VM(1)


SHCP INPUT
VM(1)
tsu
th
tsu
th
DS INPUT
VM(1)
Q7' OUTPUT
VM(1)


MR INPUT
VM(1)
tW
trem
SHCP INPUT
VM(1)
tPHL
Q7' OUTPUT
VM(1)


tr
tf
OE INPUT
90%
VM(1)
10%
tPLZ
tPZL
Qn OUTPUT
LOW-to-OFF
OFF-to-LOW
VM(1)
10%
tPHZ
tPZH
Qn OUTPUT
HIGH-to-OFF
OFF-to-HIGH
90%
VM(1)
outputs enabled
outputs disabled
outputs enabled

SOP16



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

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