

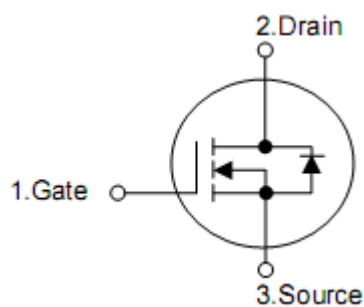
1. Features

- Advanced Trench technology
- $R_{DS(ON)}=2.4m\Omega$ (typ.) @ $V_{GS}=10V$
- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- 100% ΔV_{ds} TESTED
- 100% UIS TESTED

2. Pin configuration



DFN5*6



Pin	Function
4	Gate
5,6,7,8	Drain
1,2,3	Source

3. Ordering Information

Part Number	Package	Brand
KNY3004B	DFN5*6	KIA

4. Absolute maximum ratings

$T_A=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage ($V_{GS}=0V$)	V_{DS}	40	V
Gate-to-Source Voltage ($V_{DS}=0V$)	V_{GS}	± 20	V
Continuous Drain Current ¹⁾	$T_C=25^{\circ}\text{C}$ I_D	120	A
	$T_C=100^{\circ}\text{C}$ I_D	77	A
Pulsed Drain Current @ Current-Pulsed ²⁾	I_{DM}	480	A
Total Power Dissipation ($T_C=25^{\circ}\text{C}$) ⁴⁾	P_D	88.2	W
Avalanche Energy ³⁾	EAS	361	mJ
Operation Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

5. Thermal characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance, Junction-to-Case ¹⁾	$R_{\theta JC}$	1.7	$^{\circ}\text{C/W}$

6. Electrical characteristics

(T_A=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V,	-	-	1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =-250uA	1.0	1.6	2.5	V
Static Drain-Source On-Resistance ²⁾	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	2.4	3.2	mΩ
		V _{GS} =4.5V, I _D =20A	-	3.0	4.2	mΩ
Gate Resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1.0MHz	-	1.4	-	Ω
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1.0MHz	-	5020	-	pF
Output Capacitance	C _{oss}		-	415	-	pF
Reverse Transfer Capacitance	C _{rss}		-	350	-	pF
Turn-On Delay Time	t _{d(on)}	V _{DS} =20V, V _{GS} =10V, R _G =2.0Ω, I _D =30A	-	13	-	ns
Rise Time	t _r		-	15	-	ns
Turn-Off Delay Time	t _{d(off)}		-	48	-	ns
Fall Time	t _f		-	20	-	ns
Total Gate Charge	Q _g	V _{DS} =20V, V _{GS} =10V, I _D =30A	-	110	-	nC
Gate-Source Charge	Q _{gs}		-	8.2	-	nC
Gate-Drain Charge	Q _{gd}		-	26	-	nC
Source-Drain Current (Body Diode) ^{1),5)}	I _{SD}	—	-	-	120	A
Diode Forward Voltage ²⁾	V _{SD}	V _{GS} =0V, I _{SD} =30A, T _J =25°C	-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =30A, di/dt=100A/μs	-	42	-	nS
Reverse Recovery Charge	Q _{rr}		-	46	-	nC
Forward Turn-on Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS +LD)				

Notes:

- 1) The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2) The data tested by pulsed, pulse width≤300us, duty cycle≤2%.
- 3) The test condition is V_{DD}=24V, V_{GS}=10V, L=0.5mH, I_{AS}=38A.
- 4) The power dissipation is limited by 175°C junction temperature.
- 5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

7. Typical Characteristics

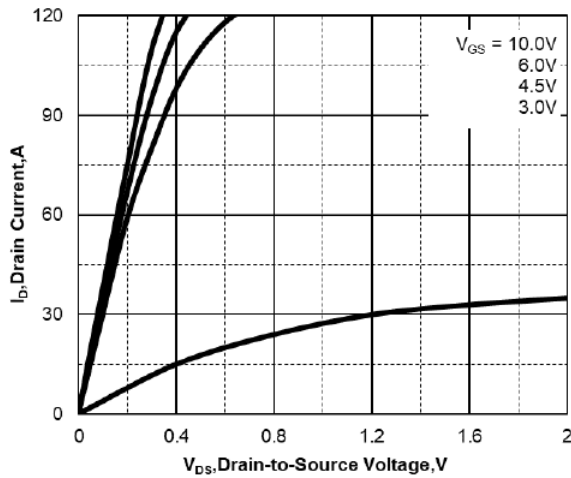


Fig1: Typical Output Characteristics

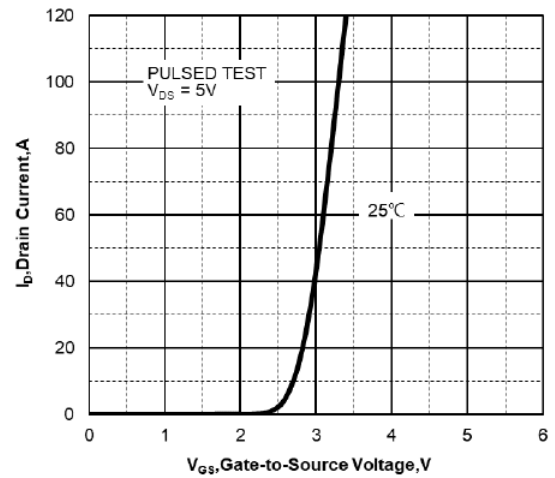


Fig 2: Typical Transfer Characteristics

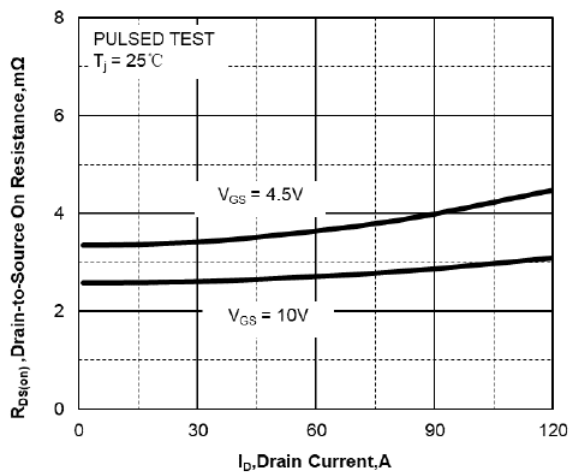


Fig 3: On-Resistance VS. Drain Current

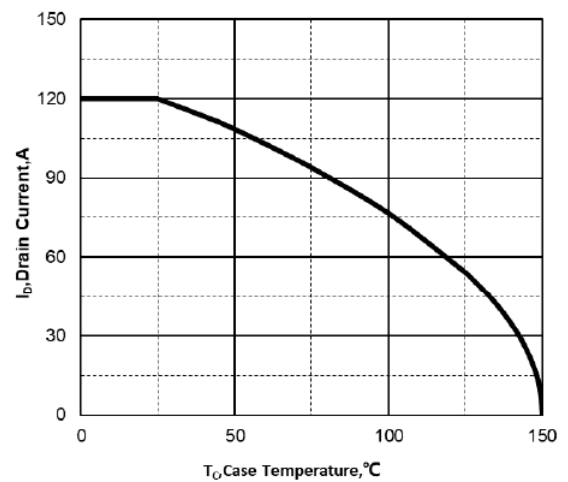


Fig 4: Maximum Continuous Drain Current VS. Case Temperature

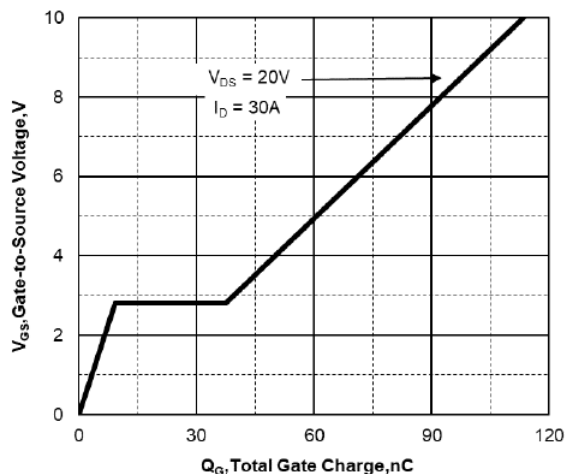


Fig 5: Gate Charge Characteristics

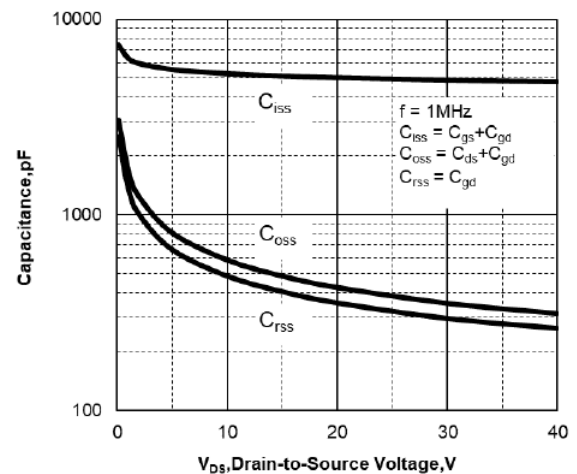


Fig 6: Capacitance Characteristics

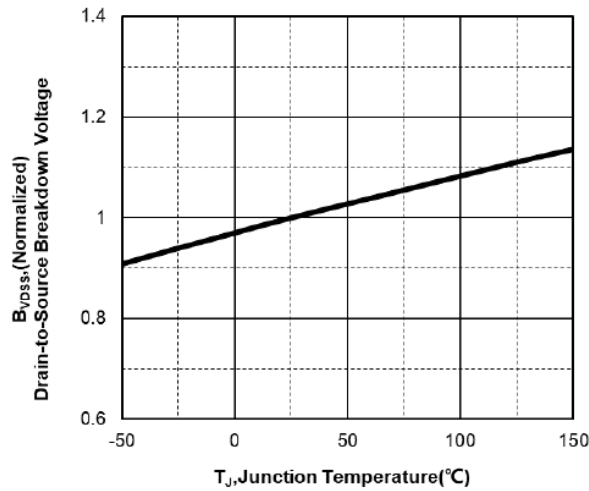


Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

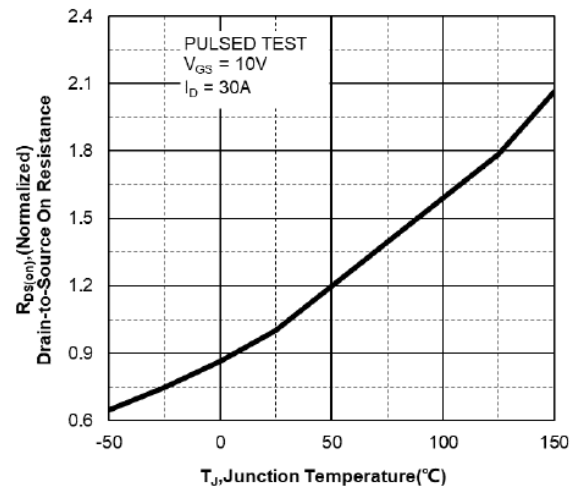


Fig 8: Normalized on Resistance VS. Junction Temperature

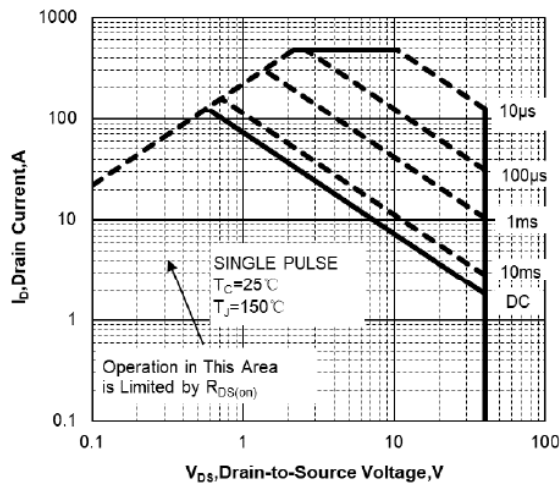


Fig 9: Maximum Safe Operating Area

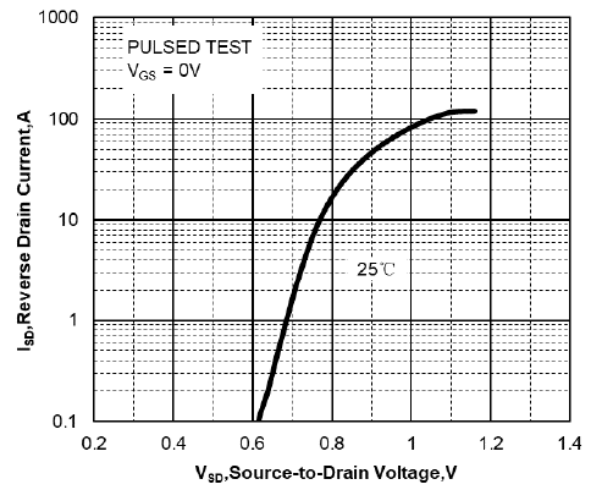


Fig 10: Body Diode Forward Characteristics

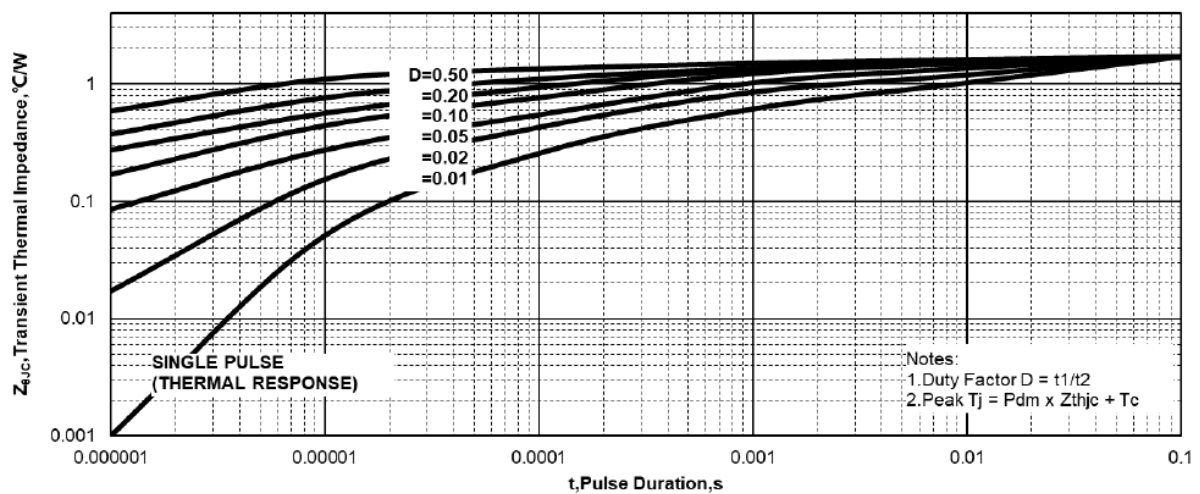


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

8. Test Circuit & Waveform

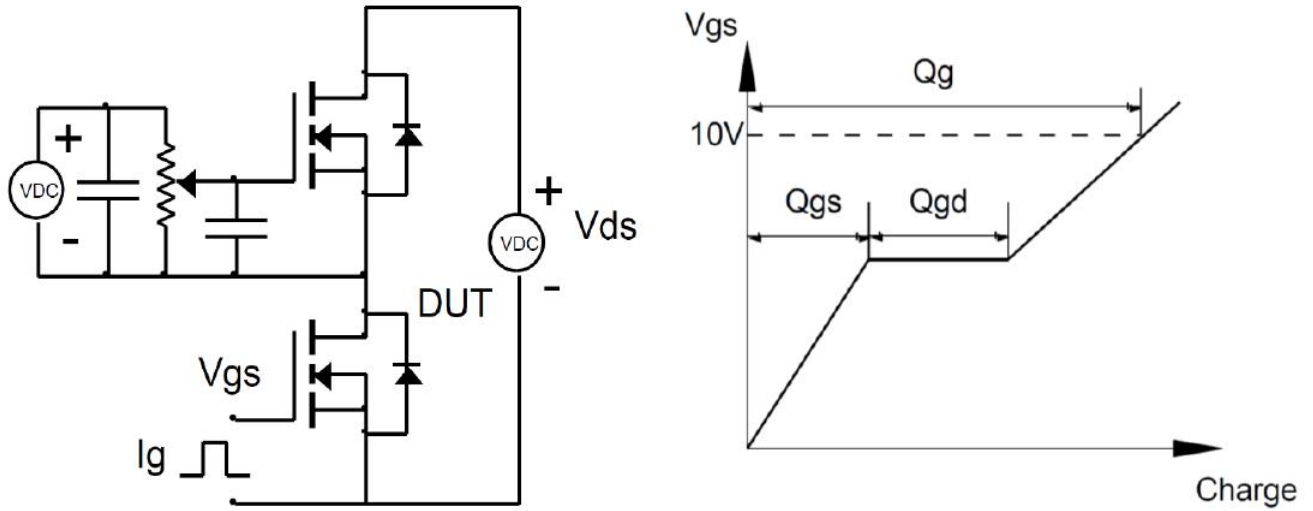


Fig 12: Gate Charge Test Circuit and Waveforms

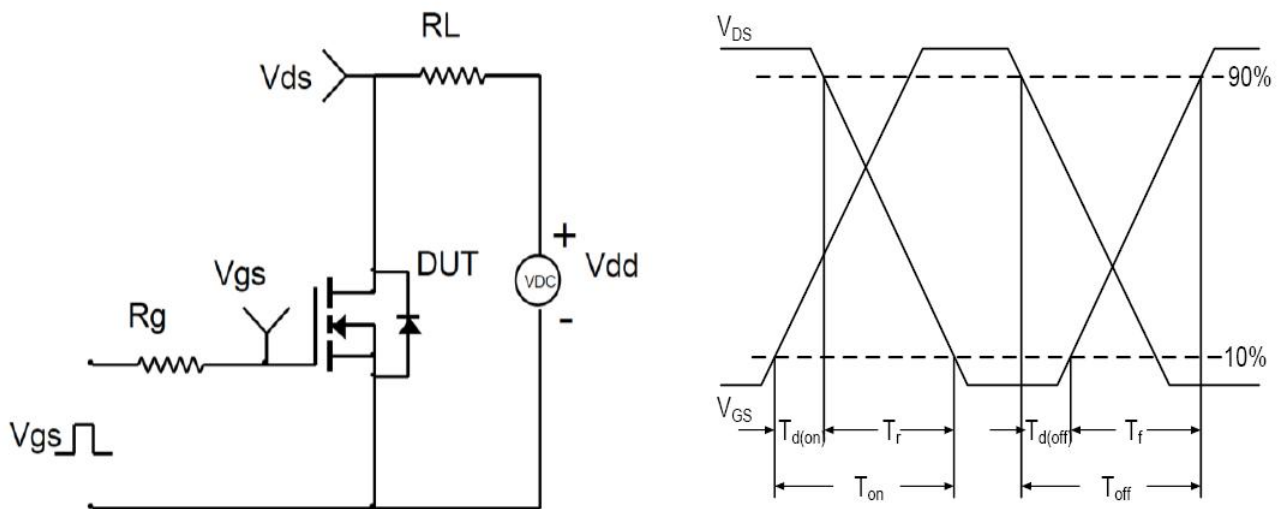


Fig 13: Resistive Switching Test Circuit and Waveforms

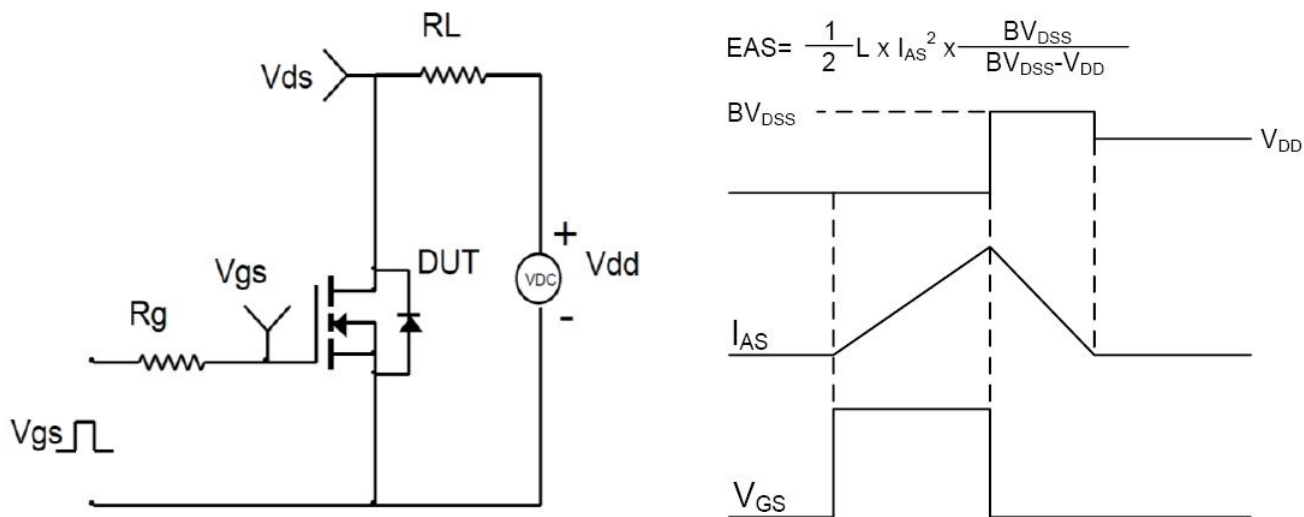


Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms