1. Features

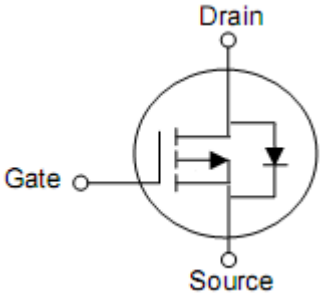
- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

2. Applications

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

3. Pin configuration

DFN5*6 TO-252



Pin		Function
DFN5*6	TO-252	
4	1	Gate
5,6,7,8	2	Drain
1,2,3	3	Source

4. Ordering Information

Part Number	Package	Brand
KPY6115A	DFN5*6	KIA
KPD6115A	TO-252	KIA

5. Absolute maximum ratings

T_C=25°C unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V_{DS}	-150	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS} @ -10V [1]	T_C=25°C	I_D	-10	A
	T_C=100°C	I_D	-6.4	A
Pulsed Drain Current [2]		I_{DM}	-40	A
Total Power Dissipation [4]	T_C=25°C	P_D	89	W
	T_C=100°C	P_D	35	W
Avalanche Energy [3]		EAS	30.2	mJ
Avalanche Current		I_{AS}	-11	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

6. Thermal characteristics

Parameter	Symbol	Typ.	Unit
Thermal Resistance, Junction-to-Ambient [1]	$R_{\theta JA}$	20	°C/W
Thermal Resistance, Junction-to-Case [1]	$R_{\theta JC}$	1.4	°C/W

7. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250uA	-150	-	-	V
Drain-Source On-State Resistance 2)	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5A	-	300	320	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250uA	-2.0	-	-4.0	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-150V,V_{GS}=0V,T_J=25°C	-	-	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Forward Transconductance	gfs	V_{DS}=-5V, I_D=-3A	-	11	-	S
Gate Resistance	R_g	V_{DS}=0V, V_{GS}=0V, f=1MHz	-	5.7	-	Ω
Input Capacitance	C_{iss}	V_{DS}=-40V, V_{GS}=0V , f=1MHz	-	2109	-	pF
Output Capacitance	C_{oss}		-	513	-	pF
Reverse Transfer Capacitance	C_{rss}		-	408	-	pF
TotalGate Charge	Q_g	V_{DS}=-50V, V_{GS}=-10V , I_D=-3A	-	35	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	8.5	-	nC
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=-50V,V_{GS}=-10V, R_G=3Ω,I_D=-3A	-	28	-	ns
Rise Time	T_r		-	30	-	ns
Turn-Off DelayTime	$T_{d(off)}$		-	230	-	ns
Fall Time	T_f		-	130	-	ns
Continuous Source Current 1),5)	I_S	V_G=V_D=0V, Force Current	-	-	-10	A
Diode Forward Voltage 2)	V_{SD}	V_{GS}=0V, I_S=-5A , T_J=25°C	-	-	-1.2	V
Reverse Recovery Time	t_{rr}	I_F=-5A , T_J=25°C dI/dt=100A/μs,	-	34	-	nS
Reverse Recovery Charge	Q_{rr}		-	32	-	nC

Notes:
1) The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2) The data tested by pulsed, pulse width≤300us, duty cycle ≤2%
3) The EAS data shows Max. rating. The test condition is V_{DD}=-50V, V_{GS}=-10V, L=0.5mH, I_{AS}=-11A
4) The power dissipation is limited by 150°C junction temperature.
5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

9. Typical Characteristics

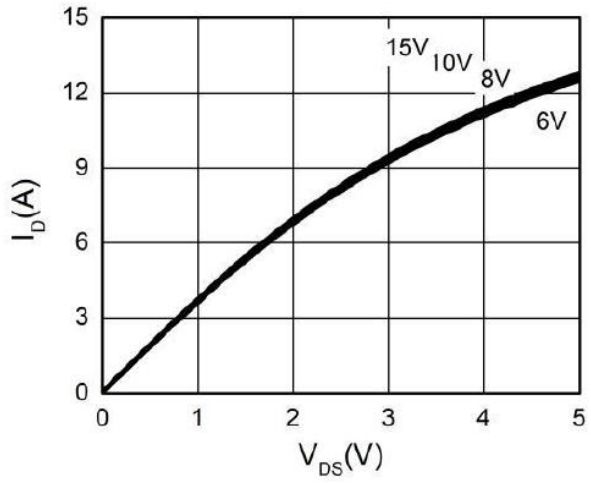


Fig.1 Typical Output Characteristics

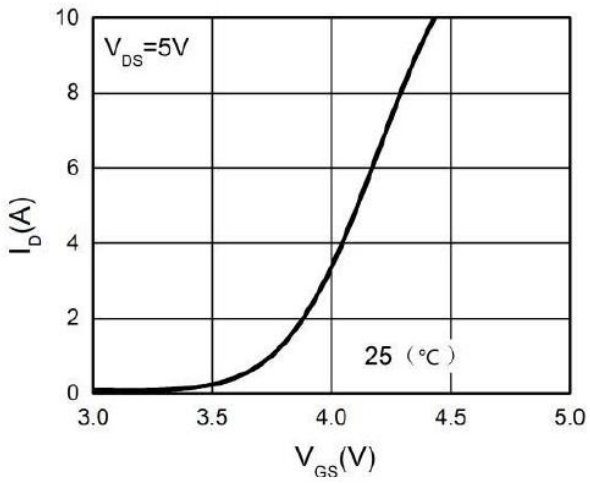


Fig.2 Transfer Characteristics

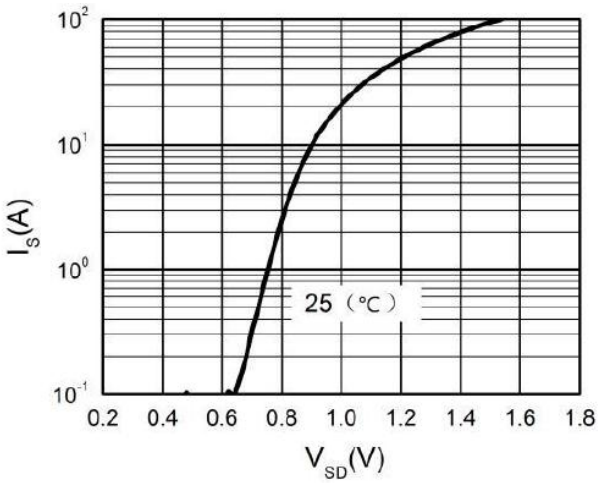


Fig.3 Forward Characteristics Of Reverse

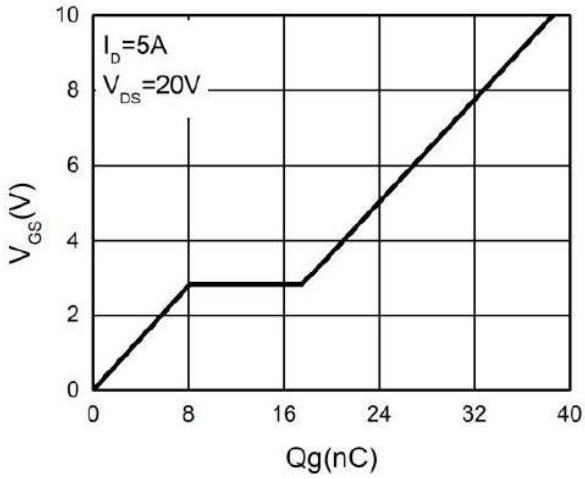


Fig.4 Gate-Charge Characteristics

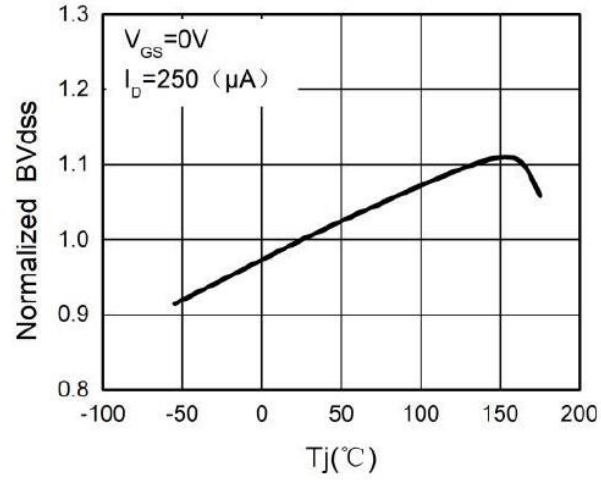


Fig.5 Normalized BV_{DSS} vs. T_J

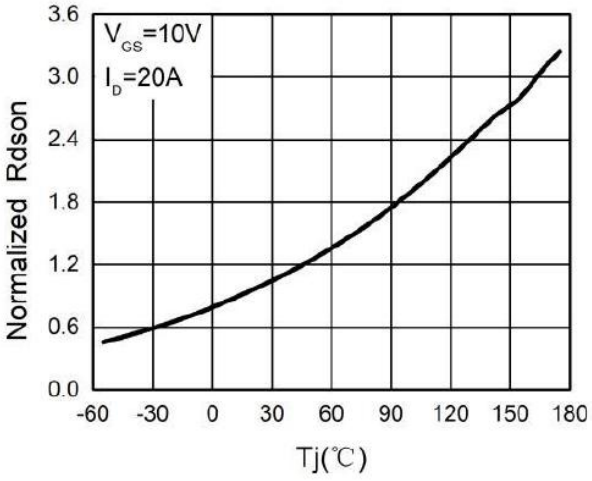


Fig.6 Normalized R_{DSON} vs. T_J

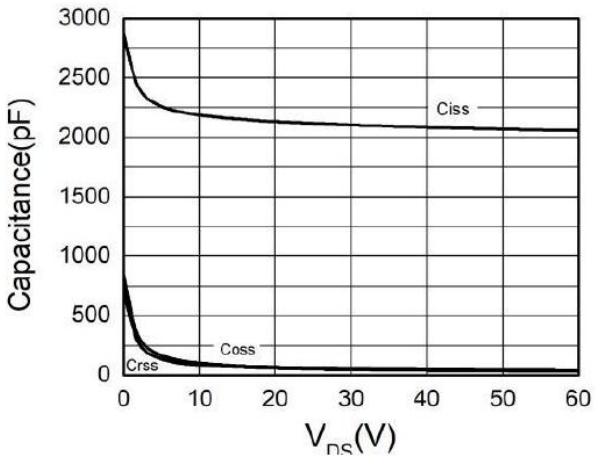


Fig.7 Capacitance

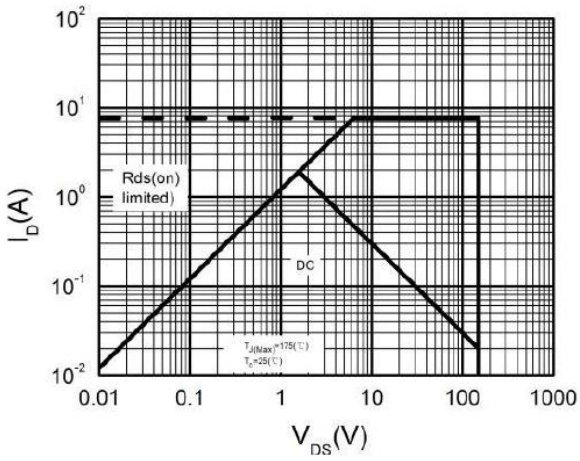


Fig.8 Safe Operating Area

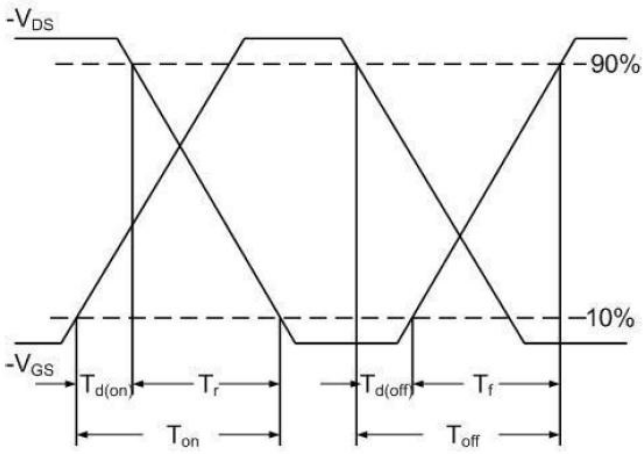


Fig.9 Switching Time Waveform

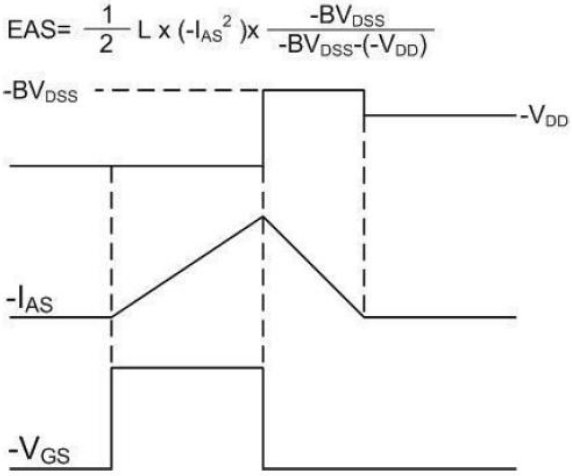


Fig.10 Unclamped Inductive Switching Waveform