Single Channel High Speed Low Side Driver with Negative Input Capability (20V Supply, 5A peak source and sink)

1 FEATURES

- 5A Peak Source Current and 5A Peak Sink Current
- 4.5V - 20V Wide Supply Voltage Range
- Down to -5V Negative Input Voltage Capability
- Fast Propagation Delay: 13ns
- Fast Rising and Falling Time: 9ns and 6ns
- TTL Input-Logic Threshold
- Under Voltage Lock Out Protection
- Low Quiescent Current: 30uA
- Output Low When Input Floating
- Available in SOT23-THN and SOIC-8L Package

2 APPLICATIONS

- Power MOSFET Gate Driver
- IGBT Gate Driver
- GaN Device Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

3 ORDERING INFORMATION

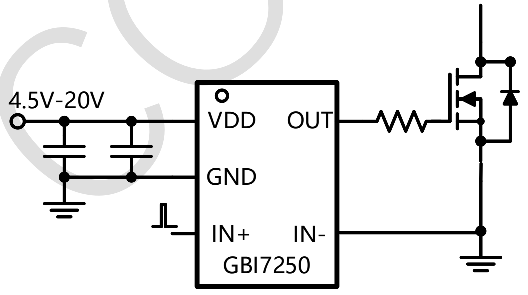
TYPE	MARKING	PACKAGE
GBI7250TJBR	7250	SOT23-THN
GBI7250SMBR	7250	SOIC-8L

4 DISCRIPTION

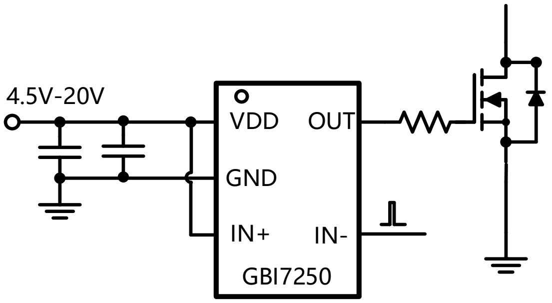
The GBI7250, single channel high speed low side gate driver, provides 5A peak source and sink current along with rail-to-rail driving capability for MOSFET, IGBT, and GaN power device. The device features a minimum 13ns input to output propagation delay and 20V power supply rail makes it suitable for high frequency power converter application. The negative input is acceptable down to -5V for enhancing the input noise immunity. The wide input hysteresis is compatible for TTL low voltage logic. The Flexible configuration of the IN+ and IN- input makes GBI7250 SOT23-THN either as non-inverting or inverting driver. It operates over a wide temperature range -40°C to 150°C.

The GBI7250 is available both in SOT23-THN and SOIC-8L package.

5 TYPICAL APPLICATIONS

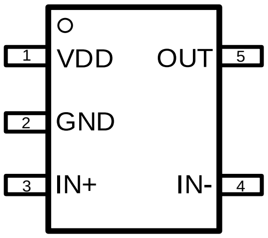


Non-Inverting Input(SOT23-THN)

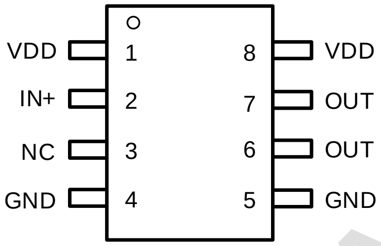


Inverting Input(SOT23-THN)

6 PIN CONFIGURATION AND FUNCTIONS



Top View: SOT23-THN



Top View: SOIC-8L

	PIN OUT		I/O	PIN FUNCTION
PACKAGE	**SOT23-THN**	**SOIC-8L**		
NAME	**NO.**	**NO.**		
VDD	1	1,8	I	Power supply of gate driver. Must be decoupled by ceramic cap. A 0.1uF, and 1uF or 10uF are recommended.
GND	2	4,5	I	Power ground. Must be soldered directly to ground planes for improved thermal performance and electrical contact.
IN+	3	2	I	Non-inverting logic input, TTL compatible. Floating logic low. In Non-Inverting configuration, apply PWM signal on IN+. In inverting configuration, connect IN+ to VDD.
IN-	4	N/A	I	Inverting logic input and only available in SOT23-THN package, TTL compatible. Floating logic low. In Non-Inverting configuration, connect IN- to GND. In inverting configuration, apply PWM signal on IN-.
OUT	5	6,7	O	Gate driver output.
NC	N/A	3	-	No connection.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Logic Input	IN+, IN-	-5	22	V
Gate Driver Output	OUT	-0.3	22	V
Supply Voltage	VDD	-0.3	24	V
Operating junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

7.2 ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 Recommended Operation Conditions

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	20	V
V_{IN+},V_{IN-}	Input voltage range	-5	20	V
T_J	Operating junction temperature	-40	150	°C

7.4 Thermal Information

PARAMETER	THERMAL METRIC	SOT23-THN	SOIC-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	107.8	130.8	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	52.4	80	°C/W
ψ_{JB}	Junction to board characterization parameter	23	70.9	°C/W
ψ_{JT}	Junction to top characterization parameter	10	22	°C/W

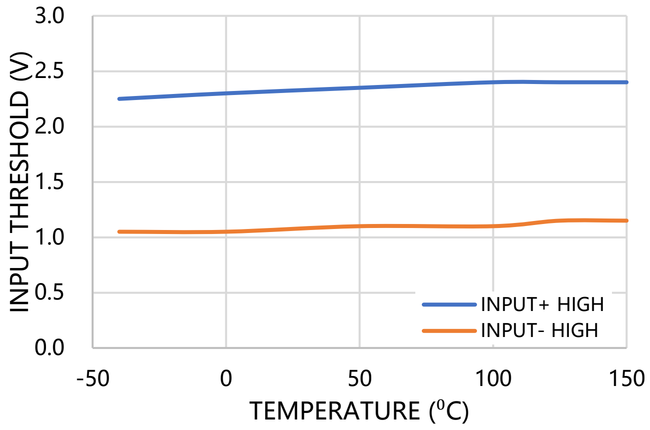
7.5 Electrical Characteristics

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{DD}	Operating supply voltage		4.5		20	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Quiescent current	IN+=GND, V_{DD}=3.5V IN-=VDD(SOT23-THN)		30		uA
		IN+=GND, V_{DD}=12V IN-=VDD(SOT23-THN)		100		uA
Inputs						
V_{IN+}	Input+ logic high threshold			2.3	2.6	V
V_{IN+}	Input+ logic low threshold		0.95	1.1		V
V_{IN+_Hys}	Hysteresis			1.2		V
V_{IN-_H}	Input- logic high threshold	SOT23-THN		2.3	2.6	V
V_{IN-_L}	Input- logic low threshold	SOT23-THN	0.95	1.1		V
V_{IN-_Hys}	Hysteresis	SOT23-THN		1.2		V
Outputs						
$I_{SINK/SRC}$	Output Sink/Source peak current	C_{Load}=10nF, F_{sw}=1kHz		5		A
R_{OH}	Output pull high resistance	I_{OUT}= - 10mA		10	14	Ω
R_{OL}	Output pull low resistance	I_{OUT}= 10mA		0.6	1.2	Ω
Timing						
T_R	Output rising time	C_{Load}=1nF	5.3	9	14	ns
T_F	Output falling time	C_{Load}=1nF	3.1	6	11	ns
T_{D_IN+}	IN+ to output propagation delay, Rising edge		6	13	25	ns
	IN+ to output propagation delay, Falling edge		6	13	25	ns
T_{D_IN-}	IN- to output propagation delay, Rising	SOT23-THN	6	13	25	ns
	IN- to output propagation delay, Falling	SOT23-THN	6	13	25	ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		15	25	ns

8 TYPICAL CHARACTERISTICS

V_{DD}=12V, Cload=1nF, T_A= 25°C.



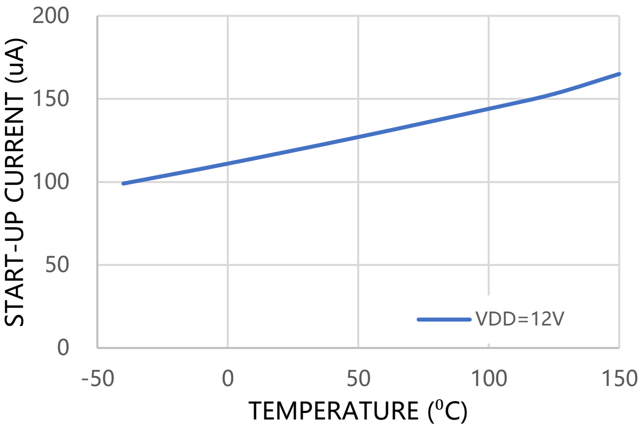
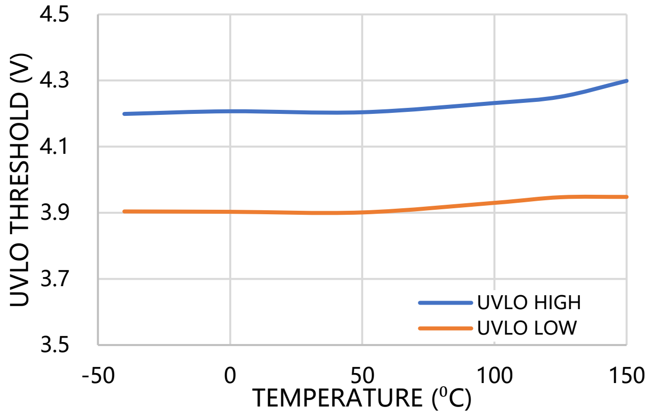


Figure 1.IN Threshold Vs Temperature

Figure 2. Start-up current Vs Temperature



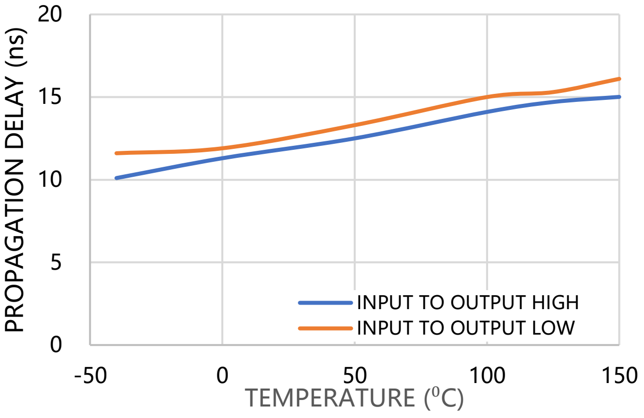
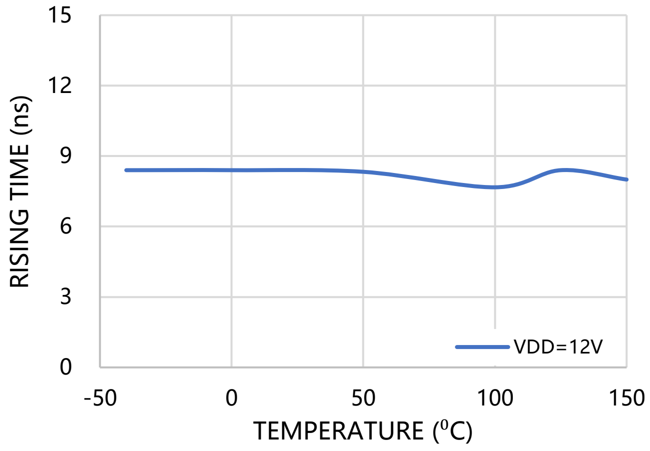


Figure 3. UVLO Vs Temperature

Figure 4. Input to Output Propagation Delay Vs Temperature



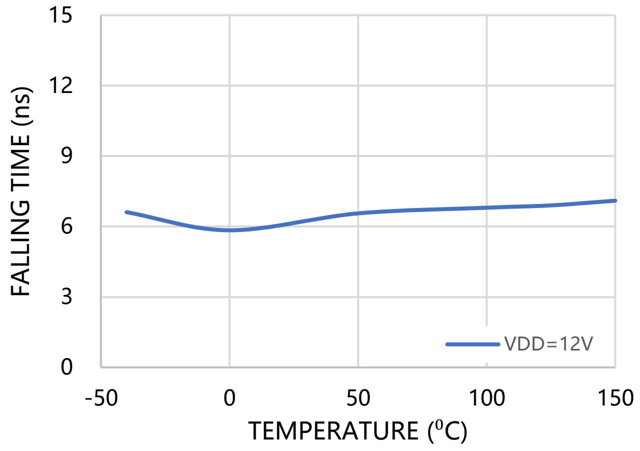


Figure 5. Output Rising Time Vs Temperature

Figure 6. Output Falling Time Vs Temperature

9 FUNCTIONAL BLOCK DIAGRAM

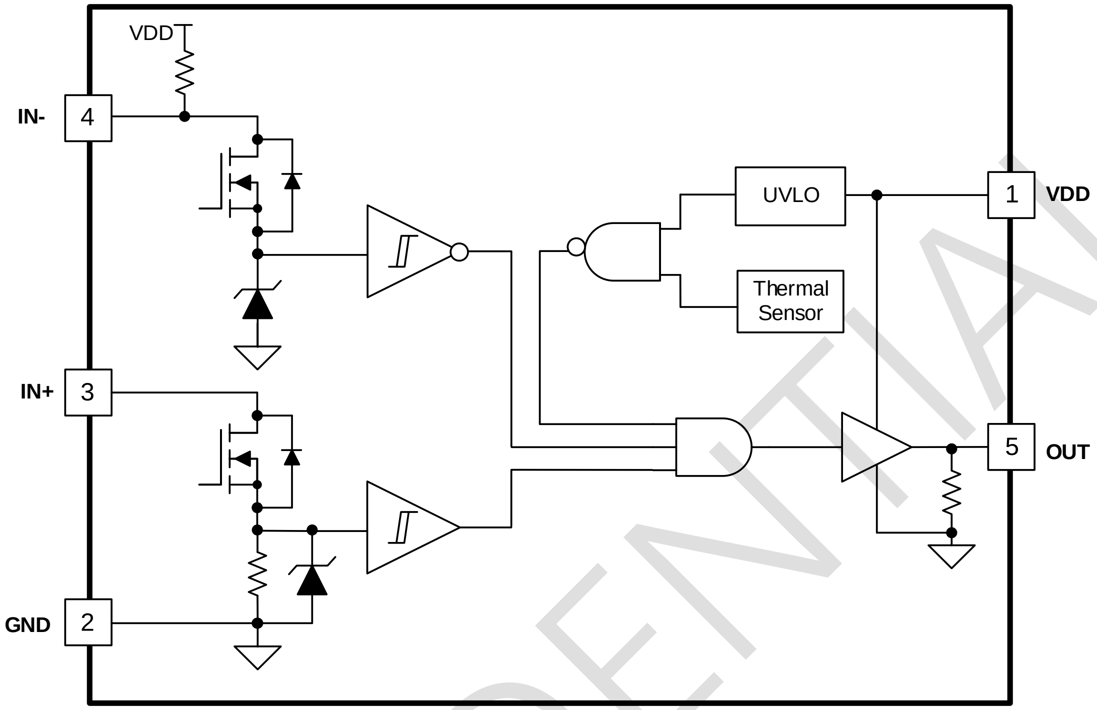


Figure 7. GBI7250 Block Diagram (SOT23-THN)

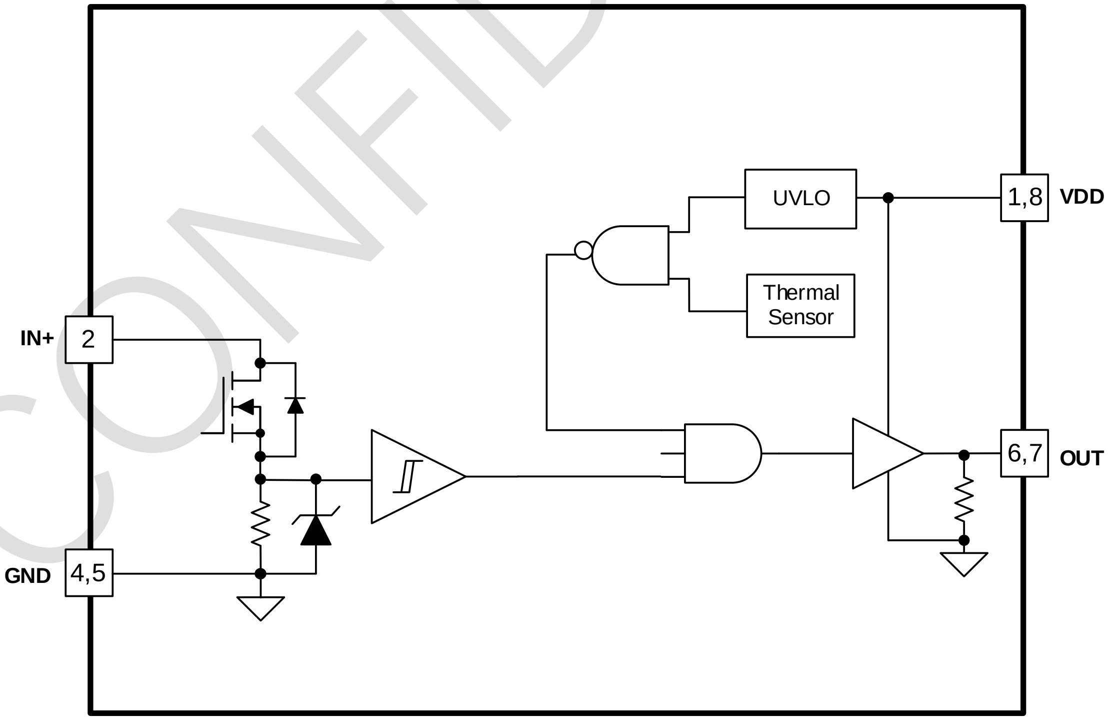


Figure 8. GBI7250 Block Diagram (SOIC-8L)

10 DISCRIPTION

10.1 Overview

The GBI7250 is a single channel, high speed, low side gate driver for power MOSFET, IGBT and GaN HMET with up to 20V wide supply and 5A source/sink peak current along with the minimum input to output propagation delay of 13ns. The input is able to be down to -5V DC which enhances the driver input stage noise immunity. The 20V rail-to-rail output improves the GBI7250 output stage robustness during the switching load fast transition.

10.2 VDD Power Supply

The GBI7250 operates under a supply voltage range between 4.5V to 20V. It’s recommended to put two VDD bypass capacitor in parallel to prevent noise problems on supply VDD. It has to put a 0.1uF SMT ceramic capacitor as close as possible between the VDD pin to the GND pin. To avoid the unexpected VDD glitch, a large capacitor (ex. 1uF or 10uF) with relatively low ESR must be connected in parallel with that 0.1uF capacitor. This parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

10.3 VDD Under Voltage Lock Out (UVLO)

The GBI7250 implements the Under Voltage Lock Out (UVLO) with rising threshold of typically 4.2V along with 300mV typical hysteresis. The VDD voltage which is able to down to 4.5V is especially suitable for driving wide band gap power device, like GaN.

The UVLO holds the output low regardless of the input status when VDD is rising but the level is below the UVLO threshold. The hysteresis prevents output bouncing caused by the noise impact on the power supply. During power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD till VDD steady state reached.

The inverting operation in Figure 9 and non-inverting operation in Figure10 show that the output remains low till the UVLO threshold reached, and then the output is in-phase with the input.

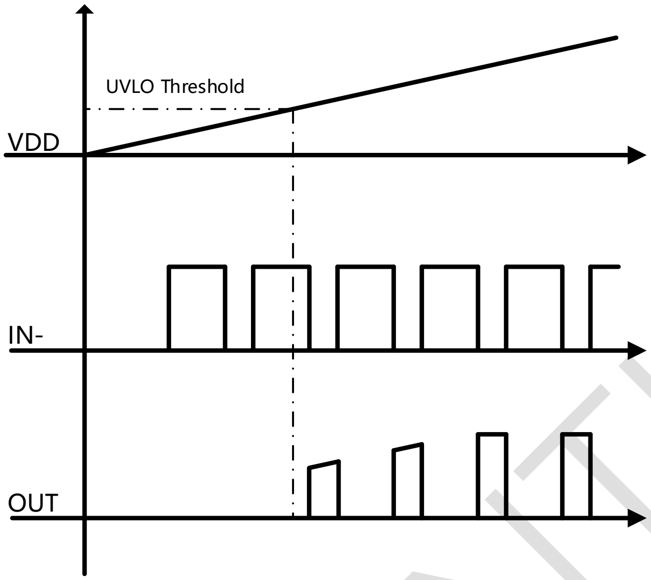


Figure 9. GBI7250 Output (IN- Input) Vs VDD

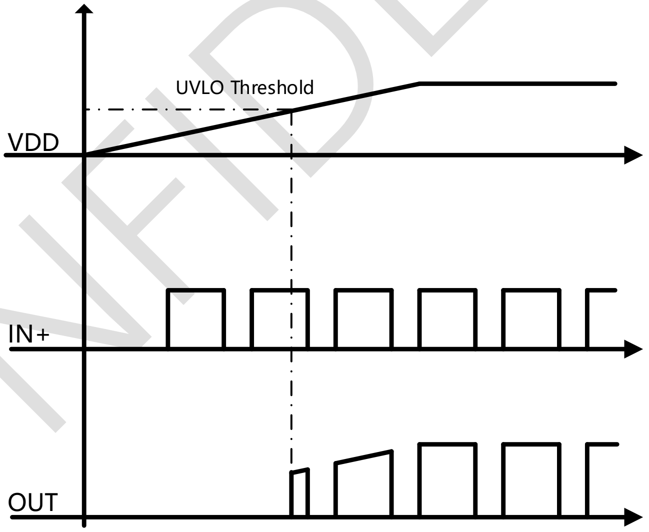


Figure 10. GBI7250 Output (IN+ Input) Vs VDD

10.4 Input Stage

The GBI7250 input is compatible on TTL logic which is independent of the VDD supply voltage. The typical threshold is 2.3V (high) and 1.0V (low), which make the device easily driven by PWM control signals derived from 3.3V and 5V digital power-controller devices. The device features wider hysteresis compared to typical threshold of 0.5V which offers enhanced noise immunity. It also implements tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

10.5 Operation Mode

The dual-input design makes the GBI7250 SOT23-THN easy to configure the operation mode of either the inverting (IN– pin) mode or the non-inverting (IN+ pin) mode. The output state is held low when the input pins are floating by the internal pull-up or pull-down resistors. As a result, the unused input pin for SOT 23-THN package must be biased properly to ensure that driver output is enabled for normal operation. Table 1 is the device logic truth table for SOT23-THN package.

Table 1. GBI7250 SOT23-THN Mode Configuration and Device Logic

Mode	Configuration	IN+	IN-	OUT
Non-Inverting Mode	IN- to GND	L	GND	L
	IN- to GND	H	GND	H
Inverting Mode	IN+ to VDD	VDD	H	L
	IN+ to VDD	VDD	L	H
Others	N/A	Floating	Any	L
	N/A	Any	Floating	L

Table 2. GBI7250 SOIC-8L Device Logic

Mode	IN+	OUT
Non-Inverting Mode	L	L
	H	H
Others	Floating	L

11 APPLICATION INFORMATION

11.1 Typical Application

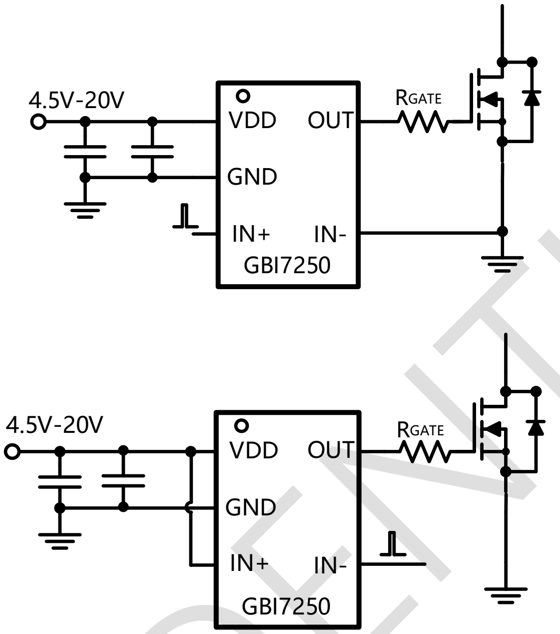


Figure 11. GBI7250 SOT23-THN Single Channel Driver Non-Inverting and Inverting Application

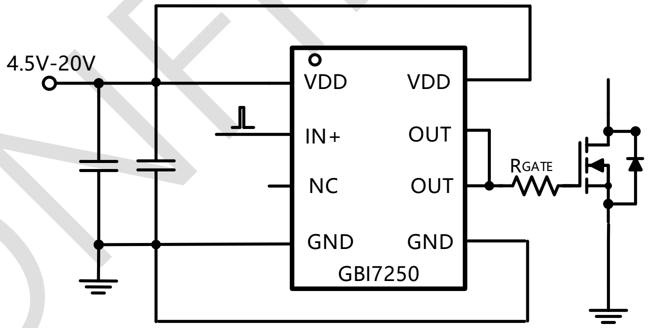


Figure 12. GBI7250 SOIC-8L Single Channel Driver Application

11.2 Driver Power Dissipation

Generally, the power dissipation depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The GBI7250 is designed with very low quiescent currents and internal logic to eliminate any output-stage shoot-through.

The power loss of GBI7250 caused by pure capacitive load is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \tag{1}$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

This equation (1) is also able to be adopted to calculate the switching load of power MOSFET, where gate charge Qg determines the capacitor charges.

$$Q_g = C_{LOAD} \times V_{DD} \tag{2}$$

Normally power device Manufacturers provide specifications with the typical and maximumQg, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \tag{3}$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

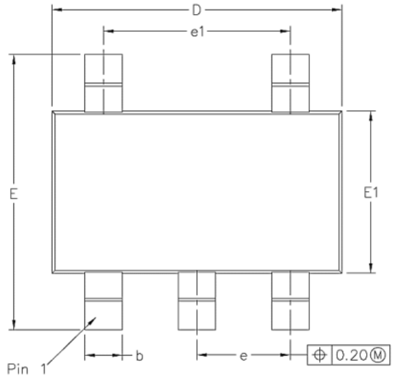
Sometimes, circuit designers put a resistor R_{GATE} between the driver output pin and the gate terminal of power device to slow down the power device transition. The power dissipation of the driver shows as below:

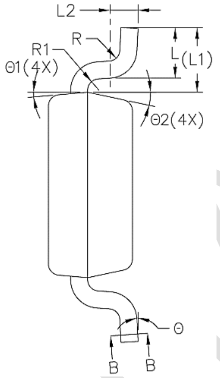
$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_L}{R_L + R_{GATE}} + \frac{R_H}{R_H + R_{GATE}}\right) \tag{3}$$

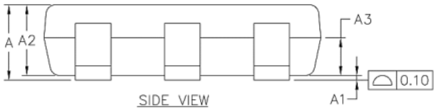
Where

- R_H is the equivalent pull up resistance of GBI7250
- R_L is the equivalent pull down resistance of GBI7250
- R_{GATE} is the gate resistance between driver output and gate of power device.

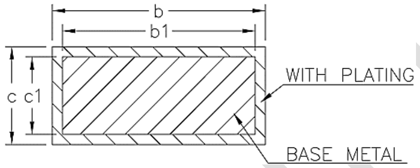
PACKAGE INFORMATION (SOT23-THN)





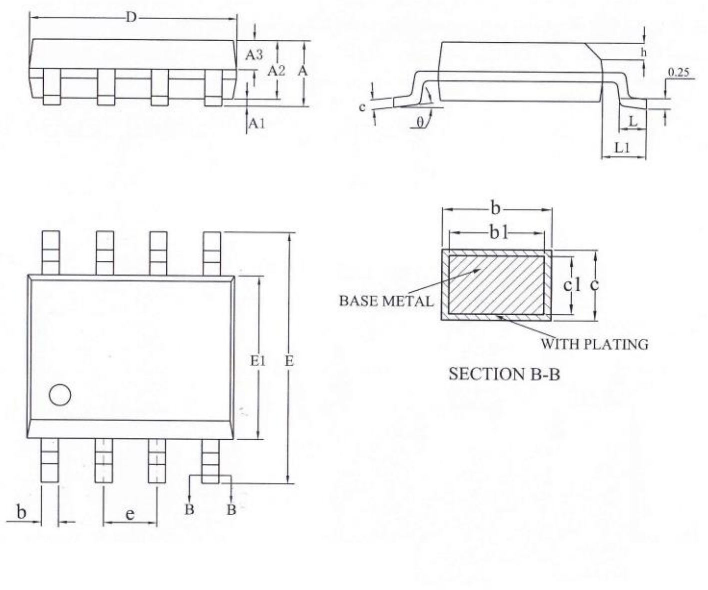


SECTION B-B



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	0.90
A1	0	-	0.15
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.85	2.95	3.05
E	2.65	2.80	2.95
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575REF		
L2	0.25BSC		
R	-	-	0.25
R1	-	-	0.25
Ɵ	0	-	8°
Ɵ1	3°	5°	7°
Ɵ2	10°	12°	14°

PACKAGE INFORMATION (SOIC-8L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
ϴ	0	-	8°