

1. Basic Features

- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green Product (RoHS compliant)
- AEC-Q100 qualified

3. Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V and 24 V truck and transportation system

2. Description

The RM77010DS is a 10mΩ single channel Smart High Side Power Switch, embedded in a DFN9*6-14L, providing protective functions and diagnosis. The power transistor is built by an N-channel MOSFET with charge pump.

4. Product Summary

Over voltage protection	$V_{S(AZ)}$	70	V
Operating voltage	$V_{S(OP)}$	5...48	V
On state resistance	$R_{DS(ON)}$	10	mΩ
Nominal load current	$I_{L(NOM)}$	9	A
Short circuit current limitation	$I_{L(SC)}$	50	A
Typical current sense ratio	$I_L:I_{IS}$	3910	

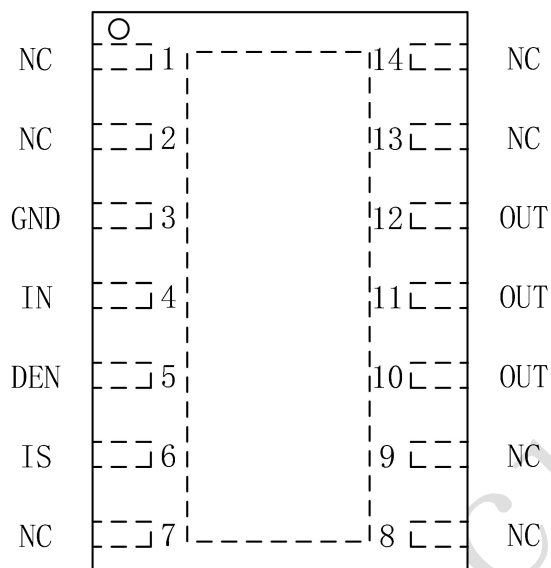
5. Ordering Code

Device	Package Type	Marking	Materials	Package			Package Qty
RM77010DS	DFN9*6-14L	RM77010DS	Halogen free	Tape&reel	10 reels/box	30k/box	3000/reel

Table of Contents

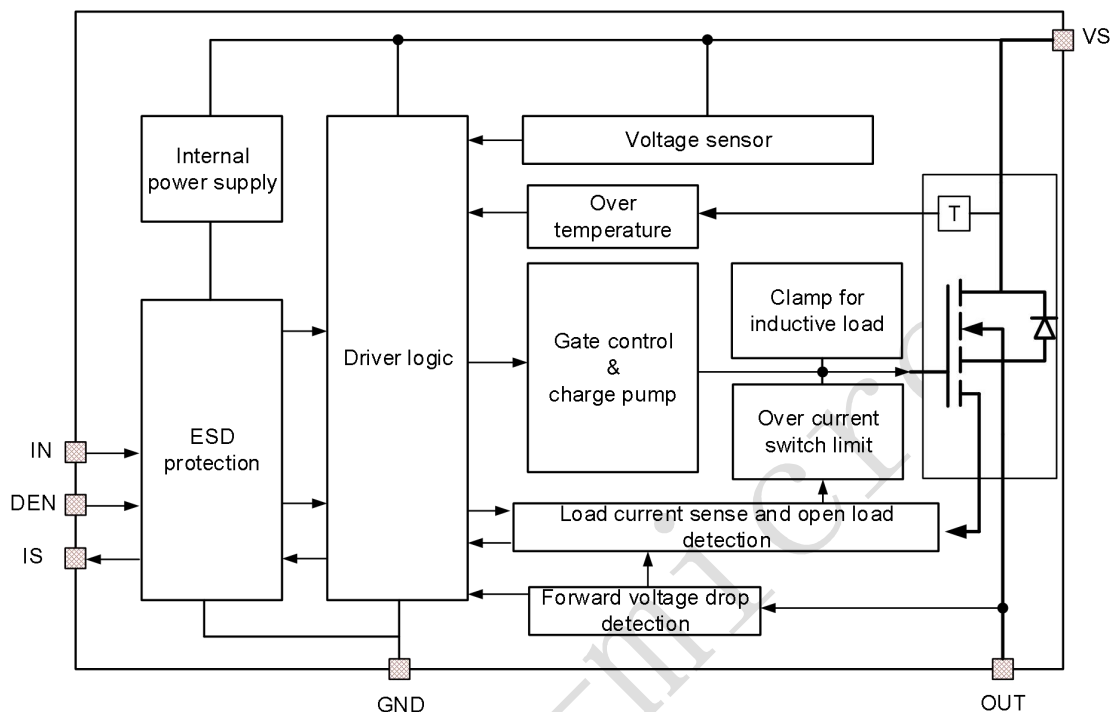
1.Basic Features.....	1
2.Description.....	1
3.Application.....	1
4.Product Summary.....	1
5.Ordering Code.....	1
6.Pin Configuration.....	3
7.Block Diagram.....	4
8.Absolute Maximum Ratings.....	4
9.Electrical Characteristics.....	5
10.Timing diagrams.....	7
11.Truth Table.....	11
12.Functions.....	12
13.Application Information.....	17
14.Package.....	18
15.Recommended Soldering Footprint.....	19
16.Revision History.....	20

6.Pin Configuration



Pin	Symbol	Function
1/2/7/8/9/13/14	NC	Not Connected; No internal connection to the chip
3	GND	GND Ground; Ground connection
4	IN	Input channel; Input signal for channel activation
5	DEN	DEN Diagnostic enable; Digital signal to enable/disable the diagnosis of the device
6	IS	Sense; Sense current of the selected channel
10/11/12	OUT	Output; Protected high side power output channel
PAD	VS	Voltage Supply; Battery voltage

7. Block Diagram



8. Absolute Maximum Ratings

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; (unless otherwise specified)

Parameter	Symbol	Values	Unit
Supply voltage	V_S	48	V
Supply voltage for short circuit protection	V_{bb}	30	V
Supply voltage for Load dump protection	$V_{Loaddump}$	65	V
Power dissipation (DC), $T_C \leq 25^{\circ}\text{C}$	P_{tot}	1.6	W
Junction temperature	T_J	-40 ... 150	$^{\circ}\text{C}$
Ambient temperature	T_a	-40 ... 125	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 ... 150	$^{\circ}\text{C}$

Notes:

1: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9. Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_S=28\text{V}$; (unless otherwise specified)

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ	Max	
R _{DS(ON)_150}	ON-state resistance	I _L =10A, V _{IN} =4.5V, T _J =150°C	-	17	22	mΩ
R _{DS(ON)_25}	ON-state resistance	T _J =25°C	-	10	-	
Supply Voltages:						
V _S	Supply Voltages	V _{IN} =4.5V, R _L =4Ω, V _{DS} <0.5V	5	-	48	V
V _{S(AZ)}	Overvoltage protection	I _{SOV} =5mA	66	70	75	V
V _{S(UV)}	Undervoltage shutdown	V _{IN} =4.5V, R _L =4Ω, From V _{DS} <1V to I _{OUT} =0A	3	3.6	4.1	V
V _{S(OP)_MIN}	Minimum functional supply voltage	V _{IN} =4.5V, R _L =4Ω, From I _{OUT} =0A to V _{DS} <0.5V	3.8	4.5	5	V
I _{S(OFF)}	Standby current	V _S =36V, V _{OUT} =0V, T _J ≤85°C, V _{IN} , V _{DEN} floating	-	0.1	0.5	μA
I _{S(OFF)_150}	Maximum standby current for whole device with load	V _S =36V, V _{OUT} =0V, T _J =150°C, V _{IN} , V _{DEN} floating	-	-	15	μA
I _{L(NOM)}	Nominal load current	T _A =85°C, T _J <150°C	-	9	-	A
V _{DS(AZ)}	Drain to source clamping voltage	I _{DS} =20mA, V _{DS(AZ)} = V _S - V _{OUT}	66	70	75	V
I _{OUT(GND)}	Output leakage current while GND disconnected	V _S =36V	-	0.2	5	μA
I _{GND}	Operating current channel active	V _S =36V, V _{IN} =V _{DEN} =5.5V	-	0.6	2	mA
Input Pin Voltage:						
V _{IN(H)}	High level input voltage range		1.4	1.7	2.3	V
V _{IN(L)}	Low level input voltage range		0.9	1.3	1.9	V
V _{IN(HYS)}	Input voltage hysteresis		-	0.4	-	V
I _{IN(H)}	High level input current	V _{IN} =5.5V	1	10	25	μA
I _{IN(L)}	Low level input current	V _{IN} =0.8V	1	5	25	μA
V _{DEN(H)}	DEN High level input voltage range		1.4	1.7	2.3	V
V _{DEN(L)}	DEN Low level input voltage range		0.9	1.3	1.9	V
V _{DEN(HYS)}	DEN Input voltage hysteresis		-	0.4	-	V
I _{DEN(H)}	DEN High level input current	V _{DEN} =5.5V	1	10	25	μA
I _{DEN(L)}	DEN Low level input current	V _{DEN} =0.8V	1	5	25	μA
dV/dI _{ON}	Turn-ON Slew rate	R _L =4 Ω , V _S =28V, From 30% to 70%V _S	0.7	1.4	2.1	V/us
-dV/dI _{OFF}	Turn-OFF Slew rate	R _L =4 Ω , V _S =28V, From 70% to 30%V _S	1.1	1.8	2.5	
t _{ON}	Turn-ON time	R _L =4 Ω , V _S =28V From V _{IN} =V _{IN_H} to V _{OUT} =90%V _S ,	-	50	150	us
t _{OFF}	Turn-OFF time	R _L =4 Ω , V _S =28V From V _{IN} =V _{IN_L} to	-	50	150	us

		$V_{OUT}=10\%V_S$,				
t_{ON_delay}	Turn-ON delay time	$R_L=4\ \Omega$, $V_S=28V$ From $V_{IN}=V_{IN_H}$ to $V_{OUT}=10\%V_S$,	-	20	70	us
t_{OFF_delay}	Turn-OFF delay time	$R_L=4\ \Omega$, $V_S=28V$ From $V_{IN}=V_{IN_L}$ to $V_{OUT}=90\%V_S$,	-	35	150	us
Diagnostic Characteristics:						
$t_{SIS(ON)}$	Current sense settling time to k_{ILIS} function stable after positive input slope on both INput and DEN	$V_{DEN}=V_{IN}=0$ to 4.5V, $V_S=28V$, $R_{IS}=1.2k\Omega$, $C_{SENSE}<100pF$, $I_L=4A$	-	-	150	us
$t_{SIS(ON_DEN)}$	Current sense settling time with load current stable and transition of the DEN	$V_{IN}=4.5V$, $V_{DEN}=0$ to 4.5V, $R_{IS}=1.2k\Omega$, $C_{SENSE}<100pF$, $I_L=4A$	-	-	65	us
$I_{IS(DIS)}$	IS pin leakage current when sense is disabled	$V_{IN}=4.5V$, $V_{DEN}=0V$, $I_L=10A$	-	-	1	uA
$I_{IS(FAULT)}$	Sense signal maximum current in fault condition	$V_{IS}=V_{IN}=V_{DSEL}=0V$, $V_{OUT}=V_S>10V$, $V_{DEN}=4.5V$	-	7	40	mA
Protection Functions:						
$I_{L(SC)}$	Short circuit current limitation	$V_{DS} = 28V$	-	50	90	A
$t_{d(SC)}$	Short circuit protection delay		-	-	200	us
$T_{J(SC)}$	Thermal shutdown temperature		-	150	-	°C
$V_S-V_{OL(OFF)}$	Open load detection threshold in OFF state	$V_{IN} = 0V$, $V_{DEN} = 4.5V$	3	-	5	V
$V_{IS(AZ)}$	Sense pin maximum voltage	$I_{IS}=5mA$	66	70	75	V
K_{ILIS1}		$I_{L1} = 0.5A$	3090	3860	4630	
K_{ILIS2}		$I_{L2} = 2A$	3490	3830	4170	
K_{ILIS3}		$I_{L3} = 4A$	3700	3890	4080	
K_{ILIS4}		$I_{L4} = 10A$	3720	3910	4080	
E_{AS}	Maximum energy dissipation Single pulse	$I_L=9A$, $T_J=150^\circ C$, $V_S=28V$	-	-	219	mJ
$V_{DS(REV)}$	Drain source diode voltage during reverse polarity	$I_L=-4A$, $T_J=25^\circ C$	200	700	750	mV

10. Timing diagrams

Figure 1: Switching a Resistive Load Timing

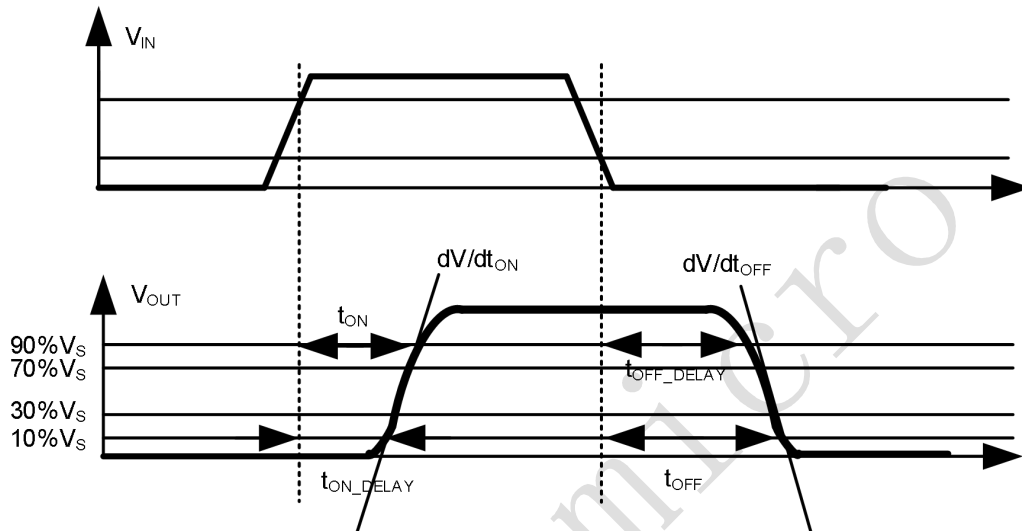


Figure 2: Switching an Inductive Load Timing

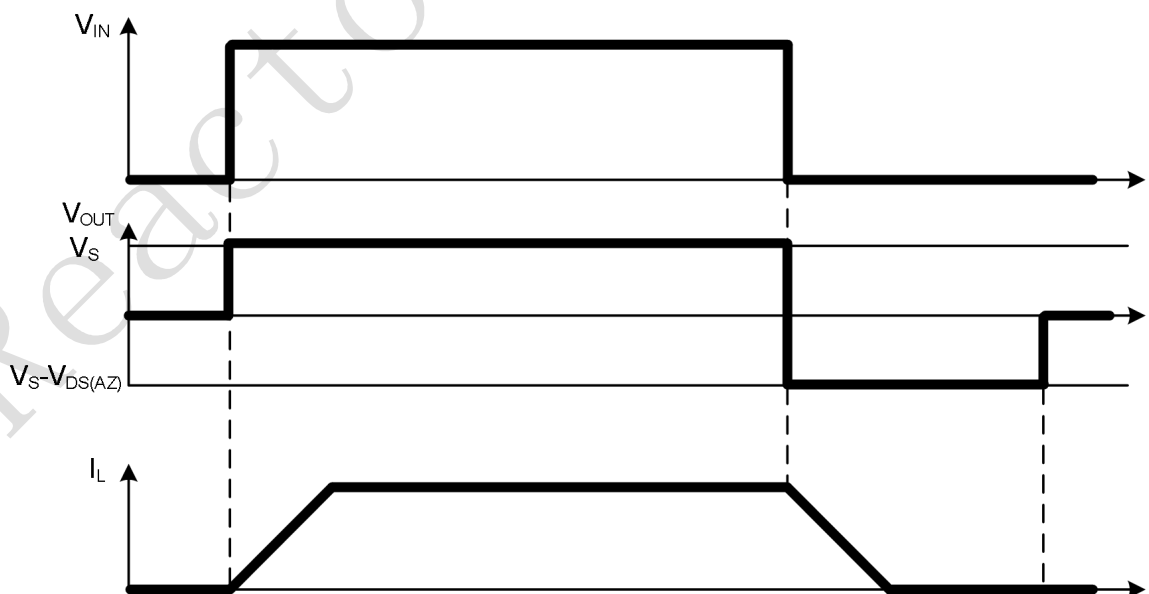


Figure 3: Current Sense Settling / Disabling Timing

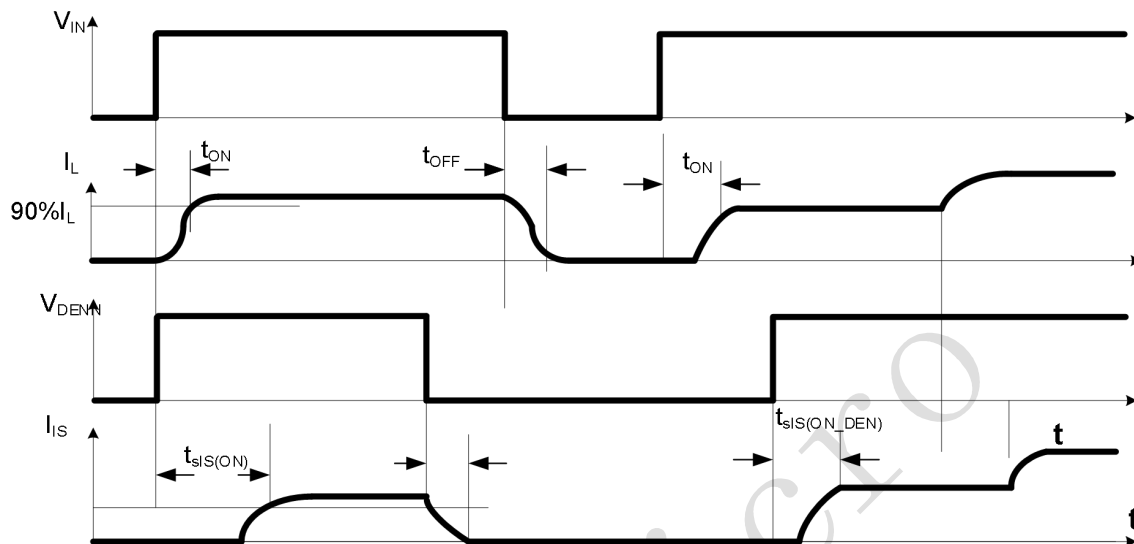


Figure 4: Sense Signal in Open Load Timing

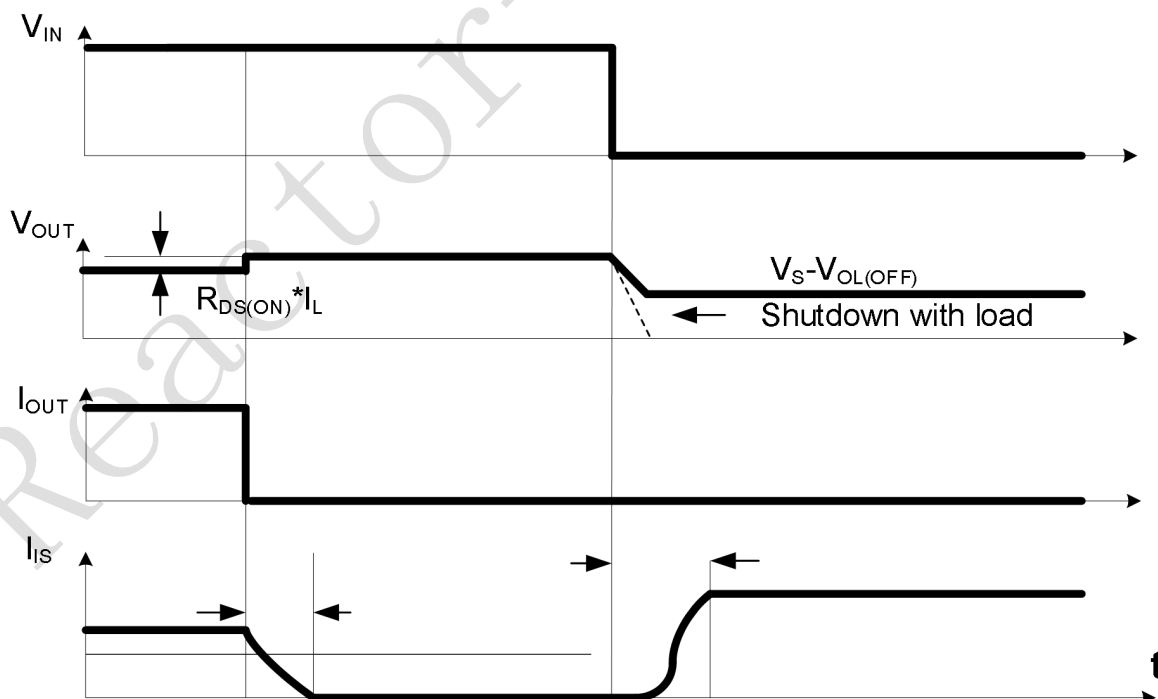


Figure 5: Over temperature

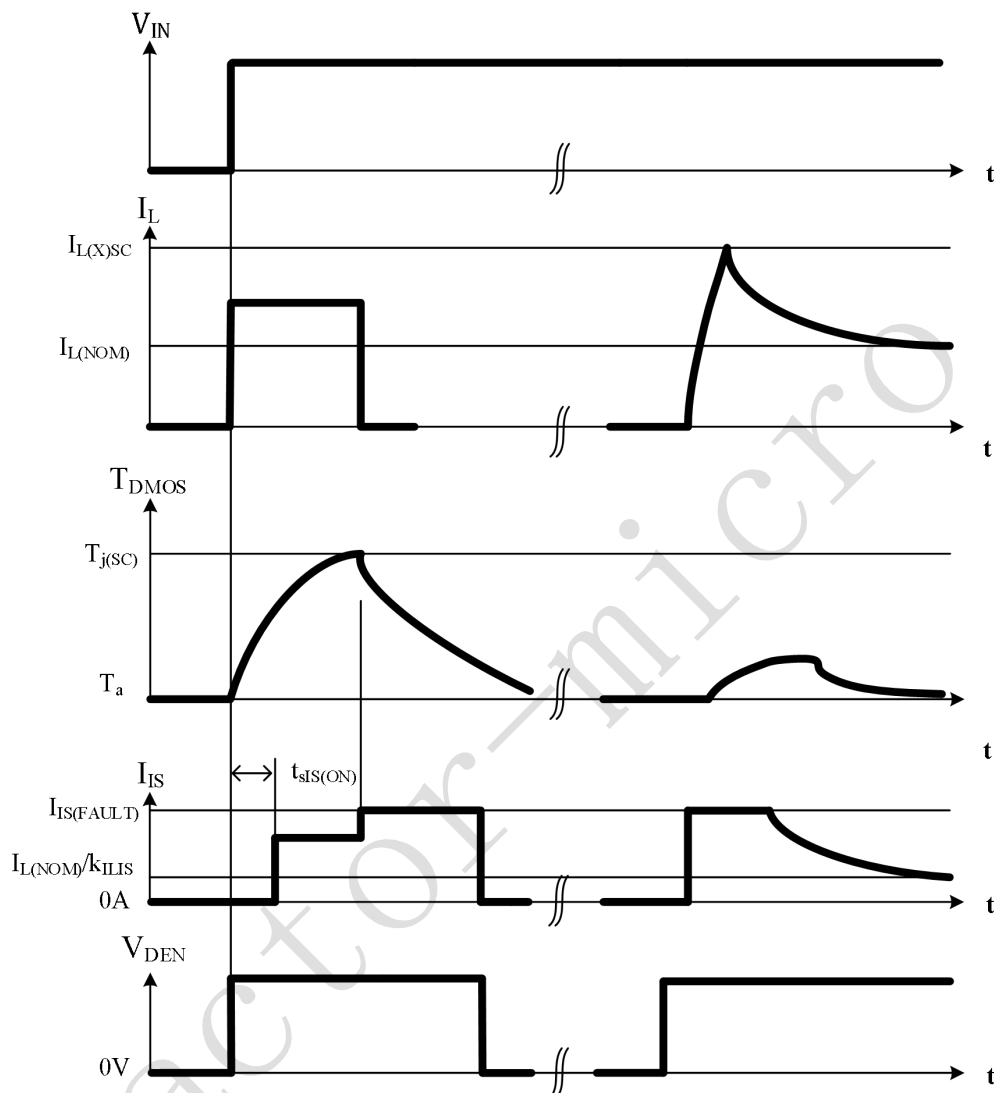


Figure 6: Undervoltage Behavior

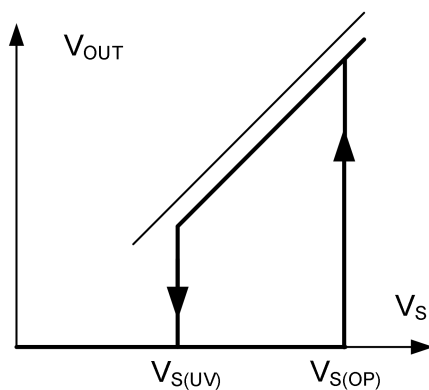
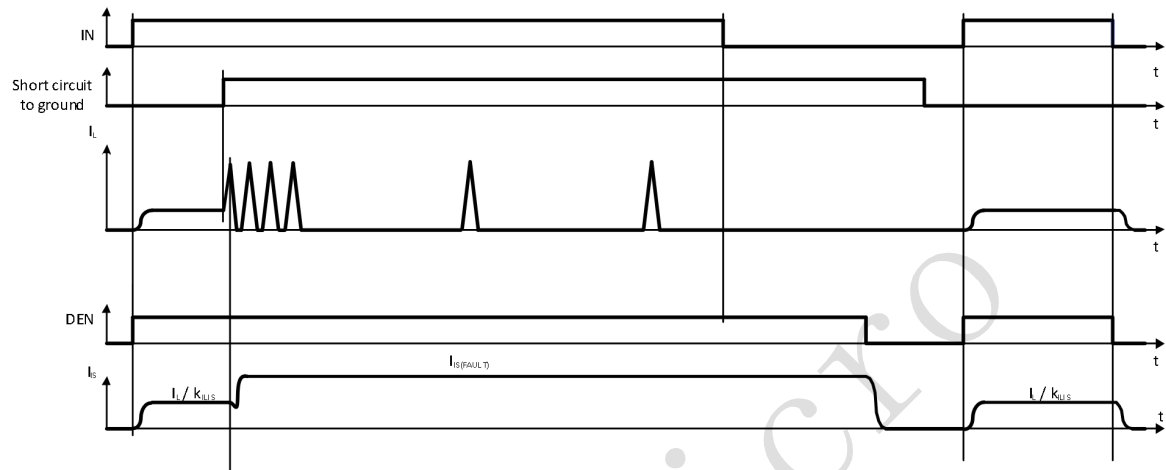


Figure 7:Retry Strategy Timing Diagram



11. Truth Table

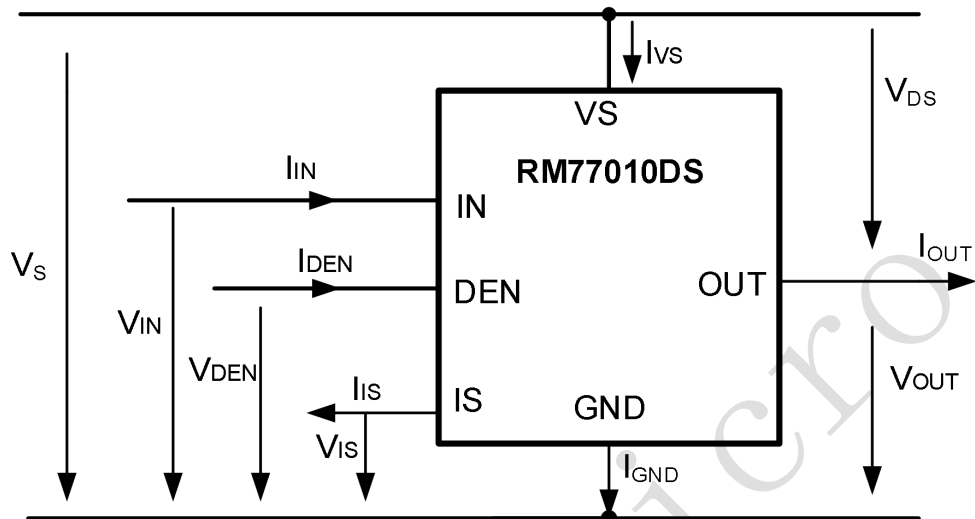
Operation Mode	Input level Channel	DEN	Output Level	Diagnostic Output
Normal operation	L H	H	L $\sim V_S$	L $I_{IS}=I_L/K_{iis}$
Short circuit to GND	L H	H	$\sim GND$ $\sim GND$	L $I_{IS}(FAULT)$
Overtemperature	L H	H	L L	L $I_{IS}(FAULT)$
Short circuit to VS	L H	H	V_S V_S	$I_{IS}(FAULT)$ $I_{IS}<I_L/K_{iis}$
Open Load	L L H	H	$<V_{OL(OFF)}$ $>V_{OL(OFF)}^{1)}$ $\sim V_S^{2)}$	L $I_{IS}(FAULT)$ $I_{IS}<I_{IS(OL)}$
Inverse current	L H	H	$\sim V_{INV}$ $\sim V_{INV}$	$I_{IS}(FAULT)$ $I_{IS}<I_{IS(OL)}^{3)}$
Current limitation	H	H	$<V_S$	$I_{IS}(FAULT)$
Underload	H	H	$\sim V_S^{4)}$	$I_{IS(OL)}<I_{IS}<I_L/K_{iis}$

L = "Low" Level, H = "High" Level

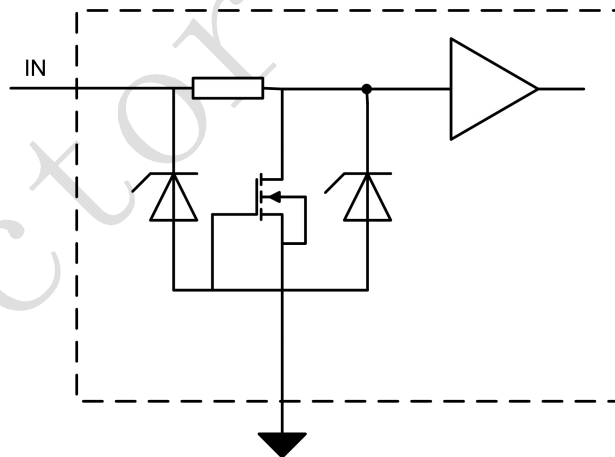
- 1) Stable with additional pull-up resistor.
- 2) The output current has to be smaller than $I_{L(OL)}$.
- 3) After maximum t_{INV} .
- 4) The output current has to be higher than $I_{L(OL)}$

12.Functions

12.1 Terms



12.2 Input circuit (ESD protection)

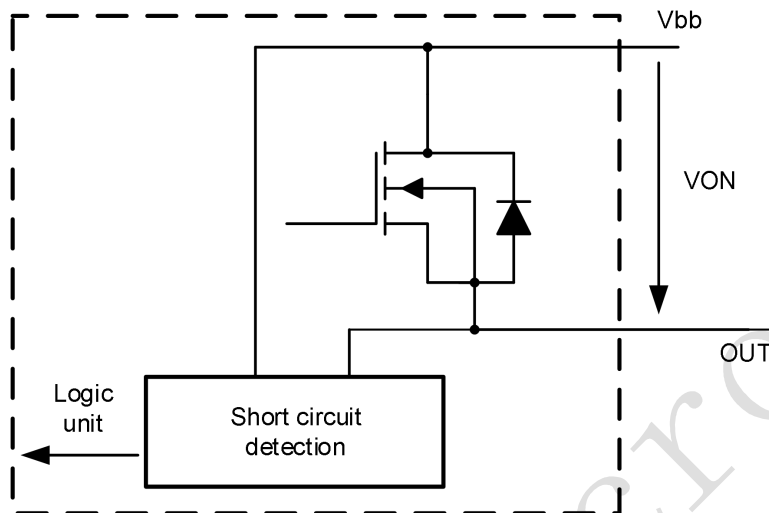


The input circuitry is compatible with 3.3 and 5 V microcontrollers. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing.

In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via an 4.7 kΩ input resistor.

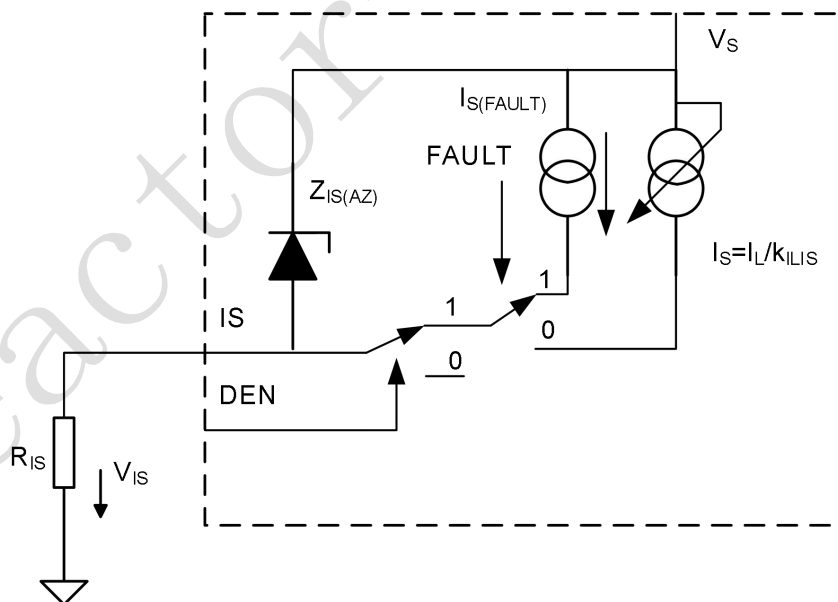
The DEN pins enable and disable the diagnostic functionality of the device. This pin has the same structure as the input pin.

12.3 Short circuit detection



Fault Condition: $V_{ON} > V_{ON(SC)}$ (6 V typ.).

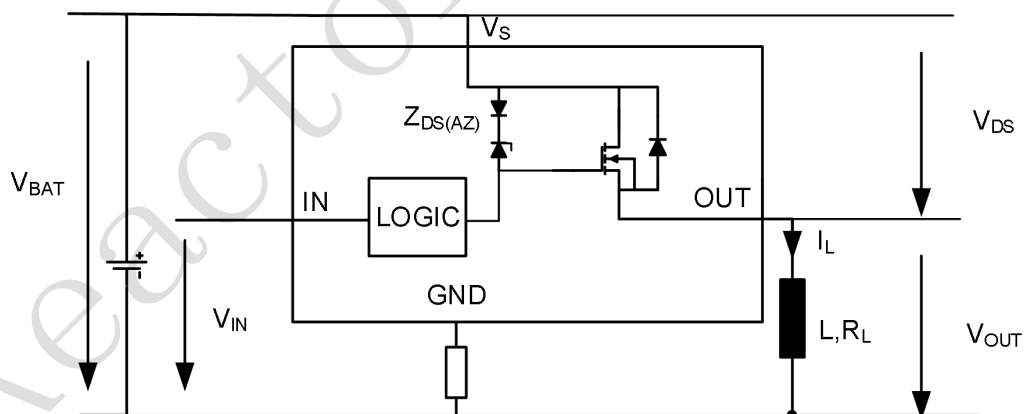
12.4 Current sense status output



As long as no “hard” failure mode occurs a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_S$) is provided; The accuracy of the sense current depends on temperature and load current.

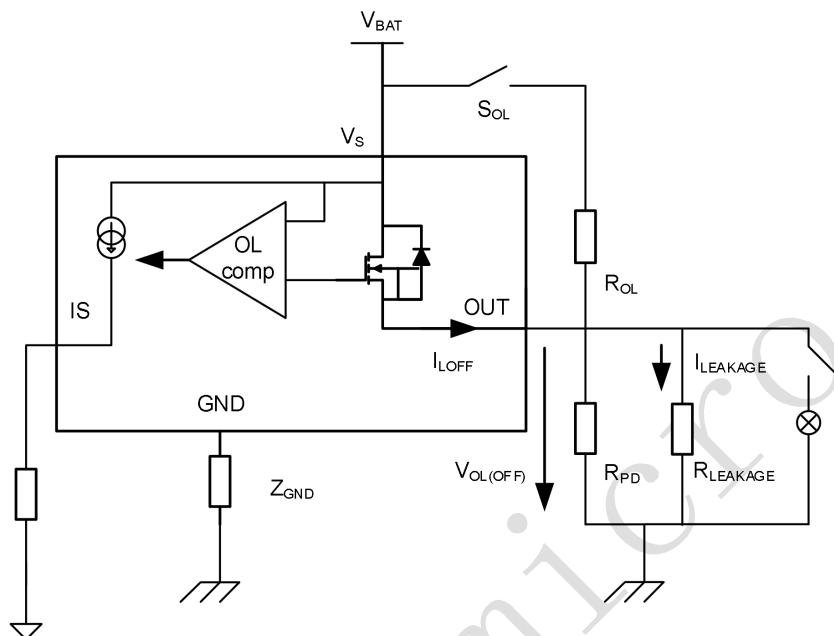
The diagram illustrates a precision current source circuit. It features a feedback loop where the output current I_S is sensed by R_{SENSE} and compared with a reference $V_{Z,VIS}$ through a diode $Z_{IS}(AZ)$. The error signal is processed by a 'Logic' block, which drives a MOSFET. The MOSFET's source is connected to ground through a diode stack $Z_{DS}(AZ)$ and $Z_D(AZ)$. The MOSFET's gate is connected to its drain through a diode $Z_{DS}(AZ)$. The output current I_S flows through R_{IN} and R_{DEN} to the MOSFET's gate. The output voltage V_{OUT} is taken across a load L, R_L connected to V_{BAT} . The circuit is enclosed in a dashed box representing the IC, with pins for R_{SENSE} , R_{IN} , R_{DEN} , V_S , $V_{Z,VIS}$, V_{BAT} , OUT , and GND .

12.6 Output Clamping



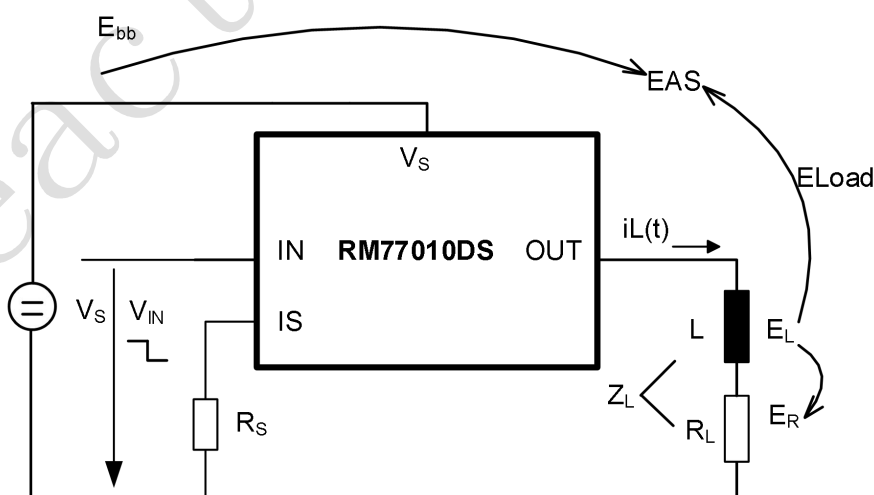
The maximum allowed load inductance is limited.

12.7 Open Load Detection in OFF Electrical Equivalent Circuit



For open load diagnosis in OFF-state, an external output pull-up resistor (R_{OL}) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account.

12.8 Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E = \frac{1}{2} * L * I^2$$

While demagnetizing load inductance, the energy dissipated in RM77010DS is:

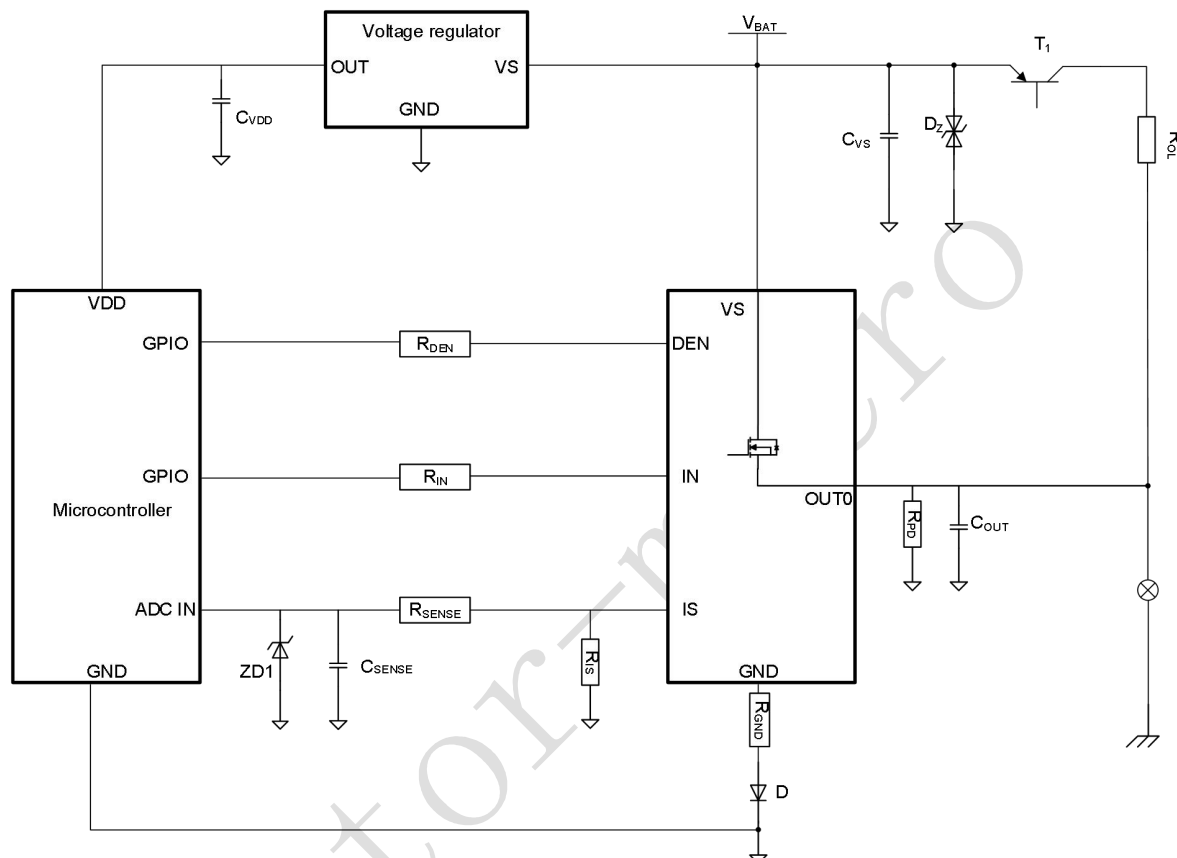
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} * i_L(t) dt$$

with an approximate solution for $R_L > 0 \Omega$:

$$E_{AS} = \frac{I_L * L}{2 * R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left(1 + \frac{I_L * R_L}{|V_{OUT(CL)}|} \right)$$

13.Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.



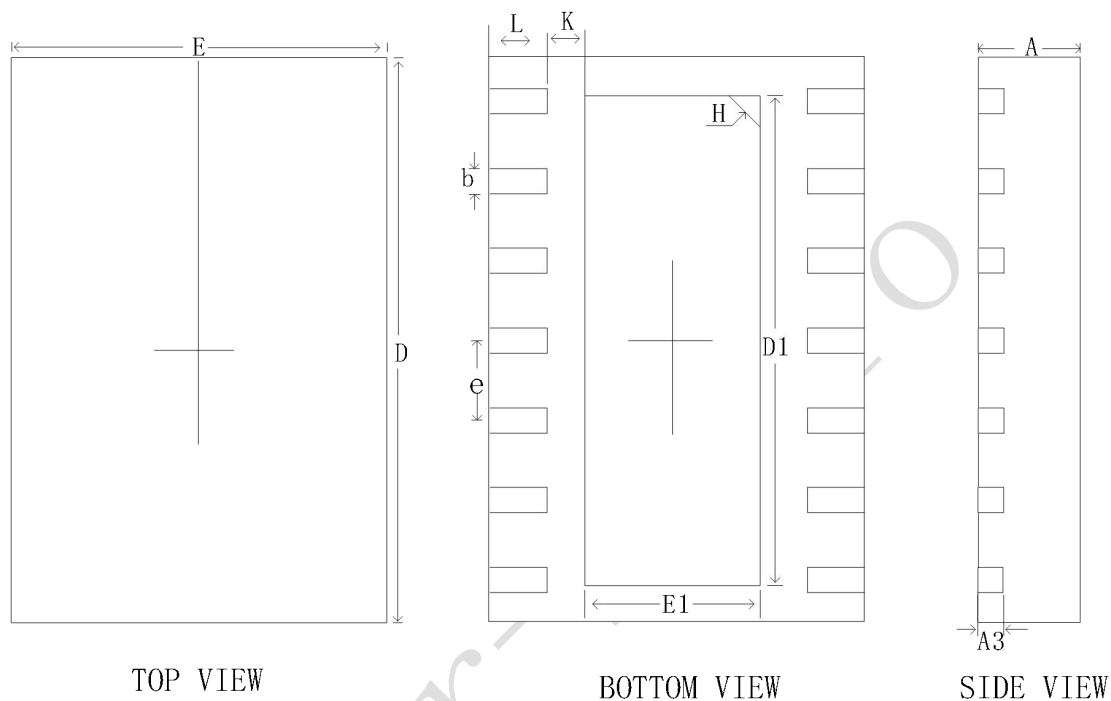
Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Bill of Material

Reference	Value	Reference	Value
R _{IN}	10KΩ	T ₁	Dual NPN/PNP
R _{DEN}	10KΩ	C _{OUT}	10nF
R _{SENSE}	10KΩ	D _Z	58V Zener diode
R _{IS}	1.2KΩ	C _{VS}	100nF
R _{GND}	330Ω	ZD1	6.2V Zener diode
R _{PD}	47KΩ	C _{SENSE}	10nF
R _{OL}	1.5KΩ	D	BAS21

14.Package

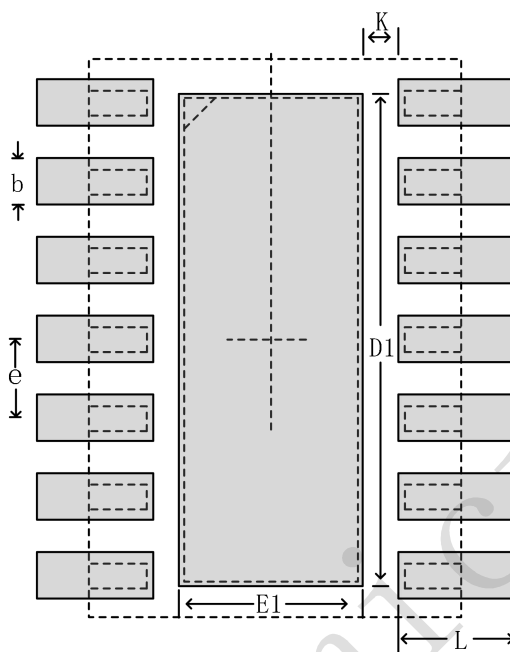
DFN9*6-14L



Unit :mm

Symbol	MIN	NOM	MAX
E	5.80	6.00	6.20
D	8.80	9.00	9.20
E1	2.75	2.80	2.85
D1	7.75	7.80	7.85
K	0.55	0.6	0.65
b	0.35	0.40	0.45
e	-	1.27	-
A	0.90	1.00	1.12
A3	-	0.25	-
L	0.90	1.00	1.10

15.Recommended Soldering Footprint



Unit : mm

Symbol	NOM	Symbol	NOM
E1	2.9	b	0.5
D1	8.0	e	1.27
K	0.5	L	1.3

16.Revision History

Version*	Change Description	Date
REV.A	Initial Version	2024/08/15
REV.B	1) Revised certain parameter in the Electrical Characteristics table.(such as current sense ratio, etc.) 2) Revised Application Information. 3) Revised package dimension tolerances. 4) Added Retry Strategy Timing Diagram	2025/02/17
NOTE*:Datasheets with alphabetic version numbers (e.g., REV.A, REV.B, REV.C) are designated for the sample phase,whereas those with numeric version numbers (e.g., V1.0, V1.1, V1.2) are intended for the mass production phase.		