

MDDG10R08D

100V N-Channel Enhancement Mode MOSFET

1. Description

This N-Channel MV MOSFET is produced using MDD Semiconductor's advanced Power Trench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

2. Features

- Max $R_{DS(on)}$ = 8 m Ω at V_{GS} = 10 V, I_D = 35 A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIS Tested
- RoHS Compliant

3. Application

- Synchronous Rectification for AC / DC Quick Charger
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter
- Battery management System

4. Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

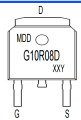
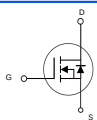
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	75	A
Pulsed Drain Current (Note 2)	I_{DM}	300	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	85.5	mJ
Thermal Resistance, steady-state	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Power Dissipation	P_D	100	W
Junction Temperature	T_J	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

Note: 1) Calculated continuous current based on maximum allowable junction temperature.

2) Repetitive rating, pulse width limited by max. junction temperature.

3) E_{AS} condition : $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=18.5\text{A}$

5. Pinning information

Pin	Symbol	Description	Simplified outline	Equivalent Circuit	Marking	Package
1	G	Gate			MDD G10R08D	TO-252
2	D	Drain				
3	S	Source				

6. $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Condition	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		$V_{GS}=0V, I_D=250\mu A$	100	—	—	V
I_{GSS}	Gate-Source Leakage Current	Forward	$V_{GS}=20V$	—	—	100	nA
		Reverse	$V_{GS}=-20V$	—	—	-100	nA
I_{DSS}	Drain-Source Leakage Current		$V_{DS}=100V, V_{GS}=0V$	—	—	1	μA
$V_{GS(TH)}$	Gate Threshold Voltage		$V_{DS}=V_{GS}, I_D=250\mu A$	1.5	2.0	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance		$V_{GS}=10V, I_D=35A$	—	6.5	8	m Ω
			$V_{GS}=4.5V, I_D=30A$	—	8.0	11	m Ω

7. Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	$V_{GS}=0V$	—	2000	—	pF
C_{oss}	Output Capacitance	$V_{DS}=50V$	—	890	—	pF
C_{rss}	Reverse Transfer Capacitance	$f=1MHz$	—	65	—	pF
Q_g	Total Gate Charge	$V_{GS}=10V$	—	41	—	nC
Q_{gs}	Gate Source Charge	$V_{DS}=50V$	—	10.3	—	nC
Q_{gd}	Gate Drain Charge	$I_D=30A$	—	7.5	—	nC

8. Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d(on)}$	Turn on Delay Time	$V_{GS}=10V$ $V_{DD}=50V$ $I_D=30A$ $R_G=2.7\Omega$	—	11	—	ns
t_r	Turn on Rise Time		—	36	—	ns
$t_{d(off)}$	Turn Off Delay Time		—	33	—	ns
t_f	Turn Off Fall Time		—	10	—	ns

9. Source Drain Diode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SD}	Drain-Source Diode Forward Voltage	$I_S=30A, V_{GS}=0V$	—	0.85	—	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=30A$	—	50	—	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$di/dt=100A/\mu s$	—	71	—	nC

10. Test Circuits And Waveforms

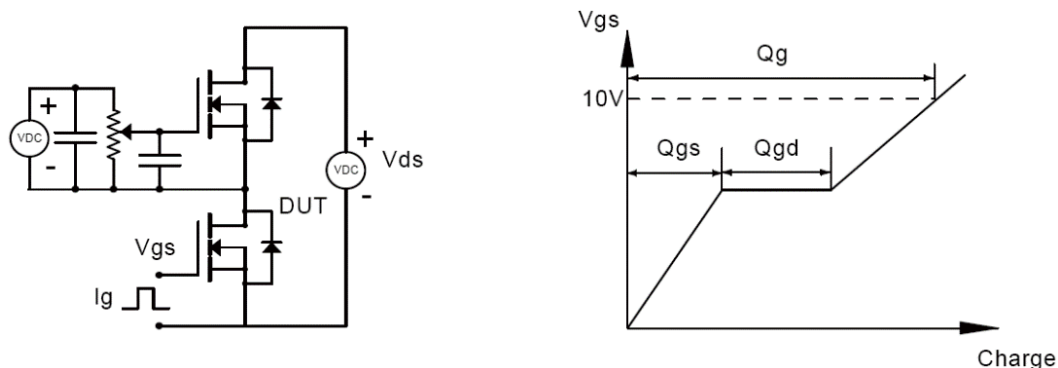


Figure 1. Gate charge test circuit & waveform

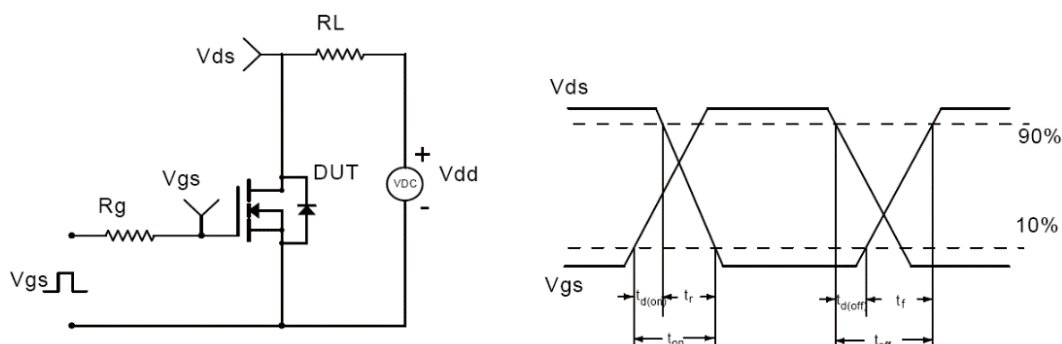


Figure 2. Switching time test circuit & waveforms

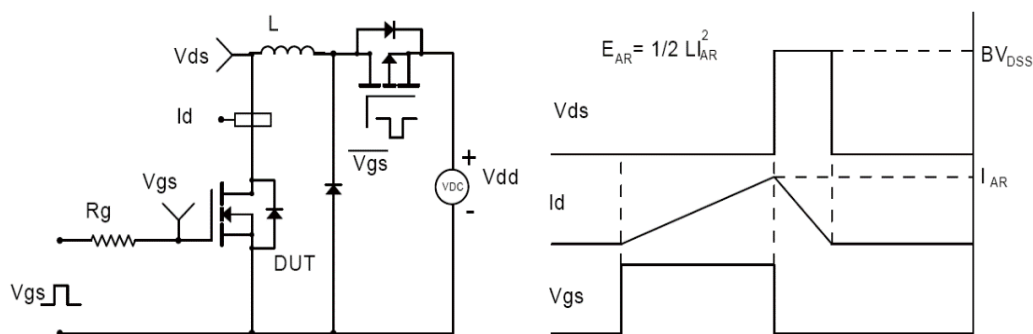


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

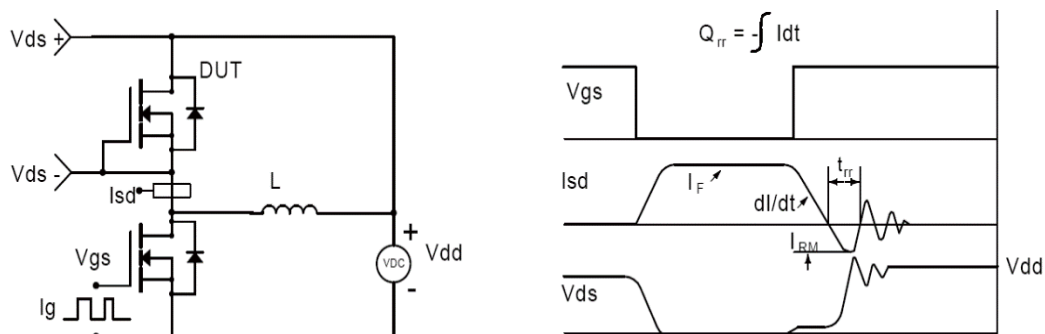


Figure 4. Diode reverse recovery test circuit & waveforms

II. Electrical Characteristics Diagrams

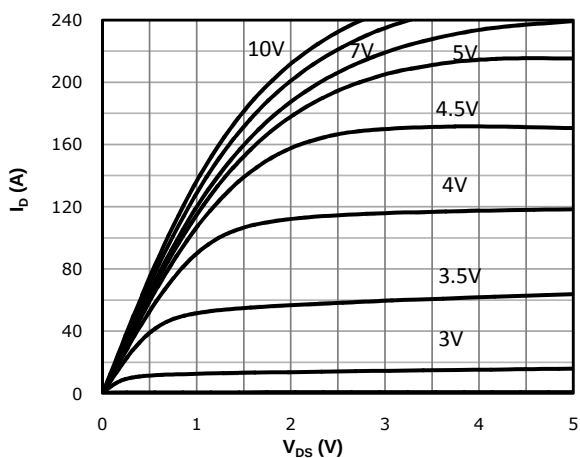


Figure 1. Typ. output characteristics

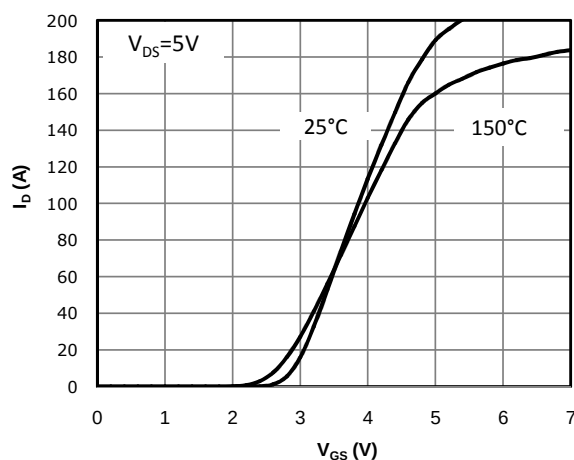


Figure 2. Typ. transfer characteristics

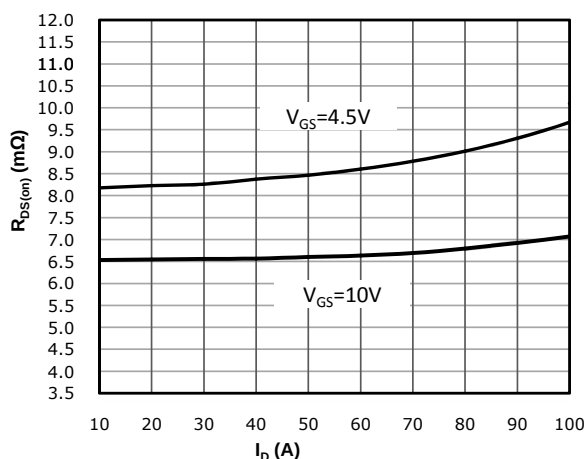


Figure 3. On-Resistance vs. Drain Current

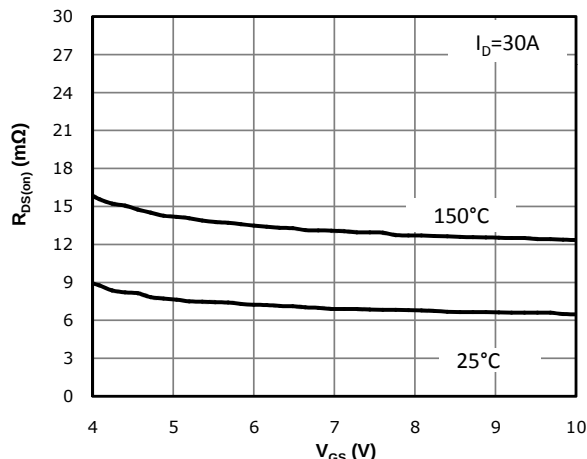


Figure 4. On-Resistance vs. Gate Voltage

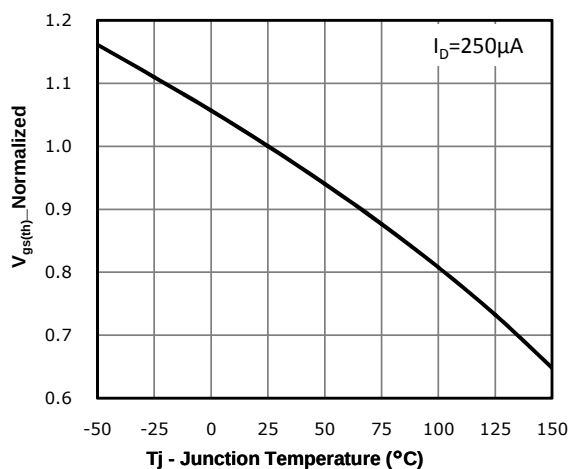


Figure 5. Normalized Threshold Voltage vs. Junction Temperature

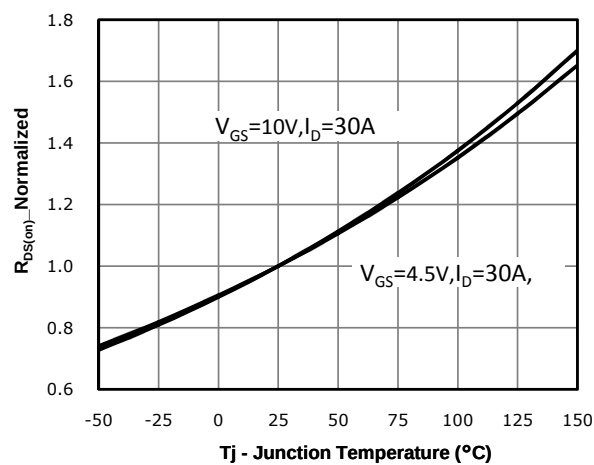
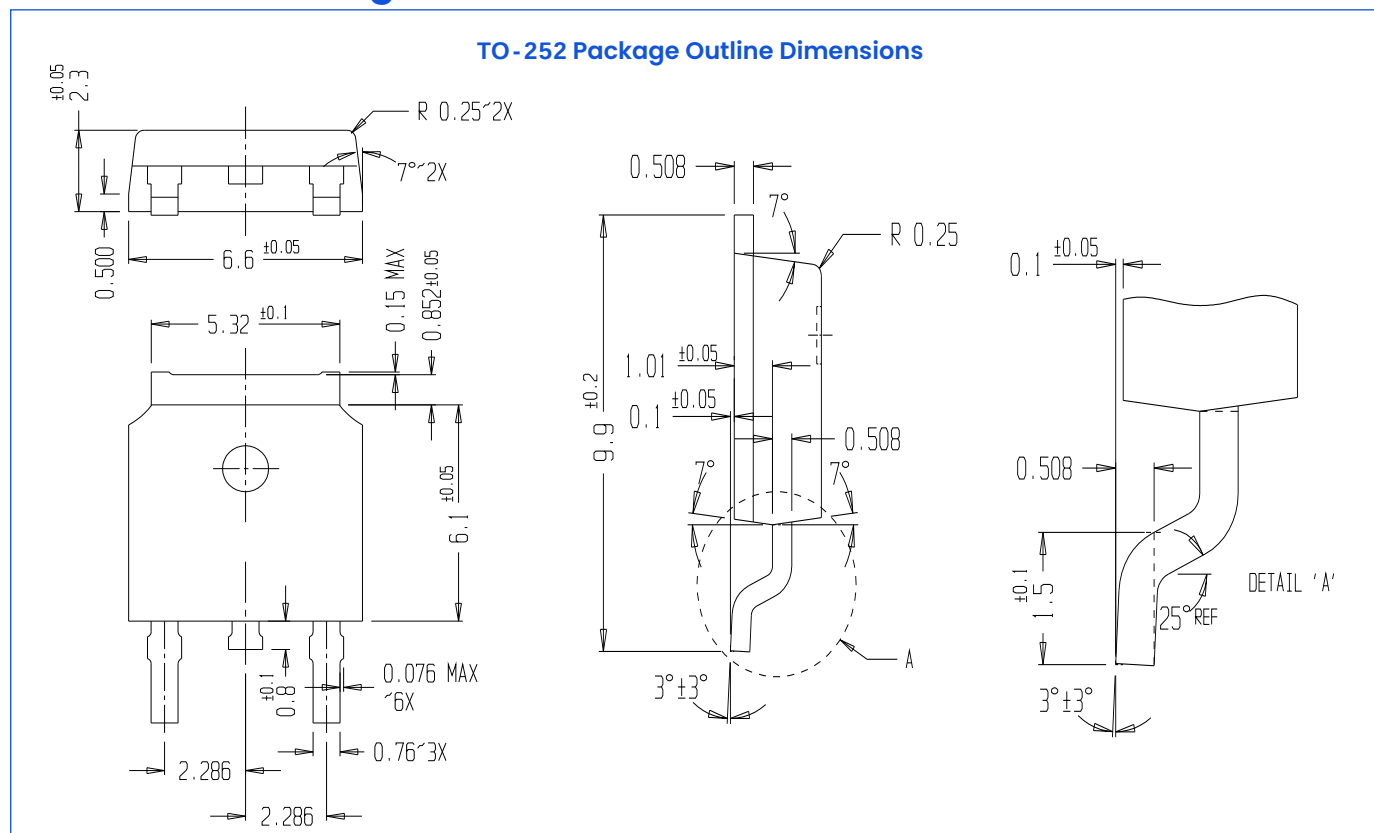


Figure 6. On-Resistance vs. Junction Temperature

12. Outline Drawing



13. Important Notice and Disclaimer

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