NCT6122D / NCT6126D

Nuvoton Super I/O

Date: September 12, 2023 Revision 2.4

Table of Contents –

LIST OF FIGURE

LIST OF TABLE

1. GENERAL DESCRIPTION

The NCT6122D / NCT6126D is a member of Nuvoton's Super I/O product line. The NCT6122D / NCT6126D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6122D / NCT6126D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6122D / NCT6126D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6122D / NCT6126D supports 6 high-speed serial communication port (UART). Each UART includes a 128-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6122D / NCT6126D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6122D / NCT6126D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6122D / NCT6126D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6122D / NCT6126D supports the Intel® PECI (Platform Environment Control Interface), AMD® SB-TSI interface, and Intel® Deep Sleep Well glue logic which helps customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6122D / NCT6126D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. With Nuvoton Port80 Analyzer AP or debug card, it will be easier and more convenient. It also supports two-color LED control to indicate system power states, Consumer IR function for remote control purpose, and also Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6122D / NCT6126D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Spec. 1.1
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Oscillator free (No external 24MHz or 48MHz clock input needed)
Support selective pins of 5 V tolerance
eSPI Interface

UART

NCT6122D - 2 high-speed, 16550-compatible UART with 128-byte send / receive FIFO
Support RS485
NCT6126D - 6 high-speed, 16550-compatible UART with 128-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset

12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system
Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
Support Current Mode (dual current source) temperature sensing method
Ten voltage inputs (CPUVCORE, VTT, VIN[0..2], VHIF, 3VCC, AVSB, 3VSB and VBAT)
Three fan-speed monitoring inputs
Three fan-speed controls
Dual mode for fan control (PWM and DC) for SYSFANOUT, CPUFANOUT and AUXFANOUT
Built-in case open detection circuit
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager support
Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
Support Consumer IR, including CIRRX

General Purpose I/O Ports

GPIO0 ~ GPIOB programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

3.3 Volt

Package

128-pin LQFP
Green

3. BLOCK DIAGRAM

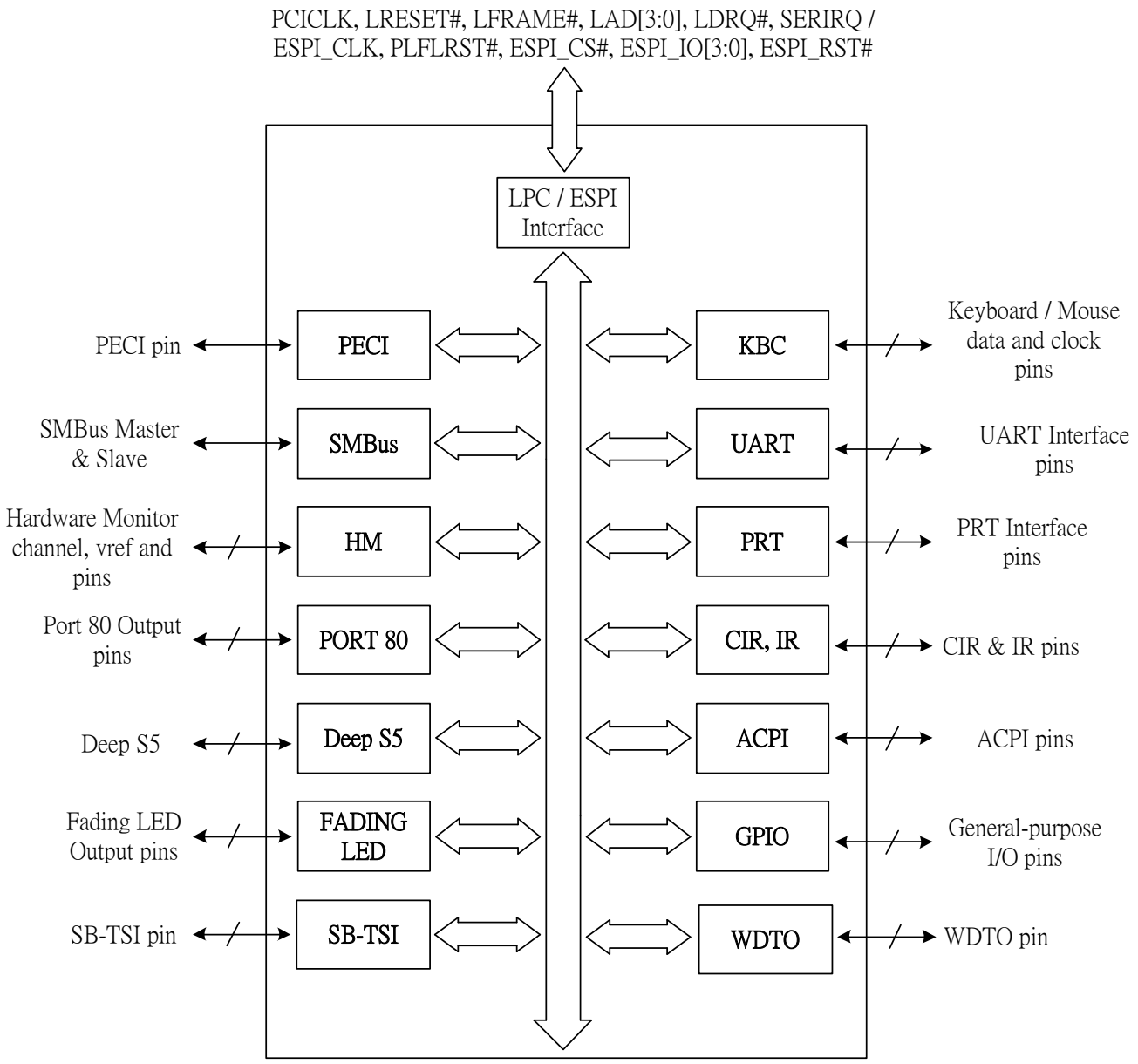


Figure 3-1 NCT6122D / NCT6126D Block Diagram

4. PIN LAYOUT

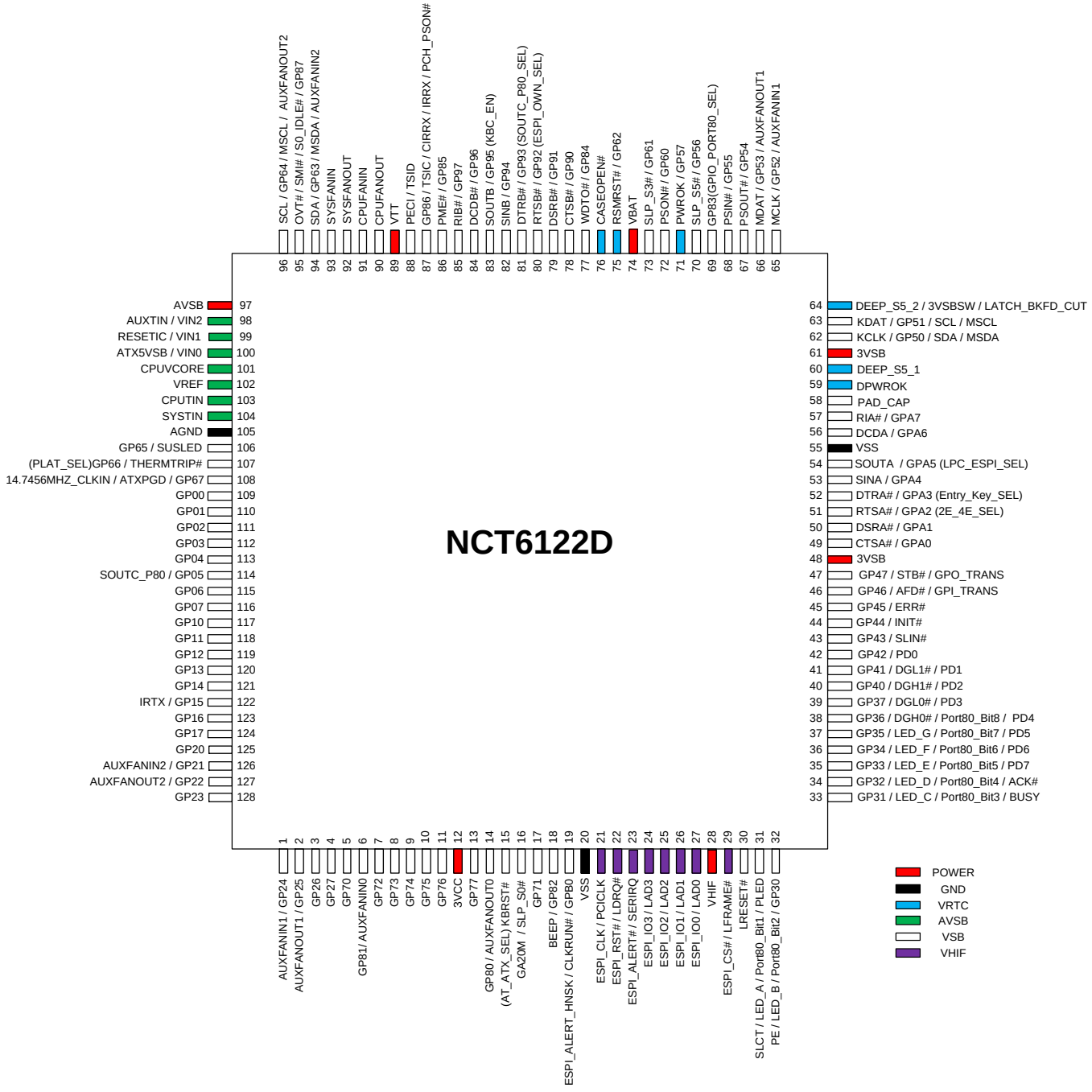


Figure 4-1 NCT6122D Pin Layout

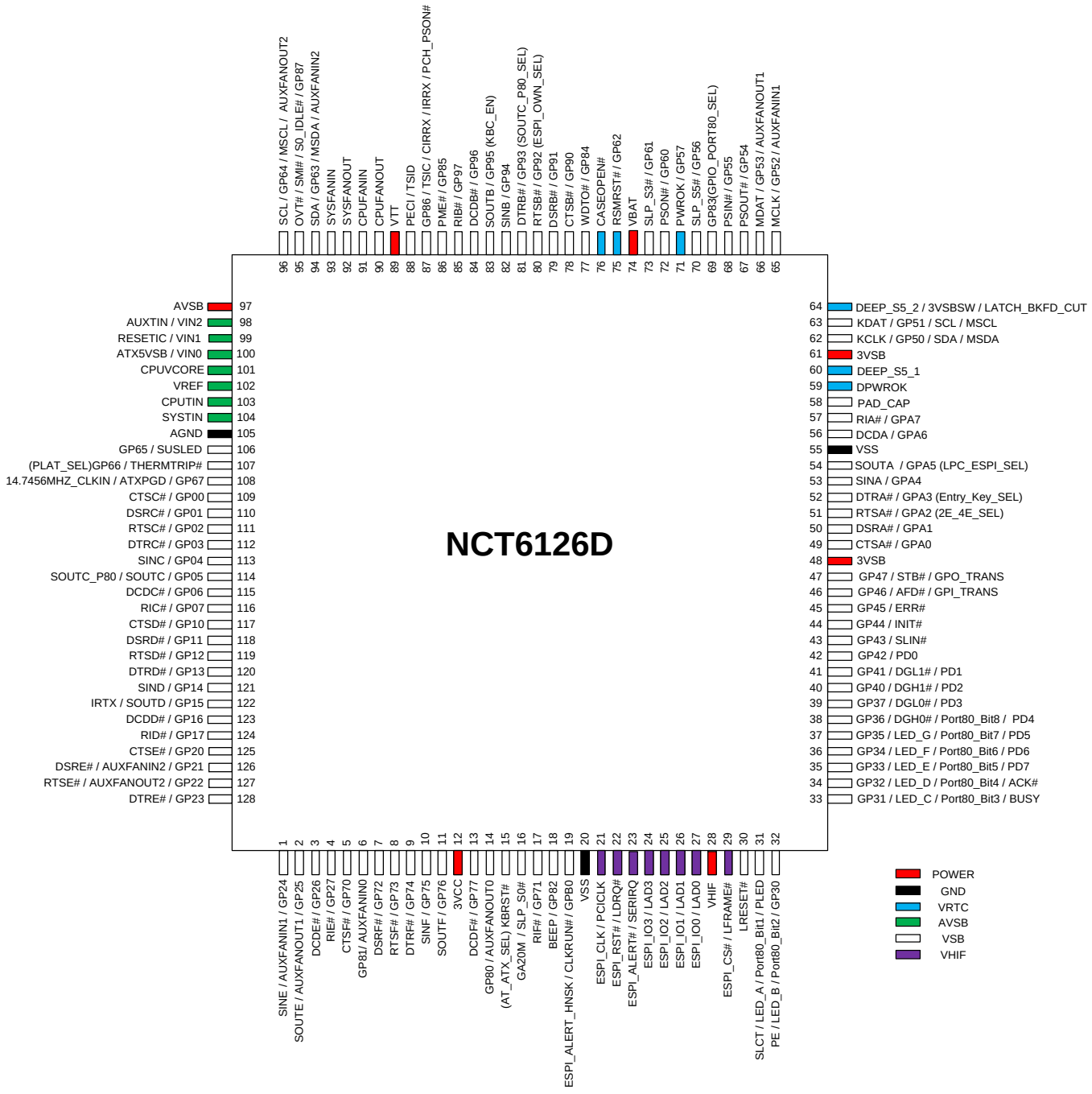


Figure 4-2 NCT6126D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 24.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp318} - 3.3V/1.8V TTL-level input pin
IN_{sp318} - 3.3V/1.8V TTL-level, Schmitt-trigger input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
IN_{tup5} - 5V TTL-level input pin with internal pull-up resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up
OX_8 - output pin with 8-mA source-sink capability and output voltage high level depend VHIF
ODX_8 - open-drain output pin with 8-mA sink capability and output voltage high level depend VHIF

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	CLKRUN#	I/O	IN_{tp318} OD_8	VSB	Clock RUN signal.
21	PCICLK	I	IN_{tp318}	VHIF	PCI-clock input. 19.2MHz-33MHz support.
22	LDRQ#	O	OX_8	VHIF	Encoded DMA Request signal.
23	SERIRQ	I/O	IN_{tp318} OX_8 ODX_8	VHIF	Serialized IRQ input / output.
24-27	LAD[3:0]	I/O	IN_{tp318} ODX_8	VHIF	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
29	LFRAME#	I	IN_{tp318}	VHIF	Indicates the start of a new cycle or the termination of a broken cycle.
30	LRESET#	I	IN_{sp318}	VSB	Reset signal. It can be connected to the PLTRST# signal on the host.

5.2 eSPI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	ESPI_ALERT_ HNSK	I/O	IN_{tp318} OD_{12}	VSB	Alert handshake signal. Pulling down a 4.7KΩ resistor to GND is recommended.
21	ESPI_CLK	I	IN_{tp318}	VHIF	The eSPI_CLK provides the reference timing for all the serial input and output operations.
22	ESPI_RST#	I	IN_{tp318}	VHIF	Reset the eSPI interface for both master and slaves.
23	ESPI_ALERT#	I/O	OX_8 ODX_8	VHIF	A dedicated Alert# pin is used to signal the Alert event.
24-27	ESPI_IO[3:0]	I/O	IN_{tp318} ODX_8	VHIF	These are bi-directional input/output pins used to transfer data between master and slaves.
29	ESPI_CS#	I	IN_{sp318}	VHIF	Driving Chip Select# low selects a particular eSPI slave for the transaction.

5.3 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
32	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
33	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
34	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
45	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
43	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
44	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
46	AFD#	O	O_{12}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
42	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
41	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
39	PD3	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
38	PD4	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
37	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
36	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
35	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.4 Serial Port Interface (NCT6122D: UART A ~ UART B; NCT6126D: UART A ~ UART F)

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
57	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
56	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
54	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
53	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
52	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
51	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
50	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
49	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
85	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
84	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
83	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
82	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
81	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
80	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
79	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
78	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
116	RIC#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
115	DCDC#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
114	SOUTC	O	O_{12}	VSB	UART C Serial Output. This pin is used to transmit serial data out to the communication link.
114	SOUTC_P80	O	O_{12}	VSB	PORT80 to UART Serial Output. This pin is used to transmit serial data out to the communication link.
113	SINC	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
112	DTRC#	O	O_{12}	VSB	UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
111	RTSC#	O	O_{12}	VSB	UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
110	DSRC#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
109	CTSC#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
124	RID#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
123	DCDD#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
122	SOUTD	O	O_{12}	VSB	UART D Serial Output. This pin is used to transmit serial data out to the communication link.
121	SIND	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
120	DTRD#	O	O_{12}	VSB	UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
119	RTSD#	O	O_{12}	VSB	UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
118	DSRD#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
117	CTSD#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
4	RIE#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
3	DCDE#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
2	SOUTE	O	O_{12}	VSB	UART E Serial Output. This pin is used to transmit serial data out to the communication link.
1	SINE	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
128	DTRE#	O	O_{12}	VSB	UART E Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
127	RTSE#	O	O_{12}	VSB	UART E Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
126	DSRE#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
125	CTSE#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
17	RIF#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
13	DCDF#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
11	SOUTF	O	O_{24}	VSB	UART F Serial Output. This pin is used to transmit serial data out to the communication link.
10	SINF	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
9	DTRF#	O	O_{24}	VSB	UART F Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
8	RTSF#	O	O_{24}	VSB	UART F Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
7	DSRF#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
5	CTSF#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
108	14.7456MHZ _CLKIN	I	IN_{tp5}	VSB	UART-clock 14.7456-MHz input

5.5 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
16	GA20M	O	O_{12}	VSB	Gate A20 output. This pin is high after system reset. (KBC P21)
15	KBRST#	O	O_{12}	VSB	Keyboard reset. This pin is high after system reset. (KBC P20) *Note1
62	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock.
63	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data.
65	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock.
66	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data.

Note1 : Refer to APN for KBRST# external circuit implementation.

5.6 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length.

5.7 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
76	CASEOPEN#	I	IN_{tp5}	VRTC	CASE OPEN detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling down a 2-MΩ resistor to GND is recommended if not in use.
107	THERMTRIP#	I	IN_{tp5}	VRTC	Thermal Trip detection. Active low signal indicating the CPU is too hot. Used to turn off to the main power supply
98	VIN2 / AUXTIN	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
99	VIN1	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
99	RESETIC	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
100	VIN0	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
100	ATX5VSB	I	AIN	AVSB	Analog input for voltage measurement (Range: 1.2 to 1.3 V)
101	CPUVCORE	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
102	VREF	O	AOUT	AVSB	Reference Voltage (around 2.048 V).
103	CPUTIN	I	AIN	AVSB	The input of temperature sensor 2. It is used for CPU temperature sensing.
104	SYSTIN	I	AIN	AVSB	The input of temperature sensor 1. It is used for system temperature sensing.
95	OVT#	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
95	SMI#	O	OD_{12}	VSB	System Management Interrupt channel output.
6	AUXFANIN0	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
14	AUXFANOUT0	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
1	AUXFANIN1	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	AUXFANOUT1	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
65	AUXFANIN1	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
66	AUXFANOUT1	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
91	CPUFANIN	I	IN_{tsp5} O_{12}	VSB	0 to +5 V amplitude fan tachometer input. This pin will keep level low when VCC off.
90	CPUFANOUT	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
93	SYSFANIN	I	IN_{tsp5} O_{12}	VSB	0 to +5 V amplitude fan tachometer input. This pin will keep level low when VCC off.
92	SYSFANOUT	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
94	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
96	AUXFANOUT2	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
126	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
127	AUXFANOUT2	O	AOUT O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
18	BEEP	O	OD_{12}	VSB	Beep function for hardware monitor.

5.8 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
88	PECI	I/O	I/O_{V3}	VTT	INTEL® CPU PECI interface. Connect to CPU.
89	VTT	I	Power	VTT	INTEL® CPU Vtt Power.

5.9 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
68	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
67	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
75	RSMRST#	O	OD_{12}	VRTC	Resume reset signal output.
73	SLP_S3#	I	IN_{tp5}	VSB	SLP_S3# input.
70	SLP_S5#	I	IN_{tp5}	VSB	SLP_S5# input.
108	ATXPGD	I	IN_{tp5}	VSB	ATX power good signal.
72	PSON#	O	OD_{12}	VSB	Power supply on-off output.
71	PWROK	O	O_{12} OD_{12}	VRTC	3VCC PWROK signal.
64	3VSBSW	O	OD_{24}	VRTC	Switch 3VSB power to memory when in S3 state.
59	DPWROK	O	OD_{12}	VRTC	V3A signal output

5.10 Advanced Sleep State Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
60	DEEP_S5_1	O	OD_{24}	VRTC	This pin is to control system power for entering “more power saving mode”.
64	DEEP_S5_2	O	OD_{24}	VRTC	This pin is to control system power for entering “more power saving mode”.

5.11 S0ix Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
16	SLP_S0#	I	IN_{tp5}	VSB	Modern Standby input signal.
87	PCH_PSON#	I	IN_{tp5}	VSB	Modern Standby input signal.
95	S0_IDLE#	O	O_{12}	VSB	Modern Standby output signal. Indicate S0ix duration.

5.12 Port 80 Message and 7 segment Display

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	PORT80_Bit1	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
32	PORT80_Bit2	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
33	PORT80_ Bit3	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
34	PORT80_ Bit4	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
35	PORT80_ Bit5	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
36	PORT80_ Bit6	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
37	PORT80_ Bit7	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
38	PORT80_ Bit8	O	O_{12}	VSB	Anode outputs for Binary LED. Common cathode output of display on decoded Port80 message.
38	DGH0#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port80 message. Switching frequency is about 250Hz.
39	DGL0#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port80 message. Switching frequency is about 250KHz.
40	DGH1#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port81 message. Switching frequency is about 250Hz.
41	DGL1#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port81 message. Switching frequency is about 250Hz.
31 32 33 34 35 36 37	LED_A LED_B LED_C LED_D LED_E LED_F LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.

5.13 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
63	SCL/MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus clock.
62	SDA/MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus bi-directional Data.
94	SDA/MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus bi-directional Data.
96	SCL/MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus clock.

5.14 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
48, 61	3VSB	I		3VSB	+3.3 V stand-by power supply for the digital circuits.
74	VBAT	I		VBAT	+3 V on-board battery for the digital circuits.
12	3VCC	I		3VCC	+3.3 V power supply for driving 3 V on host interface.
28	VHIF	I		VHIF	3.3V or 1.8V standby power supply for driving on host interface. It will be monitor by the RSMRST# signal.
97	AVSB	I		AVSB	Analog +3.3 V power input. Internally supply power to all analog circuits.
105	CPUD- / AGND	I		CPUD- / AGND	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
20, 55	VSS	I		VSS	Ground.
89	VTT	I		VTT	INTEL® CPU Vtt power.
58	PAD_CAP	O			External Filter Capacitor 1uF (for internal VSB 1.8V)

5.15 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	TSIC	O	OD_{12}	VTT	AMD SB-TSI clock output.
88	TSID	I/O	IN_{tsp3} OD_{12}	VTT	AMD SB-TSI data input / output.

5.16 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
64	LATCH_BKFD_CUT	O	O_{24}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.17 WatchDog

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	WDTO#	O	OD_{12}	VSB	Watchdog Timer output signal.

5.18 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	IRRX	I	IN_{tsp5}	VSB	IR Receiver input.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
122	IRTX	O	O_{12}	VSB	IR Transmitter output.

5.19 LED

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
106	SUSLED	O	O_{12}	VSB	Suspend Led signal. This pin can be reflects sleep s5 state through fading led register setting.
31	PLED	O	OD_{12}	VSB	Power Led signal. This pin can be reflects PWROK state through fading led register setting.

5.20 General Purpose I/O Port

5.20.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
109	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 0.
110	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 1.
111	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 2.
112	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 3.
113	GP04	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 4.
114	GP05	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 5.
115	GP06	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
116	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 7.

5.20.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
117	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
118	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
119	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
120	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
121	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
122	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
123	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
124	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.20.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
125	GP20	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
126	GP21	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 1.
127	GP22	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
128	GP23	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
1	GP24	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 4.
2	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.
3	GP26	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 6.
4	GP27	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.20.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
32	GP30	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.
33	GP31	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
34	GP32	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 2.
35	GP33	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 3.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	GP34	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.
37	GP35	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 5.
38	GP36	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 6.
39	GP37	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 7.

5.20.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
40	GP40	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
41	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
42	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
43	GP43	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 3.
44	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
45	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.
46	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
47	GP47	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.20.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	GP50	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 0.
63	GP51	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
65	GP52	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 2.
66	GP53	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 3.
67	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
68	GP55	I/O	IN_{tp5} O_{8} OD_{8}	VSB	General-purpose I/O port 5 bit 5.
70	GP56	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.
71	GP57	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.20.7 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
72	GP60	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
73	GP61	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.
75	GP62	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.
94	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
96	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
106	GP65	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.
107	GP66	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
108	GP67	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 7.

5.20.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
5	GP70	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 0.
17	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
7	GP72	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 2.
8	GP73	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 3.
9	GP74	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 4.
10	GP75	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 5.
11	GP76	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 6.
13	GP77	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 7.

5.20.9 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP80	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 0.
6	GP81	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 1.
18	GP82	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 2.
69	GP83	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 3.
77	GP84	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 4.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
86	GP85	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 5.
87	GP86	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 6.
95	GP87	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 7.

5.20.10 GPIO-9 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
78	GP90	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 0.
79	GP91	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 1.
80	GP92	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 2.
81	GP93	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 3.
82	GP94	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 4.
83	GP95	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 5.
84	GP96	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 6.
85	GP97	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 7.

5.20.11 GPIO-A Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
49	GPA0	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 0.
50	GPA1	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 1.
51	GPA2	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 2.
52	GPA3	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 3.
53	GPA4	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 4.
54	GPA5	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 5.
56	GPA6	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 6.
57	GPA7	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 7.

5.20.12 GPIO-B Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
19	GPB0	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port B bit 0.

5.20.13 GPIO Transition

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46	GPI_TRANS	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O Transition input.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
47	GPO_TRANS	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O Transition output.

5.21 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
51	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O addresses selection. (Strapped by VSB power [internal RSMRST# signal]) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
52	Entry_Key_SEL	I	IN_{tdp5}	VSB	SIO entry key selection (Strapped by VSB power [internal RSMRST# signal]) Strapped to high: The Entry Key is 88. Strapped to low: The Entry Key is 87.
69	GPIO_PORT80_SEL	I	IN_{tdp5}	VSB	Port80 function selection. (Strapped by VCC power) Strapped to high: Port80 function. Strapped to low: non-Port80 function.
15	AT_ATX_SEL	I	IN_{tdp5}	VSB	Enable AT_ATX power sequence selection. (Strapped by VSB power [internal RSMRST# signal]) Active high: ATX Active low: AT See configuration register.
54	LPC_ESPI_SEL	I	IN_{tdp5}	VSB	Host interface function selection. (Strapped by VSB) Active high: eSPI interface Active low: LPC interface See configuration register.
80	ESPI_OWN_SEL	I	IN_{tdp5}	VSB	ESPI owner setting. (Strapped by VSB power [internal RSMRST# signal]) Active high: ESPI owner. Active low: Not ESPI owner *. Pulling up a 1KΩ resistor to VSB is recommended.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
81	SOUTC_P80_SEL	I	IN_{tdp5}	VSB	SOUTC_P80 function selection. (Strapped by VSB power [internal RSMRST# signal]) Strapped to high: SOUTC_P80 function. Strapped to low: non-SOUTC_P80 function.
83	KBC_EN	I	IN_{tdp5}	VSB	Pin 62/63 65/66 PAD Function Selection. (Strapped by VSB power [internal RSMRST# signal]) Active high: KBC Function. Active low: Others
107	PLAT_SEL	I	IN_{tdp5}	VSB	Big core and Atom platform select (Strapped by VSB power [internal RSMRST# signal]) Active 3VSB: Atom platform Active 3VCC: Big core platform

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.

5.22 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					
2E_4E_SEL	51	VSB	Pull-down	47.4K	2
Entry_Key_SEL	52	VSB	Pull-down	47.4K	2
GPIO_PORT80_SEL	69	VSB	Pull-down	47.4K	1
LPC_ESPI_SEL	54	VSB	Pull-down	47.4K	2
ESPI_OWN_SEL	80	VSB	Pull-down	47.4K	2
SOUTC_P80_SEL	81	VSB	Pull-down	47.4K	2
KBC_EN	83	VSB	Pull-up	47.4K	2
PLAT_SEL	107	VSB	Pull-down	47.4K	2
Advanced Configuration & Power Interface					
PSIN#	68	VSB	Pull-up	47.03K	
AT_ATX_SEL	15	VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	70	SLP_S5# input.
PWROK	71	This pin generates the PWROK signals while 3VCC is present.
RSMRST#	75	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6122D / NCT6126D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

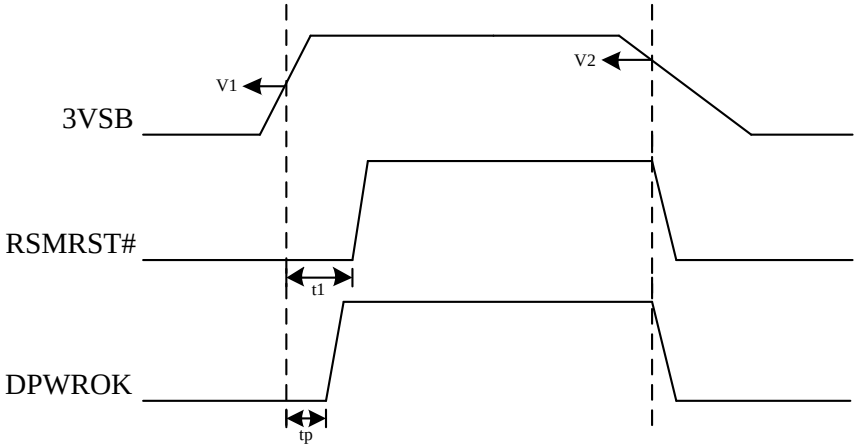


Figure 6-1 RSMRST# and DPWROK

The ATX5VSB is less than 1.2V, and the RSMRST# will be de-asserted. Please refer to the figure below.

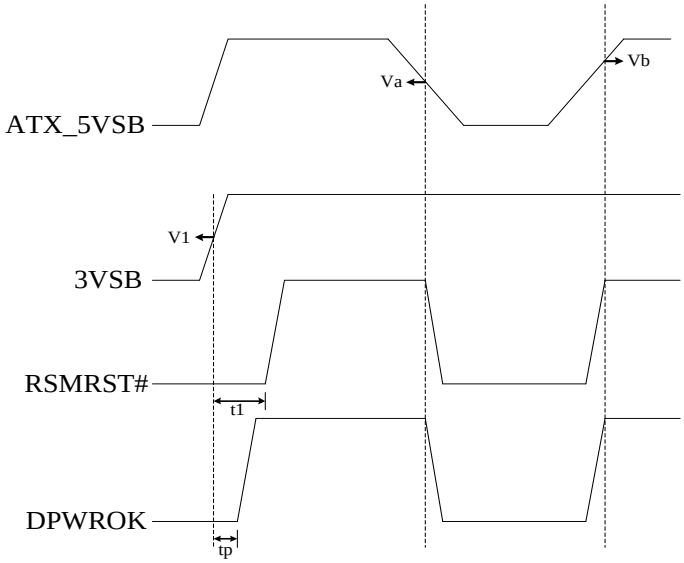


Figure 6-2 RSMRST# and DPWROK (Enable ATX5VSB detect)

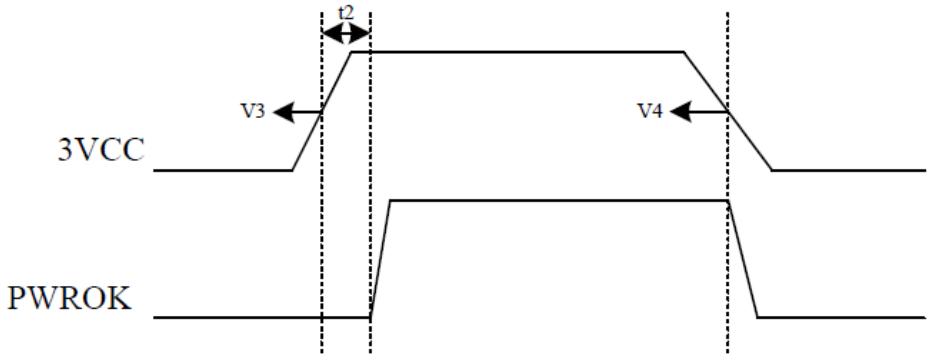


Figure 6-3 PWROK

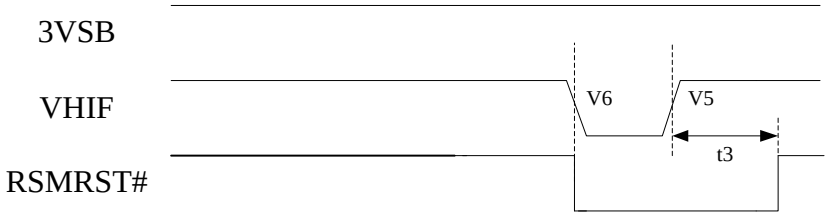


Figure 6-4 RSMRST# monitor 3VSB/VHIF

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tp	Valid 3VSB to DPWROK inactive	10	30	mS
t2	Valid 3VCC to PWROK active	300	500	mS

TIMING	PARAMETER	MIN	MAX	UNIT
t3	Valid VHIF to RSMRST#	36	40	ms

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage		3.1	Volt
V2	3VSB Ineffective Voltage	2.92		Volt
V3	3VCC Valid Voltage	-	2.75	Volt
V4	3VCC Ineffective Voltage	2.3	-	Volt
V5	VHIF Valid Voltage	-	1.3-1.4	Volt
V6	VHIF Ineffective Voltage	1.1-1.2	-	Volt
Va	ATX5VSB Ineffective Voltage	1.2	1.3	Volt
Vb	ATX5VSB Valid Voltage	1.2	1.3	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

The ResetIC function controls the PWROK on/off. The PWROK is turned off for a period 140ms when detect pin RESETIC falling edge. If RESETIC low for a long while, PWROK will turn off again after a while. Please refer to the figure below.

The main function is enable by LDE_CRE6[1], and the RESETIN pin has the debounce controlled by LDA_CRED[4].

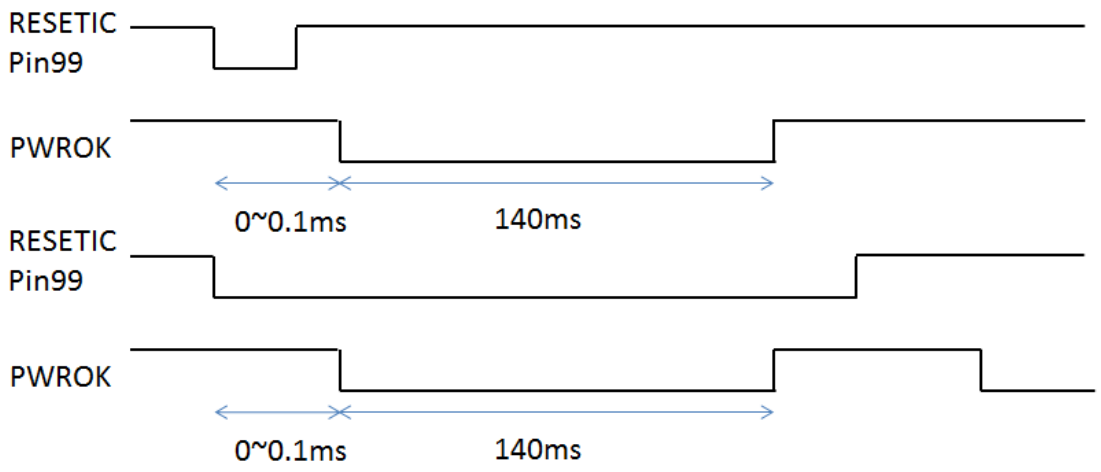


Figure 6-5 Reset IC to PWROK

6.2 LATCH_BKFD_CUT

NCT6126D supports LATCH_BKFD_CUT functions, please refer the timing diagram below.

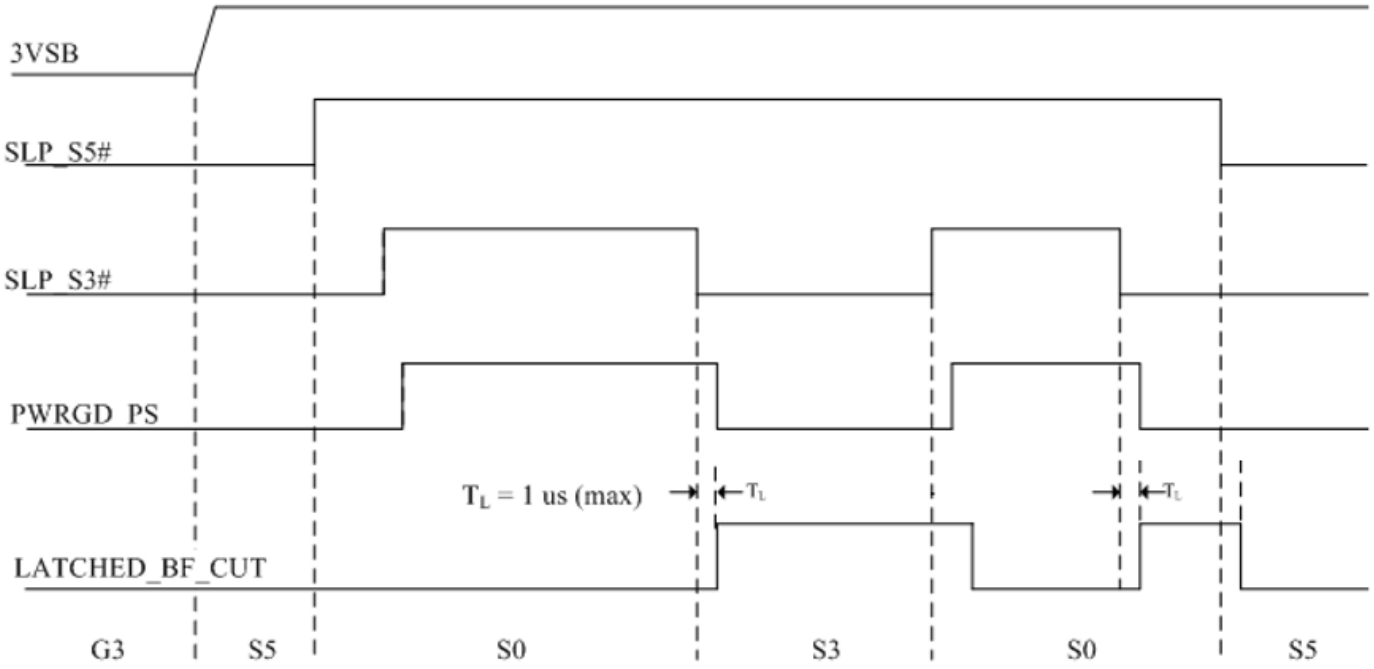


Figure 6-6 LATCH_BKFD_CUT

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

6.3 3VSBSW

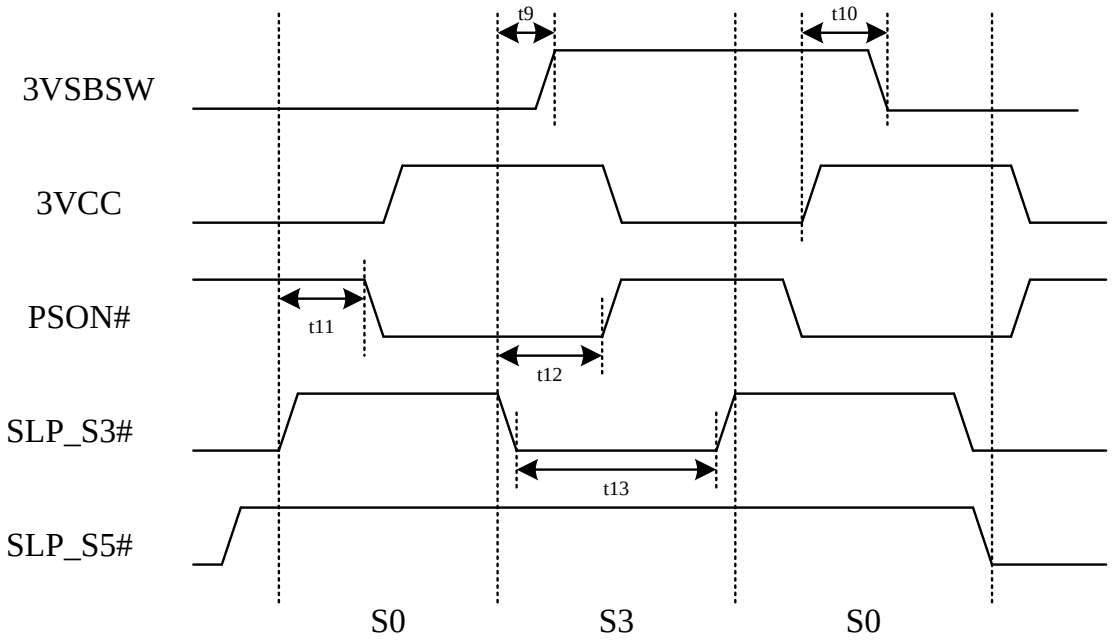


Figure 6-7 3VSBSW

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW active	0	30	mS
t10	3VCC active to 3VSBSW inactive	120	190	mS
t11	SLP_S3# inactive to PSON# active	0	80	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

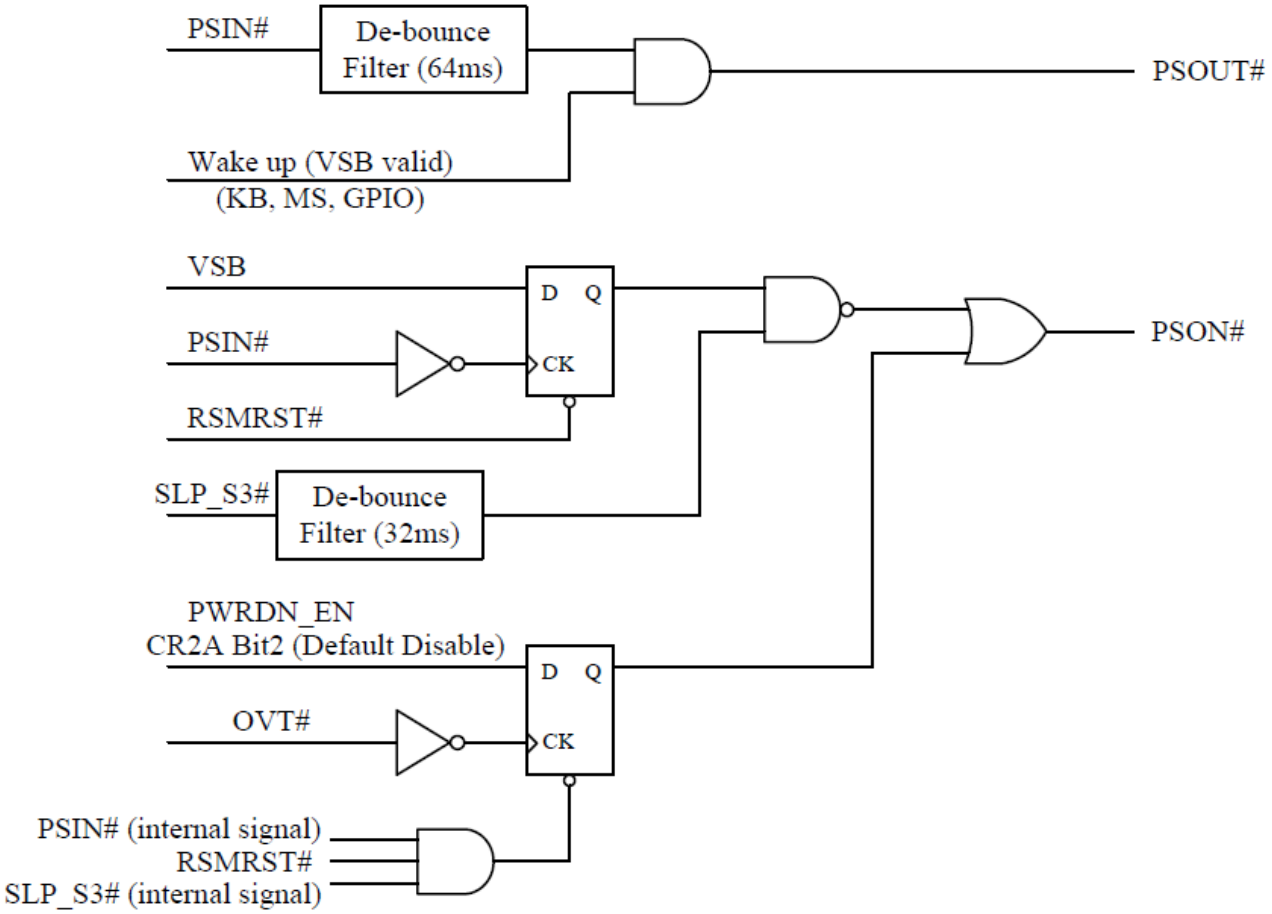


Figure 6-8 PSON# Block Diagram

6.5 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

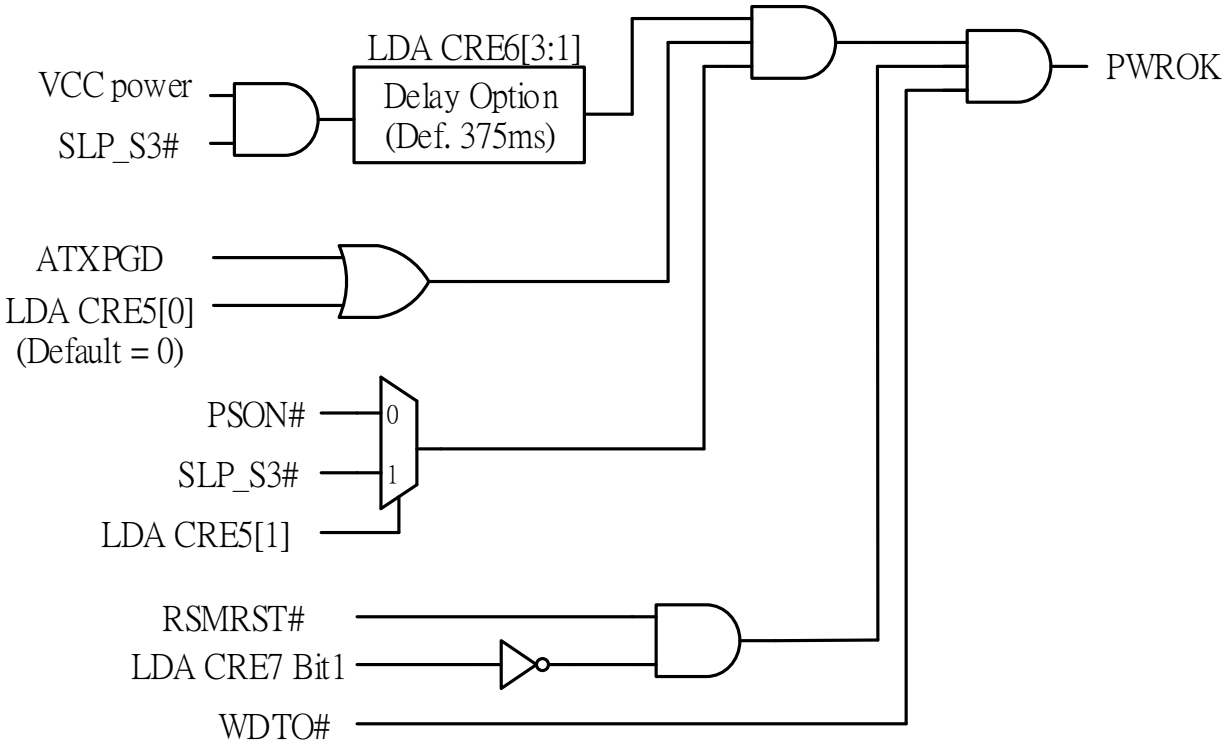


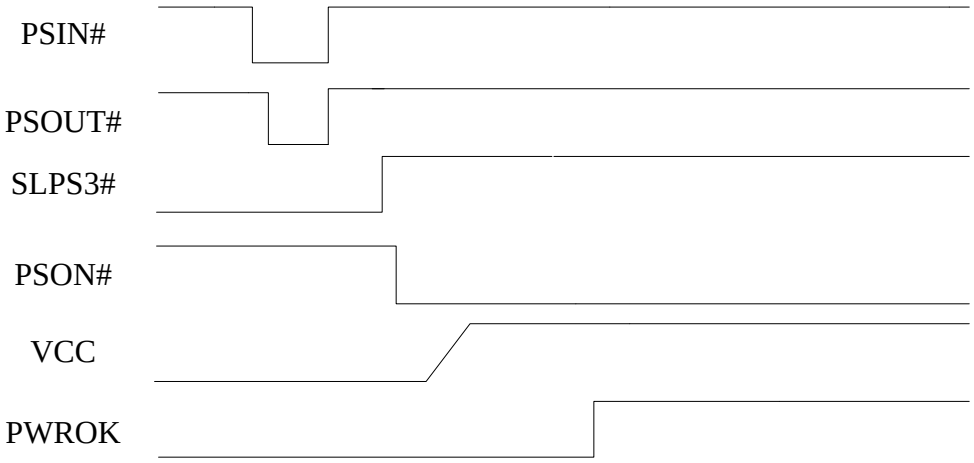
Figure 6-9 PWROK Block Diagram

6.6 AT / ATX Mode

NCT6122D / NCT6126D supports different power supply operation, AT mode / ATX mode, please refer to the decription and timing diagram below. AT mode or ATX mode operation depends on a hardware strapping pin, pin15 KBRST#. The strapping result shows in CR 2F[6].

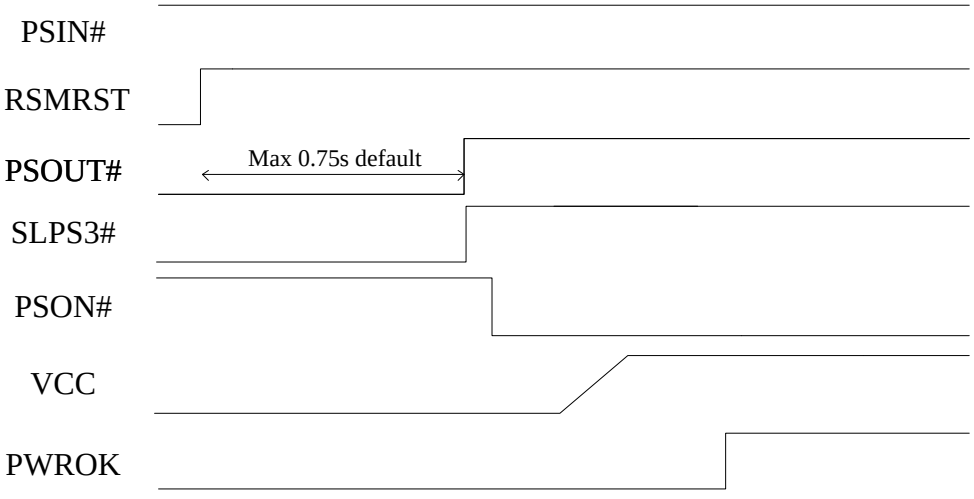
6.6.1 ATX Mode

If pin 15 is strapping high, NCT6122D / NCT6126D operates at ATX mode. In this mode, user needs to push power button to turn on system power. The illustration is as following diagram:



6.6.2 AT Mode

If pin 15 is strapping low, NCT6122D / NCT6126D operates at AT mode. In this mode, NCT6122D / NCT6126D will auto turn on system power within LD9_CRE4[1:0]. The default value of LD9_CRE4[1:0] is 0.75 second maximum. The illustration is as following diagram.



6.7 Front Panel LEDs

NCT6122D / NCT6126D supports two LED control to some GPIO pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

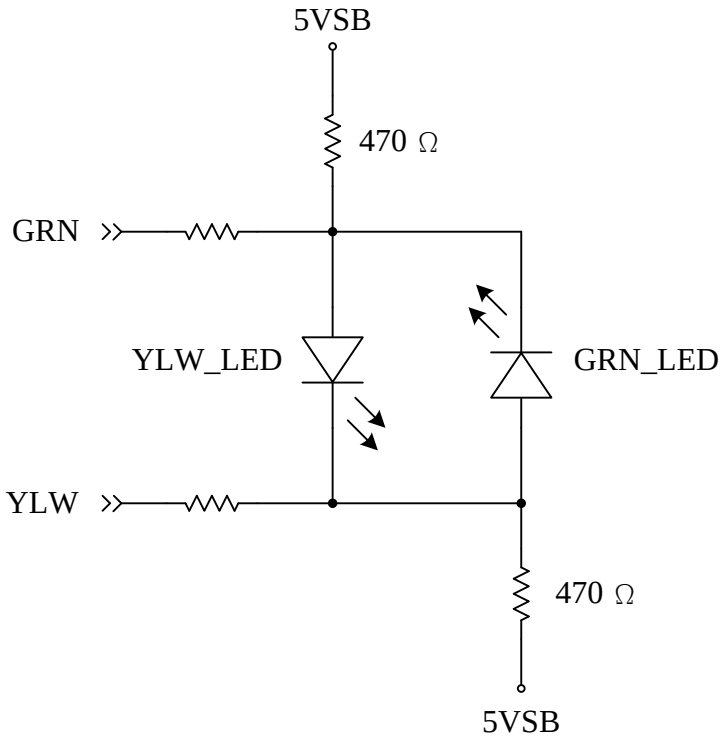


Figure 6-10 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

6.7.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

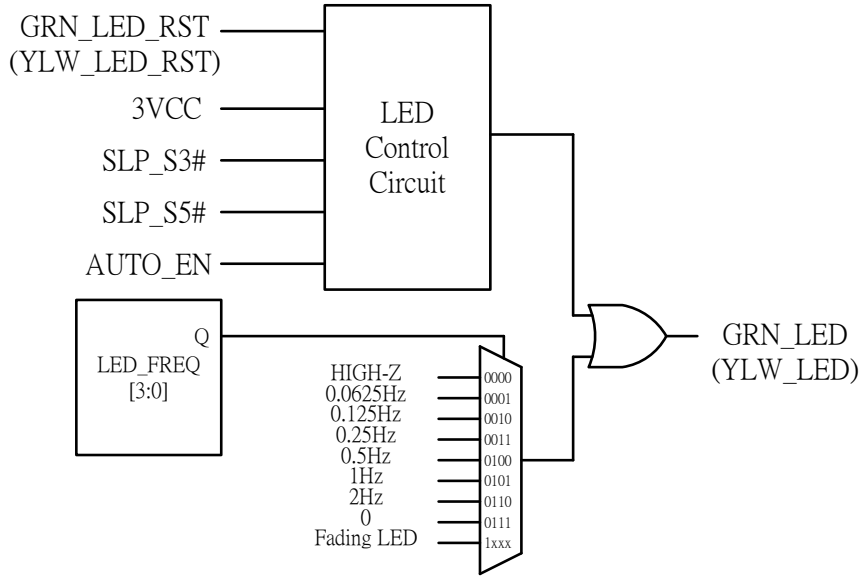
AUTO_EN	3VCC	Power State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	1	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	0	S3	0	1	HIGH-Z	YLW_BLK_FREQ
1	0	S4,S5	0	0	HIGH-Z	HIGH-Z

6.7.2 Manual Mode

AUTO_EN	GRN_LED_RST# (YLW_LED_RST#)	3VCC	Power State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	0	S4,S5	0	0	HIGH-Z	HIGH-Z
0	1	X	S0 ~ S5	X	X	GRN_BLK_FREQ	YLW_BLK_FREQ

Register Name	Register Location
AUTO_EN	Logical Device B, CRF5h, bit7
GRN_BLK_FREQ	Logical Device B, CRF5h, bit3~0
YLW_BLK_FREQ	Logical Device B, CRF6h, bit3~0
GRN_LED_RST#	Logical Device B, CRF5h, bit6
YLW_LED_RST#	Logical Device B, CRF6h, bit6

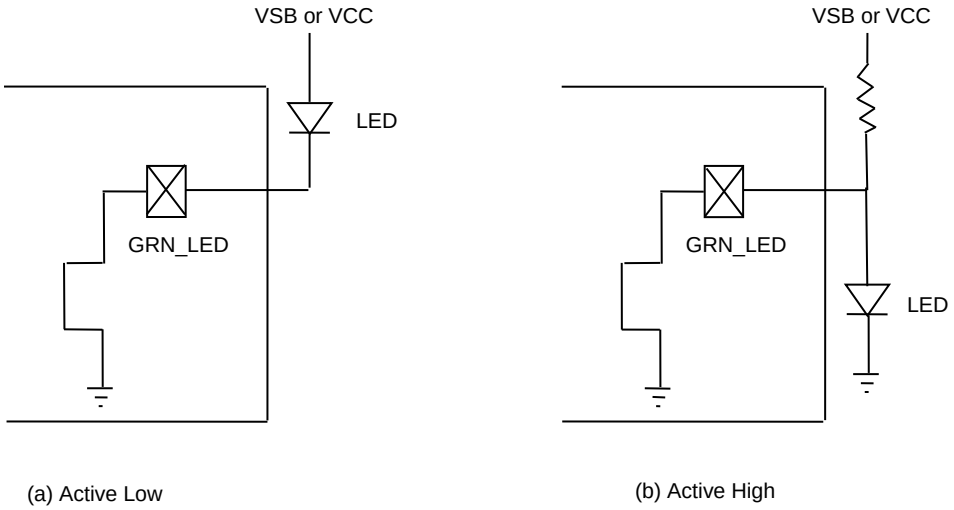
6.7.3 S0~S5 LED Blink Block Diagram



6.7.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure (a)

Set to 1b, GRN_LED output is active high, as the following Figure (b)



(a) Active Low

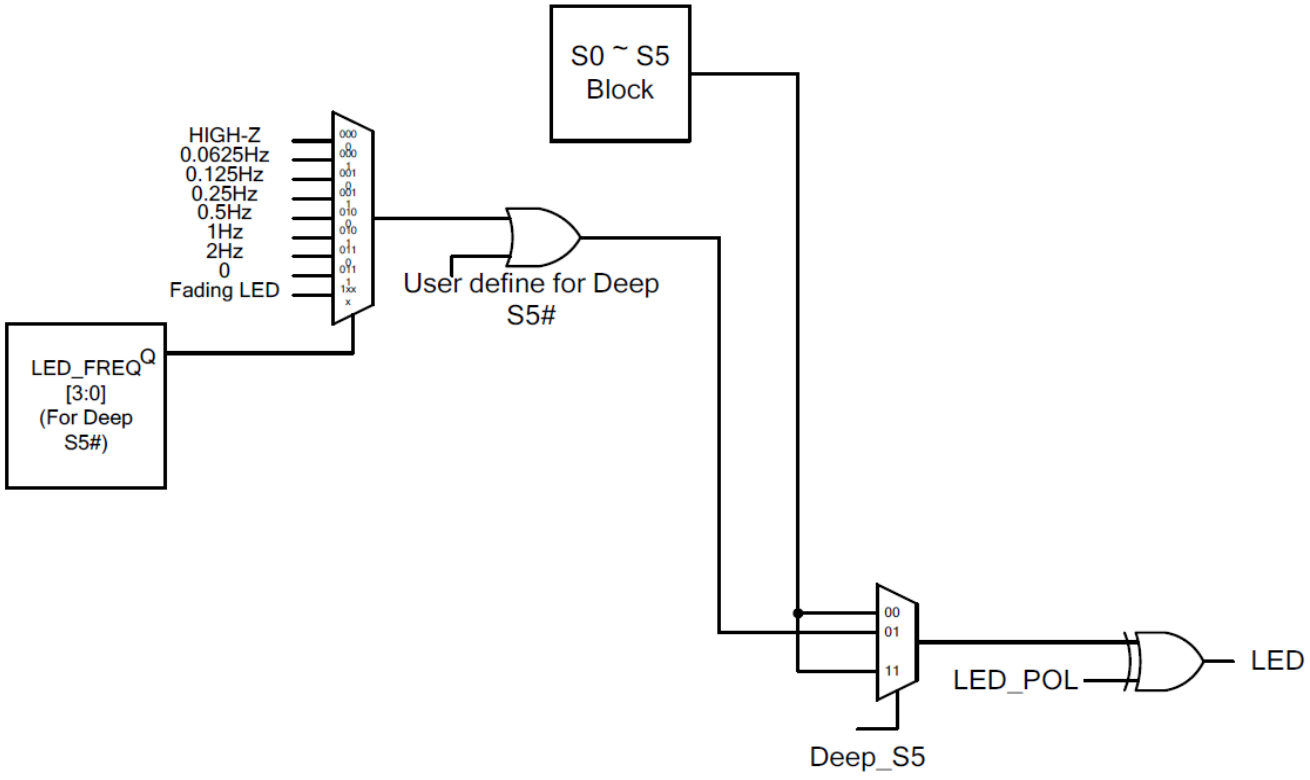
(b) Active High

Figure 6-11 Illustration of LED polarity

6.7.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Power State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior



6.8 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S5 state. The purpose of this function is to provide a method to reduce power consumption at S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logical Device 16 CRE0h ~ CRE3h.

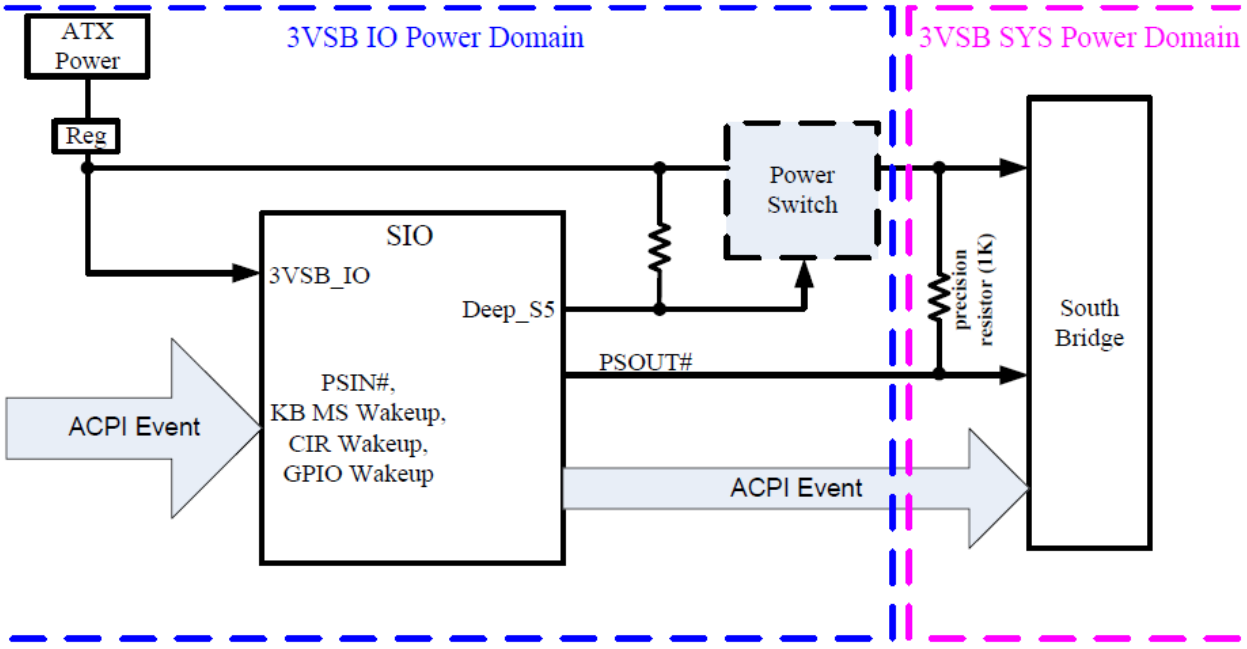
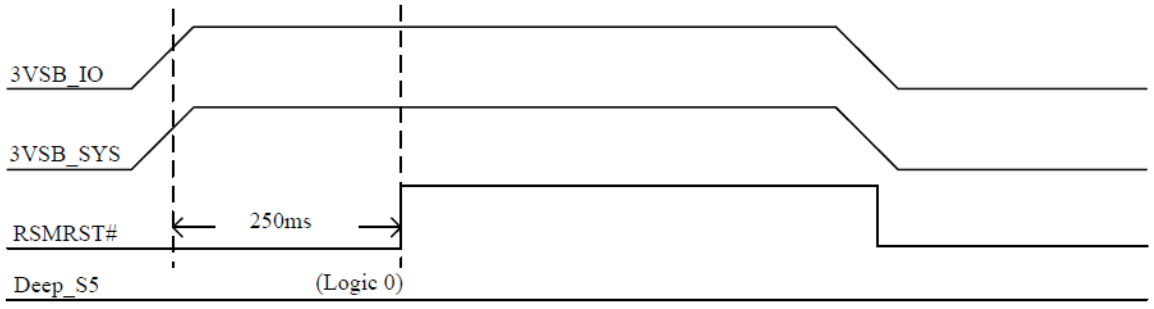


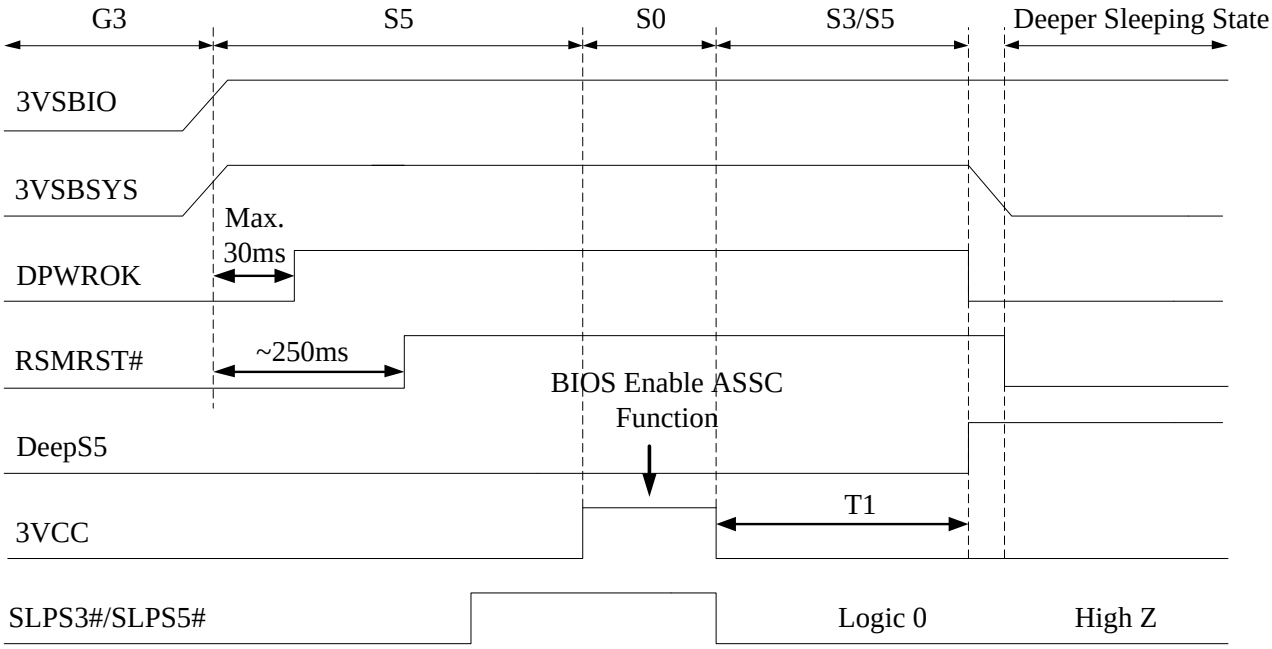
Figure 6-12 ASSC Application Diagram

6.8.1 When ASSC is disabled



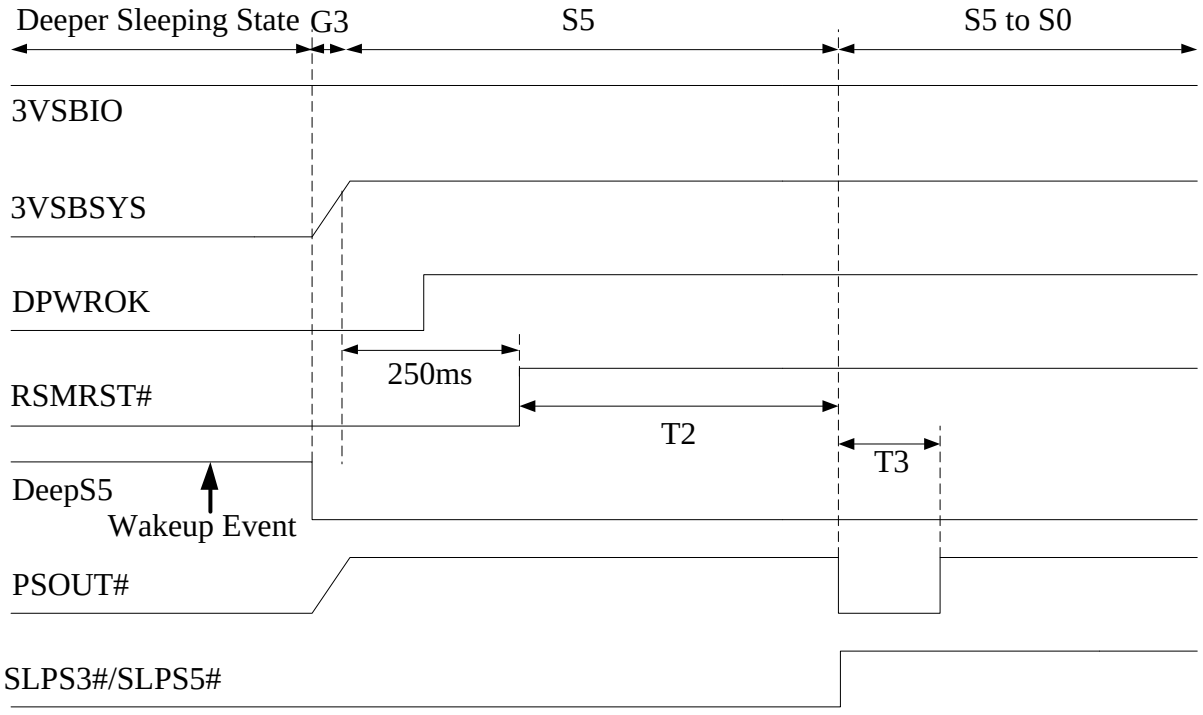
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.8.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS5), when the system enters S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the “Deeper Sleeping State (DSS)” where system’s VSB power is cut off. When pin DEEP_S5 asserts, the pin DPWROK will de-assert and the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSBSYS Power).

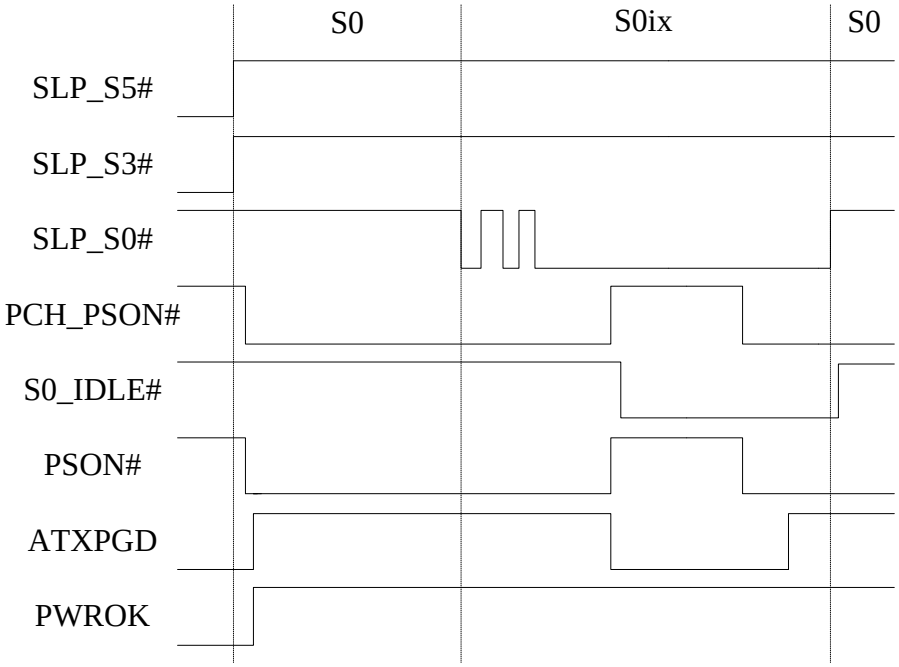
6.8.3 When ASSC is enabled (Exit Deeper Sleeping State)



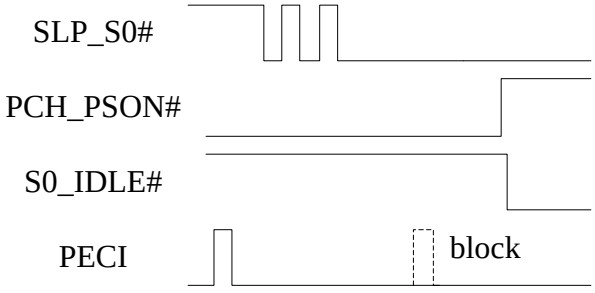
When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSBSYS power reach valid voltage (by detecting PSOUT# signal). The pin DWROK will assert after leaving DeepS5. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time (wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1).

6.9 Modern Standby (S0ix)

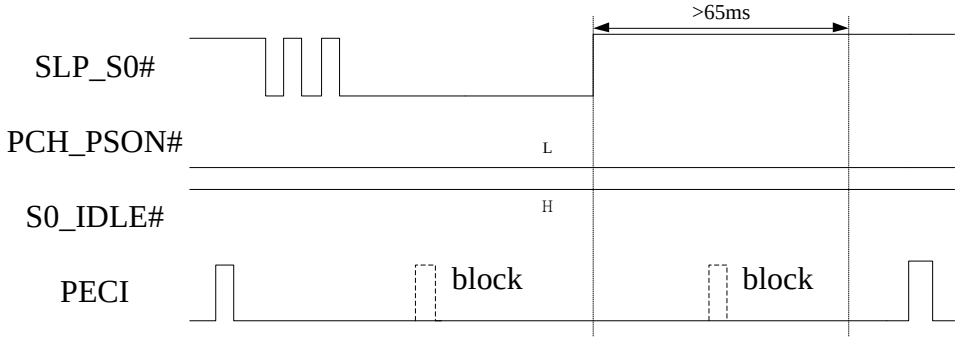
NCT6122D / NCT6126D support Intel coffee lake new function “S0 idle power mode”.User can enable S0ix during S0 mode through Logical Device E CRFA bit0.

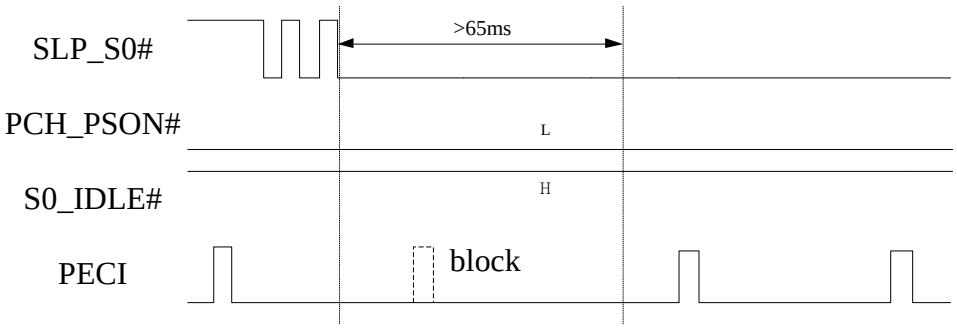


PCH_PSON# can be inverted by Logical Device E CRFA bit4 is asserted. Some associated functions are suspended during S0ix (ex: PECI) to avoid stop CPU can’t get into S0ix (reference to LDE CRFB register).



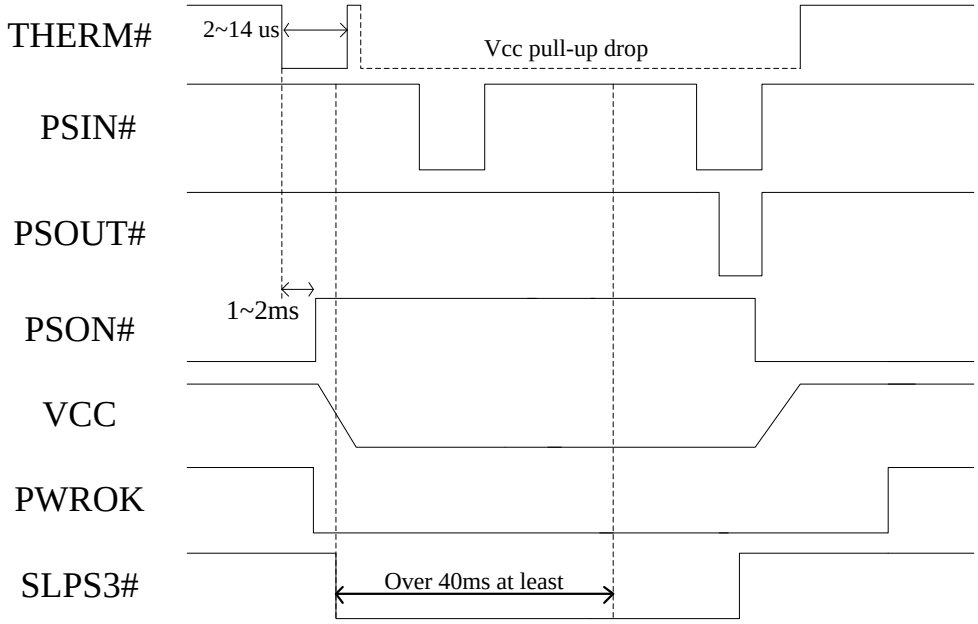
NCT6122D / NCT6126D also support cancel S0ix by assert Logical Device E CRFA bit2.The cancel mechanism depends on time out counter about 65ms.SLPS0# keep high or low over 65ms, SIO will judge this is fail S0ix and release the associated suspend function. Notice that if cancel is judged by SLPS0# keep low too long. User need to pull SLPS0# back to high before next time entering S0ix.



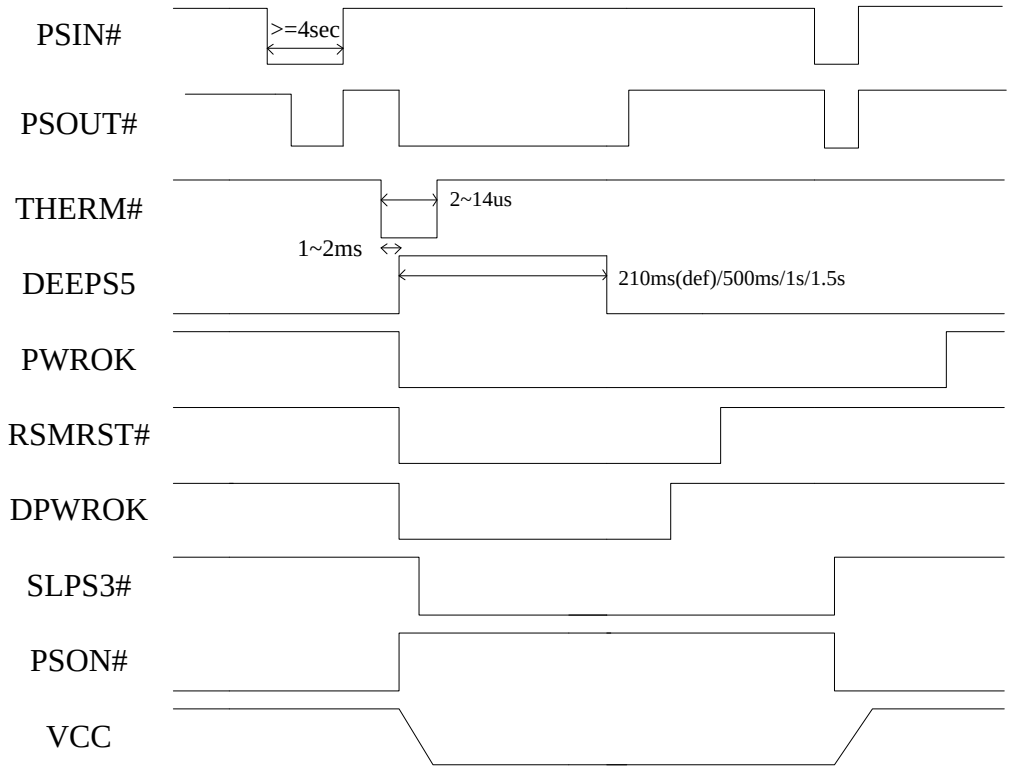

SLP_S0#
>65ms
PCH_PSON#
L
S0_IDLE#
H
PECI
block

6.10 Thermtrip Function

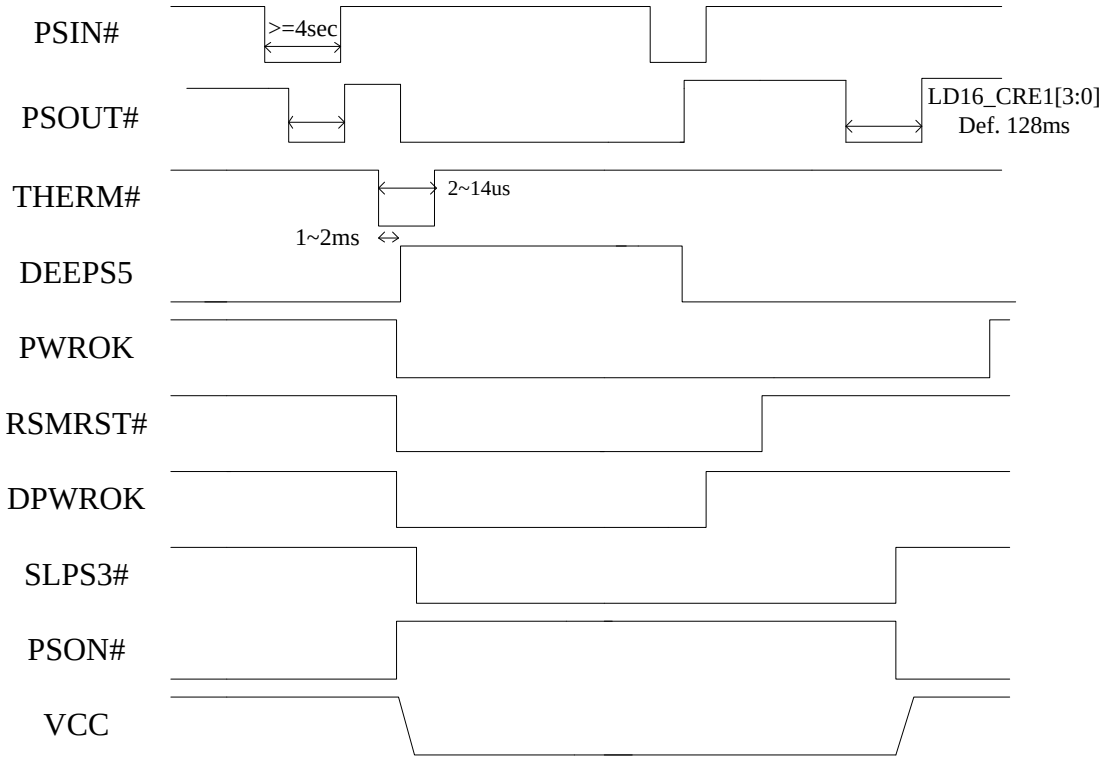
NCT6126D supports thermtrip functions. Pin 107 THERMTRIP# asserts when PCH got overheat issue or global reset fail issue. NCT6126D will control ACPI associate pins, within 40ms after SLPS3# drop, to the corresponding situation.



Strap Pin107 PLAT_SEL to **3VSB** make NCT6122D / NCT6126D support 4 second PSIN# with Thermtrip mode. Logical Device 9 CR30 Bit6-5 control DEEPS5 timing (default as 210ms).


PSIN#
>=4sec
PSOUT#
THERM#
2~14us
1~2ms
DEEPS5
210ms(def)/500ms/1s/1.5s
PWROK
RSMRST#
DPWROK
SLPS3#
PSON#
VCC

Enable Logical Device 9 CR30 Bit7 makes NCT6122D / NCT6126D change from 210ms DeepS5 mode to stay at DeepS5 mode while event occurred.



7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT6122D / NCT6126D uses a special protocol to access configuration registers to set up different types of configurations. The NCT6122D / NCT6126D has a total of 17 Logical Devices (from Logical Device 0 to Logical Device 16 with the exception of Logical Device 4 & C for backward compatibility) corresponding to fourteen individual functions: PRT (Logical Device 1), UARTA (Logical Device 2), UARTB (Logical Device 3), KBC (Logical Device 5), CIR (Logical Device 6), GPIO (Logical Device 7), GPIO & WDT1 (Logical Device 8), GPIO (Logical Device 9), ACPI (Logical Device A), HM & LED (Logical Device B), WDT2 (Logical Device D), CIR WAKE-UP (Logical Device E), GPIO (Logical Device F), UARTC (Logical Device 10), UARTD (Logical Device 11), UARTE (Logical Device 12), UARTF (Logical Device 13), PORT80 & IR (Logical Device 14), FADING LED (Logical Device 15) and DEEP SLEEP (Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT6122D / NCT6126D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

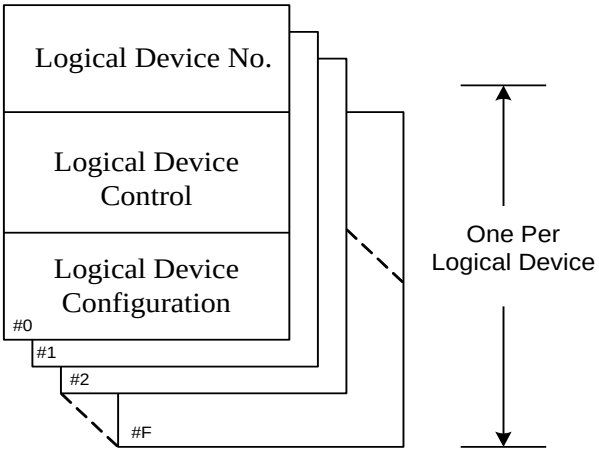


Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	PRT	100h ~ FF8h
2	UARTA	100h ~ FF8h
3	UARTB	100h ~ FF8h
4	Reserved	
5	KBC	100h ~ FFFh
6	CIR	100h ~ FF8h
7	GPIO	Reserved
8	GPIO, WDT1	Reserved
9	GPIO	Reserved
A	ACPI	Reserved
B	HM, LED	100h ~ FFEh
C	Reserved	
D	WDT2	Reserved
E	CIR WAKE-UP	100h ~ FF8h
F	GPIO	Reserved
10	UARTC	100h ~ FF8h
11	UARTD	100h ~ FF8h
12	UARTE	100h ~ FF8h
13	UARTF	100h ~ FF8h
14	PORT80, IR	100h ~ FF8h
15	FADING LED	Reserved
16	DEEP SLEEP	Reserved

7.1 Configuration Sequence

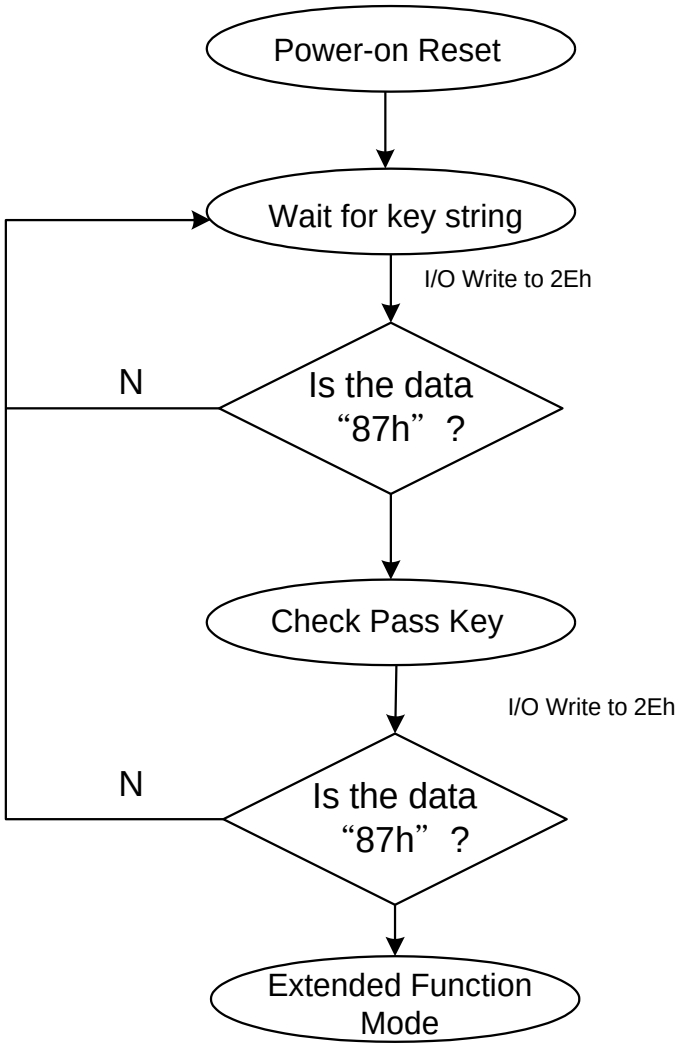


Figure 7-2 Configuration Register

To program the NCT6122D / NCT6126D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

(4). Read the **Extended Function Data Register (EFDR)** when the interface is eSPI.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA when entry key is 0x87 or 0xBB when entry key is 0x88 to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Read the Extended Function Data Register (EFDR) when the interface is eSPI

When the interface is eSPI, read the **Extended Function Data Register (EFDR)** (i.e. 2Fh or 4Fh) at the end programming of SIO. This step restores all IO resource port data to 0xFF.

7.1.5 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR [26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of Logical Device 2 (UART A) to the value of 02h (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 02h. Then program Index F0h to 02h. Finally, exit the Extended Function Mode. When the interface is eSPI, read the EFDR to restore all IO resource port data be 0xFF.

```
;-------------------------------------------------------
; Enter the Extended Function Mode
;-------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;-------------------------------------------------------------------------
; Configure Logical Device 2, Configuration Register CRF0
;-------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 02H
OUT    DX, AL          ; select Logical Device 2
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
```

```
MOV     DX, 2FH
MOV     AL, 02H
OUT     DX, AL              ; update CRF0 with value 02H
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL

;-------------------------------------------------------------------------
; Read the Extended Function Data Register (EFDR)
;-------------------------------------------------------------------------
MOV    DX, 2FH
IN         DX
```

8. HARDWARE MONITOR

8.1 General Description

The NCT6122D / NCT6126D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT6122D / NCT6126D can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (six internal voltages CPUVCORE, VTT, VBAT, 3VSB, 3VCC and AVSB; three external voltage inputs)
- Five fan tachometer inputs
- Three remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT6122D / NCT6126D can generate the following outputs:

- Three PWM (pulse width modulation) or DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT6122D / NCT6126D provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT6122D / NCT6126D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT6122D / NCT6126D provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

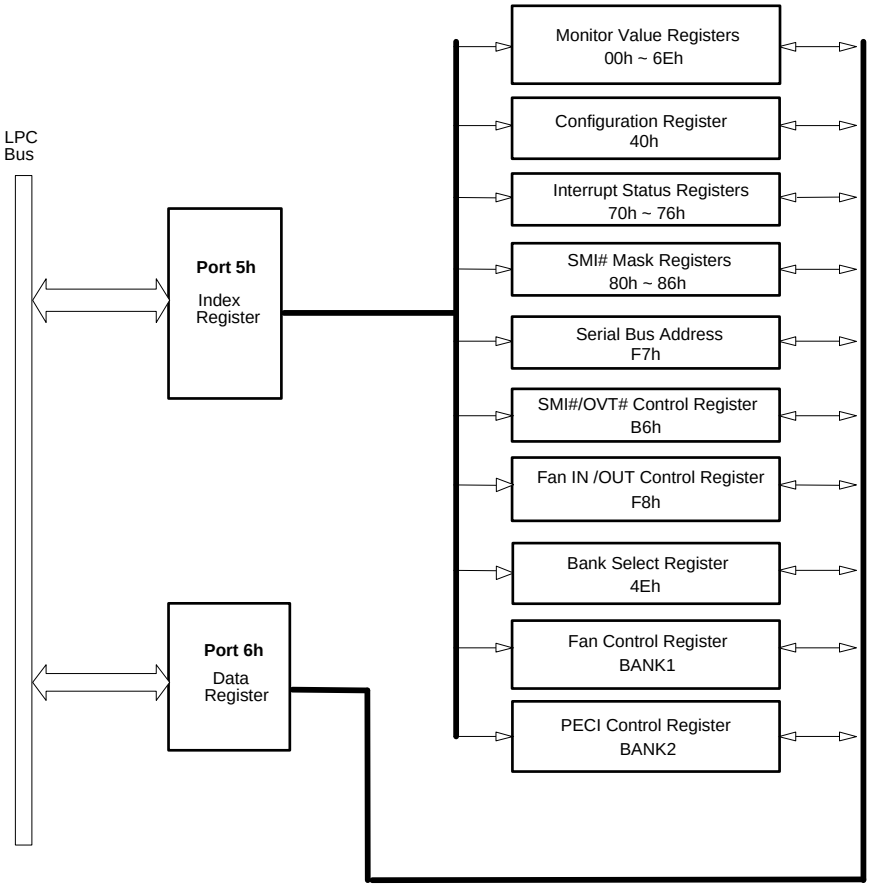


Figure 8-1 LPC Bus’ Reads from / Write to Internal Registers

8.4 ESPI interface

The Enhanced Serial Peripheral Interface (ESPI) operates in master/slave mode of operation where the eSPI master dictates the flow of command and data between itself and the eSPI slave by controlling the Chip Select# pins for each of the eSPI slaves. At any one time, the eSPI must ensure that only one of the Chip Select# pins is asserted based on source code, thus allowing transactions to flow between the eSPI master and the corresponding eSPI slave associated with the Chip Select# pin. The eSPI master is the only component that is allowed to drive Chip Select# when eSPI Reset# is de-asserted.

For an eSPI bus, there is only the eSPI master and one or more eSPI slaves. In single Master-Single Slave configuration, a single eSPI master will be connected to a single eSPI slave.

The eSPI provided an alternative for connecting an SIO to the platform (besides the LPC interface). Note the LPC and eSPI co-exist on the platform but only one interface can be enabled at a time via a hardware strap.

The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses The NCT6122D / NCT6126D's eSPI is only support IO Read and Write, Get PCH temperature by OOB, and virtual wire. The OOB setting register at Logical Device E CRF2. The OOB polling is blocked when system in S0ix state, it can set register (Logical Device E CRF3 [4]) to unblocked.

Because the limitation for internal clock frequence, NCT6126D & NCT6122D eSPI only support the eSPI_CLK 20~33MHz.

The basic protocol is shown as below. For the detail eSPI specification, please refer to ***Enhanced Serial Peripheral Interface Base Specification (for Client and Server Platform) Rev 0.75***

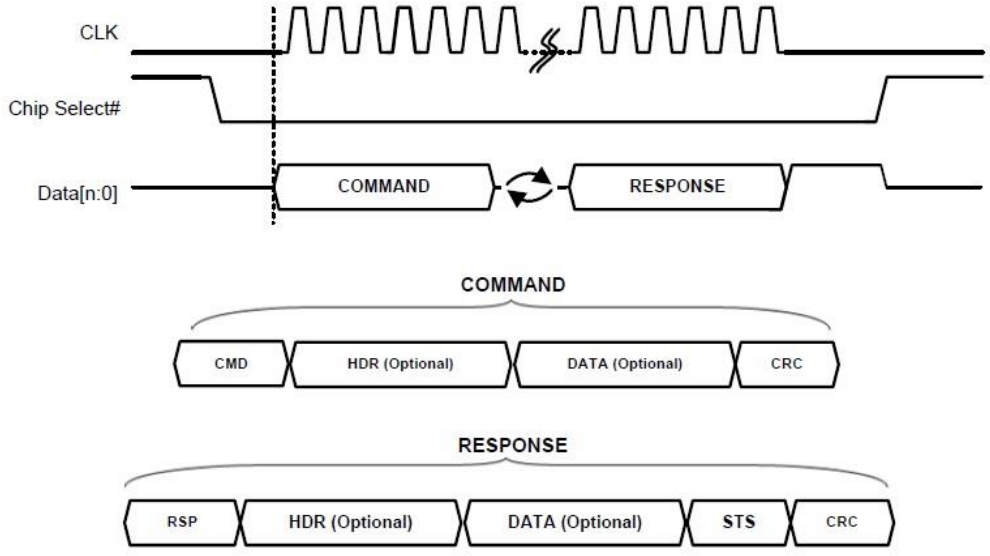


Figure 8-2 eSPI Protocol Transaction

8.5 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT6122D / NCT6126D hardware monitor and control fan speeds.

The address of the I²C peripheral is set by the register located at Index F7h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

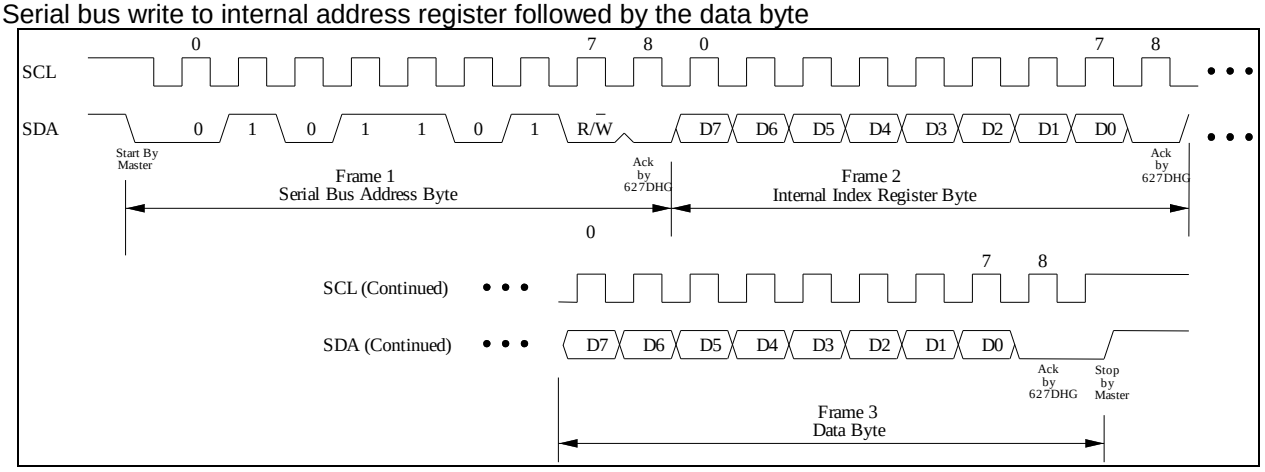


Figure 8-3 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

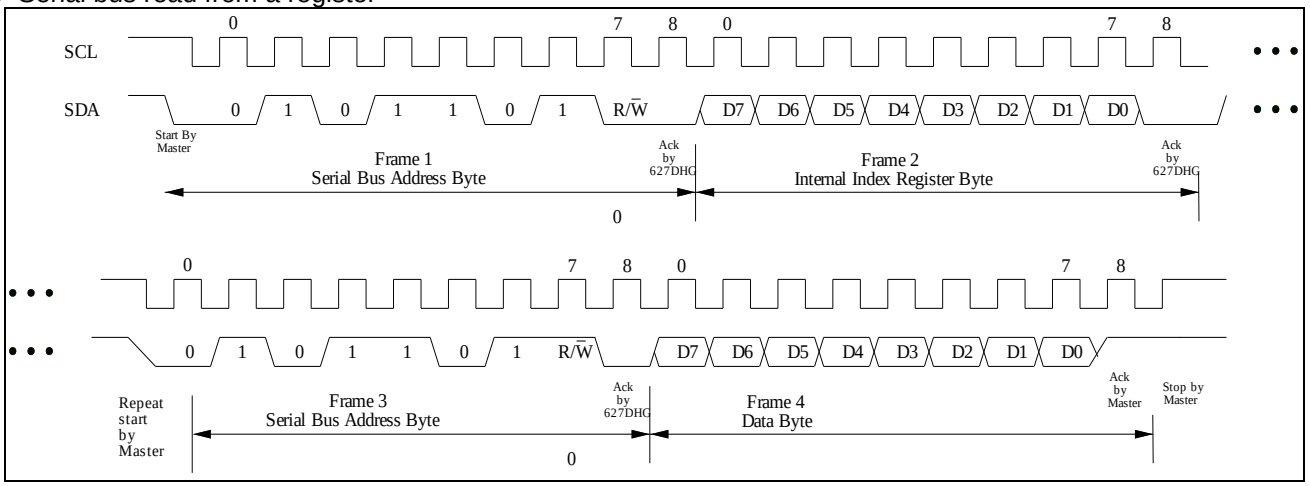


Figure 8-4 Serial Bus Read from Internal Address Register

8.6 Analog Inputs

The nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 4 general-purpose inputs connected to external device pins (VIN0 – VIN2) and five internal signals connected to the power supplies (CPUVCORE, AVSB, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

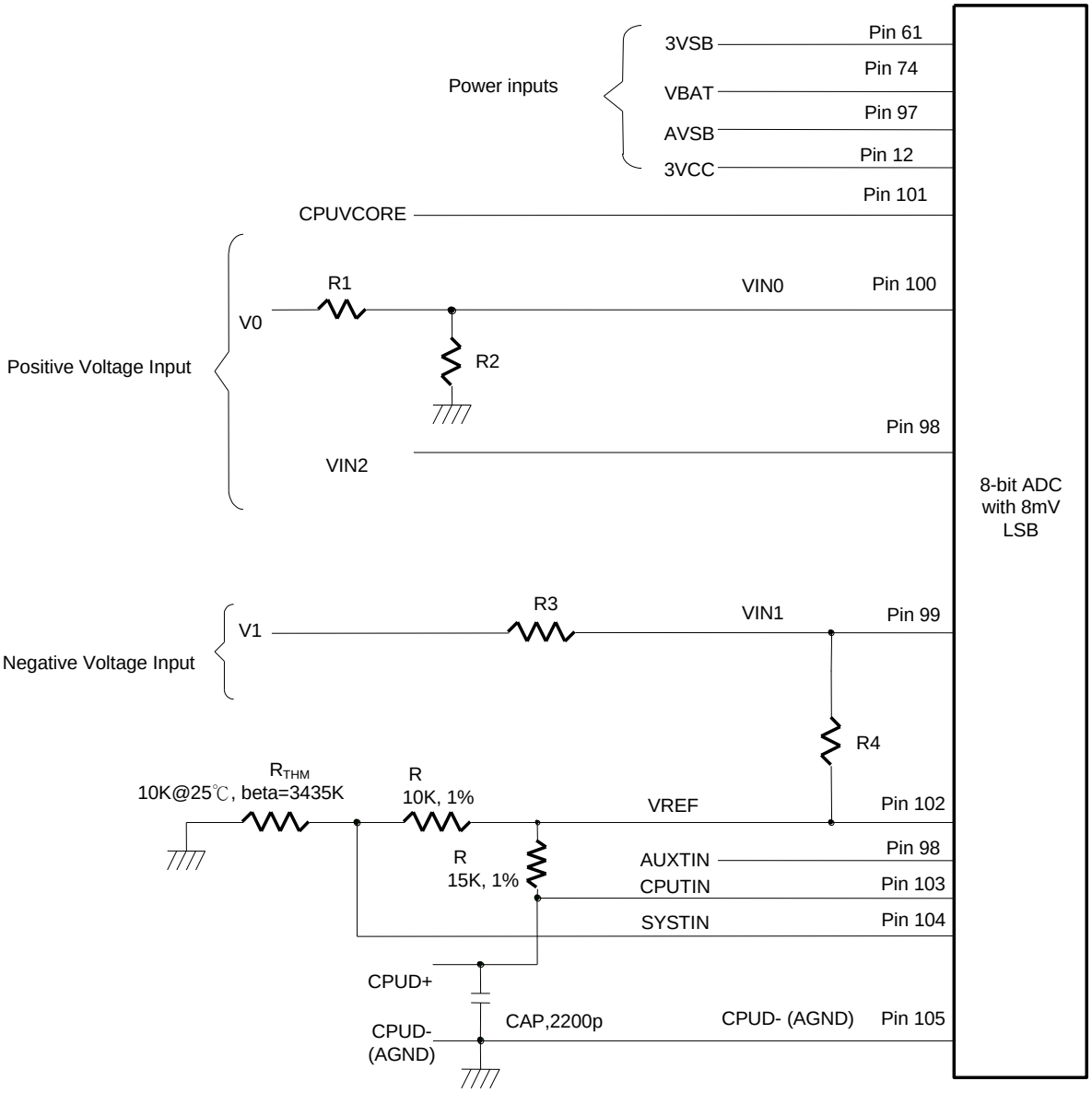


Figure 8-5 Analog Inputs and Application Circuit of the NCT6122D / NCT6126D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.6.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVSB, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.6.2 Voltage Data Format

CPUVCORE, VIN1, VIN0, VIN2, and VTT, the data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

AVSB, 3VCC, 3VSB, VBAT, and VHIF, the data format for voltage detection is an eight-bit value, and each unit represents an interval of 16 mV.

Detected Voltage = Reading * 0.016 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.6.2.1. Voltage Reading

NCT6122D / NCT6126D has 10 voltage reading:

	3VCC	**AVSB**	**3VSB**	**VBAT**	**VHIF**
Voltage reading	Bank0, Index 03h	Bank0, Index 02h	Bank0, Index 07h	Bank0, Index 08h	Bank0, Index 06h
	CPUVCORE	**VIN0**	**VIN1**	**VIN2**	**VTT**
Voltage reading	Bank0, Index 00h	Bank0, Index 01h	Bank0, Index 04h	Bank0, Index 05h	Bank0, Index 09h

8.6.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN and AUXTIN is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0Fah
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1Ceh
-55°C	1100,1001	C9h	1,1001,0010	192h

8.6.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF. The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 3, 18h, and 19h.

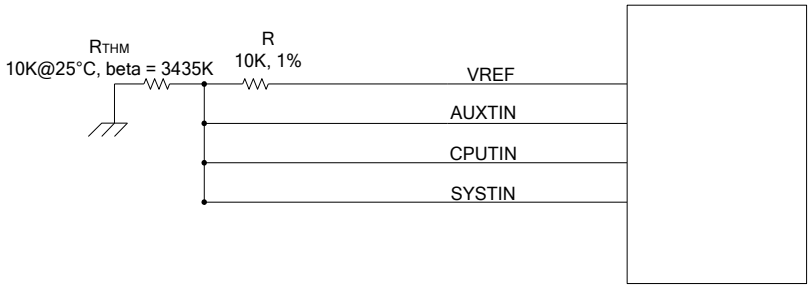


Figure 8-6 Monitoring Temperature from Thermistor

8.6.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND, and the D+ pin is connected to the temperature sensor pin in the NCT6122D / NCT6126D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 3, Index 18h, and 19h.

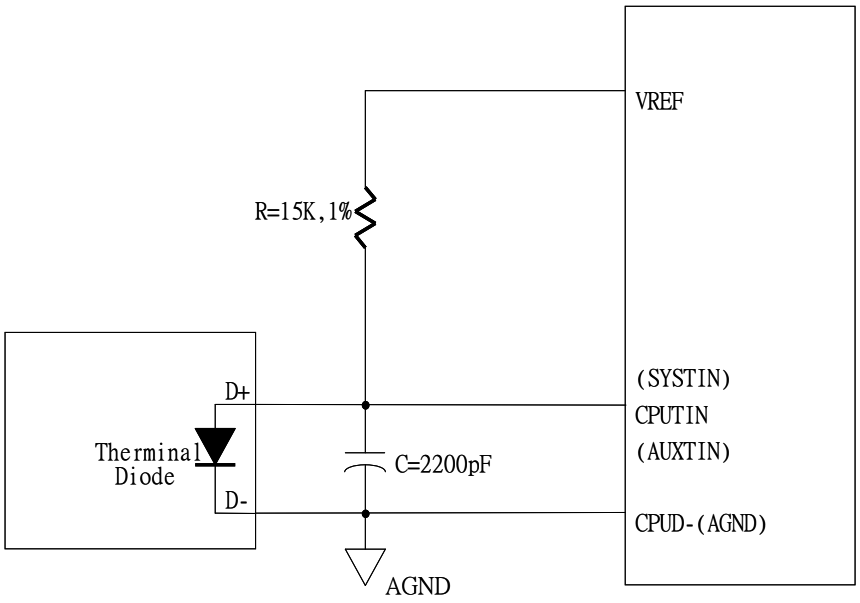


Figure 8-7 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.6.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT6122D / NCT6126D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

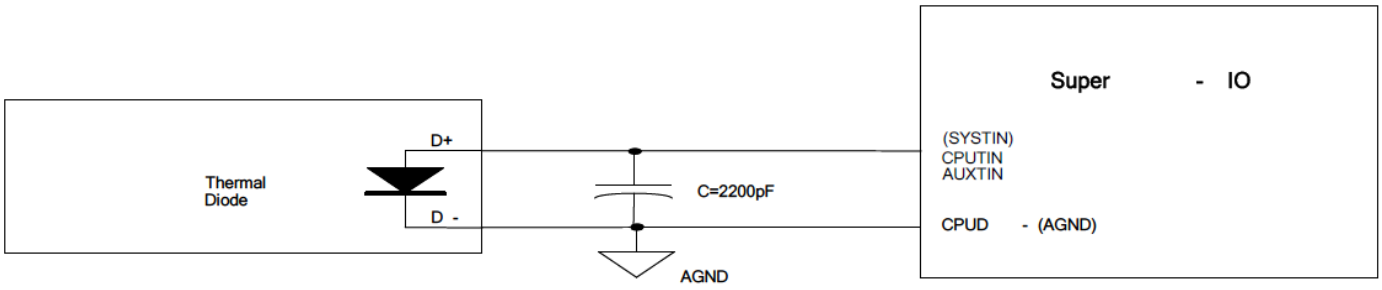


Figure 8-8 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- and the pin D+ is connected to temperature sensor pin in the NCT6122D / NCT6126D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 3, 18h, and 19h.

8.6.3.4. Temperature Reading

NCT6122D / NCT6126D has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, AUXTIN, PECI…etc).

	SMIOVT1	SMIOVT2	SMIOVT3
Temperature source select	Bank0, IndexB0 bit[4:0]	Bank0, IndexB1 bit[4:0]	Bank0, IndexB2 bit[4:0]

	default: SYSTIN	default: CPUTIN	default: AUXTIN
Temperature reading (2's complement)	Bank0, Index10 & Index16 bit0	Bank0, Index11 & Index16 bit1	Bank0, Index12 & Index16 bit2

8.7 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT6122D / NCT6126D supports. The NCT6122D / NCT6126D contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-9 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

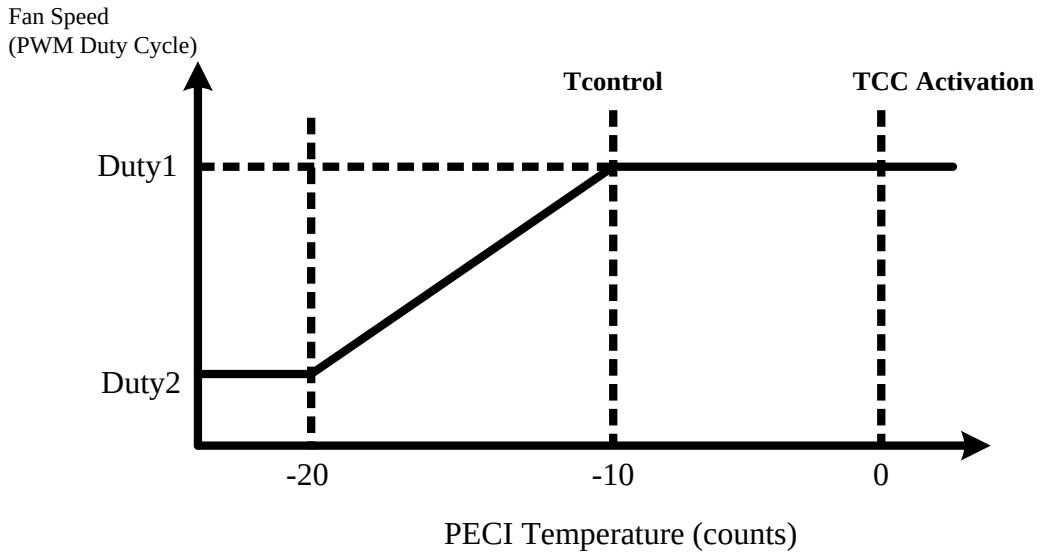


Figure 8-9 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore, Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

NCT6122D / NCT6126D's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan ™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the Tbase registers located at Bank2, Index04h for PECI_BASE0; Bank2, Index05h for PECI_BASE1; separately. All default values of these Tbase registers are 8'h00.These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure 8-11 shows the temperature/fan speed relationship after Tbase offsets are applied (based on Figure 8-9 PECI Temperature). This view is from the perspective of the NCT6122D / NCT6126D fan control circuit.

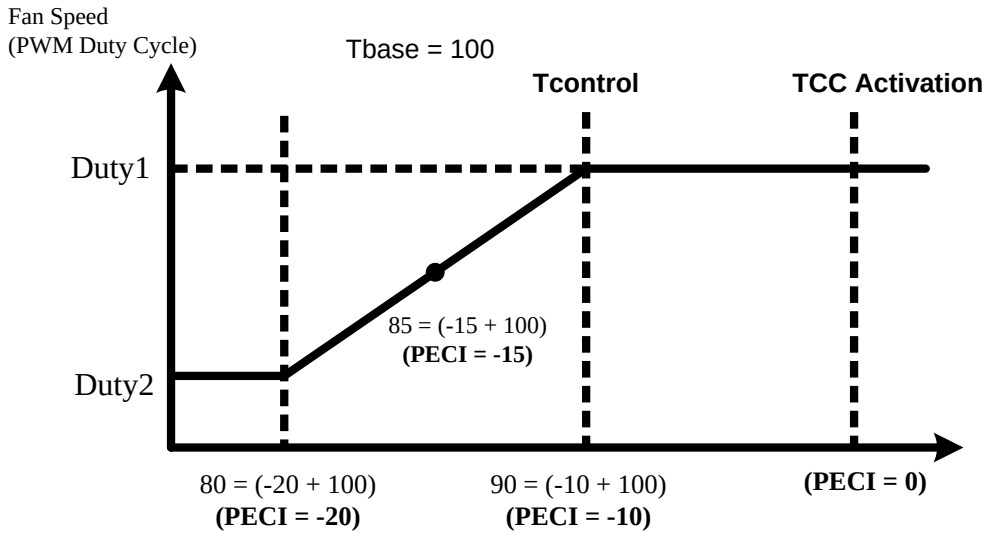


Figure 8-10 Temperature and Fan Speed Relation after Tbase Offsets

Assuming Tbase is set to 100 and the PECI temperature is -15, the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT6122D / NCT6126D, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.8 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.8.1 Fan Speed Reading

The fan speed reading is at

	FAN COUNT READING		FAN RPM READING	
	13-bit		16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank0, Index20	Bank0, Index21	Bank0, Index30	Bank0, Index31
CPUFANIN	Bank0, Index22	Bank0, Index23	Bank0, Index32	Bank0, Index33
AUXFANIN0	Bank0, Index24	Bank0, Index25	Bank0, Index34	Bank0, Index35
AUXFANIN1	Bank0, Index26	Bank0, Index27	Bank0, Index36	Bank0, Index37
AUXFANIN2	Bank0, Index28	Bank0, Index29	Bank0, Index38	Bank0, Index39

8.8.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.8.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.8.4 Fan Speed Control

The NCT6122D / NCT6126D has five output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 Index F3h, bits 0 for SYSFANOUT, bits 1 for CPUFANOUT and bit 2 for AUXFANOUT.

Pin14 AUXFANOUT0 Function Output Enable controls by CR24 bit3 default disable.

	SYSFANOUT	CPUFANOUT	AUXFANOUT0	AUXFANOUT1	AUXFANOUT2
Output Type Select	Bank0, IndexF3 bit0 0: PWM output(default) 1: DC output	Bank0, IndexF3 bit1 0: PWM output (default) 1: DC output	Bank0, IndexF3 bit2 0: PWM output (default) 1: DC output	PWM output	PWM output

Output Type Select (in PWM output)		CR24 bit6 0: open-drain (default) 1: push-pull	CR24 bit5 0: open-drain (default) 1: push-pull	CR24 bit4 0: open-drain (default) 1: push-pull	CR22 bit1 0: open-drain (default) 1: push-pull	CR22 bit2 0: open-drain (default) 1: push-pull
PWM Output Frequency		Bank0, IndexF0	Bank0, IndexF1	Bank0, IndexF2	Bank0, IndexF9	Bank0, IndexFA
Fan Control Mode Select		Bank1, Index13, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, Index23, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, Index33, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, Index93, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank1, IndexA3, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank1, Index19 bit[7:0]	Bank1, Index29 bit[7:0]	Bank1, Index39 bit[7:0]	Bank1, Index99 bit[7:0]	Bank1, IndexA9 bit[7:0]
	DC output (Voltage)	Bank1, Index19 bit[7:2]	Bank1, Index29 bit[7:2]	Bank1, Index39 bit[7:2]	Bank1, Index99 bit[7:2]	Bank1, IndexA9 bit[7:2]
Current Output Value (read)		Bank0, Index4A	Bank0, Index4B	Bank0, Index4C	Bank0, IndexD8	Bank0, IndexD9

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 19h for SYSFANOUT, Bank1 Index 29h for CPUFANOUT, Bank1 Index 39h for AUXFANOUT, Bank1 Index 99h for AUXFANOUT1 and Bank1 Index A9h for AUXFANOUT2. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 4Ah, Index 4Bh, and Index 4Ch.

For DC, the NCT6122D / NCT6126D has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 19h bit[7:2] for SYSFANOUT, Bank1 Index 29h bit[7:2] for CPUFANOUT and Bank1 Index 39h bit[7:2] for AUXFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = Vref \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.8.5 SMART FAN™ Control

The NCT6122D / NCT6126D supports various different fan control features:

- SMART FAN™ I (Thermal Cruise & Speed Cruise)
- SMART FAN™ IV
- Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Mode Select	Bank1, Index13, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	Bank1, Index23, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	Bank1, Index33, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV
	AUXFANOUT1	**AUXFANOUT2**	
Fan Control Mode Select	Bank1, Index93, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	Bank1, IndexA3, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN™ IV	

8.8.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Temperature Source Select	Bank1, Index10 bit[4:0] Default: SYSTIN	Bank1, Index20 bit[4:0] Default: CPUTIN	Bank1, Index30 bit[4:0] Default: AUXTIN
Fan Control Temperature Reading	Bank0, Index18 & Bank0, Index1B bit0	Bank0, Index19 & Bank0, Index1B bit1	Bank0, Index1A & Bank0, Index1B bit2
Close-Loop Fan Control RPM mode	Bank1, Index1E bit0	Bank1, Index2E bit0	Bank1, Index3E bit0
	AUXFANOUT1	**AUXFANOUT2**	
Fan Control Temperature Source Select	Bank1, Index90 bit[4:0] Default: AUXTIN	Bank1, IndexA0 bit[4:0] Default: AUXTIN	
Fan Control Temperature Reading	Bank0, IndexDB & Bank0, Index1B bit3	Bank0, IndexDC & Bank0, Index1B bit4	
Close-Loop Fan Control RPM mode	Bank1, Index9E bit0	Bank1, IndexAE bit0	

8.9 SMART FAN™ I

8.9.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains

below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified "stop value".

This "stop value enable" is enabled by the Bank1, Index10h, Bit7 for SYSFANOUT; Bank1, Index20h, Bit7 for CPUFANOUT and Bank1, Index30h, Bit7 for AUXFANOUT. Index90h, Bit7 for AUXFANOUT1 and IndexA0h, Bit7 for AUXFANOUT2.

The "stop value" itself is separately specified in Bank1 Index16h, Bank1 Index26h and Bank1 Index36h, Bank1 Index96h and Bank1 IndexA6h.

The "stop time" means fan remains at the stop value for the period of time also separately defined in Bank1 Index18h, Bank1 Index28h and Bank1 Index38h, Bank1 Index98h and Bank1 IndexA8h

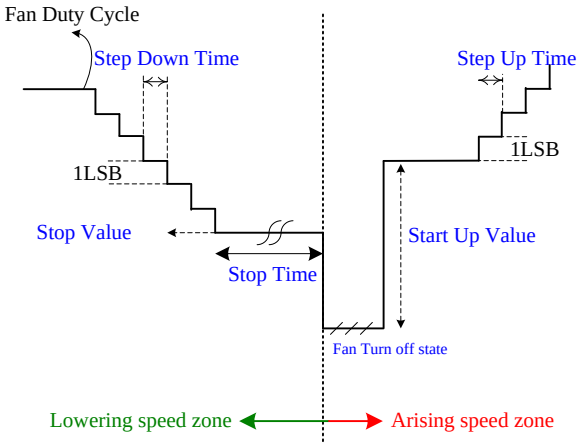


Figure 8-11 Thermal Cruise™ Mode Parameters Figure

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

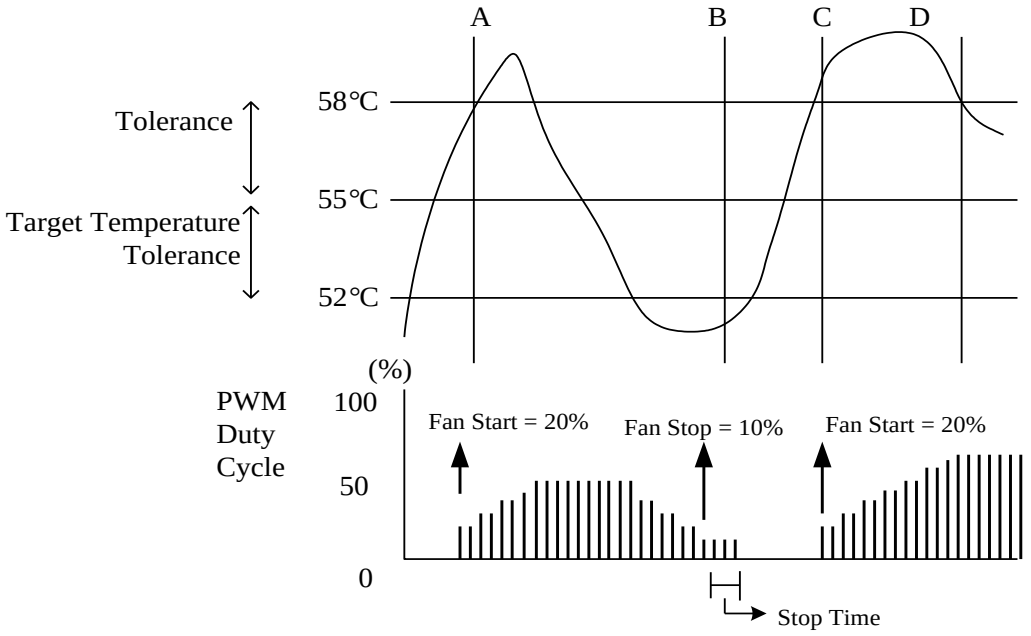


Figure 8-12 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

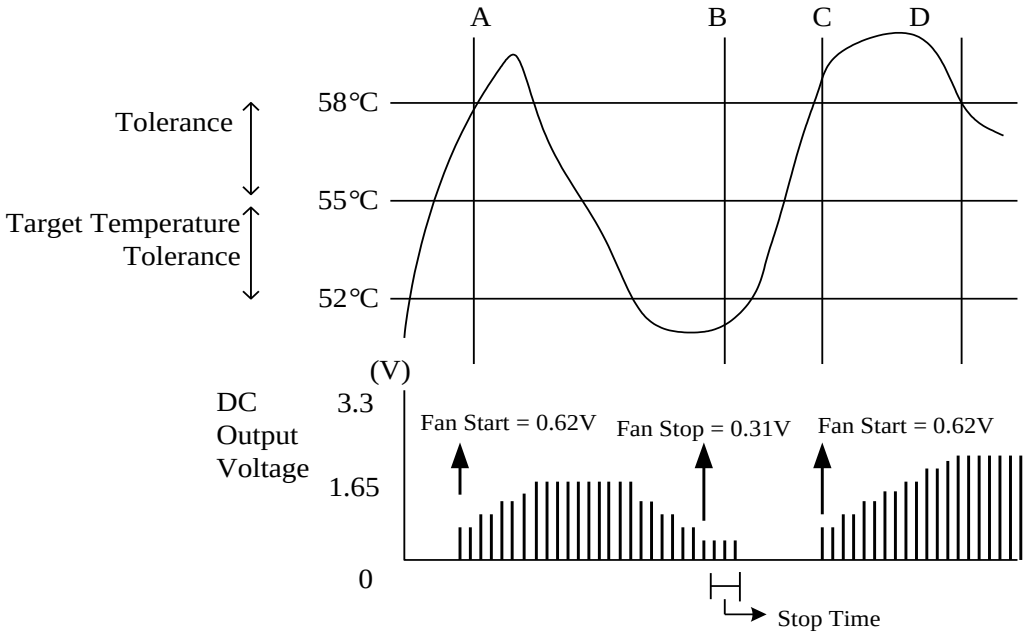


Figure 8-13 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.9.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

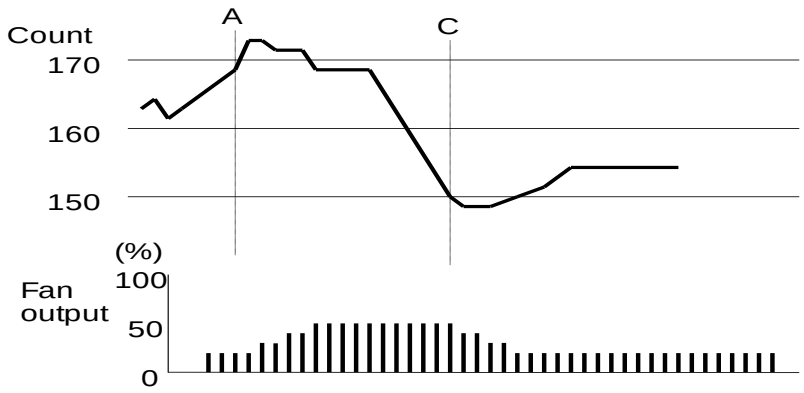


Figure 8-14 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Display Registers – at SMART FAN™ I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current SYSFANOUT Temperature	Bank0, Index18h, Index1Bh bit0	SYSFAN MUX Temperature Sensor (default: SYSTIN)	Read only	Index 18h, unit 1°C Index 1Bh, bit 0, unit 0.5 °C
Current CPUFANOUT Temperature	Bank0, Index19h, Index1Bh bit1	CPUFAN MUX Temperature Sensor (default: CPUTIN)	Read only	Index 19h, unit 1°C Index 1Bh, bit 1, unit 0.5 °C
Current AUXFANOUT Temperature	Bank0, Index1Ah, Index1Bh bit2	AUXFAN MUX Temperature Sensor (default: AUXTIN)	Read only	Index 1Ah, unit 1°C Index 1Bh, bit 2, unit 0.5 °C
Current AUXFANOUT1 Temperature	Bank0, IndexDBh, Index1Bh bit3	AUXFAN1 MUX Temperature Sensor (default: AUXTIN)	Read only	Index DBh, unit 1°C Index 1Bh, bit 3, unit 0.5 °C
Current AUXFANOUT2 Temperature	Bank0, IndexDCh, Index1Bh bit4	AUXFAN2 MUX Temperature Sensor (default: AUXTIN)	Read only	Index DCh, unit 1°C Index 1Bh, bit 4, unit 0.5 °C
Current SYSFANOUT Output Value	Bank0, Index 4Ah	SYSFANOUT Output Value Select	Read only	
Current CPUFANOUT Output Value	Bank0, Index 4Bh	CPUFANOUT Output Value Select	Read only	
Current AUXFANOUT Output Value	Bank0, Index 4Ch	AUXFANOUT Output Value Select	Read only	
Current	Bank0,	AUXFANOUT1 Output Value Select	Read only	

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
AUXFANOUT1 Output Value	Index D8h			
Current AUXFANOUT2 Output Value	Bank0, Index D9h	AUXFANOUT2 Output Value Select	Read only	

Table 8-3 Relative Registers – at Thermal Cruise™ Mode

THERMAL CRUISE MODE	CRITICAL TEMPERATURE	STEP- UP TIME	STEP- DOWN TIME	ENABLE THERMAL CRUISE MODE	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, Index 1Ah	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 01h	Bank 1, Index 1Ch, bit4	Bank 1, Index 1Dh
CPUFANOUT	Bank 1, Index 2Ah	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 01h	Bank 1, Index 2Ch, bit4	Bank 1, Index 2Dh
AUXFANOUT0	Bank 1, Index 3Ah	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 01h	Bank 1, Index 3Ch, bit4	Bank 1, Index 3Dh
AUXFANOUT1	Bank 1, Index 9Ah	Bank 1, Index 94h	Bank 1, Index 95h	Bank 1, Index 93h,bit[7:4] = 02h	Bank 1, Index 9Ch, bit4	Bank 1, Index 9Dh
AUXFANOUT2	Bank 1, Index Aah	Bank 1, Index A4h	Bank 1, Index A5h	Bank 1, Index A3h,bit[7:4] = 02h	Bank 1, Index Ach, bit4	Bank 1, Index Adh

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STOP VALUE	START-UP VALUE	STOP TIME
SYSFANOUT	Bank 1, Index 11h	Bank 1, Index 13h,Bit[2:0]	Bank 1, Index 10h, bit7	Bank 1, Index 16h	Bank 1, Index 17h	Bank 1, Index 18h
CPUFANOUT	Bank 1, Index 21h	Bank 1, Index 23h,Bit[2:0]	Bank 1, Index 20h, bit7	Bank 1, Index 26h	Bank 1, Index 27h	Bank 1, Index 28h
AUXFANOUT0	Bank 1, Index 31h	Bank 1, Index 33h,Bit[2:0]	Bank 1, Index 30h, bit7	Bank 1, Index 36h	Bank 1, Index 37h	Bank 1, Index 38h
AUXFANOUT1	Bank 1, Index 91h	Bank 1, Index 93h,Bit[2:0]	Bank 1, Index 90h, bit7	Bank 1, Index 96h	Bank 1, Index 97h	Bank 1, Index 98h

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STOP VALUE	START-UP VALUE	STOP TIME
AUXFANOUT2	Bank 1, Index A1h	Bank 1, Index A3h,Bit[2:0]	Bank 1, Index A0h, bit7	Bank 1, Index A6h	Bank 1, Index A7h	Bank 1, Index A8h

Table 8-4 Relative Registers – at Speed Cruise™ Mode

SPEED CRUISE MODE	STEP- UP TIME	STEP- DOWN TIME	ENABLE THERMAL CRUISE MODE	STEP UP VALUE	STEP DOWN VALUE
SYSFANOUT	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 02h	Bank 3, Index D8h, Bit[7:4]	Bank 3, Index D8h, Bit[3:0]
CPUFANOUT	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 02h	Bank 3, Index D9h, Bit[7:4]	Bank 3, Index D9h, Bit[3:0]
AUXFANOUT0	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 02h	Bank 3, Index Dah, Bit[7:4]	Bank 3, Index Dah, Bit[3:0]
AUXFANOUT1	Bank 1, Index 94h	Bank 1, Index 95h	Bank 1, Index 93h,bit[7:4] =02h	Bank 3, Index DBh, Bit[7:4]	Bank 3, Index DBh, Bit[3:0]
AUXFANOUT2	Bank 1, Index A4h	Bank 1, Index A5h	Bank 1, Index A3,bit[7:4] =02h	Bank 3, Index DCh, Bit[7:4]	Bank 3, Index DCh, Bit[3:0]

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE_H
SYSFANOUT	Bank 1, Index 11h	Bank 1, Index 12,bit[3:0]	Bank 1, Index 13h,Bit[2:0]	Bank 1, Index 12, bit[7:5]
CPUFANOUT	Bank 1, Index 21h	Bank 1, Index 22,bit[3:0]	Bank 1, Index 23h,Bit[2:0]	Bank 1, Index 22, bit[7:5]
AUXFANOUT0	Bank 1, Index 31h	Bank 1, Index 32,bit[3:0]	Bank 1, Index 33h,Bit[2:0]	Bank 1, Index 32, bit[7:5]
AUXFANOUT1	Bank 1, Index 91h	Bank 1, Index 92,bit[3:0]	Bank 1, Index 93h,Bit[2:0]	Bank 1, Index 92, bit[7:5]
AUXFANOUT2	Bank 1, Index A1h	Bank 1, Index A2,bit[3:0]	Bank 1, Index A3h,Bit[2:0]	Bank 1, Index A2, bit[7:5]

8.10 SMART FAN™ IV & Close Loop Fan Control RPM Mode

SMART FAN™ IV and Close Loop Fan Control RPM Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Address $1A_{HEX}$, Bank1 Address $2A_{HEX}$, Bank1 Address $3A_{HEX}$**

- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50 RPM. So the maximum controllable RPM is 50*255=12,750 rpm.
  If for High Speed Fan Control at RPM Mode, Set **RPM_High of Bank1 Address $1F_{HEX}$ bit[7]. Address $2F_{HEX}$ bit[7]. Address $3F_{HEX}$ bit[7].**
  The unit is 100 RPM, Support 100 rpm ~ 25500 rpm.
- Set **Hysteresis of Temperature, Bank1 Address 13_{HEX} bit[2:0] . Bank1 Address 23_{HEX} bit[2:0]. Bank1 Address 33_{HEX} bit[2:0]**.

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X2 = \frac{(FanDuty3/RPM3) - (FanDuty2/RPM2)}{(T3 - T2)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

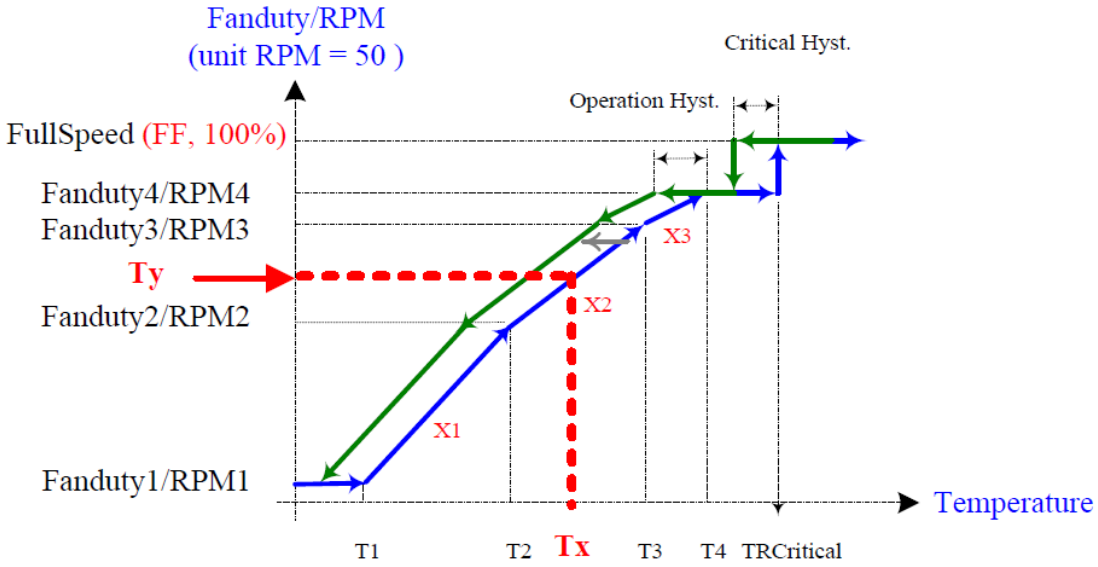


Figure 8-15 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-5 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 60h	Bank 1, Index 61h	Bank 1, Index 62h	Bank 1, Index 63h
CPUFANOUT	Bank 1, Index 70h	Bank 1, Index 71h	Bank 1, Index 72h	Bank 1, Index 73h
AUXFANOUT	Bank 1, Index 80h	Bank 1, Index 81h	Bank 1, Index 82h	Bank 1, Index 83h
AUXFANOUT1	Bank 1,	Bank 1,	Bank 1,	Bank 1,

DESCRIPTION	T1	T2	T3	T4
	Index D0h	Index D1h	Index D2h	Index D3h
AUXFANOUT2	Bank 1, Index E0h	Bank 1, Index E1h	Bank 1, Index E2h	Bank 1, Index E3h

DESCRIPTION	FD1/RPM1	FD2/RPM2	FD3/RPM3	FD4/RPM4
SYSFANOUT	Bank 1, Index 64h	Bank 1, Index 65h	Bank 1, Index 66h	Bank 1, Index 67h
CPUFANOUT	Bank 1, Index 74h	Bank 1, Index 75h	Bank 1, Index 76h	Bank 1, Index 77h
AUXFANOUT	Bank 1, Index 84h	Bank 1, Index 85h	Bank 1, Index 86h	Bank 1, Index 87h
AUXFANOUT1	Bank 1, Index D4h	Bank 1, Index D5h	Bank 1, Index D6h	Bank 1, Index D7h
AUXFANOUT2	Bank 1, Index E4h	Bank 1, Index E5h	Bank 1, Index E6h	Bank 1, Index E7h

DESCRIPTION	STEP- UP TIME	STEP-DOWN TIME	ENABLE SMART IV MODE	STEP UP VALUE	STEP DOWN VALUE	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, Index 14h	Bank 1, Index 15h	Bank 1, Index 13h,bit[7:4] = 04h	Bank 3, Index D8h, Bit[7:4]	Bank 3, Index D8h, Bit[3:0]	Bank 1, Index 1Ch, bit4	Bank 1, Index 1Dh
CPUFANOUT	Bank 1, Index 24h	Bank 1, Index 25h	Bank 1, Index 23h,bit[7:4] = 04h	Bank 3, Index D9h, Bit[7:4]	Bank 3, Index D9h, Bit[3:0]	Bank 1, Index 2Ch, bit4	Bank 1, Index 2Dh
AUXFANOUT	Bank 1, Index 34h	Bank 1, Index 35h	Bank 1, Index 33h,bit[7:4] = 04h	Bank 3, Index Dah, Bit[7:4]	Bank 3, Index Dah, Bit[3:0]	Bank 1, Index 3Ch, bit4	Bank 1, Index 3Dh
AUXFANOUT1	Bank 1, Index 94h	Bank 1, Index 95h	Bank 1, Index 93h,bit[7:4] = 04h	Bank 3, Index DBh, Bit[7:4]	Bank 3, Index DBh, Bit[3:0]	Bank 1, Index 9Ch, bit4	Bank 1, Index 9Dh
AUXFANOUT2	Bank 1, Index A4h	Bank 1, Index A5h	Bank 1, Index A3h,bit[7:4] = 04h	Bank 3, Index DCh, Bit[7:4]	Bank 3, Index DCh, Bit[3:0]	Bank 1, Index Ach, bit4	Bank 1, Index Adh

DESCRIPTION	CRITICAL TEMPERATURE	CRITICAL TOLERANCE	TEMPERATURE TOLERANCE	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 1Ah	Bank 1, Index 1Bh, bit[2:0]	Bank1, Index 13h, bit[2:0]	Bank 1, Index 1Eh, bit0	Bank1, Index 1Fh, bit[3:0]	Bank 1, Index 1Fh, bit7

CPUFANOUT	Bank 1, Index 2Ah	Bank 1, Index 2Bh, bit[2:0]	Bank1, Index 23h, bit[2:0]	Bank 1, Index 2Eh, bit0	Bank1, Index 2Fh, bit[3:0]	Bank 1, Index 2Fh, bit7
AUXFANOUT	Bank 1, Index 3Ah	Bank 1, Index 3Bh, bit[2:0]	Bank1, Index 33h, bit[2:0]	Bank 1, Index 3Eh, bit0	Bank1, Index 3Fh, bit[3:0]	Bank 1, Index 3Fh, bit7
AUXFANOUT1	Bank 1, Index 9Ah	Bank 1, Index 9Bh, bit[2:0]	Bank1, Index 93h, bit[2:0]	Bank 1, Index 9Eh, bit0	Bank1, Index 9Fh, bit[3:0]	Bank 1, Index 9Fh, bit7
AUXFANOUT2	Bank 1, Index Aah	Bank 1, Index Abh, bit[2:0]	Bank1, Index A3h, bit[2:0]	Bank 1, Index Aeh, bit0	Bank1, Index Afh, bit[3:0]	Bank 1, Index Afh, bit7

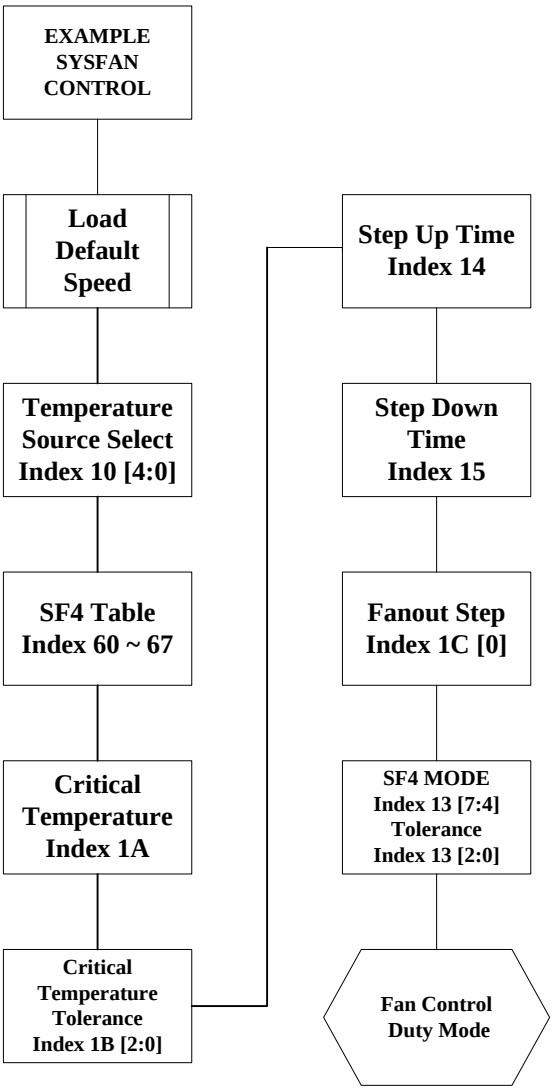


Figure 8-16 Fan Control Duty Mode Programming Flow

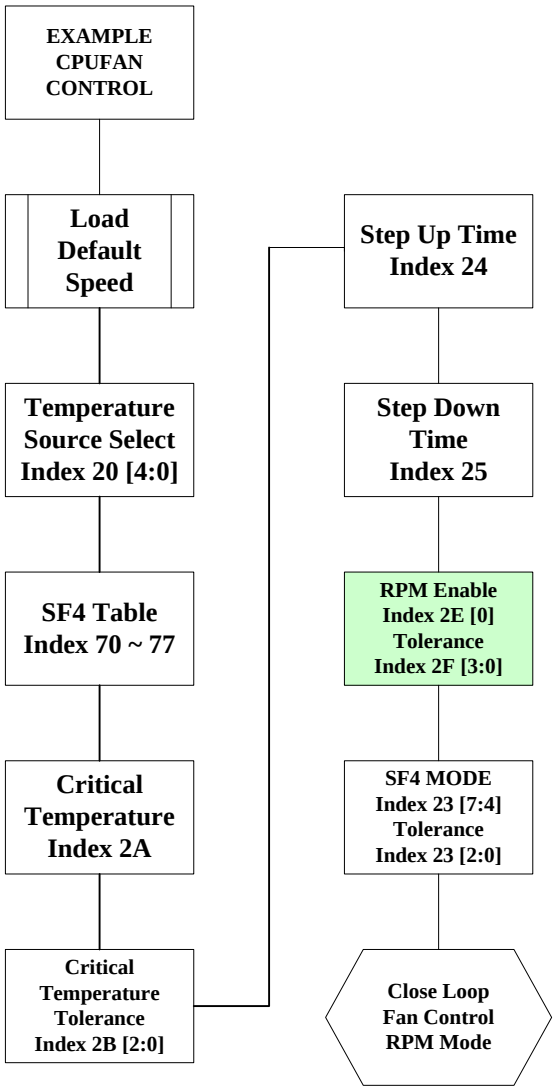


Figure 8-17 Close-Loop Fan Control RPM Mode Programming Flow

8.10.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed.
On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0, otherwise, the fan duty will be abnormal.

8.10.2 Fan Output Step

The “Fanout Step” itself is separately specified in Bank1 Index1Ch bit0 for SYSFANOUT, Index2Ch bit0 for CPUFANOUT and Index3Ch bit0 for AUXFANOUT.

This example for Fanout Step exposition:

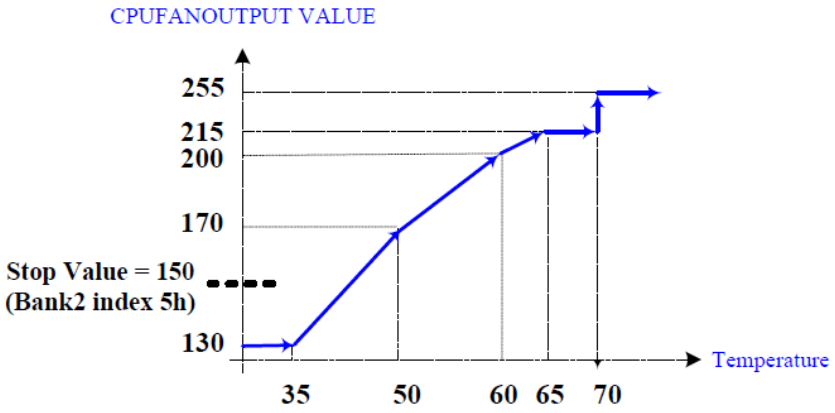


Figure 8-18 CPUFAN SMART FAN™ IV Table Parameters Figure

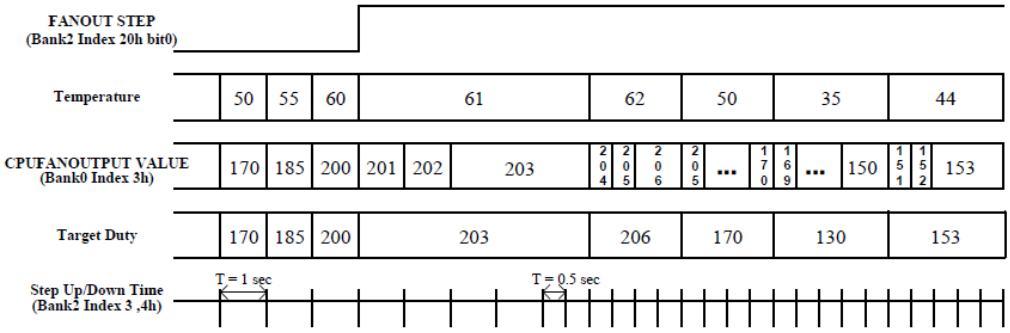


Figure 8-19 Fanout Step Relation of CPUFANOUT

8.10.3 Revolution Pulse Selection

The NCT6122D / NCT6126D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution. The others could be set by HM register at Bank0, IndexF6, Bit1-0 for SYSFANIN; Bank0, IndexF6, Bit3-2 for CPUFANIN and Bank0, IndexF6, Bit5-4 for AUXFANIN, IndexF6, Bit7-6 for AUXFANIN1 and IndexF5, Bit7-6 for AUXFANIN2. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selections Bits”:

00: 4 pulses per revolution
01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.10.4 Weight Value Control

The NCT6122D / NCT6126D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of Thermal Cruise Mode or SMART FAN™ IV Duty Mode and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

Figure 8-21 SYS TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

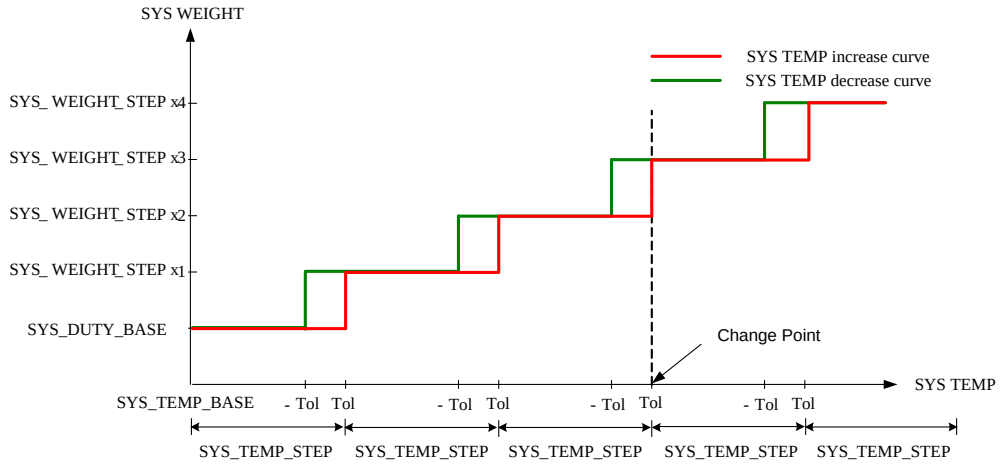


Figure 8-20 SYS TEMP and Weight Value Relations

Table 8-6 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
SYSFANOUT	Bank 1, Index 68h, bit7	Bank 1, Index 68h, bit[4:0]
CPUFANOUT	Bank 1, Index 78h, bit7	Bank 1, Index 78h, bit[4:0]
AUXFANOUT0	Bank 1, Index 88h, bit7	Bank 1, Index 88h, bit[4:0]

DESCRIPTION	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP	TEMP BASE	DUTY BASE
SYSFANOUT	Bank 1, Index 69h	Bank 1, Index 6Ah	Bank 1, Index 6Bh	Bank 1, Index 6Ch	Bank 1, Index 6Dh
CPUFANOUT	Bank 1, Index 79h	Bank 1, Index 7Ah	Bank 1, Index 7Bh	Bank 1, Index 7Ch	Bank 1, Index 7Dh
AUXFANOUT0	Bank 1, Index 89h	Bank 1, Index 8Ah	Bank 1, Index 8Bh	Bank 1, Index 8Ch	Bank 1, Index 8Dh

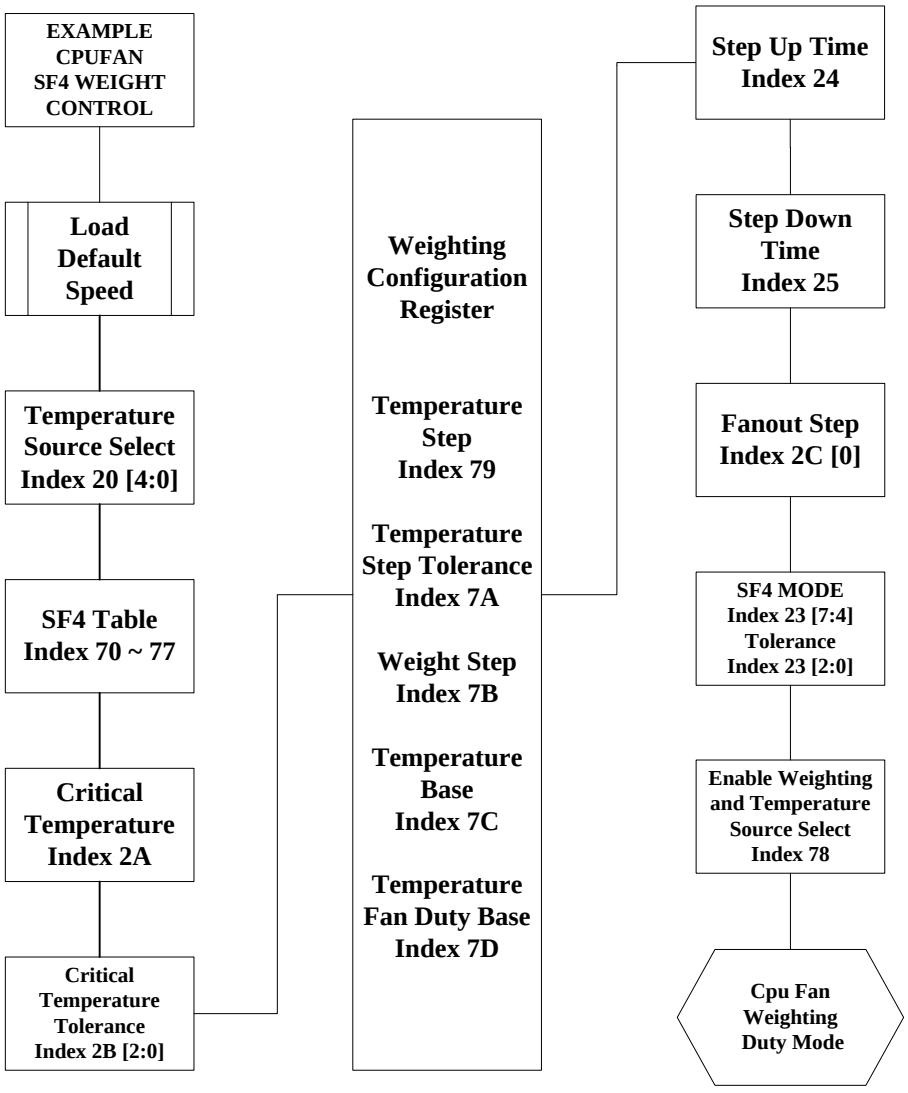


Figure 8-21 Weighting Duty Mode Programming Flow

8.10.5 Max Duty Compare Source

The NCT6126D supports the max duty compare source. The function can be enabled by selected one of the bit in Index BAh bit[7:4], Index BBh, Index BCh of Bank 3. When the function is enabled, the fan will compare the duty and the fan will output the max duty.

DESCRIPTION	Bank	Bit7/Bit3	Bit6/Bit2	Bit5/Bit1	Bit4/Bit0
SYSFANOUT	Bank 3, Index BBh, bit[3:0]	AUXFAN2	AUXFAN1	AUXFAN0	CPUFAN
CPUFANOUT	Bank 3, Index BBh, bit[7:4]	AUXFAN2	AUXFAN1	AUXFAN0	SYSFAN
AUXFANOUT0	Bank 3, Index BCh, bit[3:0]	AUXFAN2	AUXFAN1	CPUFAN	SYSFAN
AUXFANOUT1	Bank 3, Index BCh, bit[7:4]	AUXFAN2	AUXFAN0	CPUFAN	SYSFAN
AUXFANOUT2	Bank 3, Index BAh, bit[7:4]	AUXFAN1	AUXFAN0	CPUFAN	SYSFAN

8.11 Alert and Interrupt

NCT6122D / NCT6126D supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2	SMIOVT3
Temperature source select	Bank 0, IndexB0h bit[4:0] default: SYSTIN	Bank 0 IndexB1h bit[4:0] default: CPUTIN	Bank 0, IndexB2h bit[4:0] default: AUXTIN
Temperature reading (2's complement)	Bank 0, Index 10h & Index 16h bit0	Bank 0, Index 11h & Index 16h bit1	Bank 0, Index 12h & Index 16h bit2
Temperature High Limit	Bank0, IndexC2h & Index B7h bit6	Bank0, Index C6h & Index B8h bit6	Bank 0, Index CAh & Index B9h bit6
Temperature Low Limit	Bank0, IndexC3h & Index B7h bit7	Bank 1, IndexC7h & Index B8h bit7	Bank 2, Index CBh & Index B9h bit7

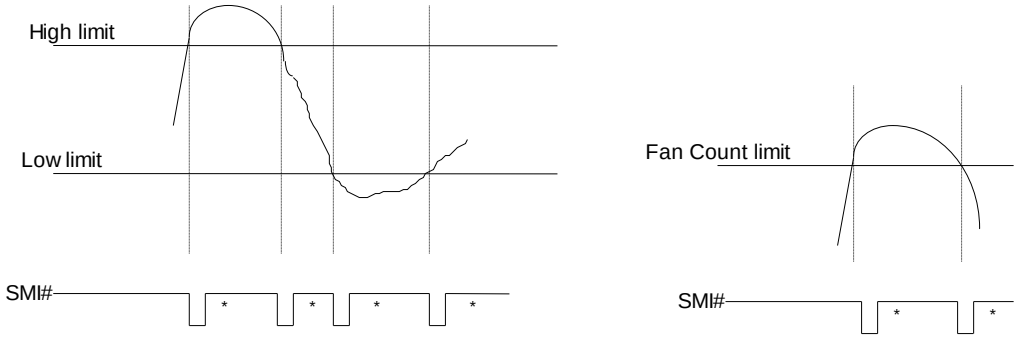
SMIOVT Relative Temperature Registers

8.11.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin95) is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register Logical Device E, CR FA, bit6 and CR1Dh, bit [3:2]. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.11.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-22 SMI Mode of Voltage and Fan Inputs

8.11.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.11.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

8.11.4.1. Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

The SMI# pin has five interrupt modes with Temperature Sensor 1.

(1) Shut-down Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_{OL} and setting Bank0 Index 40h, bit 4 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

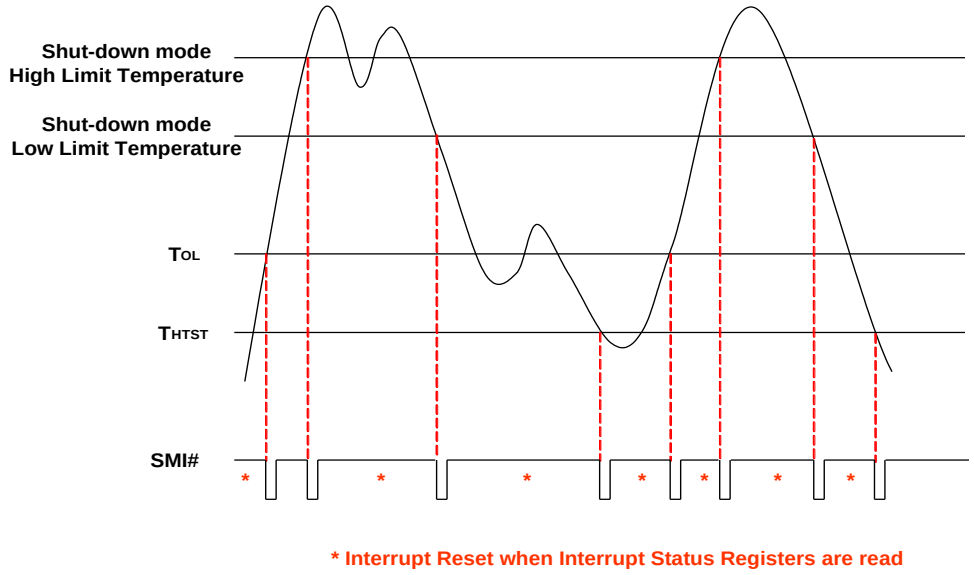
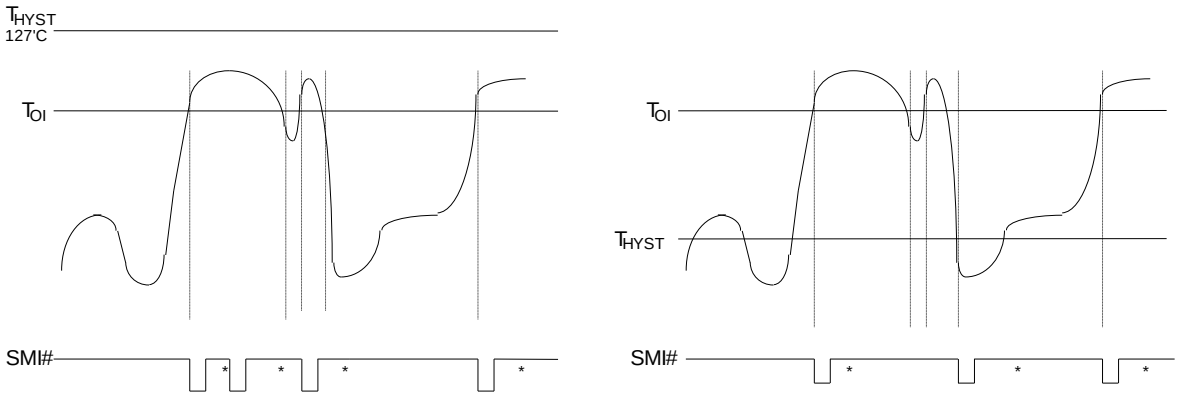


Figure 8-23 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-24 SMI Mode of SYSTIN I

(3) Two-Times Interrupt Mode

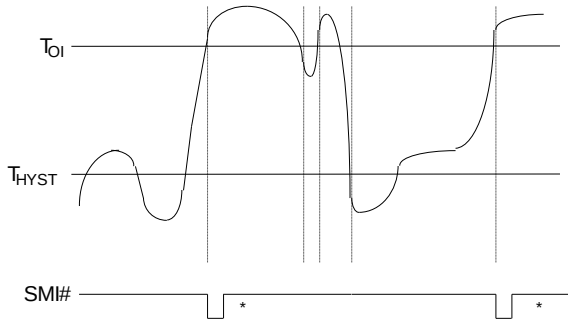
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index B6h, bit1 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(1) **One-Time Interrupt Mode**

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index B6h, bit1 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-25 SMI Mode of SYSTIN II

8.11.4.2. SMI# Interrupt of Temperature Sensor 2 (Default: CPUTIN) and Temperature Sensor 3 (Default: AUXTIN)

The SMI# pin has 5 interrupt modes with Temperature Sensor 2~3.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2 to zero and Bank0 Index B8h, bit2 to one for Temperature Sensor 2; Bank0 Index B9h, bit2 to one for Temperature Sensor 3; Bank0 Index Bah, bit2 to one for Temperature Sensor 4; Bank0 Index BBh, bit2 to one for Temperature Sensor 5 and Bank0 Index BCh, bit2 to one for Temperature Sensor 6.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

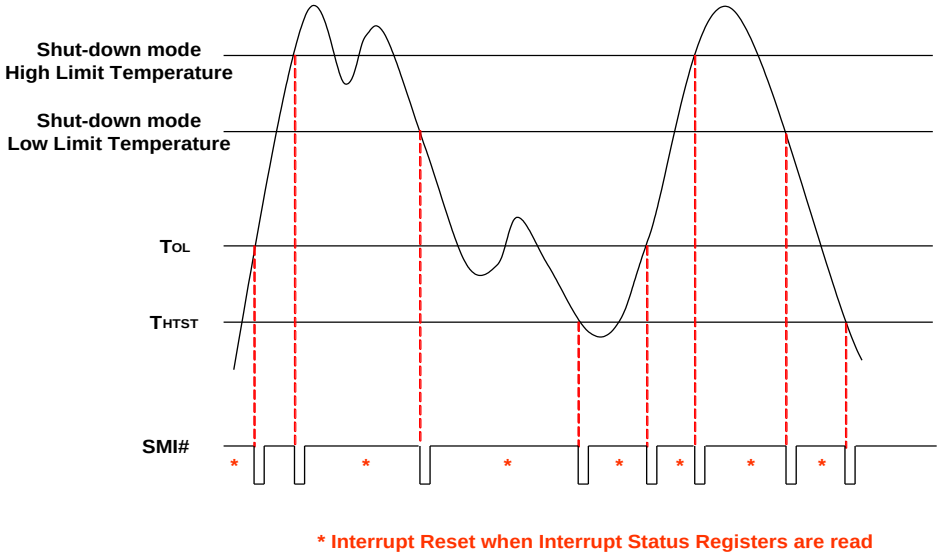
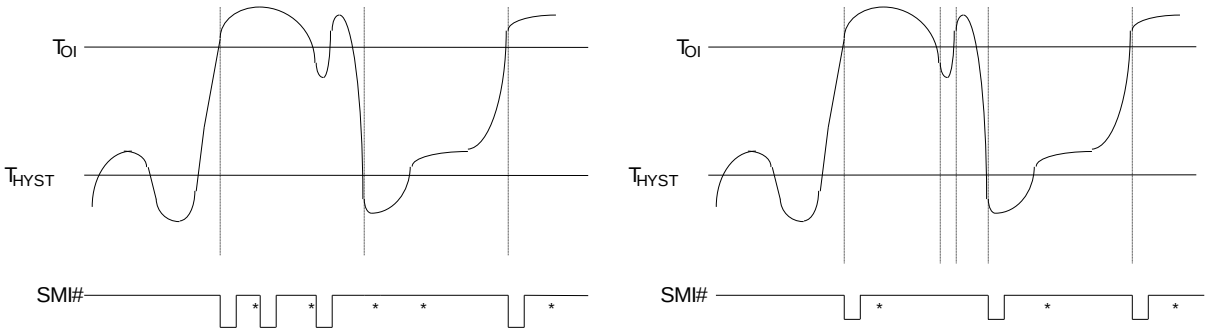


Figure 8-26 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-27 SMI Mode of CPUTIN

(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index B6h, bit 2, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-7 Relative Register of SMI functions

	SHUTDOWN MODE	COMPARATOR MODE	TWO-TIME INTERRUPT MODE	ONE-TIME INTERRUPT MODE
SMIOVT1	Bank0,IndexB7_Bit2 (EN_WS=1) Bank0,Index82 _Bit0(TIN=0) Bank0,Index83 _Bit0 (Shut = 0)	Bank0,Index82_Bit0 (TIN=0) Bank0,IndexC3 (Thyst = 8'h7F)	Bank0,Index82_Bit0 (TIN=0) Bank0,IndexB6_Bit1 (EN_T1_One = 0)	Bank0,Index82_ Bit0 (TIN=0) Bank0,IndexB6_ Bit1 (EN_T1_One= 1)
SMIOVT2	Bank0,IndexB8_Bit2 (EN_WS=1) Bank0,Index82_ Bit1(TIN=0) Bank0,Index83_ Bit1 (Shut = 0)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	
SMIOVT3	Bank0,IndexB9_Bit2 (EN_WS=1) Bank0,Index82_ Bit2(TIN=0) Bank0,Index83_ Bit2 (Shut = 0)	Bank0,Index82_Bit2 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=1)	Bank0,Index82_Bit1 (TIN=0) Bank0,IndexB6_ Bit2 (T2T3_INT=0)	

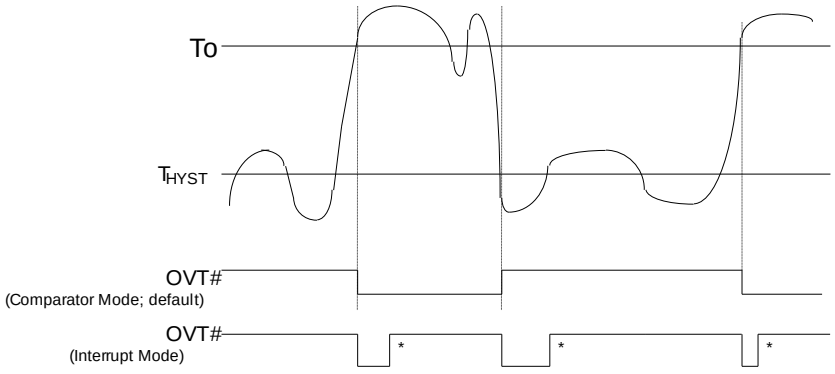
Table 8-8 Relative Register of OVT functions

SMIOVT1	SMIOVT2	SMIOVT3
Bank0, IndexB7_Bit0 **0:** Start to monitor the source of SMIOVT1 temperature. **1:** Stop to monitor the source of SMIOVT1 temperature. **Bank 0, IndexB7_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB7_Bit 3** **0:** Enable SMIOVT1 temperature sensor over temperature output **1:** Disable SMIOVT1 temperature sensor over temperature output	**Bank0, IndexB8_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature. **1:** Stop to monitor the source of SMIOVT2 temperature. **Bank 0, IndexB8_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB8_Bit 3** **0:** Enable SMIOVT2 temperature sensor over temperature output **1:** Disable SMIOVT2 temperature sensor over temperature output	**Bank0, IndexB9_Bit0** **0:** Start to monitor the source of SMIOVT3 temperature. **1:** Stop to monitor the source of SMIOVT3 temperature. **Bank 0, IndexB9_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 0, InedexB9_Bit 3** **0:** Enable SMIOVT3 temperature sensor over temperature output **1:** Disable SMIOVT3 temperature sensor over temperature output

8.11.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register Logical Device E, CR FA, bit6 and CR1Dh, bit [3:2]. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index B7h, bit 3 for Temperature Sensor 1(default: SYSTIN); Bank0 Index B8h, bit 3 for Temperature Sensor 2(default: CPUTIN); Bank0 Index B9h, bit3 for Temperature Sensor 3(default: AUXTIN).

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.



*Interrupt Reset when Temperature sensor registers are read

Figure 8-28 OVT# Modes of Temperature Inputs

If Bank0 Index B7h, bit 1, is set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the

temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index B7h, bit 1, is set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.11.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 74 (VBAT) or Pin 61 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN# (pin 76) must be pulled high by an externally pulled-up 2MΩ resistor that is connected to VBAT (pin 74). When the case is opened, CASEOPEN# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The CASEOPEN# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to “1” first and then to “0”.

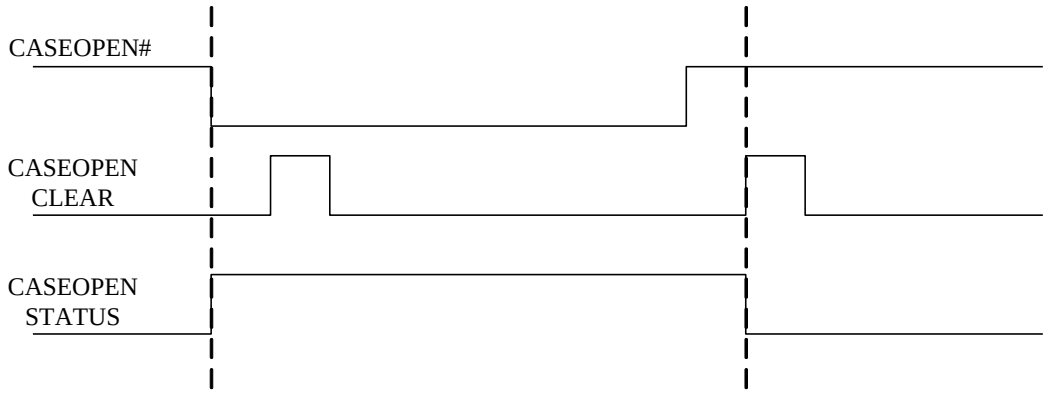


Figure 8-29 Caseopen Mechanism

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Index 04Eh. Indexes from 000h to 04Fh are “global” or accessible from all banks, while indexes 050h to 0FFh are specific to each bank.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6-0	READ/WRITE.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 Value RAM — Index 00h ~ 6Fh (Bank 0)

ADDRESS 00-6F	DESCRIPTION
00h	CPUVCORE reading
01h	VIN0 reading
02h	AVSB reading
03h	3VCC reading
04h	VIN1 reading
05h	VIN2 reading
06h	VHIF reading
07h	3VSB reading.
08h	VBAT reading
09h	VTT reading
0Ah	Reserved
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Reserved
0Fh	Reserved
10h	SMIOVT1 temperature reading
11h	SMIOVT2 temperature reading
12h	SMIOVT3 temperature reading
16h	SMIOVT1~3 temperature reading LSB
17h	Reserved
18h	System fan control temperature reading
19h	CPU fan control temperature reading
1Ah	AUX fan0 control temperature reading
1Bh	Fan control temperature reading LSB
1Ch	System fan weighting temperature reading
1Dh	CPU fan weighting temperature reading
1Eh	AUX fan0 weighting temperature reading
1Fh	fan weighting temperature reading LSB
20h	SYS fan count reading [12:5]
21h	SYS fan count reading [4:0]
22h	CPU fan count reading [12:5]
23h	CPU fan count reading [4:0]
24h	AUX fan0 count reading [12:5]

ADDRESS 00-6F	DESCRIPTION
25h	AUX fan0 count reading [4:0]
26h	AUX fan1 count reading [12:5]
27h	AUX fan1 count reading [4:0]
28h	AUX fan2 count reading [12:5]
29h	AUX fan2 count reading [4:0]
2Ah	SYS fan target
2Bh	CPU fan target
2Ch	AUX fan0 target
2Dh	AUX fan1 target
2Eh	AUX fan2 target
2Fh	Reserved
30h	System fan RPM value reading high byte
31h	System fan RPM value reading low byte
32h	CPU fan RPM value reading high byte
33h	CPU fan RPM value reading low byte
34h	AUX fan0 RPM value reading high byte
35h	AUX fan0 RPM value reading low byte
36h	AUX fan1 RPM value reading high byte
37h	AUX fan1 RPM value reading low byte
38h	AUX fan2 RPM value reading high byte
39h	AUX fan2 RPM value reading low byte
3Ah	System FANIN RPM target (unit is 50 RPM)
3Bh	CPU FANIN RPM target (unit is 50 RPM)
3Ch	AUX FANIN0 RPM target (unit is 50 RPM)
3Dh	AUX FANIN1 RPM target (unit is 50 RPM)
3Eh	AUX FANIN2 RPM target (unit is 50 RPM)
3Fh	Reserved
40h	Reserved
41h	Reserved
42h	Reserved
43h	Reserved
44h	Reserved
45h	Reserved
46h	Port 80 data [7:0] input
47h	Port 80 data [15:8] input
48h	Port 80 data [23:16] input
49h	Port 80 data [31:24] input

ADDRESS 00-6F	DESCRIPTION
4Ah	System fan duty
4Bh	CPU fan duty
4Ch	AUX fan0 duty
4Dh	Reserved
4Eh	Bank select register
4Fh	Reserved
50h	PCH_CHIP_CPU_MAX_Temperature
51h	PCH_CHIP_Temperature
52h	PCH_CPU_TEMP_H
53h	PCH_CPU_TEMP_L
54h	PCH_MCH_TEMP
55h	PCH_DIM0_TEMP
56h	PCH_DIM1_TEMP
57h	PCH_DIM2_TEMP
58h	PCH_DIM3_TEMP
59h	TSI Agent 0 temperature high byte
5Ah	TSI Agent 0 temperature low byte
5Bh	TSI Agent 1 temperature high byte
5Ch	TSI Agent 1 temperature low byte
69h	Byte Temperature high byte
6Ah	Byte Temperature low byte
6Bh	Reserved
6Ch	Reserved
6Dh	Reserved
6Eh	Reserved
6Fh	Reserved

9.4 SMIOVT1 Temperature Source (High Byte) Register – Index 10h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.5 SMIOVT2 Temperature Source (High Byte) Register – Index 11h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.6 SMIOVT3 Temperature Source (High Byte) Register – Index 12h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.7 SMIOVT1-3 Temperature Source (Low Byte) Register – Index 16h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SMIOVT3_ TEMP<0>	SMIOVT2_ TEMP<0>	SMIOVT1_ TEMP<0>

BIT	DESCRIPTION
7-3	Reserved.
2	**SMIOVT3 Temperature <0> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5˚C.
1	**SMIOVT2 Temperature <0> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5˚C.
0	**SMIOVT1 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5˚C.

9.8 System Fan Control Temperature Register (Integer Value)- Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	SYSFANControlTemp [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANControlTemp [8:1]** SYSFANOUT fan control temperature reading.

9.9 CPU Fan Control Temperature Register (Integer Value)- Index 19h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANControlTemp [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANControlTemp [8:1]** CPUFANOUT fan control temperature reading.

9.10 AUX Fan0 Control Temperature Register (Integer Value)- Index 1Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0ControlTemp [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFAN0ControlTemp [8:1]** AUXFANOUT0 fan control temperature reading.

9.11 Fan Temperature Register (Fractional Value)- Index 1Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7-5	4	3	2	1	0
NAME	Reserved	AUXFAN2 ControlTemp[0]	AUXFAN1 ControlTemp[0]	AUXFAN0 ControlTemp[0]	CPUFAN ControlTemp[0]	SYSFAN ControlTemp[0]
DEFAULT	0	0	0	0	0	0

BIT	DESCRIPTION

7-5	Reserved.
4	**AUXFAN2ControlTemp[0]** AUXFANOUT2 fan control temperature reading
3	**AUXFAN1ControlTemp[0]** AUXFANOUT1 fan control temperature reading
2	**AUXFAN0ControlTemp[0]** AUXFANOUT0 fan control temperature reading
1	**CPUFANControlTemp[0]** CPUFANOUT fan control temperature reading
0	**SYSFANControlTemp[0]** SYSFANOUT fan control temperature reading

9.12 (SYSFANIN) FANIN1 COUNT High-byte Register – Index 20h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT1_H:** 13-bit SYSFANIN Fan Count, High Byte

9.13 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index 21h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				
DEFAULT	0			**0**				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANCNT1_L:** 13-bit SYSFANIN Fan Count, Low Byte

9.14 (CPUFANIN) FANIN2 COUNT High-byte Register – Index 22h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT2_H:** 13-bit CPUFANIN Fan Count, High Byte

9.15 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index 23h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANCNT2[4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANCNT2_L:** 13-bit CPUFANIN Fan Count, Low Byte

9.16 (AUXFANIN0) FANIN3 COUNT High-byte Register – Index 24h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT3 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT3_H:** 13-bit AUXFANIN Fan Count, High Byte

9.17 (AUXFANIN0) FANIN3 COUNT Low-byte Register – Index 25h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANCNT3 [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANCNT3_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.18 (AUXFANIN1) FANIN4 COUNT High-byte Register – Index 26h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT4 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT4_H:** 13-bit AUXFANIN1 Fan Count, High Byte

9.19 (AUXFANIN1) FANIN4 COUNT Low-byte Register – Index 27h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANCNT4 [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANCNT4_L:** 13-bit AUXFANIN1 Fan Count, Low Byte

9.20 (AUXFANIN2) FANIN5 COUNT High-byte Register – Index 28h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT5 [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANCNT5_H:** 13-bit AUXFANIN2 Fan Count, High Byte

9.21 (AUXFANIN2) FANIN5 COUNT Low-byte Register – Index 29h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANCNT5 [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT5_L:** 13-bit AUXFANIN2 Fan Count, Low Byte

9.22 (SYSFANIN) FANIN1 SYSFAN Duty Target Register – Index 2Ah (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN duty target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	SYSFAN duty target

9.23 (CPUFANIN) FANIN2 CPUFAN Duty Target Register – Index 2Bh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN duty target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	CPUFAN duty target

9.24 (AUXFANIN0) FANIN3 AUXFAN0 Duty Target Register – Index 2Ch (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 duty target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN0 duty target

9.25 (AUXFANIN1) FANIN4 AUXFAN1 Duty Target Register – Index 2Dh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 duty target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN1 duty target

9.26 (AUXFANIN2) FANIN4 AUXFAN2 Duty Target Register – Index 2Eh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 duty target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN2 duty target

9.27 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 30h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFANIN SPEED HIGH-BYTE VALUE.

9.28 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 31h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFANIN SPEED LOW-BYTE VALUE.

9.29 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 32h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED HIGH-BYTE VALUE.

9.30 CPUFANIN SPEED LOW-BYTE VALUE (RPM) - Index 33h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED LOW-BYTE VALUE.

9.31 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) - Index 34h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN0 SPEED HIGH-BYTE VALUE.

9.32 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) - Index 35h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN0 SPEED LOW-BYTE VALUE.

9.33 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) - Index 36h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH-BYTE VALUE							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN1 SPEED HIGH-BYTE VALUE.

9.34 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) - Index 37h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN1 SPEED LOW-BYTE VALUE.

9.35 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) - Index 38h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN2 SPEED HIGH-BYTE VALUE.

9.36 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) - Index 39h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN2 SPEED LOW-BYTE VALUE.

9.37 (FANIN) FANIN1 SYSFAN RPM Target Register – Index 3Ah (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	SYSFAN RPM target
DEFAULT	8'h00

BIT	DESCRIPTION
7-0	SYSFAN RPM target

9.38 (FANIN) FANIN2 CPUFAN RPM Target Register – Index 3Bh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN RPM target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	CPUFAN RPM target

9.39 (FANIN) FANIN3 AUXFAN0 RPM Target Register – Index 3Ch (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 RPM target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN0 RPM target

9.40 (FANIN) FANIN4 AUXFAN1 RPM Target Register – Index 3Dh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 RPM target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN1 RPM target

9.41 (FANIN) FANIN5 AUXFAN2 RPM Target Register – Index 3Eh (Bank 0)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 RPM target							
DEFAULT	8'h00							

BIT	DESCRIPTION
7-0	AUXFAN2 RPM target

9.42 PORT 80 DATA INPUT Register 1 – Index 46h (Bank 0)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Port 80 Data Input							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Port 80 Data [7:0] Input

9.43 PORT 80 DATA INPUT Register 2 – Index 47h (Bank 0)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Port 80 Data Input							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Port 80 Data [15:8] Input for eSPI mode

9.44 PORT 80 DATA INPUT Register 3 – Index 48h (Bank 0)

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Port 80 Data Input							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Port 80 Data [23:16] Input for eSPI mode

9.45 PORT 80 DATA INPUT Register 4 – Index 49h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Port 80 Data Input							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Port 80 Data [31:24] Input for eSPI mode

9.46 SYSFAN Max Duty Output Register – Index 4Ah (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	SYSFAN Max Duty Output

9.47 CPUFAN Max Duty Output Register – Index 4Bh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	CPUFAN Max Duty Output

9.48 AUXFAN0 Max Duty Output Register – Index 4Ch (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	AUXFAN0 Max Duty Output

9.49 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved					BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6-2	Reserved.	
1	**BANKSEL1.**	Bank Select for Bank0 to Bank3. The Two –bit binary value corresponds to the bank number. For example, “01” selects bank1.
0	**BANKSEL0.**	

9.50 PCH_CHIP_CPU_MAX_TEMP Register – Index 50h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_CPU_MAX_TEMP:** The maximum temperature in absolute degree C, of the CPU and MCH.

9.51 PCH_CHIP_TEMP Register – Index 51h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_TEMP** The IBX_CHIP temperature in degree C.

9.52 PCH_CPU_TEMP_H Register – Index 52h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CPU_TEMP_H** The CPU temperature in degree C. (Integer Part)

9.53 PCH_CPU_TEMP_L Register – Index 53h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading _Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**PCH_CPU_TEMP_L** The CPU temperature in degree C. (Fractional Part)
1	Reserved.
0	**Reading_Flag:** If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.

9.54 PCH_MCH_TEMP Register – Index 54h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_MCH_TEMP** The MCH temperature in degree C.

9.55 PCH_TSI0_TEMP_H Register – Index 59h (Bank 0)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI0_TEMP_H** The TSI0 High-Byte temperature in degree C. (Integer Part)

9.56 PCH_TSI0_TEMP_L Register – Index 5Ah (Bank 0)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI0_TEMP_L** The TSI0 Low-Byte temperature in degree C. (Fractional Part)
4-0	Reserved.

9.57 PCH_TSI1_TEMP_H Register – Index 5Bh (Bank 0)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI1_TEMP_H** The TSI1 High-Byte temperature in degree C. (Integer Part)

9.58 PCH_TSI1_TEMP_L Register – Index 5Ch (Bank 0)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI1_TEMP_L** The TSI1 Low-Byte temperature in degree C. (Fractional Part)
4-0	Reserved.

9.59 ByteTemp_H Register – Index 69h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7		6	5	4	3	2	1	0
NAME		ByteTemp_H							
DEFAULT	0		0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_H** The Byte format Device0 Byte temperature in degree C.

9.60 ByteTemp_L Register – Index 6Ah (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_L** The Byte format Device1 Byte temperature in degree C.

9.61 PECI Agent0 Temp Register – Index 6Bh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Agent0 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PECI Agent0 Temp** The PECI Agent0 temperature in degree C.

9.62 PECI Agent1 Temp Register – Index 6Dh (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Agent1 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**PECI Agen1 Temp** The PECI Agent1 temperature in degree C.

9.63 Interrupt Status Register 1 – Index 70h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB	VHIF	VIN2	VIN1	3VCC	AVSB	VIN0	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.
6	**VHIF.** A one indicates the high or low limit of VHIF has been exceeded
5	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded
4	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVSB.** A one indicates the high or low limit of AVSB has been exceeded.
1	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.64 Interrupt Status Register 2 – Index 71h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						VTT	VBAT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	Reserved.
1	**VTT.** A one indicates the high or low limit of VTT has been exceeded.
0	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.

9.65 Interrupt Status Register 3 – Index 72h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	SOURCE3_SMI	SOURCE2_SMI	SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**SOURCE3_SMI.** A one indicates the high limit of SMIOVT SOURCE3 temperature has been exceeded. (AUXTIN is default temperature)
1	**SOURCE2_SMI.** A one indicates the high limit of SMIOVT SOURCE2 temperature has been exceeded. (CPUTIN is default temperature)
0	**SOURCE1_SMI.** A one indicates the high limit of SMIOVT SOURCE1 temperature has been exceeded. (SYSTIN is default temperature)

9.66 Interrupt Status Register 4 – Index 73h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Shut_SOURCE3_SMI	Shut_SOURCE2_SMI	Shut_SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**Shut_SOURCE3_SMI.** "1" indicates the high limit of SMIOVT _SOURCE3 temperature of SMI# Shut-down mode has been exceeded. (AUXTIN is default temperature)
1	**Shut_SOURCE2_SMI.** "1" indicates the high limit of SMIOVT _SOURCE2 temperature of SMI# Shut-down mode has been exceeded. (CPUTIN is default temperature)
0	**Shut_SOURCE1_SMI.** "1" indicates the high limit of SMIOVT _SOURCE1 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)

9.67 Interrupt Status Register 5 – Index 74h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	AUXFANIN2	AUXFANIN1	AUXFANIN0	CPUFANIN	SYSFANIN

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	**AUXFANIN2.** A one indicates the fan count limit of AUXFANIN2 has been exceeded.
3	**AUXFANIN1.** A one indicates the fan count limit of AUXFANIN1 has been exceeded.
2	**AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
1	**CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
0	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.

9.68 Interrupt Status Register 6 – Index 75h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**AUX FANOUT0**	**CPU FANOUT**	**SYS FANOUT**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	**AUXFANOUT0.** “1” indicates that AUXFANOUT works for three minutes at the full fan speed.
1	**CPUFANOUT.** “1” indicates that CPUFANOUT works for three minutes at the full fan speed.
0	**SYSFANOUT.** “1” indicates that SYSFANOUT works for three minutes at the full fan speed.

9.69 Interrupt Status Register 7 – Index 76h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**CASEOPEN1**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	Reserved.
1	Reserved.
0	**CASEOPEN1.** A one indicates the case has been opened. 1: Caseopen is detected and latched. 0: Caseopen is not latched.

9.70 Real Time Status Register 1 – Index 77h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB _STS	VHIF _STS	VIN2 _STS	VIN1 _STS	3VCC _STS	AVSB _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**3VSB_STS.** 1: 3VSB voltage is over or under the allowed range. 0: 3VSB voltage is in the allowed range.
6	**VHIF_STS.** 1: VHIF voltage is over or under the allowed range. 0: VHIF voltage is in the allowed range.
5	**VIN2_STS.** 1: VIN2 voltage is over or under the allowed range. 0: VIN2 voltage is in the allowed range.
4	**VIN1_STS.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.
3	**3VCC_STS.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVSB_STS.** 1: AVSB voltage is over or under the allowed range. 0: AVSB voltage is in the allowed range.
1	**VIN0_STS.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.

BIT	DESCRIPTION
0	**CPUVCORE_STS.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.71 Real Time Status Register 2 – Index 78h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**VTT _STS**	**VBAT _STS**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	Reserved.
1	**VTT_STS.** 1: VTT voltage is over or under the allowed range. 0: VTT voltage is in the allowed range.
0	**VBAT_STS.** 1: VBAT voltage is over or under the allowed range. 0: VBAT voltage is in the allowed range.

9.72 Real Time Status Register 3 – Index 79h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**SMIOVT3 _STS**	**SMIOVT2 _STS**	**SMIOVT1 _STS**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**SMIOVT3_STS.** 1: SMIOVT3 Temperature exceeds the over-temperature value. 0: SMIOVT3 Temperature is under the hysteresis value.
1	**SMIOVT2_STS.**

BIT	DESCRIPTION
	1: SMIOVT2 Temperature exceeds the over-temperature value. 0: SMIOVT2 Temperature is under the hysteresis value.
0	**SMIOVT1_STS.** 1: SMIOVT1 Temperature exceeds the over-temperature value. 0: SMIOVT1 Temperature is under the hysteresis value.

9.73 Real Time Status Register 4 – Index 7Ah (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Shut_ SMIOVT3 _STS**	**Shut_ SMIOVT2 _STS**	**Shut_ SMIOVT1 _STS**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**Shut_SMIOVT3_STS.** 1: SMIOVT3 Temperature exceeds the Shut –temperature value. 0: SMIOVT3 Temperature is under the Shut-hysteresis value.
1	**Shut_SMIOVT2_STS.** 1: SMIOVT2 Temperature exceeds the Shut –temperature value. 0: SMIOVT2 Temperature is under the Shut-hysteresis value.
0	**Shut_SMIOVT1_STS.** 1: SMIOVT1 Temperature exceeds the Shut –temperature value. 0: SMIOVT1 Temperature is under the Shut-hysteresis value.

9.74 Real Time Status Register 5 – Index 7Bh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**AUX FANIN2 _STS**	**AUX FANIN1 _STS**	**AUX FANIN0 _STS**	**CPU FANIN _STS**	**SYS FANIN _STS**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	**AUXFANIN2_STS.**

BIT	DESCRIPTION
	1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
3	**AUXFANIN1_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	**AUXFANIN0_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CPUFANIN_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
0	**SYSFANIN_STS.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.

9.75 Real Time Status Register 6 – Index 7Ch (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**AUX FANOUT0 _STS**	**CPU FANOUT _STS**	**SYS FANOUT _STS**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	**AUXFANOUT0_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
1	**CPUFANOUT_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
0	**SYSFANOUT_STS.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.

9.76 Real Time Status Register 7 – Index 7Dh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Caseopen_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	Reserved.
1	Reserved.
0	**CASEOPEN_PIN_STATUS.**

9.77 Reserved Register – Index 7Eh ~ 7Fh (Bank 0)

9.78 SMI# Mask Register 1 – Index 80h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB	Reserved	VIN2	VIN1	3VCC	AVSB	VIN0	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**3VSB.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 70h (Bank0))
6	Reserved.	
5	**VIN2.**	
4	**VIN1.**	
3	**3VCC.**	
2	**AVSB.**	
1	**VIN0.**	
0	**CPUVCORE.**	

9.79 SMI# Mask Register 2 – Index 81h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**VTT**	**VBAT**
DEFAULT	0	0	0	0	1	1	1	1

BIT	DESCRIPTION	
7	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 2 – Index 71h (Bank0))
6	Reserved.	
5	Reserved.	
4	Reserved.	
3	Reserved.	
2	Reserved.	
1	**VTT.**	
0	**VBAT.**	

9.80 SMI# Mask Register 3 – Index 82h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**SMIOVT3**	**SMIOVT2**	**SMIOVT1**
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7-3	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 3 – Index 72h (Bank0))
2	**SMIOVT3.**	
1	**SMIOVT2.**	
0	**SMIOVT1.**	

9.81 SMI# Mask Register 4 – Index 83h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Shut_ SMIOVT3**	**Shut_ SMIOVT2**	**Shut_ SMIOVT1**
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7-3	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 4 – Index 73h (Bank0))
2	**Shut_SMIOVT3.**	
1	**Shut_SMIOVT2.**	

BIT	DESCRIPTION	
0	**Shut_SMIOVT1.**	

9.82 SMI# Mask Register 5 – Index 84h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**	**Reserved**	**Reserved**	**AUX FANIN2**	**AUX FANIN1**	**AUX FANIN0**	**CPU FANIN**	**SYS FANIN**
DEFAULT	0	0	0	1	1	1	1	1

BIT	DESCRIPTION	
7	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 5 – Index 74h (Bank0))
6	Reserved.	
5	Reserved.	
4	**AUXFANIN2.**	
3	**AUXFANIN1.**	
2	**AUXFANIN0.**	
1	**CPUFANIN.**	
0	**SYSFANIN.**	

9.83 SMI# Mask Register 6 – Index 85h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**					**AUX FANOUT0**	**CPU FANOUT**	**SYS FANOUT**
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION	
7	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 6 – Index 75h (Bank0))
6	Reserved.	
5	Reserved.	
4	Reserved.	
3	Reserved.	
2	**AUXFANOUT0.**	
1	**CPUFANOUT.**	
0	**SYSFANOUT.**	

9.84 SMI# Mask Register 7 – Index 86h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					Caseopen_clr	Reserved	Caseopen
DEFAULT	0	0	1	1	0	0	1	1

BIT	DESCRIPTION	
7	Reserved.	A one disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register 7 – Index 76h (Bank0))
6	Reserved.	
5	Reserved.	
4	Reserved.	
3	Reserved.	
2	**Caseopen_clr.**	
1	Reserved.	
0	**Caseopen.**	

9.85 CPUVCORE High Limit Voltage Register – Index 90h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUVCORE High Limit Voltage							
DEFAULT	1	1	0	1	1	0	1	0

BIT	DESCRIPTION
7-0	**CPUVCORE High Limit Voltage.** Default: 0xDAh

9.86 CPUVCORE Low Limit Voltage Register – Index 91h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUVCORE Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUVCORE Low Limit Voltage.** Default: 0x00h

9.87 VIN0 High Limit Voltage Register – Index 92h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**VIN0 High Limit Voltage.** Default: 0xFFh

9.88 VIN0 Low Limit Voltage Register – Index 93h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN0 Low Limit Voltage.** Default: 0x00h

9.89 AVSB High Limit Voltage Register – Index 94h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVSB High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AVSB High Limit Voltage.** Default: 0xFFh

9.90 AVSB Low Limit Voltage Register – Index 95h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVSB Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

7-0	**AVSB Low Limit Voltage.** Default: 0x00h

9.91 3VCC High Limit Voltage Register – Index 96h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VCC High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**3VCC High Limit Voltage.** Default: 0xFFh

9.92 3VCC Low Limit Voltage Register – Index 97h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VCC Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**3VCC Low Limit Voltage.** Default: 0x00h

9.93 VIN1 High Limit Voltage Register – Index 98h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**VIN1 High Limit Voltage.** Default: 0xFFh

9.94 VIN1 Low Limit Voltage Register – Index 99h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN1 Low Limit Voltage.** Default: 0x00h

9.95 VIN2 High Limit Voltage Register – Index 9Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN2 High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**VIN2 High Limit Voltage.** Default: 0xFFh

9.96 VIN2 Low Limit Voltage Register – Index 9Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN2 Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN2 Low Limit Voltage.** Default: 0x00h

9.97 VHIF High Limit Voltage Register – Index 9Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VHIF High Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VHIF High Limit Voltage.** Default: 0xFFh

9.98 VHIF Low Limit Voltage Register – Index 9Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VHIF Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-0	**VHIF Low Limit Voltage.** Default: 0x00h

9.99 3VSB High Limit Voltage Register – Index 9Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**3VSB High Limit Voltage.** Default: 0xFFh

9.100 3VSB Low Limit Voltage Register – Index 9Fh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	3VSB Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**3VSB Low Limit Voltage.** Default: 0x00h

9.101 VBAT High Limit Voltage Register – Index A0h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VBAT High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**VBAT High Limit Voltage.** Default: 0xFFh

9.102 VBAT Low Limit Voltage Register – Index A1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	VBAT Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VBAT Low Limit Voltage.** Default: 0x00h

9.103 VTT High Limit Voltage Register – Index A2h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VTT High Limit Voltage							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**VBAT High Limit Voltage.** Default: 0xFFh

9.104 VTT Low Limit Voltage Register – Index A3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VTT Low Limit Voltage							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VTT Low Limit Voltage.** Default: 0x00h

9.105 Reserved Register – Index A4h ~ AFh (Bank 0)

9.106 SMIOVT1 Temperature Source Select Register – Index B0h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	Reserved.

4-0	**SMIOVT1 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT1 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT1 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT1 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT1 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT1 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT1 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT1 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT1 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT1 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT1 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT1monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT1 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT1 monitoring source.

9.107 SMIOVT2 Temperature Source Select Register – Index B1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	Reserved.
4-0	**SMIOVT2 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT2 monitoring source. (Default) 0 0 0 1 1: Select **AUXTIN** as SMIOVT2 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT2 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT2 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT2 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT2 monitoring source.

	0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT2 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT2 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT2 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT2 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT2 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT2monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT2 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT2 monitoring source.

9.108 SMIOVT3 Temperature Source Select Register – Index B2h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	Reserved.
4-0	**SMIOVT3 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT3 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT3 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT3 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT3 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT3 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT3 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT3 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT3 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT3 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT3 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT3 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT3 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT3 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT3 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT3 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT3monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT3 monitoring source.

	1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT3 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT3 monitoring source.

9.109 SMI/OVT Control Register – Index B6h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	OVTPOL	Reserved	T2ToT6 _INTMODE	EN_T1 _ONE	SMI# ENABLE
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	Reserved.
6	Reserved.
5	Reserved.
4	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
3	Reserved.
2	**T2ToT6_INTMode.** 1: SMI# output type of Temperature SMIOVT2, SMIOVT3 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3 temperature source is in Two-Times Interrupt mode. (Default)
1	**EN_T1_ONE.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
0	**SMI# Enable.** A one enables the SMI# Interrupt output.

9.110 SMIOVT1 Control Register – Index B7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST1<0>	TOVF1<0>	FAULT1		DIS_ OVT1	EN_ WS1	OVT1_ Mode	STOP1
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST1<0>:** Hysteresis temperature bit0.
6	**TOVF1<0>:** Over-temperature bits0.
5-4	**Fault1.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.

BIT	DESCRIPTION
3	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
2	**EN_WS1.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT1_Mode. SMIOVT1 Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
0	**STOP1.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.111 SMIOVT2 Control Register – Index B8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST2<0>	TOVF2<0>	FAULT2		DIS_ OVT2	EN_ WS2	OVT2_ Mode	STOP2
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST2<0>:** Hysteresis temperature bit0.
6	**TOVF2<0>:** Over-temperature bits0.
5-4	**Fault2.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT2.** 0: Enable SMIOVT2 OVT# output. (Default) 1: Disable temperature sensor SMIOVT2 over-temperature (OVT#) output.
2	**EN_WS2.** 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT2_Mode. SMIOVT2 Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
0	**STOP2.** **0: Monitor SMIOVT2 temperature source.** **1: Stop monitoring SMIOVT2 temperature source.**

9.112 SMIOVT3 Control Register – Index B9h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST3<0>	TOVF3<0>	FAULT3		DIS_ OVT3	EN_ WS3	OVT3_ Mode	STO3
DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**THYST3<0>:** Hysteresis temperature bit0.
6	**TOVF3<0>:** Over-temperature bits0.
5-4	**Fault3.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
3	**DIS_OVT3.** 0: Enable SMIOVT3 OVT# output. (Default) 1: Disable temperature sensor SMIOVT3 over-temperature (OVT#) output.
2	**EN_WS3.** 1: SMI# output type of SMIOVT Source3 temperature (Default: AUXTIN) is Shut-down Interrupt Mode. 0: SMI# output type is in Interrupt Mode. (Default)
1	**OVT3_Mode. SMIOVT3 Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
0	**STOP3.** **0: Monitor SMIOVT3 temperature source.** **1: Stop monitoring SMIOVT3 temperature source.**

9.113 Reserved Register – Index BDh ~ BFh (Bank 0)

9.114 SMIOVT1 Shut-down mode High Limit Temperature Register – Index C0h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT1 Shut-down mode High Limit Temperature.

9.115 SMIOVT1 Shut-down mode Low Limit Temperature Register – Index C1h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT1 Shut-down mode Low Limit Temperature.

9.116 SMIOVT1 Temperature Source Over-temperature (High Byte) Register – Index C2h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF1<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF1<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.117 SMIOVT1 Temperature Source Hysteresis (High Byte) Register – Index C3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST1<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST1<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.118 SMIOVT2 Shut-down mode High Limit Temperature Register – Index C4h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT2 Shut-down mode High Limit Temperature.

9.119 SMIOVT2 Shut-down mode Low Limit Temperature Register – Index C5h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT2 Shut-down mode Low Limit Temperature.

9.120 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index C6h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF2<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF2<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.121 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index C7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST2<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST2<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.122 SMIOVT3 Shut-down mode High Limit Temperature Register – Index C8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT3 Shut-down mode High Limit Temperature.

9.123 SMIOVT3 Shut-down mode Low Limit Temperature Register – Index C9h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	SMIOVT3 Shut-down mode Low Limit Temperature.

9.124 SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index Cah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF3<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF3<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.125 SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index CBh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST3<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST3<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.126 Reserved Register – Index D8h ~ DFh (Bank 0)

9.127 (SYSFANIN) Fan Count Limit High-byte Register – Index E0h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	FANIN1_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.128 (SYSFANIN) Fan Count Limit Low-byte Register – Index E1h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANIN1_HL [4:0]				
DEFAULT	0			11111				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.129 (CPUFANIN) Fan Count Limit High-byte Register – Index E2h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.130 (CPUFANIN) Fan Count Limit Low-byte Register – Index E3h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANIN2_HL [4:0]				
DEFAULT	0			11111				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.131 (AUXFANIN0) Fan Count Limit High-byte Register – Index E4h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, High Byte

9.132 (AUXFANIN0) Fan Count Limit Low-byte Register – Index E5h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANIN3_HL [4:0]				
DEFAULT	0			11111				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, Low Byte

9.133 (AUXFANIN1) Fan Count Limit High-byte Register – Index E6h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN4_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, High Byte

9.134 (AUXFANIN1) Fan Count Limit Low-byte Register – Index E7h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANIN4_HL [4:0]				
DEFAULT	0			11111				

BIT	DESCRIPTION
7-5	Reserved.

4-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, Low Byte

9.135 (AUXFANIN2) Fan Count Limit High-byte Register – Index E8h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN5_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, High Byte

9.136 (AUXFANIN2) Fan Count Limit Low-byte Register – Index E9h (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			FANIN5_HL [4:0]				
DEFAULT	0			11111				

BIT	DESCRIPTION
7-5	Reserved.
4-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, Low Byte

9.137 FANIN5 IN/OUT Control Register – Index EAh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5-0
NAME	FANOPV5	FANINC5	Reserved
DEFAULT	0	0	0

BIT	DESCRIPTION
7	**FANOPV5. AUXFANIN2 output value**, only if bit 2 is set to zero. 1: AUXFANIN2 generates a logic-high signal. 0: AUXFANIN2 generates a logic-low signal. (Default)
6	**FANINC5. AUXFANIN2 Input Control.** 1: AUXFANIN2 acts as a fan tachometer input. (Default) 0: AUXFANIN2 acts as a fan control signal, and the output value is set by bit 1.
5-0	Reserved.

9.138 Reserved Register – Index EBh ~ EFh (Bank 0)

9.139 SYSFAN PWM Output Frequency Configuration Register – Index F0h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	3						

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index F3h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

9.140 CPUFAN PWM Output Frequency Configuration Register – Index F1h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	3						

The register is meaningful only when CPUFANOUT is progarmmed for PWM output (i.e., Bank0, Index F3h, bit 1 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

9.141 AUXFAN0 PWM Output Frequency Configuration Register – Index F2h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	3						

This register is only meaningful when AUXFANOUT0 is programmed for PWM output (i.e. Bank0, Index F3h, bit 2 is 0)

BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **92.5/ (Divisor[6:0]+1) KHz**
Mapped Divisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	92.5KHz	.....		
0000001	2	46.3KHz			
0000010	3	31.2KHz			
0000011	4	23.3KHz			
0000100	5	18.5KHz	0001111	16	5.8KHz
0000101	6	15.6KHz	0011111	32	2.9KHz
0000110	7	13.3KHz	0111111	64	1.4KHz
0000111	8	11.6KHz	1111111	128	724Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
Mapped Divisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1000Hz	1000	12	83Hz
0001	2	500Hz	1001	16	62.5Hz
0010	3	333Hz	1010	32	31.25Hz
0011	4	250Hz	1011	64	15.62Hz
0100	5	200Hz	1100	128	7.81Hz
0101	6	166Hz	1101	256	3.9Hz
0110	7	142Hz	1110	512	2Hz
0111	8	125Hz	1111	1024	0.98Hz

9.142 FAN Output Mode Configuration – Index F3h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT0_SEL	CPUFANOUT_SEL	SYSFANOUT_SEL
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**AUXFANOUT0 Output Mode Selection.**

BIT	DESCRIPTION
	0: AUXFANAOUT0 pin produces a PWM output duty cycle. (Default) 1: AUXFANOUT0 pin produces DC output.
1	**CPUFANOUT Output Mode Selection.** 0: CPUFANOUT pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT pin produces DC output.
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. (Default) 1: SYSFANOUT pin produces DC output.

9.143 Reserved Register – Index F4h (Bank 0)

9.144 FANIN5 Revolution Pulses Selection Register – Index F5h (Bank 0)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**HM_Rev_Pulse_Fan5_Sel**		Reserved					
DEFAULT	10		0					

BIT	DESCRIPTION
7-6	**AUXFANIN2 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.
5-0	Reserved.

9.145 FANIN1~4 Revolution Pulses Selection Register – Index F6h (Bank 0)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**HM_Rev_Pulse_Fan4_Sel**		**HM_Rev_Pulse_Fan3_Sel**		**HM_Rev_Pulse_Fan2_Sel**		**HM_Rev_Pulse_Fan1_Sel**	
DEFAULT	10		10		10		10	

BIT	DESCRIPTION
7-6	**AUXFANIN1 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.
5-4	**AUXFANIN0 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution.

	= 10, two pulses per revolution. (default) = 11, three pulses per revolution.
3-2	**CPUFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.146 Serial Bus Address Register – Index F7h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Serial Bus Address						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	Reserved. (Read Only).
6-0	**Serial Bus Address <7:1>**

9.147 FANIN1~4 IN/OUT Control Register – Index F8h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOPV4	FANINC4	FANOPV3	FANINC3	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION
7	**FANOPV4. AUXFANIN1 output value**, only if bit 6 is set to zero. 1: AUXFANIN1 generates a logic-high signal. 0: AUXFANIN1 generates a logic-low signal. (Default)
6	**FANINC4. AUXFANIN1 Input Control.** 1: AUXFANIN1 acts as a fan tachometer input. (Default) 0: AUXFANIN1 acts as a fan control signal, and the output value is set by bit 1.
5	**FANOPV3. AUXFANIN0 output value**, only if bit 4 is set to zero. 1: AUXFANIN0 generates a logic-high signal. 0: AUXFANIN0 generates a logic-low signal. (Default)
4	**FANINC3. AUXFANIN0 Input Control.** 1: AUXFANIN0 acts as a fan tachometer input. (Default)

BIT	DESCRIPTION
	0: AUXFANIN0 acts as a fan control signal, and the output value is set by bit 1.
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: CPUFANIN generates a logic-high signal. 0: CPUFANIN generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: CPUFANIN acts as a fan tachometer input. (Default) 0: CPUFANIN acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: SYSFANIN generates a logic-high signal. 0: SYSFANIN generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: SYSFANIN acts as a fan tachometer input. (Default) 0: SYSFANIN acts as a fan control signal, and the output value is set by bit 1.

9.148 AUXFAN1 PWM Output Frequency Configuration Register – Index F9h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL4	PWM_SCALE4						
DEFAULT	0	3						

BIT	DESCRIPTION
7	**PWM_CLK_SEL4. AUXFANOUT1 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE4. AUXFANOUT1 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

9.149 AUXFAN2 PWM Output Frequency Configuration Register – Index Fah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL5	PWM_SCALE5						
DEFAULT	0	3						

BIT	DESCRIPTION
7	**PWM_CLK_SEL5. AUXFANOUT2 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.

BIT	DESCRIPTION
6-0	**PWM_CLK_SCALE5. AUXFANOUT2 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **92.5/ (Divisor[6:0]+1) KHz**
Mapped Divisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	92.5KHz	.....		
0000001	2	46.3KHz			
0000010	3	31.2KHz			
0000011	4	23.3KHz			
0000100	5	18.5KHz	0001111	16	5.8KHz
0000101	6	15.6KHz	0011111	32	2.9KHz
0000110	7	13.3KHz	0111111	64	1.4KHz
0000111	8	11.6KHz	1111111	128	724Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
Mapped Divisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1000Hz	1000	12	83Hz
0001	2	500Hz	1001	16	62.5Hz
0010	3	333Hz	1010	32	31.25Hz
0011	4	250Hz	1011	64	15.62Hz
0100	5	200Hz	1100	128	7.81Hz
0101	6	166Hz	1101	256	3.9Hz
0110	7	142Hz	1110	512	2Hz
0111	8	125Hz	1111	1024	0.98Hz

9.150 Reserved Register – Index FBh ~ FCh (Bank 0)

9.151 Nuvoton Vendor ID Register by I2C Interface – Index FDh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.152 Nuvoton Vendor ID Register by LPC Interface – Index FEh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.153 Chip ID – Index FFh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.154 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 10h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		SYSFAN SOURCE[4:0]				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, Index16h) at most if necessary.
6-5	Reserved.
4-0	**SYSFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.155 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 11h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**SYSFAN Target Temperature / SYSFANIN Target Speed_L**							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate Index 12h[3:0]							

9.156 SYSFANIN Tolerance_H / Target Speed_H Register – Index 12h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN TOL_H			Reserved.	SYSFANIN Target Speed_H			
DEFAULT	0			0	0			

BIT	DESCRIPTION
7-5	SYSFANIN Tolerance_H [5:3]
4	Reserved.
3-0	SYSFANIN Target Speed_H [11:8]

9.157 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 13h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. (Default) 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN™ IV Mode.
3	Reserved.
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.158 SYSFAN Step Up Time Register – Index 14h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.159 SYSFAN Step Down Time Register – Index 15h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.160 SYSFAN Stop Value Register – Index 16h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.161 SYSFAN Start-up Value Register – Index 17h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.162 SYSFAN Stop Time Register – Index 18h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.163 SYSFAN Output Value Select Register – Index 19h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	7F							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is around 2.048V.						Reserved	

9.164 SYSFAN Temperature Critical Register – Index 1Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	SYSFAN Temperature Critical Register.

9.165 SYSFAN Critical Temperature Tolerance Register – Index 1Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		

DEFAULT	0	0

BIT	DESCRIPTION
7-3	Reserved.
2-0	SYSFAN Critical Temperature Tolerance

9.166 SYSFAN Enable Critical Duty / Fanout Step Register – Index 1Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**En_SYS_3WFAN**	**Reserved**		**En_SYS_CRITICAL_DUTY**	**Reserved**			
DEFAULT	0	0		0	0			

BIT	DESCRIPTION
7	**En_SYS_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	Reserved.
4	**En_SYS_CRITICAL_FUNC** 0: Disable critical function for SYSFANOUT. 1: Used Index 1D CRITICAL_DUTY Value for SYSFANOUT.
3-0	Reserved.

9.167 SYSFAN Critical Duty Register – Index 1Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**SYSFAN Critical Duty**							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.168 SYSFAN Enable Close Loop Fan Control RPM Mode Register – Index 1Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Reserved**							**En_SYS_RPM**
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved.
0	**En_SYS_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.169 SYSFAN Enable RPM High Mode / RPM Mode Tolerance Register – Index 1Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_SYS_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_SYS_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	Reserved.
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.170 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 20h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		CPUFAN SOURCE[4:0]				
DEFAULT	0	0		2				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank1, Index 26h) at most if necessary.
6-5	Reserved.
4-0	**CPUFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. (Default)

BIT	DESCRIPTION
	0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

9.171 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 21h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFAN Target Temperature / CPUFANIN Target Speed_L**							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate Index 22h[3:0]							

9.172 CPUFANIN Tolerance_H / Target Speed_H Register – Index 22h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**CPUFANIN TOL_H**			**Reserved**	**CPUFANIN Target Speed_H**			
DEFAULT	0			0	0			

BIT	DESCRIPTION
7-5	CPUFANIN Tolerance_H [5:3]

4	Reserved.
3-0	CPUFANIN Target Speed_H [11:8]

9.173 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN™ IV Mode.
3	Reserved.
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.174 CPUFAN Step Up Time Register – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.175 CPUFAN Step Down Time Register – Index 25h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.176 CPUFAN Stop Value Register – Index 26h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.177 CPUFANOUT Start-up Value Register – Index 27h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.178 CPUFAN Stop Time Register – Index 28h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.

The time unit is 0.1sec.

9.179 CPUFANOUT Output Value Select Register – Index 29h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	CPUFANOUT Value
DEFAULT	7F

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 1 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 1 is 1)	DESCRIPTION	CPUFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is around 2.048V.						Reserved	

9.180 CPUFAN Temperature Critical Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Temperature Critical							
DEFAULT	4B							

BIT	DESCRIPTION
7-0	CPUFAN Temperature Critical Register.

9.181 CPUFAN Critical Temperature Tolerance Register – Index 2Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0		

BIT	DESCRIPTION
7-3	Reserved.
2-0	CPUFAN Critical Temperature Tolerance

9.182 CPUFAN Enable Critical Duty / Fanout Step Register – Index 2Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	En_CPU_3WFAN	Reserved	En_CPU_CRITICAL_DUTY	Reserved
DEFAULT	0	0	0	0

BIT	DESCRIPTION
7	**En_CPU_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	Reserved.
4	**En_CPU_CRITICAL_FUNC** 0: Disable critical function for CPUFANOUT. 1: Used Index 1D CRITICAL_DUTY Value for CPUFANOUT.
3-0	Reserved.

9.183 CPUFAN Critical Duty Register – Index 2Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.184 CPUFAN Enable Close Loop Fan Control RPM Mode Register – Index 2Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPU_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved.
0	**En_CPU_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.185 CPUFAN Enable RPM High Mode / RPM Mode Tolerance Register – Index 2Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	En_CPU_RPM_High	Reserved	Generic_Tol_RPM
DEFAULT	0	0	2

BIT	DESCRIPTION
7	**En_CPU_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	Reserved.
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.186 AUXFAN0 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 30h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN0 SOURCE[4:0]				
DEFAULT	0	0		3				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT0 Stop Value (Bank1, Index 36h) at most if necessary.
6-5	Reserved.
4-0	**AUXFAN0 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN0 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN0 monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN0 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN0 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN0 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN0 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN0 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN0 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN0 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN0 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN0 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN0 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN0 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN0 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN0 monitoring source.

BIT	DESCRIPTION
	1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN0 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN0 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN0 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN0 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN0 monitoring source.

9.187 AUXFAN0 Target Temperature Register / AUXFANIN0 Target Speed_L Register – Index 31h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFAN0 Target Temperature / AUXFANIN0 Target Speed_L**							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN0 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN0 Target Speed [7:0], [11:8] associate Index 32h[3:0]							

9.188 AUXFANIN0 Tolerance_H / Target Speed_H Register – Index 32h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANIN0 TOL_H**			**Reserved**	**AUXFANIN0 Target Speed_H**			
DEFAULT	0			0	0			

BIT	DESCRIPTION
7-5	AUXFANIN0 Tolerance_H [5:3]
4	Reserved.
3-0	AUXFANIN0 Target Speed_H [11:8]

9.189 AUXFAN0 MODE Register / AUXFAN0 TOLERRANCE Register – Index 33h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFAN MODE**				**Reseved**	**Tolerance of AUXFAN0 Target Temperature or AUXFANIN0**		

			Target Speed_L
DEFAULT	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT0 Mode Select.** 0000: AUXFANOUT0 is in Manual Mode. (Default) 0001: AUXFANOUT0 is in Thermal Cruise Mode. 0010: AUXFANOUT0 is as Fan Speed Cruise Mode. 0100: AUXFANOUT0 is in SMART FAN™ IV Mode.
3	Reseved.
2-0	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L.

9.190 AUXFAN0 Step Up Time Register – Index 34h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Step Up Time Value**							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to increase its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.191 AUXFAN0 Step Down Time Register – Index 35h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Step Down Time Value**							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to decrease its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.192 AUXFAN0 Stop Value Register – Index 36h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANOUT0 Stop Value**							

DEFAULT	1

In Thermal Cruise mode, the AUXFANOUT0 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.193 AUXFAN0 Start-up Value Register – Index 37h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, AUXFANOUT0 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.194 AUXFAN0 Stop Time Register – Index 38h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.195 AUXFAN0 Output Value Select Register – Index 39h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value							
DEFAULT	FF							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index F3h, bit 2 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index F3h, bit 2 is	DESCRIPTION	AUXFANOUT0 voltage control. The output voltage is calculated according to this equation.						Reserved	

1)		**OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is around 2.048V.	

9.196 AUXFAN0 Temperature Critical Register – Index 3Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	AUXFAN0 Temperature Critical Register.

9.197 AUXFAN0 Critical Temperature Tolerance Register – Index 3Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT0 Critical Temperature Tolerance		
DEFAULT	0					0		

BIT	DESCRIPTION
7-3	Reserved.
2-0	AUXFAN0 Critical Temperature Tolerance

9.198 AUXFAN0 Enable Critical Duty / Fanout Step Register – Index 3Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX_3WFAN	Reserved		En_AUX_CRITICAL_DUTY	Reserved			Reserved
DEFAULT	0	0		0	0			0

BIT	DESCRIPTION
7	**En_AUX_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	Reserved.
4	**En_AUX_CRITICAL_FUNC** 0: Disable critical function for AUXFANOUT.

	1: Used Index 1D CRITICAL_DUTY Value for AUXFANOUT.
3-0	Reserved.

9.199 AUXFAN0 Critical Duty Register – Index 3Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN0 Critical Duty.

9.200 AUXFAN0 Enable Close Loop Fan Control RPM Mode Register – Index 3Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved.
0	**En_AUX_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.201 AUXFAN0 Enable RPM High Mode / RPM Mode Tolerance Register – Index 3Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_AUX_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	Reserved.

3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.202 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 60h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FANTM IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.203 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 61h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FANTM IV) Temperature 2							
DEFAULT	23							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.204 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 62h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FANTM IV) Temperature 3							
DEFAULT	2D							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.205 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 63h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FANTM IV) Temperature 4							
DEFAULT	37							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.206 SYSFAN (SMART FAN™ IV) FD1/RPM1 Register – Index 64h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD1/RPM1 Register.

9.207 SYSFAN (SMART FAN™ IV) FD2/RPM2 Register – Index 65h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD2/RPM2 Register.

9.208 SYSFAN (SMART FAN™ IV) FD3/RPM3 Register – Index 66h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD3/RPM3 Register.

9.209 SYSFAN (SMART FAN™ IV) FD4/RPM4 Register – Index 67h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FANTM IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) FD4/RPM4 Register.

9.210 SYSFAN Weight value Configuration Register – Index 68h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_SYSFAN_WEIGHT	Reserved		SYS_WEIGHT_SEL				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**EN_SYSFAN_WEIGHT.** 0: Disable Weight Value Control for SYSFAN. 1: Enable Weight Value Control for SYSFAN.
6-5	Reserved.
4-0	**SYSFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.211 SYSFAN Weight Temperature Step Register – Index 69h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step (SYS_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Temperature Step

9.212 SYSFAN Weight Temperature Step Tolerance Register – Index 6Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Temperature Step Tolerance

9.213 SYSFAN Weight Step Register – Index 6Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Weight Step (SYS_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Weight Step

9.214 SYSFAN Weight Temperature Base Register – Index 6Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Temperature Base

9.215 SYSFAN Weight Fan Duty Base Register – Index 6Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Start point of Fan Duty increasing**

9.216 SYSFAN Enable PECIERR DUTY Register – Index 6Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_SYS_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved.
1-0	**EN_SYS_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.217 SYSFAN Pre-Configured Register For PECI Error – Index 6Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECI error (PECI_ERR_SYSOUT)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	**SYSFANOUT pre-configured register for PECI error.**

9.218 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 70h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FANTM IV) Temperature 1							
DEFAULT	28							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.219 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 71h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FANTM IV) Temperature 2							
DEFAULT	32							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.220 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 72h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.221 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 73h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	46							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.222 CPUFAN (SMART FAN™ IV) FD1/RPM1 Register – Index 74h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FANTM IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD1/RPM1 Register.

9.223 CPUFAN (SMART FAN™ IV) FD2/RPM2 Register – Index 75h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FANTM IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD2/RPM2 Register.

9.224 CPUFAN (SMART FAN™ IV) FD3/RPM3 Register – Index 76h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD3/RPM3 Register.

9.225 CPUFAN (SMART FAN™ IV) FD4/RPM4 Register – Index 77h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FANTM IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) FD4/RPM4 Register.

9.226 CPUFAN Weight value Configuration Register – Index 78h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_WEIGHT	Reserved		CPU_WEIGHT_SEL				

DEFAULT	0	0	1

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	Reserved.
4-0	**CPUFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

9.227 CPUFAN Weight Temperature Step Register – Index 79h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Step

9.228 CPUFAN Weight Temperature Step Tolerance Register – Index 7Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Step Tolerance

9.229 CPUFAN Weight Step Register – Index 7Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Weight Step

9.230 CPUFAN Weight Temperature Base Register – Index 7Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Temperature Base

9.231 CPUFAN Weight Fan Duty Base Register – Index 7Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	CPUFANOUT Start point of Fan Duty increasing

9.232 CPUFAN Enable PECIERR DUTY Register – Index 7Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_CPU_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	Reserved.
1-0	**EN_CPU_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.233 CPUFAN Pre-Configured Register For PECI Error – Index 7Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECI error (PECI_ERR_CPUOUT)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	CPUFANOUT pre-configured register for PECI error.

9.234 AUXFAN0 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 80h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 1 Register (T1).

9.235 AUXFAN0 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 81h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	AUXFAN0 (SMART FANTM IV) Temperature 2
DEFAULT	23

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 2 Register (T2).

9.236 AUXFAN0 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 82h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) Temperature 3							
DEFAULT	2D							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 3 Register (T3).

9.237 AUXFAN0 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 83h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) Temperature 4							
DEFAULT	37							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 4 Register (T4).

9.238 AUXFAN0 (SMART FAN™ IV) FD1/RPM1 Register – Index 84h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) FD1/RPM1 Register.

9.239 AUXFAN0 (SMART FAN™ IV) FD2/RPM2 Register – Index 85h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) FD2/RPM2 Register.

9.240 AUXFAN0 (SMART FAN™ IV) FD3/RPM3 Register – Index 86h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) FD3/RPM3 Register.

9.241 AUXFAN0 (SMART FAN™ IV) FD4/RPM4 Register – Index 87h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FANTM IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) FD4/RPM4 Register.

9.242 AUXFAN0 Weight value Configuration Register – Index 88h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN0_WEIGHT	Reserved		AUX_WEIGHT_SEL				
DEFAULT	0	0		1				

BIT	DESCRIPTION
7	**EN_AUXFAN0_WEIGHT.** 0: Disable Weight Value Control for AUXFAN0. 1: Enable Weight Value Control for AUXFAN0.
6-5	Reserved.

BIT	DESCRIPTION
4-0	**AUXFAN0 Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN0 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN0 monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN0 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN0 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN0 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN0 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN0 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN0 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN0 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN0 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN0 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN0 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN0 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN0 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN0 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN0 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN0 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN0 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN0 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN0 monitoring source.

9.243 AUXFAN0 Weight Temperature Step Register – Index 89h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Step (AUX_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT0 Temperature Step

9.244 AUXFAN0 Weight Temperature Step Tolerance Register – Index 8Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Step Tolerance (AUX_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT0 Temperature Step Tolerance

9.245 AUXFAN0 Weight Step Register – Index 8Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Weight Step (AUX_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT0 Weight Step

9.246 AUXFAN0 Weight Temperature Base Register – Index 8Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Base (AUX_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT0 Temperature Base

9.247 AUXFAN0 Weight Fan Duty Base Register – Index 8Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Temperature Base (AUX_DUTY_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	AUXFANOUT0 Start point of Fan Duty increasing

9.248 AUXFAN0 Enable PECIERR DUTY Register – Index 8Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX_PECIERR_DUTY	
DEFAULT	0						0	

BIT	DESCRIPTION
7-2	Reserved.
1-0	**EN_AUX_PECIERR_DUTY** 00 : Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.249 AUXFAN0 Pre-Configured Register For PECI Error – Index 8Fh (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 pre-configured register for PECI error (PECI_ERR_AUXOUT)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	AUXFANOUT0 pre-configured register for PECI error.

9.250 AUXFAN1 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 90h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN1 SOURCE[4:0]				
DEFAULT	0	0		3				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT1 Stop Value (Bank1, Index96h) at most if necessary.
6-5	Reserved.
4-0	**AUXFAN1 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN1 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN1 monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN1 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN1 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN1 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN1 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN1 monitoring source.

BIT	DESCRIPTION
	0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN1 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN1 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN1 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN1 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN1 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN1 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN1 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN1 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN1 monitoring source.

9.251 AUXFAN1 Target Temperature Register / AUXFANIN1 Target Speed_L Register – Index 91h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFAN1 Target Temperature / AUXFANIN1 Target Speed_L**							
DEFAULT	0							

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN1 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN1 Target Speed [7:0], [11:8] associate Index 92h[3:0]							

9.252 AUXFANIN1 Tolerance_H / Target Speed_H Register – Index 92h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**AUXFANIN1 TOL_H**			**Reserved**	**AUXFANIN1 Target Speed_H**			
DEFAULT	0			0	0			

BIT	DESCRIPTION
7-5	AUXFANIN1 Tolerance_H [5:3]
4	Reserved.
3-0	AUXFANIN1 Target Speed_H [11:8]

9.253 AUXFAN1 MODE Register / AUXFAN1 TOLERRANCE Register – Index 93h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 MODE				Reseved	Tolerance of AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**AUXFANOUT1 Mode Select.** 0000: AUXFANOUT1 is in Manual Mode. (Default) 0001: AUXFANOUT1 is in Thermal Cruise Mode. 0010: AUXFANOUT1 is as Fan Speed Cruise Mode. 0100: AUXFANOUT1 is in SMART FAN™ IV Mode.
3	Reserved.
2-0	Tolerance of AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L.

9.254 AUXFAN1 Step Up Time Register – Index 94h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to increase its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.255 AUXFAN1 Step Down Time Register – Index 95h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to decrease its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.256 AUXFAN1 Stop Value Register – Index 96h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the AUXFANOUT1 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.257 AUXFAN1 Start-up Value Register – Index 97h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, AUXFANOUT1 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.258 AUXFAN1 Stop Time Register – Index 98h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.259 AUXFAN1 Output Value Select Register – Index 99h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value							
DEFAULT	FF							

FUNCTION MODE		7	6	5	4	3	2	1	0

PWM Output	**DESCRIPTION**	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.

9.260 AUXFAN1 Temperature Critical Register – Index 9Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	AUXFAN1 Temperature Critical Register.

9.261 AUXFAN1 Critical Temperature Tolerance Register – Index 9Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT1 Critical Temperature Tolerance		
DEFAULT	0					0		

BIT	DESCRIPTION
7-3	Reserved.
2-0	AUXFAN1 Critical Temperature Tolerance

9.262 AUXFAN1 Enable Critical Duty / Fanout Step Register – Index 9Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX1_3WFAN	Reserved		En_AUX1_CRITICAL_DUTY	Reserved			
DEFAULT	0	0		0	0			

BIT	DESCRIPTION
7	**En_AUX1_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	Reserved.
4	**En_AUX1_CRITICAL_FUNC** 0: Disable critical function for AUXFAN1OUT. 1: Used Index 1D CRITICAL_DUTY Value for AUXFAN1OUT.

3-0	Reserved.

9.263 AUXFAN1 Critical Duty Register – Index 9Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN1 Critical Duty.

9.264 AUXFAN1 Enable Close Loop Fan Control RPM Mode Register – Index 9Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX1_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved.
0	**En_AUX1_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.265 AUXFAN1 Enable RPM High Mode / RPM Mode Tolerance Register – Index 9Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX1_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_AUX1_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	Reserved.
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.266 AUXFAN2 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index A0h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN2 SOURCE[4:0]				
DEFAULT	0	0		3				

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank1, IndexA6h) at most if necessary.
6-5	Reserved.
4-0	**AUXFAN2 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN2 monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN2 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN2 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN2 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN2 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN2 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN2 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN2 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN2 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN2 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN2 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN2 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN2 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN2 monitoring source.

9.267 AUXFAN2 Target Temperature Register / AUXFANIN2 Target Speed_L Register – Index A1h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	AUXFAN2 Target Temperature / AUXFANIN2 Target Speed_L
DEFAULT	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN2 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN2 Target Speed [7:0], [11:8] associate Index A2h[3:0]							

9.268 AUXFANIN2 Tolerance_H / Target Speed_H Register – Index A2h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 TOL_H			Reserved	AUXFANIN2 Target Speed_H			
DEFAULT	0			0	0			

BIT	DESCRIPTION
7-5	AUXFANIN2 Tolerance_H [5:3]
4	Reserved.
3-0	AUXFANIN2 Target Speed_H [11:8]

9.269 AUXFAN2 MODE Register / AUXFAN2 TOLERRANCE Register – Index A3h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 MODE				Reseved	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L		
DEFAULT	0				0	0		

BIT	DESCRIPTION
7-4	**AUXFANOUT2 Mode Select.** 0000: AUXFANOUT2 is in Manual Mode. (Default) 0001: AUXFANOUT2 is in Thermal Cruise Mode. 0010: AUXFANOUT2 is as Fan Speed Cruise Mode. 0100: AUXFANOUT2 is in SMART FAN™ IV Mode.
3	Reserved.
2-0	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L.

9.270 AUXFAN2 Step Up Time Register – Index A4h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Step Up Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to increase its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.271 AUXFAN2 Step Down Time Register – Index A5h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Step Down Time Value							
DEFAULT	A							

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to decrease its value by one step.

For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.272 AUXFAN2 Stop Value Register – Index A6h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Stop Value							
DEFAULT	1							

In Thermal Cruise mode, the AUXFANOUT2 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.273 AUXFAN2 Start-up Value Register – Index A7h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Start-Up Value							
DEFAULT	1							

In Thermal Cruise mode, AUXFANOUT2 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.274 AUXFAN2 Stop Time Register – Index A8h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Stop Time							
DEFAULT	3C							

In Thermal Cruise mode, Define the retention time to the fan stop. It is required by Fan Stop Function.
The time unit is 0.1sec.

9.275 AUXFAN2 Output Value Select Register – Index A9h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	FF							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.276 AUXFAN2 Temperature Critical Register – Index Aah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Temperature Critical							
DEFAULT	3C							

BIT	DESCRIPTION
7-0	AUXFAN2 Temperature Critical Register.

9.277 AUXFAN2 Critical Temperature Tolerance Register – Index Abh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT2 Critical Temperature Tolerance		

DEFAULT	0	0

BIT	DESCRIPTION
7-3	Reserved.
2-0	AUXFAN2 Critical Temperature Tolerance

9.278 AUXFAN2 Enable Critical Duty / Fanout Step Register – Index Ach (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX2_3WFAN	Reserved		En_AUX2_CRITICAL_DUTY	Reserved			
DEFAULT	0	0		0	0			

BIT	DESCRIPTION
7	**En_AUX2_3WFAN** 0: 4-wire fan 1: 3-wire fan
6-5	Reserved.
4	**En_AUX2_CRITICAL_FUNC** 0: Disable critical function for AUXFAN2OUT. 1: Used Index 1D CRITICAL_DUTY Value for AUXFAN2OUT.
3-0	Reserved.

9.279 AUXFAN2 Critical Duty Register – Index Adh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN2 Critical Duty.

9.280 AUXFAN2 Enable Close Loop Fan Control RPM Mode Register – Index Aeh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX2_RPM
DEFAULT	0							0

BIT	DESCRIPTION
7-1	Reserved.
0	**En_AUX2_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.281 AUXFAN2 Enable RPM High Mode / RPM Mode Tolerance Register – Index Afh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En_AUX2_RPM_High	Reserved			Generic_Tol_RPM			
DEFAULT	0	0			2			

BIT	DESCRIPTION
7	**En_AUX2_RPM_High** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
6-4	Reserved.
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode, unit is 100 RPM.

9.282 AUXFAN1 (SMART FAN™ IV) Temperature 1 Register(T1) – Index D0h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 1 Register (T1).

9.283 AUXFAN1 (SMART FAN™ IV) Temperature 2 Register(T2) – Index D1h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) Temperature 2							
DEFAULT	23							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 2 Register (T2).

9.284 AUXFAN1 (SMART FAN™ IV) Temperature 3 Register(T3) – Index D2h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) Temperature 3							
DEFAULT	2D							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 3 Register (T3).

9.285 AUXFAN1 (SMART FAN™ IV) Temperature 4 Register(T4) – Index D3h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) Temperature 4							
DEFAULT	37							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 4 Register (T4).

9.286 AUXFAN1 (SMART FAN™ IV) FD1/RPM1 Register – Index D4h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) FD1/RPM1 Register.

9.287 AUXFAN1 (SMART FAN™ IV) FD2/RPM2 Register – Index D5h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) FD2/RPM2 Register.

9.288 AUXFAN1 (SMART FAN™ IV) FD3/RPM3 Register – Index D6h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) FD3/RPM3 Register.

9.289 AUXFAN1 (SMART FAN™ IV) FD4/RPM4 Register – Index D7h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FANTM IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) FD4/RPM4 Register.

9.290 AUXFAN1 Enable PECIERR DUTY Register – Index DEh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX1_PECIERR_DUTY	
DEFAULT	0						0	

BIT	DESCRIPTION
7-2	Reserved.
1-0	**EN_AUX1_PECIERR_DUTY** 00 : Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.291 AUXFAN1 Pre-Configured Register For PECI Error – Index DFh (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 pre-configured register for PECI error (PECI_ERR_AUXOUT1)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	AUXFANOUT1 pre-configured register for PECI error.

9.292 AUXFAN2 (SMART FANTM IV) Temperature 1 Register(T1) – Index E0h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) Temperature 1							
DEFAULT	19							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FANTM IV) Temperature 1 Register (T1).

9.293 AUXFAN2 (SMART FANTM IV) Temperature 2 Register(T2) – Index E1h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) Temperature 2							
DEFAULT	23							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FANTM IV) Temperature 2 Register (T2).

9.294 AUXFAN2 (SMART FANTM IV) Temperature 3 Register(T3) – Index E2h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) Temperature 3							
DEFAULT	2D							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FANTM IV) Temperature 3 Register (T3).

9.295 AUXFAN2 (SMART FAN™ IV) Temperature 4 Register(T4) – Index E3h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) Temperature 4							
DEFAULT	37							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 4 Register (T4).

9.296 AUXFAN2 (SMART FAN™ IV) FD1/RPM1 Register – Index E4h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) FD1/RPM1							
DEFAULT	8C							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) FD1/RPM1 Register.

9.297 AUXFAN2 (SMART FAN™ IV) FD2/RPM2 Register – Index E5h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) FD2/RPM2							
DEFAULT	AA							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) FD2/RPM2 Register.

9.298 AUXFAN2 (SMART FAN™ IV) FD3/RPM3 Register – Index E6h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) FD3/RPM3							
DEFAULT	C8							

BIT	DESCRIPTION

7-0	AUXFAN2 (SMART FAN™ IV) FD3/RPM3 Register.

9.299 AUXFAN2 (SMART FAN™ IV) FD4/RPM4 Register – Index E7h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FANTM IV) FD4/RPM4							
DEFAULT	E6							

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) FD4/RPM4 Register.

9.300 AUXFAN2 Enable PECIERR DUTY Register – Index Eeh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX2_PECIERR_DUTY	
DEFAULT	0						0	

BIT	DESCRIPTION
7-2	Reserved.
1-0	**EN_AUX2_PECIERR_DUTY** 00 : Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT 10,11: Keep Full Speed

9.301 AUXFAN2 Pre-Configured Register For PECI Error – Index Efh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 pre-configured register for PECI error (PECI_ERR_AUXOUT2)							
DEFAULT	FF							

BIT	DESCRIPTION
7-0	AUXFANOUT2 pre-configured register for PECI error.

9.302 Reserved Register – Index F0h~FFh (Bank 1)

9.303 PECI Function Control Registers – Index 00h~03h (Bank 2)

9.304 PECI Enable Function Register – Index 00h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Reserved				Is_PECI 30	Manual _En	Routine _En
DEFAULT	0	0	0	0	0	1	0	1

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function.(**PECI_En**)
6-3	R / W	Reserved.
2	R / W	Enable PECI 3.0 Command function (**Is_PECI30**)
1	R / W	Enable PECI Manual Function(**Manual_En**)
0	R / W	Enable PECI Routine Function(**Routine_En**)

9.305 PECI Timing Config Register – Index 01h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Polling_time		TN_Extend		Adj[2 :0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	**Polling_time** Adjust PECI polling time. 00_{BIN} = 100 ms (Default) 01_{BIN} = 250 ms 10_{BIN} = 500 ms 11_{BIN} = 1 s
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate, the frequency will be change by different outside loading. Measurement frequency without loading as below: 00_{BIN} = 1 MHz (Default) 01_{BIN} = 600 KHz 10_{BIN} = 334 KHz 11_{BIN} = 177 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	

BIT	READ / WRITE	DESCRIPTION
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.306 PECI Agent Config Register – Index 02h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		En_Agt[1 :0]		Reserved		Dmn1_Agt[1 :0]	
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5	R / W	PECI host to process related agent 31 Enable or Disable. 0 = Agent Disable 1 = Agent Enable
4	R / W	PECI host to process related agent 30 Enable or Disable. 0 = Agent Disable 1 = Agent Enable
3-2	R / W	Reserved.
1	R / W	Indicate agent 31 domain1. 0 = Agent does not have domain 1. 1 = Agent has domain 1.
0	R / W	Indicate agent 30 domain1. 0 = Agent does not have domain 1. 1 = Agent has domain 1.

9.307 PECI Temperature Config Register – Index 03h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_ En	Reserved		Clamp	Reserved	RtDmn_Agt[1 :0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(**Virtual_En)** When enable this function, the temperature raw data can use LPC to write raw data to Bank7 Index 17h ~ Index 1Eh
6-5	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
3	R / W	Reserved.
2	R / W	Agent 31 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
1	R / W	Agent 30 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.308 PECI Command Tbase0 Register – Index 04h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Agent0 base temperature for calculating agent0 absolute temperature.

9.309 PECI Command Tbase1 Register – Index 05h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Agent1 base temperature for calculating agent1 absolute temperature.

9.310 PECI Agent Relative Temperature Register – Index 06h ~ 0Dh (Bank 2)

These registers return the raw data retrieved from PECI GetTemp(). The data may be the error code (range: 8000H~81FFH) or relative temperatures to process the defined **Tbase**. The error code will only be update in **ARTR** and absolute Temperature will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return

priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is 8001_{HEX}, in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

ADDRESS 17-1E	DESCRIPTION
06h[15:8],07h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
08h[15:8],09h[7:0]	Domain1 Relative Temperature Agent0 [15:0]
0Ah[15:8],0Bh[7:0]	Domain0 Relative Temperature Agent1 [15:0]
0Ch[15:8],0Dh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valid temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127℃ back to the temperature readouts.

8004_{HEX} ~ $81FF_{HEX}$	Reserved.	No further operation.

9.311 PECI Command Write Data Registers – Index 10h ~ 1Fh (Bank 2)

9.312 PECI Command Address Register – Index 10h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.313 PECI Command Write Length Register – Index 11h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.314 PECI Command Read Length Register – Index 12h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.315 PECI Command Code Register – Index 13h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.316 PECI Command Write Data 1 Register – Index 14h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.317 PECI Command Write Data 2 Register – Index 15h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.318 PECI Command Write Data 3 Register – Index 16h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.319 PECI Command Write Data 4 Register – Index 17h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.320 PECI Command Write Data 5 Register – Index 18h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.321 PECI Command Write Data 6 Register – Index 19h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.322 PECI Command Write Data 7 Register – Index 1Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 7							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.323 PECI Command Write Data 8 Register – Index 1Bh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.324 PECI Command Write Data 9 Register – Index 1Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.325 PECI Command Write Data 10 Register – Index 1Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.326 PECI Command Write Data 11 Register – Index 1Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.327 PECI Command Write Data 12 Register – Index 1Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	The data would be sent to client through issuing Manual Command.

9.328 PECI Command Read Data Registers – Index 20h ~ 24h (Bank 2)

9.329 PECI Absolute Temperature value Register – Index 20h-21h (Bank 2)

[ATH_Agent [8:2] +ATL_Agent[1:0]]] = Tbase + [RTH_Agent + RTL_Agent]

9.330 PECI Absolute Temperature value Register – Index 20h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Absolute Temperature Vaule[9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7-0	Absolute Temperature value of all Agent [9] (Sign bit) Absolute Temperature value of all Agent [8:2] (Integer bits)

BIT	DESCRIPTION
	Absolute Temperature value of all Agent [1:0] (Fraction bits)

9.331 PECI Absolute Temperature value Register – Index 21h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Absolute Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Absolute Temperature value of all Agent [9] (Sign bit) Absolute Temperature value of all Agent [8:2] (Integer bits) Absolute Temperature value of all Agent [1:0] (Fraction bits)

9.332 PECI Command Alive Agent and Warning Flag Register – Index 24h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Alive Agent[1:0]		Reserved		Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved
5	Agent 31 Alive Bit 1: agent31 is able to respond to Ping() command. Agent alive 0: agent31 isn't able to respond to Ping() command. Agent is not alive
4	Agent 30 Alive Bit 1: agent30 is able to respond to Ping() command. Agent alive 0: agent30 isn't able to respond to Ping() command. Agent is not alive
3-2	Reserved
1	Agent31 Alert Bit (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions.
0	Agent30 Alert Bit (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions.

9.333 PECI Command Read Data Register – Index 30h ~ 38h (Bank 2)

9.334 PECI Command Read Data 1 Register – Index 30h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.335 PECI Command Read Data 2 Register – Index 31h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.336 PECI Command Read Data 3 Register – Index 32h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.337 PECI Command Read Data 4 Register – Index 33h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.338 PECI Command Read Data 5 Register – Index 34h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.339 PECI Command Read Data 6 Register – Index 35h (Bank 2)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.340 PECI Command Read Data 7 Register – Index 36h (Bank 2)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.341 PECI Command Read Data 8 Register – Index 37h (Bank 2)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

9.342 PECI Command Read Data 9 Register – Index 38h (Bank 2)

Attribute: Read only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Retrieve related data from client through issuing Manual mode. The data would be getting from client.

PECI Manual Command Address Table

Command Bank 2	Address CR 10_{HEX}	Write Length CR 11_{HEX}	Read Length CR 12_{HEX}	Command Code CR 13_{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7

GetTemp		**01**	**02**	**01**
PCIRd30		**06**	**02 / 03 / 05**	**61**
PCIWr30		**08 / 09 / 0B**	**01**	**65**
PCIRdLocal30		**05**	**02 / 03 / 05**	**E1**
PCIWrLocal30		**07 / 08 / 0A**	**01**	**E5**
PKGRd30		**05**	**02 / 03 / 05**	**A1**
PKGWr30		**07 / 08 / 0A**	**01**	**A5**
IAMSRRd30		**05**	**02 / 03 / 05 / 09**	**B1**
IAMSRWr30		**07 / 08 / 0A / 0E**	**01**	**B5**

PECI Manual Command Read Data Table

Command	**PCI Rd30**	**PCI Wr30**	**PCIRd Local30**	**PCIWr Local30**	**PKG Rd30**	**PKG Wr30**	**IAMSR Rd30**	**IAMSR Wr30**	**GetDIB**	**GetTemp**
Command Code	**61**	**65**	**E1**	**E5**	**A1**	**A5**	**B1**	**B5**	**F7**	**01**
RdData 1 CR 30$_{HEX}$	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR 31$_{HEX}$	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3 CR 32$_{HEX}$	X	X	X	X	X	X	Data LSB_2	X	Revision Number	X
RdData 4 CR 33$_{HEX}$	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR 34$_{HEX}$	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6 CR 35$_{HEX}$	Data LSB_1	X	Data LSB_1	X	Data LSB_1	X	Data LSB_5	X	Reserved 3	X
RdData 7 CR 36$_{HEX}$	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 37$_{HEX}$	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9 CR 38$_{HEX}$	Data MSB	X	Data MSB	X	Data MSB	X	Data MSB	X	Reserved 6	Temp_HB

Note: X mean don't care

PECI Manual Command Write Data Table

Command	**PCI Rd30**	**PCI Wr30**	**PCIRd Local30**	**PCIWr Local30**	**PKG Rd30**	**PKG Wr30**	**IAMSR Rd30**	**IAMSR Wr30**
Command Code	**61**	**65**	**E1**	**E5**	**A1**	**A5**	**B1**	**B5**
WrData 1 CR 14$_{HEX}$	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID

WrData 2 CR 15$_{HEX}$	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Processor ID	Processor ID
WrData 3 CR 16$_{HEX}$	Addr LSB_2	Addr LSB_2	Addr LSB_2	Addr LSB_2	Param LSB	Param LSB	Addr LSB	Addr LSB
WrData 4 CR 17$_{HEX}$	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 18$_{HEX}$	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 19$_{HEX}$	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR 1A$_{HEX}$	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR 1B$_{HEX}$	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR 1C$_{HEX}$	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR 1D$_{HEX}$	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR 1E$_{HEX}$	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR 1F$_{HEX}$	X	X	X	X	X	X	X	Data MSB

Note: X mean don't care

9.343 Voltage and Temperature Read Register – Index 00h~0Fh (Bank 3)

Attribute: Read only at VSB domain

Size: 8 bits

ADDRESS 00-0F	DESCRIPTION
00h	CPUVCORE reading
01h	VIN0 reading
02h	AVSB reading
03h	3VCC reading
04h	VIN1 reading
05h	VIN2 reading
06h	Reserved
07h	3VSB reading.
08h	VBAT reading
09h	VTT reading
0Ah	Reserved
0Bh	Reserved

ADDRESS 00-0F	DESCRIPTION
0Ch	SYSTIN
0Dh	CPUTIN
0Eh	AUXTIN
0Fh	Reserved

9.344 SYSTIN Temperature Sensor Offset Register – Index 11h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.345 CPUTIN Temperature Sensor Offset Register – Index 12h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.346 AUXTIN Temperature Sensor Offset Register – Index13h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.347 Reserved Register – Index 14h ~ 16h (Bank 3)

9.348 Configuration Register – Index 17h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6-4	3	2	1	0
NAME	INITIALIZATION	Reserved	INT_CLEAR	Reserved	Reserved	START
DEFAULT	0	0	0	0	0	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	Reserved.
5	Reserved.
4	Reserved.
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	Reserved.
1	Reserved.
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.349 VBAT Monitor Control Register – Index 18h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	**DIODES 3. Sensor type selection for AUXTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
2	**DIODES 2. Sensor type selection for CPUTIN.** 1: Diode sensor. (default) 0: Thermistor sensor.

BIT	DESCRIPTION
1	**DIODES 1. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.350 Current Mode Enable Register – Index 19h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EN_ AUXTIN CURRENT MODE	EN_ CPUTIN CURRENT MODE	EN_ SYSTIN CURRENT MODE
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-3	Reserved.
2	**Enable AUXTIN Current Mode**. With AUXTIN is selected to Diode sensor (Bank3, Index 18h, Bit 3 = 1). 1: Temperature sensing of AUXTIN by Current Mode. 0: Temperature sensing of AUXTIN depends on the setting of Index 18h.(Default)
1	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank3, Index 18h, Bit 2 = 1). 1: Temperature sensing of CPUTIN by Current mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 18h.
0	**Enable SYSTIN Current Mode.** With SYSTIN is selected to Diode sensor (Bank3, Index 18h, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 18h. (Default)

9.351 Reserved Register – Index 1Ah ~ 8Fh (Bank 3)

9.352 PECI Agent Enable Register – Index 90h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	Reserved.
1	**Enable PECI Agent1 Mode.**
0	**Enable PECI Agent0 Mode.**

9.353 Reserved Register – Index 91h ~ B9h (Bank 3)

9.354 AUXFAN2 Max Duty Compare Source Select Register – Index BAh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Max Duty Compare Source Select				Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFAN2 Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
6	**AUXFAN2 Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
5	**AUXFAN2 Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty
4	**AUXFAN2 Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty
3-0	Reserved.

9.355 SYSFAN CPUFAN Max Duty Compare Source Select Register – Index BBh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Max Duty Compare Source Select				SYSFAN Max Duty Compare Source Select			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFAN Max Duty Source Select** 0: Disable AUXFAN2 Duty 1: Enable AUXFAN2 Duty

BIT	DESCRIPTION
6	**CPUFAN Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
5	**CPUFAN Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
4	**CPUFAN Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty
3	**SYSFAN Max Duty Source Select** 0: Disable AUXFAN2 Duty 1: Enable AUXFAN2 Duty
2	**SYSFAN Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
1	**SYSFAN Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
0	**SYSFAN Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty

9.356 AUXFAN0 AUXFAN1 Max Duty compare Source Select Register – Index BCh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Max Duty Compare Source Select				AUXFAN0 Max Duty Compare Source Select			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFAN1 Max Duty Source Select** 0: Disable AUXFAN2 Duty 1: Enable AUXFAN2 Duty
6	**AUXFAN1 Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
5	**AUXFAN1 Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty
4	**AUXFAN1 Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty
3	**AUXFAN0 Max Duty Source Select**

BIT	DESCRIPTION
	0: Disable AUXFAN2 Duty 1: Enable AUXFAN2 Duty
2	**AUXFAN0 Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
1	**AUXFAN0 Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty
0	**AUXFAN0 Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty

9.357 BEEP Control Register1 – Index C0h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**En3VSB_BP**	**EnVHIF_BP**	**EnVIN2_BP**	**EnVIN1_BP**	**En3VCC_BP**	**EnAVSB_BP**	**EnVIN0_BP**	**EnCPUVCORE_BP**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En3VSB_BP** 1 : Enable 3VSB Beep function 0 : Disable 3VSB Beep fuction
6	**EnVHIF_BP** 1 : Enable VHIF Beep function 0 : Disable VHIF Beep fuction
5	**EnVIN2_BP** 1 : Enable VIN2 Beep function 0 : Disable VIN2 Beep fuction
4	**EnVIN1_BP** 1 : Enable VIN1 Beep function 0 : Disable VIN1 Beep fuction
3	**En3VCC_BP** 1 : Enable 3VCC Beep function 0 : Disable 3VCC Beep fuction
2	**EnAVSB_BP** 1 : Enable AVSB Beep function 0 : Disable AVSB Beep fuction
1	**EnVIN0_BP** 1 : Enable VIN0 Beep function 0 : Disable VIN0 Beep fuction
0	**EnCPUVCORE_BP**

BIT	DESCRIPTION
	1 : Enable CPUVCORE Beep function 0 : Disable CPUVCORE Beep fuction

9.358 BEEP Control Register2 – Index C1h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				Reserved	Reserved	EnVTT_BP	EnVBAT_BP
DEFAULT	0				0	0	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	Reserved.
2	Reserved.
1	**EnVTT_BP** 1 : Enable VTT Beep function 0 : Disable VTT Beep fuction
0	**EnVBAT_BP** 1 : Enable VBAT Beep function 0 : Disable VBAT Beep fuction

9.359 BEEP Control Register3 – Index C2h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					EnT3_BP	EnT2_BP	EnT1_BP
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**EnT3_BP** 1 : Enable SMIOVT3 Beep function 0 : Disable SMIOVT3 Beep fuction
1	**EnT2_BP** 1 : Enable SMIOVT2 Beep function 0 : Disable SMIOVT2 Beep fuction
0	**EnT1_BP** 1 : Enable SMIOVT1 Beep function 0 : Disable SMIOVT1 Beep fuction

9.360 BEEP Control Register4 – Index C3h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	En AUXFANIN2 _BP	En AUXFANIN1 _BP	En AUXFANIN0 _BP	En CPUFANIN _BP	En SYSFANIN _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
4	**En AUXFANIN2_BP** 1 : Enable AUXFANIN2 Beep function 0 : Disable AUXFANIN2 Beep fuction
3	**En AUXFANIN1_BP** 1 : Enable AUXFANIN1 Beep function 0 : Disable AUXFANIN1 Beep fuction
2	**En AUXFANIN0_BP** 1 : Enable AUXFANIN0 Beep function 0 : Disable AUXFANIN0 Beep fuction
1	**En CPUFANIN _BP** 1 : Enable CPUFANIN Beep function 0 : Disable CPUFANIN Beep fuction
0	**En SYSFANIN _BP** 1 : Enable SYSFANIN Beep function 0 : Disable SYSFANIN Beep fuction

9.361 BEEP Control Register5 – Index C4h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	En Caseopen0_BP	Reserved	En_Beep
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	Reserved.
2	**En Caseopen0_BP** 1 : Enable Caseopen0_bp Beep function 0 : Disable Caseopen0_bp Beep fuction
1	Reserved.

BIT	DESCRIPTION
0	**Enable Beep Function:** 1 : Enable Beep Function 0 : Disable Beep Fuction

9.362 SYSFAN DUTY PER STEP Register – Index D8h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.363 CPUFAN DUTY PER STEP Register – Index D9h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.364 AUXFAN0 DUTY PER STEP Register – Index DAh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.

3-0	DOWN unit.

9.365 AUXFAN1 DUTY PER STEP Register – Index DBh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.366 AUXFAN2 DUTY PER STEP Register – Index DCh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.367 SYSFAN Max Duty Output Register – Index E0h (Bank 3)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	SYSFAN Max Duty Output

9.368 CPUFAN Max Duty Output Register – Index E1h (Bank 3)

Attribute: Read Only

Size: 8 bits
Reset by: PWROK

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	CPUFAN Max Duty Output

9.369 AUXFAN0 Max Duty Output Register – Index E2h (Bank 3)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	AUXFAN0 Max Duty Output

9.370 AUXFAN1 Max Duty Output Register – Index E3h (Bank 3)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	AUXFAN1 Max Duty Output

9.371 AUXFAN2 Max Duty Output Register – Index E4h (Bank 3)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
0	AUXFAN2 Max Duty Output

9.372 HM Read Only Register

ADDRESS A6-A0	DESCRIPTION
00h	CPUVCORE reading
01h	VIN0 reading
02h	AVSB reading
03h	3VCC reading
04h	VIN1 reading
05h	VIN2 reading
06h	VHIF reading
07h	3VSB reading
08h	VBAT reading
09h	VTT reading
0Ah	Reserved
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Reserved
0Fh	Reserved
10h	SYSTIN temperature reading
11h	CPUTIN temperature reading
12h	AUXTIN temperature reading
13h	Reserved
14h	Reserved
15h	Reserved
16h	Reserved
17h	Local temperature reading
18h	Reserved
19h	SYSFANOUT fan control temperature reading
1Ah	CPUFANOUT fan control temperature reading
1Bh	AUXFANOUT0 fan control temperature reading
1Ch	AUXFANOUT1 fan control temperature reading
1Dh	AUXFANOUT2 fan control temperature reading
1Eh	Reserved
1Fh	SYS_Weight temperature reading
20h	CPU_Weight temperature reading

ADDRESS A6-A0	DESCRIPTION
21h	AUX_Weight temperature reading
22h	SYSFAN duty target or rpm target reading
23h	CPUFAN duty target or rpm target reading
24h	AUXFAN0 duty target or rpm target reading
25h	AUXFAN1 duty target or rpm target reading
26h	AUXFAN2 duty target or rpm target reading
27h	Reserved
28h	SYSFAN rpm reading, unit 50rpm
29h	CPUFAN rpm reading, unit 50rpm
2Ah	AUXFAN0 rpm reading, unit 50rpm
2Bh	AUXFAN1 rpm reading, unit 50rpm
2Ch	AUXFAN2 rpm reading, unit 50rpm
2Dh	Reserved
2Eh	SYSFANIN COUNT High-byte reading
2Fh	SYSFANIN COUNT Low-byte reading
30h	CPUFANIN COUNT High-byte reading
31h	CPUFANIN COUNT Low-byte reading
32h	AUXFANIN0 COUNT High-byte reading
33h	AUXFANIN0 COUNT Low-byte reading
34h	AUXFANIN1 COUNT High-byte reading
35h	AUXFANIN1 COUNT Low-byte reading
36h	AUXFANIN2 COUNT High-byte reading
37h	AUXFANIN2 COUNT Low-byte reading
38h	Reserved
39h	Reserved
3Ah	SYSFANIN SPEED High-byte (rpm) reading
3Bh	SYSFANIN SPEED Low-byte (rpm) reading
3Ch	CPUFANIN SPEED High-byte (rpm) reading
3Dh	CPUFANIN SPEED Low-byte (rpm) reading
3Eh	AUXFANIN0 SPEED High-byte (rpm) reading
3Fh	AUXFANIN0 SPEED Low-byte (rpm) reading
40h	AUXFANIN1 SPEED High-byte (rpm) reading
41h	AUXFANIN1 SPEED Low-byte (rpm) reading
42h	AUXFANIN2 SPEED High-byte (rpm) reading
43h	AUXFANIN2 SPEED Low-byte (rpm) reading
44h	Reserved
45h	Reserved

ADDRESS A6-A0	DESCRIPTION
46h	Reserved
47h	Reserved
48h	Reserved
49h	Reserved
4Ah	Reserved
4Bh	Reserved
4Ch	SYSFANOUT Output Value reading
4Dh	CPUFANOUT Output Value reading
4Eh	AUXFANOUT0 Output Value reading
4Fh	AUXFANOUT1 Output Value reading
50h	AUXFANOUT2 Output Value reading
51h	Reserved
52h	PECI Agent 0 reading
53h	Reserved
54h	PECI Agent 1 reading
55h	Reserved
56h	PCH_CHIP_CPU_MAX_TEMP reading
57h	PCH_CHIP_TEMP reading
58h	PCH_CPU_TEMP_H reading
59h	PCH_CPU_TEMP_L reading
5Ah	PCH_MCH_TEMP reading
5Bh	Agent0 Dimm0 reading
5Ch	Agent0 Dimm1 reading
5Dh	Agent1 Dimm0 reading
5Eh	Agent1 Dimm1 reading
5Fh	PCH_TSI0_TEMP_H reading
60h	PCH_TSI0_TEMP_L reading
61h	PCH_TSI1_TEMP_H reading
62h	PCH_TSI1_TEMP_L reading
63h	Reserved
64h	Reserved
65h	Reserved
66h	Reserved
67h	Reserved
68h	Reserved
69h	Reserved
6Ah	Reserved

ADDRESS A6-A0	DESCRIPTION
6Bh	Reserved
6Ch	Reserved
6Dh	Reserved
6Eh	Reserved
6Fh	ByteTemp_H reading
70h	ByteTemp_L reading
71h	Reserved
72h	Reserved
73h	Reserved
74h	Reserved
75h	SMIOVT1 temperature source reading.
76h	SMIOVT2 temperature source reading.
77h	SMIOVT3 temperature source reading.

10. UART PORT

NCT6122D / NCT6126D supports 6 UART – UART A, UART B, UART C, UART D, UART E and UART F.

10.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0).
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits

DLS1	DLS0	DATA LENGTH
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

10.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	Reserved**.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	Reserved.	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	**16**	**80**	**112**
0	1	04	**32**	**88**	**116**
1	0	08	**48**	**96**	**120**
1	1	14	**64**	**104**	**124**

10.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION

7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.	
5-4	Reserved.	
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.

BIT	DESCRIPTION
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

10.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A.

10.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

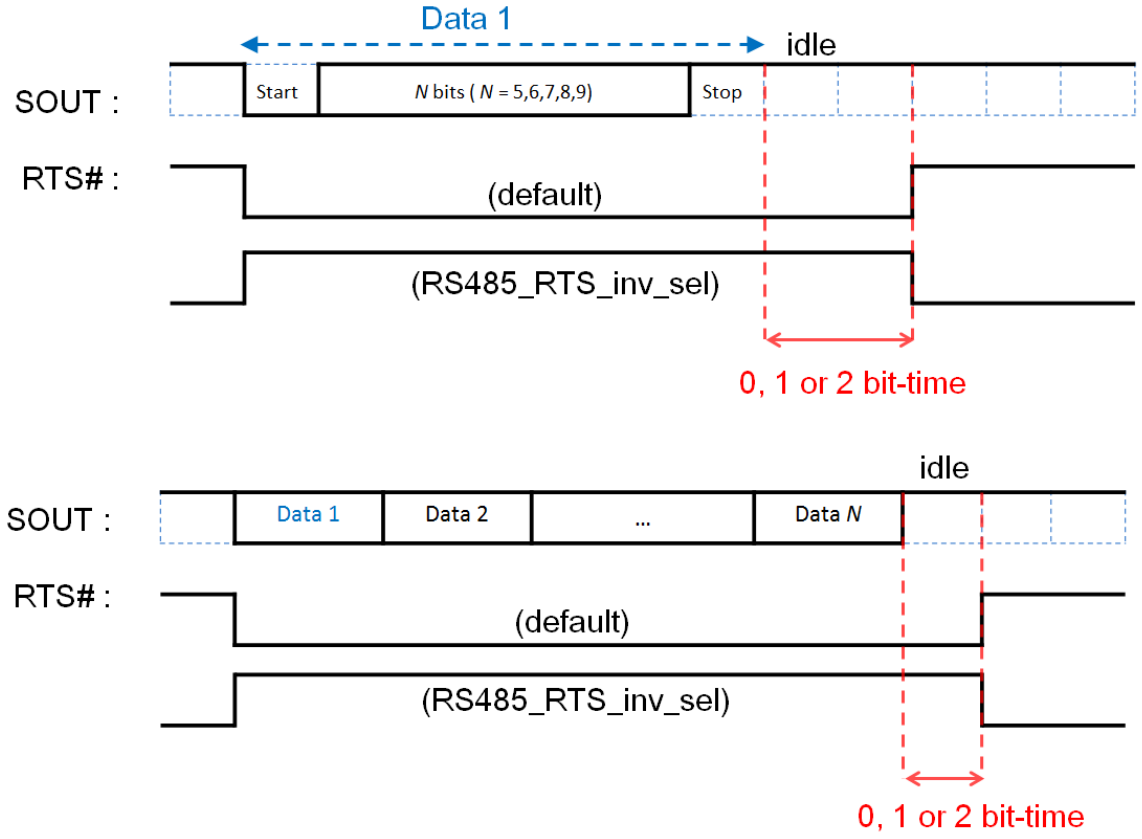
10.10 Extending FIFO

NCT6122D / NCT6126D supports FIFO size extending to 128bytes for RX and TX block. (Enable bit: CRF8, Bit0)

10.11 UART RS485 Auto Flow Control

NCT6122D / NCT6126D supports RS485 auto flow control function for UARTA ~ UARTF. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA ~ UARTF when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA ~ UARTF.



The default behavior of RTS# pin will drive logic low the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic high later than **Stop bit** about 0, 1 or 2 Bit-Time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA ~ UARTF.

	UARTA	UARTB	UARTC	UARTD	UARTE	UARTF
RTS485_enable	Logical Device 2, CRF2_Bit1	Logical Device 3, CRF2_Bit1	Logical Device 10, CRF2_Bit1	Logical Device 11, CRF2_Bit1	Logical Device 12, CRF2_Bit1	Logical Device 13, CRF2_Bit1
RTS485_inv_sel	Logical Device 2, CRF2_Bit4	Logical Device 3, CRF2_Bit4	Logical Device 10, CRF2_Bit4	Logical Device 11, CRF2_Bit4	Logical Device 12, CRF2_Bit4	Logical Device 13, CRF2_Bit4

RTS_low_time_sel	Logical Device 2, CRF2_Bit5	Logical Device 3, CRF2_Bit5	Logical Device 10, CRF2_Bit5	Logical Device 11, CRF2_Bit5	Logical Device 12, CRF2_Bit5	Logical Device 13, CRF2_Bit5
RTS485_no_delay	Logical Device 2, CRF7_Bit5	Logical Device 3, CRF7_Bit5	Logical Device 10, CRF7_Bit5	Logical Device 11, CRF7_Bit5	Logical Device 12, CRF7_Bit5	Logical Device 13, CRF7_Bit5

10.12 UART 9BIT-MODE

10.12.1 Function Description

► **Tx function block:**

1. 9bit-TX block supports 9bit-mode or original RS232 mode TX signal output.
2. 9bit-TX block supports sending address byte
   (Setting **En_9bit_mode =1** and **En_address_byte =1** will force parity bit turned to high bit)
3. 9bit-TX block supports 9bit-mode RS485 RTS or original RS232 mode RTS signal output.
4. 9bit-TX block supports 9bit-mode inverted and time selected for the RS485 RTS signal.
   (RS485 RTS time selected: one or two TXC period)
5. 9bit-TX block supports clear “en_address_byte” bit automatic.

	Register location (UART A) Logical Device 2	**Register location (UART B) Logical Device 3**	**Register location (UART C) Logical Device 10**	**Register location (UART D) Logical Device 11**	**Register location (UART E) Logical Device 12**	**Register location (UART F) Logical Device 13**
En_address_byte	CRF7_B7	CRF7_B7	CRF7_B7	CRF7_B7	CRF7_B7	CRF7_B7

► **Rx function block:**

1. 9bit-RX block supports 9bit-mode or original RS232 mode RX signal output.
2. 9bit-RX block supports comparison between with the slave address and broadcast address byte determined by the two registers. (see blow: slave_address and slave_address_mask registers)

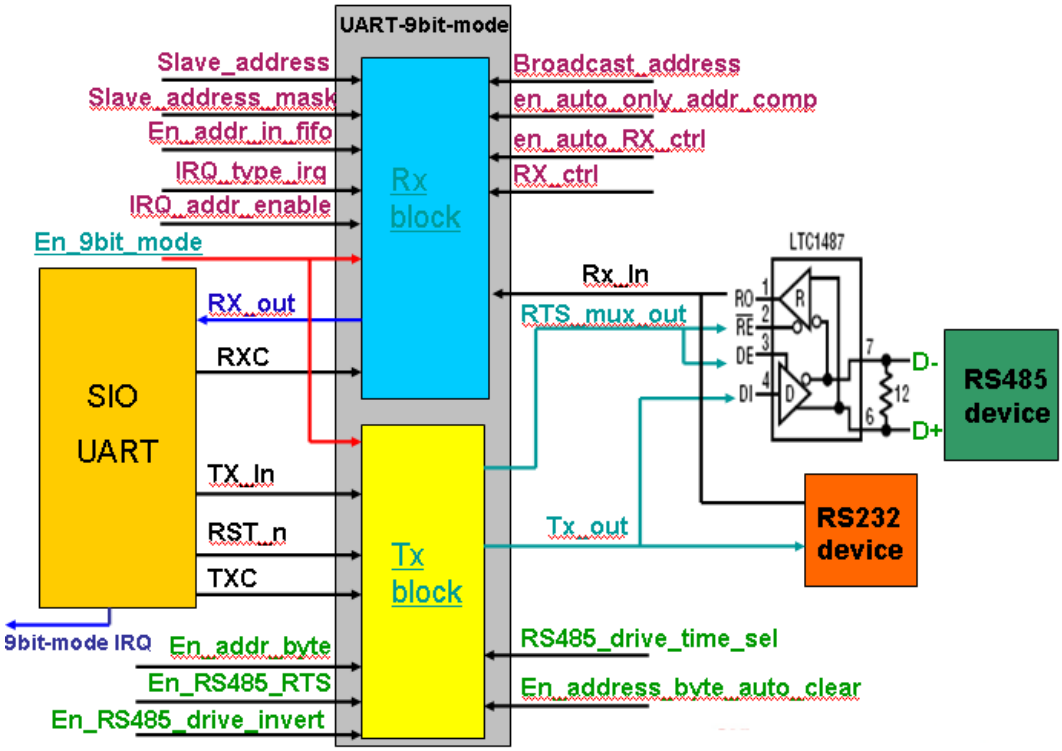
3. 9bit-RX block supports received address byte pass into RX block FIFO.
4. 9bit-RX block supports UART 9bit-mode IRQ output and could select to be issued only when receiving any address bytes or only received address matched.
5. 9bit-RX block will automatic modify parity bit of address/data byte to meet parity check from UART receiver block when using 9bit-bit mode.
6. 9bit-RX block supports different mode that have different functions by setting RX_ctrl_set[2:0].
   (default: RX_ctrl_set[2:0] = 000)

	Register location (UART A) Logical Device 2	Register location (UART B) Logical Device 3	Register location (UART C) Logical Device 10	Register location (UART D) Logical Device 11	Register location (UART E) Logical Device 12	Register location (UART F) Logical Device 13
RX_ctrl_set[2]: **(**en_auto_only_addr_comp**)**	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6	CRF2_B6
RX_ctrl_set[1]: **(**en_auto_RX_ctrl**)**	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7	CRF2_B7
RX_ctrl_set[0]: **(**RX_ctrl**)**	CRF7_B6	CRF7_B6	CRF7_B6	CRF7_B6	CRF7_B6	CRF7_B6

RX_ctrl_set[2:0]	Function Description
000	1. 9bit-mode RX block function will pass all data or address bytes to UART receiver block directly. 2. 9bit-mode RX block function will not compare any address byte. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
001	1. 9bit-mode RX block function will only pass address bytes to UART receiver block. 2. 9bit-mode RX block function will not compare any address byte. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
010	1. 9bit-mode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, 9bit-mode RX block function will update RX_ctrl=1 automatically. In order to receive address byte at next byte cycle. (RX block function will ignore the current address byte. Then the transmitter needs to resend this address byte again.) 2. 9bit-mode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
011	1. 9bit-mode RX block function will update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, 9bit-mode RX block function will update RX_ctrl=0 automatically. In order to receive data byte at next byte cycle. 2. 9bit-mode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block.

	4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
100 (The same as 000)	1. 9bit-mode RX block function will pass all data or address bytes to UART receiver block directly. 2. 9bit-mode RX block function will not compare any address byte. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
101 (The same as 001)	1. 9bit-mode RX block function will only pass address bytes to UART receiver block. 2. 9bit-mode RX block function will not compare any address byte. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
110	1. 9bit-mode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 0: If receive address byte, in order to receive the address byte, we need set RX_ctrl = 1 manually. 2. 9bit-mode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)
111	1. 9bit-mode RX block function will not update RX_ctrl Bit automatically. When RX_ctrl = 1: If address byte matched, in order to receive the proceeding data bytes, we need set RX_ctrl = 0 manually. 2. 9bit-mode RX block function will compare the address byte automatically and will pass the matched address or not depending on CRF2_B2 setting. 3. 9bit-mode RX block function will correct parity check bit before sending any data or address byte into UART receiver block. 4. 9bit-mode RX block function will generate IRQ. (Refer to CRF6 description.)

10.12.2 Function Block



10.13 UART switch

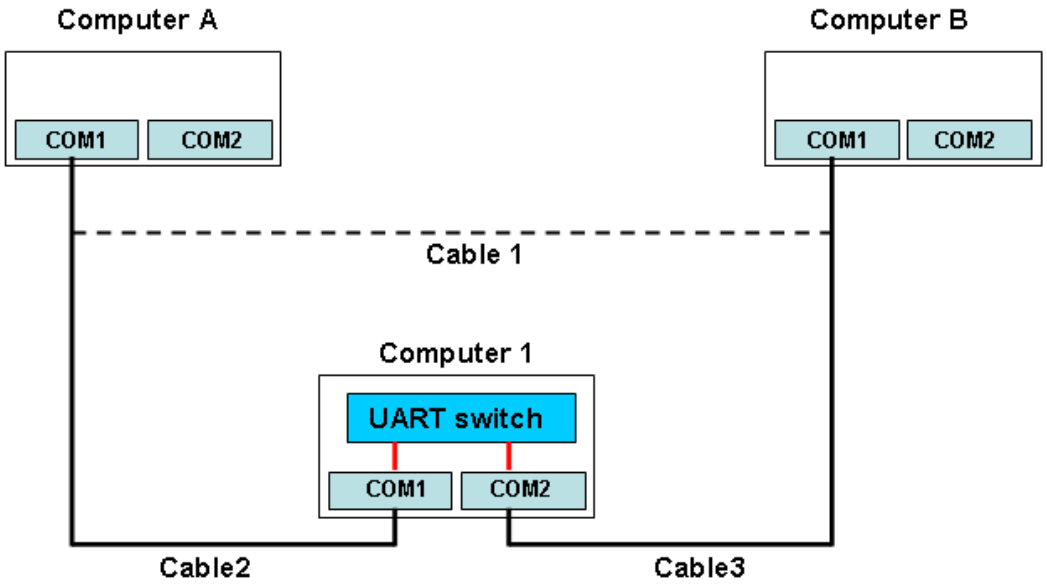
Due to the limitation length of the cable for the communication of UART,

We support 3 sets of switches to fix this limitation. They are UARTAB, UARTCD and UARTEF switches.

Switch Name	Switch Enable Bit	Description
UARTAB switch	Logical Device 02, IndexF8_Bit4	Connection with UARTA and UARTB
UARTCD switch	Logical Device 10, IndexF8_Bit4	Connection with UARTC and UARTD
UARTEF switch	Logical Device 12, IndexF8_Bit4	Connection with UARTE and UARTF

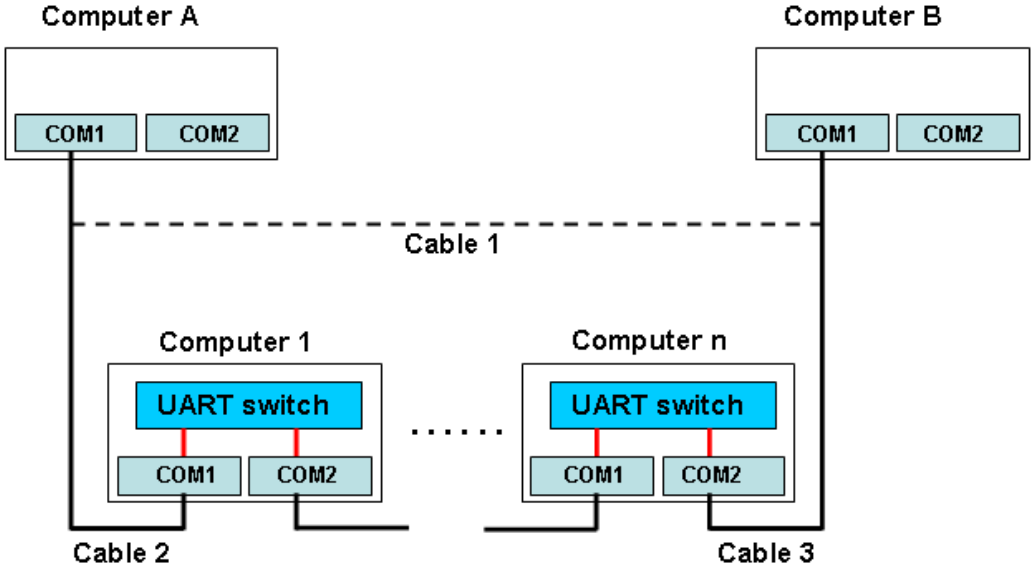
For example, if computer A and computer B will transfer data to each other with UART, but the distance between computer A and B is over the limitation length of the cable. See the figure in below, the cable 1 is over the limitation.

And we could use UART switch to fix this limitation. If the switch of computer1 is enabled, computer A could transfer data to computer 1 and computer 1 would bypass the data to computer B. In the same method, computer B also could achieve the goal to transfer data to computer A.



The connection of UART switch with single computer

We also could connect multi-switch to fix the limitation length of the cable, if the distance between computer A and computer B is too far. Below figure shows the connection method of multi-switch.



The connection of UART switch with multi-computer

11. PARALLEL PORT

11.1 Printer Interface Logic

The NCT6122D / NCT6126D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6122D / NCT6126D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 11-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF NCT6122D / NCT6126D	PIN ATTRIBUTE	SPP	EPP	ECP
1	47	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	35-42	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	34	I	nACK	Intr	nACK, PeriphClk[2]
11	33	I	BUSY	nWait	BUSY, PeriphAck[2]
12	32	I	PE	PE	Peerror, nAckReverse[2]
13	31	I	SLCT	Select	SLCT, Xflag[2]
14	46	O	Nafd	nDStrb	nAFD, HostAck[2]
15	45	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	44	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	43	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF NCT6122D / NCT6126D	PIN ATTRIBUTE	SPP
1	47	O	nSTB
2	42	I/O	PD0
3	41	I/O	PD1
4	40	I/O	PD2
5	39	I/O	PD3
6	38	I/O	PD4
7	37	I/O	PD5
8	36	I/O	PD6
9	35	I/O	PD7
10	34	I	nACK
11	33	I	BUSY
12	32	I	PE
13	31	I	SLCT
14	46	O	nAFD
15	45	I	nERR

HOST CONNECTOR	PIN NUMBER OF NCT6122D / NCT6126D	PIN ATTRIBUTE	SPP
16	44	O	nINIT
17	43	O	nSLIN

11.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 11-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 11-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7		6	5	4	3	2	1	0
Data Port (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#		ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1		1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1		1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7		PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

11.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

11.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0

NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	Reserved.
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means that no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

11.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	Reserved. These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

11.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

11.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

11.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
Nwrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
Nwait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

11.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

11.2.8 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

11.2.9 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

11.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6122D / NCT6126D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6122D / NCT6126D ECP supports the following modes.

Table 11-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)

MODE	DESCRIPTION
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

11.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 11-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 11-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	Perror	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

11.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

11.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	Perror	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**Perror.** This bit reflects the Perror input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

11.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	Reserved. These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes,

BIT	DESCRIPTION
	0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

11.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

11.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

11.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

11.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

11.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.

BIT	DESCRIPTION
5	**IRQx2.** Reflects the IRQ resource assigned for ECP port.
4	**IRQx1.**
3	**IRQx0.**

cnfgB[5:3]	IRQ resource
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

BIT	DESCRIPTION
2-0	Reserved. These three bits are logical 1 during a read and can be written.

11.3.10ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	**Mode.** Read/Write. These bits select the mode.

000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	EPP Mode. EPP mode is activated if the EPP mode is selected.
101	Reserved.
110	Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.

BIT	DESCRIPTION
	111 — Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.
3	**dmaEn.** Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

11.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
Nstrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
Perror (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.

NAME	TYPE	DESCRIPTION
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

11.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

11.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

11.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

11.3.12.3. Data Compression

The NCT6122D / NCT6126D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

11.3.13 FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

11.3.14 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or Cfifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

11.3.15 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

12. KEYBOARD CONTROLLER

The NCT6122D / NCT6126D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

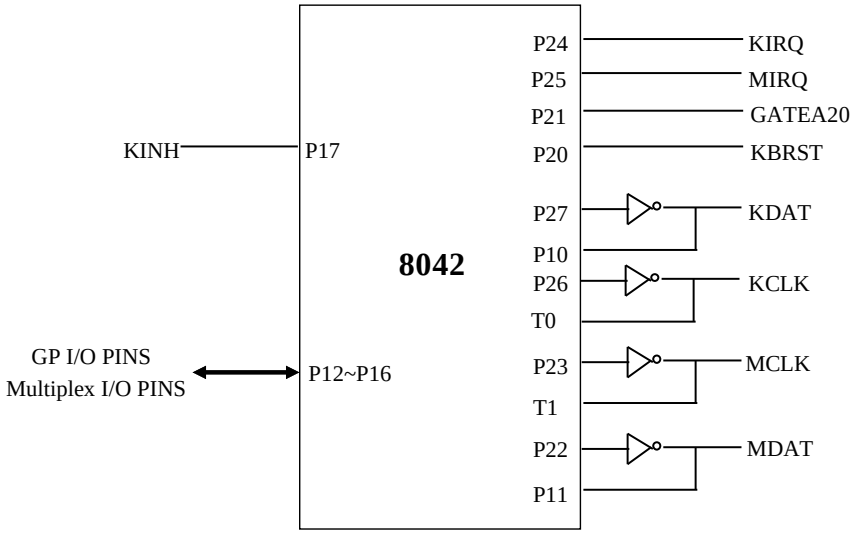


Figure 12-1 Keyboard and Mouse Interface

12.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

12.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

12.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 12-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	AUXiliary Device Output Buffer	0: AUXiliary device output buffer empty 1: AUXiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

12.4 Commands

Table 12-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable AUXiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable AUXiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>Adh</td><td>Disable Keyboard Interface</td></tr>
</table>

COMMAND	FUNCTION
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from AUXiliary Device
D4h	Output next received byte of data from system to AUXiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

12.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

12.5.1 KB Control Register (Logical Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	1	1

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	Reserved.	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

12.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

13. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of High and Low Level. The results are saved/stored in 32 bytes RX FIFO. The max widths of High and Low Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

13.1 CIR Register Table

Table 13-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	Reserved			RXEN	Reserved	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	Reserved			GH
base+2	IREN	RDR	RTR	PE	RFO	Reserved			GH
base+3	RXFCONT	RXFIFO Count							
base+4		Reserved							
base+5		Reserved							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved		
base+A	SRXFIFO	Sample RX FIFO							
base+B		Reserved							
base+C		Reserved							
base+D		Reserved							
base+E		Reserved							
base+F	IRFSM	R	Decoder FSM			Reserved			

13.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Resevered			RXEN	Reserved	RXINV	Sample Period Select	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-5	Reserved.
4	**RX Enable**
3	Reserved.
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

13.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3-1	Reserved.
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

13.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3-1	Reserved.
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

13.1.4 RX FIFO Count– Base Address + 3

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	**RX FIFO Count**

13.1.5 IR RX Sample Limited Count High Byte Register (SLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

13.1.6 IR RX Sample Limited Count Low Byte Register (SLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

13.1.7 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	**RX FIFO Cleared**.
2	Reserved.
1-0	**RX Trigger Level** **Bits** **1 0** 0 0 : 1 0 1 : 8 1 0 : 16 1 1 : 24

13.1.8 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
5	**RX FIFO Trigger Level Active**.
4	**RX FIFO Empty Flag**.
3	**RX FIFO Full Flag**.
2-0	Reserved.

13.1.9 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

13.1.10 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3-0	Reserved.

14. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT6122D / NCT6126D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

14.1 CIR WAKE-UP Register Table

Table 14-1 CIR Wake-Up Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending
base+2	IREN	RDR	RTR	PE	RFO	GH	R		
Base+3		FIFO_COMPARE_DEEP							
base+4		FIFO_COMPARE_TOLERANCE							
base+5		FIFO_Count							
Base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	SRXFSTS	GS	FTA	Empty	Full	R			
base+A		Sample RX FIFO							
base+B		WR_FIFO_DATA							
Base+C		Read FIFO Only							
Base+D		Read FIFO Only Index							
Base+E	IGNORE	FIFO_Ignore							
Base+F	IRFSM	R	Decoder FSM			R			Wakeup Event

14.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DEC_RST	Mode[1]	Mode[0]	RXEN	Ignore EN	RXINV	Sample Period Select	
DEFAULT	0	0	1	0	0	1	1	0

BIT	DESCRIPTION
7	**Reset CIR DECODER** (Write 1 to clear)
6	**Mode[1]** : 0: FIFO can't be written 1: FIFO can be written
5	**Mode[0]** 0: Learning Mode 1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	**RX Enable**
3	**Ignore Bit Enable**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

BIT	DESCRIPTION
2-1	Reserved.
0	**IR Pending** 1: No Interrupt 0: Interrupt issue

14.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**Min Length Detected**
2-0	Reserved.

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.4 IR FIFO Compare Depth Configuration Register – Base Address + 3

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Depth							
DEFAULT	0	1	0	0	0	0	1	1

14.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FIFO Data Tolerance between Learning mode and Wakeup mode**. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeup mode data)

14.1.6 RX FIFO Count– Base Address + 5

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	RX FIFO Count

14.1.7 IR RX Sample Limited Count High Byte Register (SLCH) – Base Address + 6

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.8 IR RX Sample Limited Count Low Byte Register (SLCL) – Base Address + 7

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	Reserved.
3	**RX FIFO Cleared.**
2	Reserved.
1-0	**RX Trigger Level** **Bits** **1 0** 0 0: 67 0 1: 66 1 0: 65 1 1: 64

14.1.10 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
6	**RX FIFO Trigger Level Active.**
5	**RX FIFO Empty Flag**.
4	**RX FIFO Full Flag**.
3-0	Reserved.

14.1.11 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.12 Write FIFO – Base Address + B

Attribute: Write Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

14.1.13 Read FIFO Only – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Voltage Level** 0: Low, 1: High
0	RX data length (Unit : Sample Period)

Note. Only Read FIFO Data.

14.1.14 Read FIFO Index – Base Address + D

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Indicate that FIFO Index when only read FIFO data(Base Address + C)

Note. Only Read FIFO Data.

14.1.15 FIFO Ignore (IGNORE) – Base Address + E

Attribute: Read / Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	FIFO Ignore						
DEFAULT	0	0	1	0	0	1	1	1

BIT	DESCRIPTION
7	Reserved.
6-0	Ignore the three data from the indicated fifo index (def. d'39)

14.1.16 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			Wakeup event
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved.
6-4	CIR State Machine
3-1	Reserved.
0	Wake up event: 0 : CIR wake up event has not been triggered. 1 : CIR wake up event has been triggered. (Wake up event Read clear.)

15. POWER MANAGEMENT EVENT

The PME# (pin 86) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and five registers in the NCT6122D / NCT6126D are associated with the PME# function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME# function. If this bit is set to "0", the NCT6122D / NCT6126D won't output any PME# signal when any of the wake-up events has occurred and is enabled. The five registers are divided into PME# status registers and PME# interrupt registers of wake-up events Note.1.

1) The PME# status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME# status should be cleared by writing a "1" before enabling its corresponding bit in the PME# interrupt registers
2) The PME# interrupt registers of wake-up event:
   - At Logical Device A, CR[F5h], CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME# wake-up events that the NCT6126D supports include:

i. Supporting S0, S1 states
   - UART IRQ event (A~F)
   - IR IRQ event
   - Hardware Monitor IRQ event
   - WDT1 event
   - Printer IRQ event

ii. Supporting S0i3 Note.2, S3, S5 states
   - Mouse event
   - Keyboard event
   - GPIO event (GPIO 44/45/63/64)
   - RIA (UARTA Ring Indicator) PIN event
   - RIB (UARTB Ring Indicator) PIN event

Note.2 For activating PME# in S0i3, please reference to LDE_CRFB[6].

15.1 Power Control Logic

This chapter describes how the NCT6122D / NCT6126D implements its ACPI function via these power control pins: PSIN# (Pin 68), PSOUT# (Pin 67), SLP_S3# (Pin 73) and PSON# (Pin 72). The following figure illustrates the relationships.

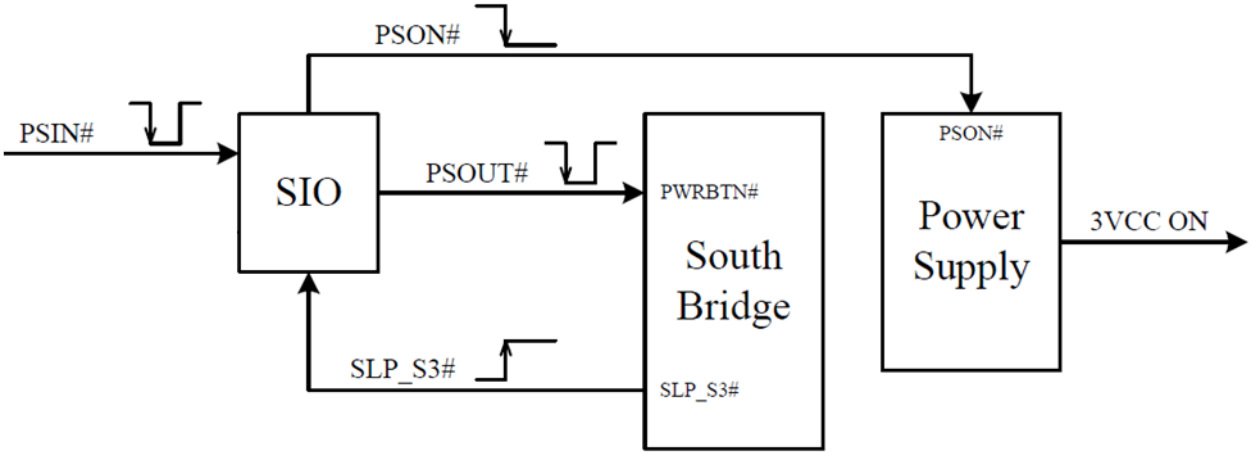


Figure 15-1 Power Control Mechanism

15.1.1 PSON# Logic

15.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 16-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

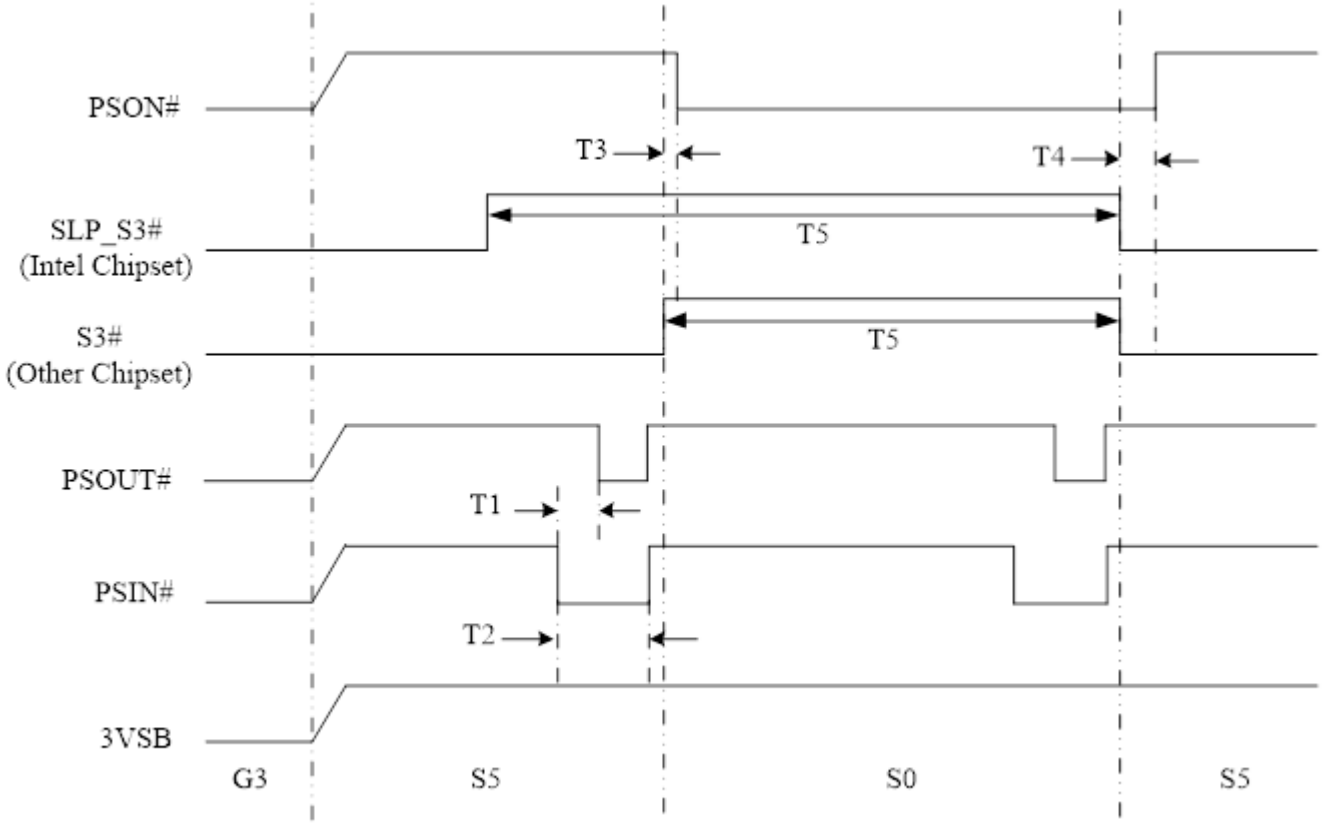


Figure 15-2 Power Sequence from S5 to S0, then Back to S5

15.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT6122D / NCT6126D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 15-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT6122D / NCT6126D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

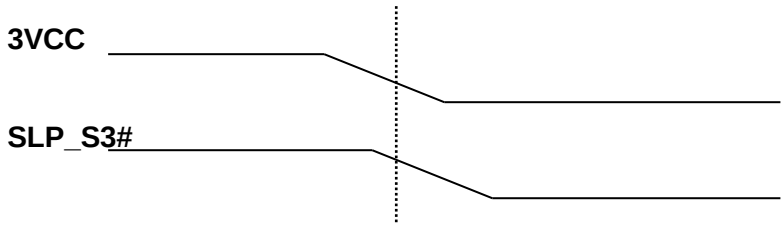


Figure 15-3 The previous state is “on”

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

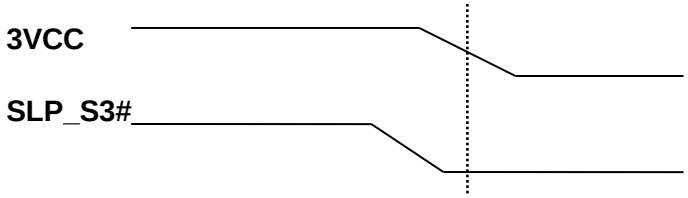


Figure 15-4 The previous state is “off”.

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6122D / NCT6126D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

15.2 Wake Up the System by Keyboard and Mouse

The NCT6122D / NCT6126D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT6122D / NCT6126D works.

15.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to “1”.

There are two keyboard events can be used for the wake-up

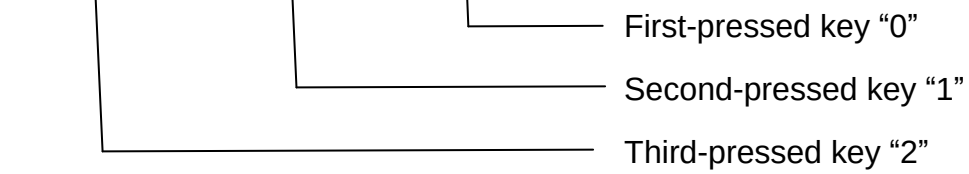
1) Any key – Set bit 0 at Logical Device A, CR[E0h] to “1” (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make

code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



15.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 15-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

15.3 Resume Reset Logic

The RSMRST# (Pin 75) signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT6122D / NCT6126D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-5 and Table 15-3.

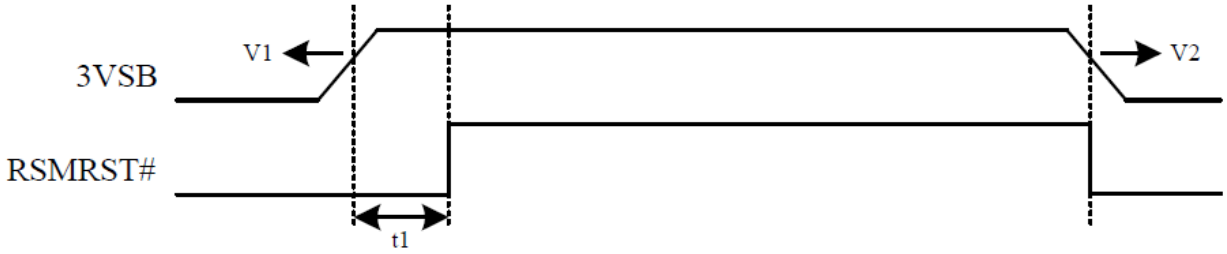


Figure 15-5 Mechanism of Resume Reset Logic

Table 15-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.1	V
V2	3VSB Ineffective Voltage	2.92	-	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

16. SERIALIZED IRQ

The NCT6122D / NCT6126D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

16.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6122D / NCT6126D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6122D / NCT6126D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

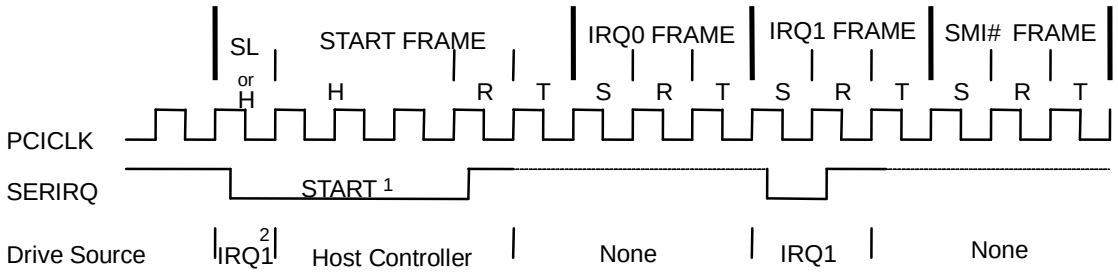


Figure 16-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6122D / NCT6126D because IRQ1 of the NCT6122D / NCT6126D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

16.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6122D / NCT6126D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6122D / NCT6126D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6122D / NCT6126D device drives the SERIRQ high. During the Turn-around phase, the NCT6122D / NCT6126D device leaves the SERIRQ tri-stated. The NCT6122D / NCT6126D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 16-1.

Table 16-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

16.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

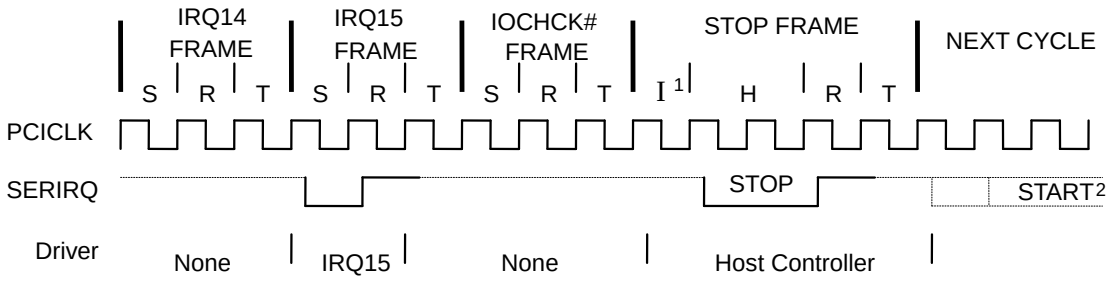


Figure 16-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

17. WATCHDOG TIMER

The Watchdog Timer of the NCT6122D / NCT6126D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9 and GPIOA provide an alternative WDT1 function. This function can be configured by the relative GPIO control register. WDT1 enable register is Logical Device 8 CR[30] bit[0]. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F0h], bit[3]. The time-out value is set at Logical Device 8 CR[F1h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0 bit[1], [5], GPIO2, bit[3], [7], GPIO3 bit[1], [5], GPIO5 bit[0], [4], GPIO6 bit[2], [7], GPIO7 bit[0], [4], GPIO8 bit[1], [5], GPIO9 bit[4] and GPIOA bit[4] will trigger a low pulse about 100mS. Also the event could go to pin77 WDTO#. When the value is counted down to zero, the timer stops, and the NCT6122D / NCT6126D sets the WDT1 status bit in Logical Device 8, CR[F2h], bit[4]. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# or PWROK signal is asserted.

Watchdog Timer 1 also provides ACPI associate functions. Write Logical Device D CRF0 bit[7] and [6] as 2'b01 make Watchdog Timer 1 event trigger 250ms low pulse on RSMRST#. Enable Logical Device 16 CRE3 bit[2] can generate 100ms PSOUT# low pulse after 1.5 second of RSMRST# low pulse. Timing illustrations are defined in Figure 17-1. Write Logical Device D CRF0 bit [7] and [6] as 2'b10 or 2'b11 make Watchdog Timer 1 event trigger PWROK or Internal SLPS3# make system get into DeepS5 state. Timing illustrations are defined in Figure 17-2 and 17-3.

The Watchdog Timer 2 of the NCT6122D / NCT6126D consists of an 8-bit programmable time-out counter register (Logical Device D, CRE2) and status register (Logical Device D, CRE4 bit7). When Logical Device D, CRE3[bit0] and Logical Device D, CRF0 bit[1] both are set to one, the timer will start count down. The timeout event will trigger PWROK pin to generate a 100ms low pulse. When Logical Device D, CRE3 bit[0] and CRF0 bit[1] are set to 2'b01. The timer will start count down when LRESET# drop. The timeout event will trigger PWROK pin to generate a 100ms low pulse.

The Watchdog Timer 3 can bit enable by Logical Device 9, CRE4 bit[2]. It will trigger 100ms low pulse to pin77 WDTO# at 6 second after entering S0 state each time system get into S0 state.

Watchdog Timer Time-Out Trigger Event	Watchdog Timer 1	Watchdog Timer 2	Watchdog Timer 3
KBRST#	✓	×	×
PWROK	×	✓	×
GPIO Pin	✓	×	×
WDTO# Pin	✓	×	✓
RSMRST# Event	✓	×	×
PWROK Event Then Into Deep S5	✓	×	×

Internal SLP_S3# Event Then Into Deep S5	✓	✖	✖

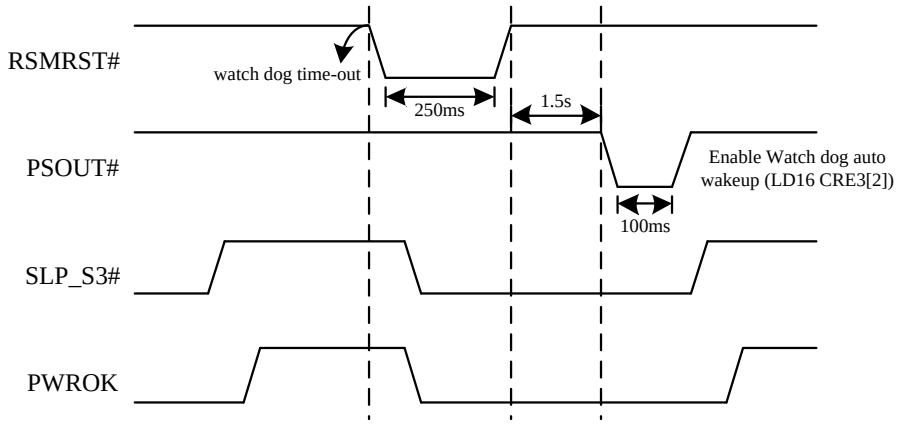


Figure 17-1 RSMRST# Event When Logical Device D CRF0 Bit[7] and Bit[6] as 2'b01

Enable auto wakeup by LD16 CRE3[2]. PSOUT# will pull low 100ms after Watchdog timer 1 to RSMRST# Event end for 1.5 second. If SLP_S3# pull high before the PSOUT# triggered. PSOUT# low pulse event will cancel.

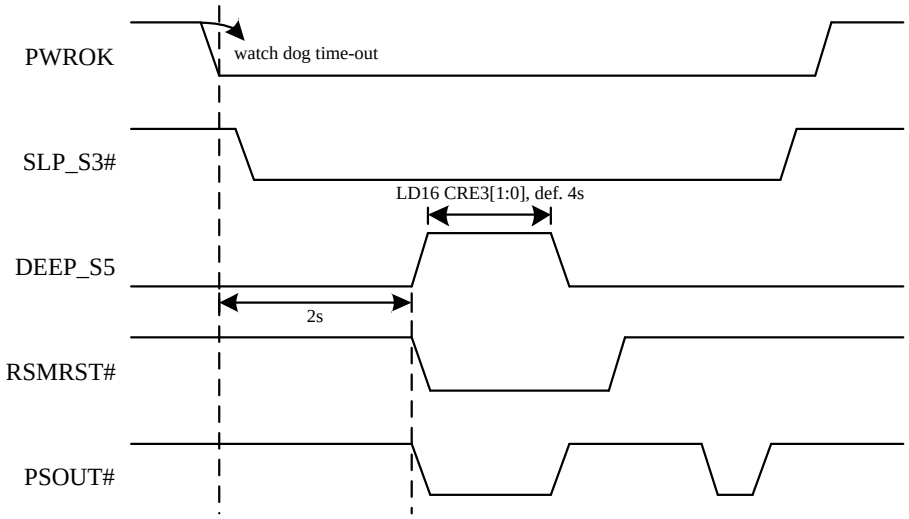


Figure 17-2 PWROK Event When Logical Device D CRF0 Bit[7] and Bit[6] as 2'b10

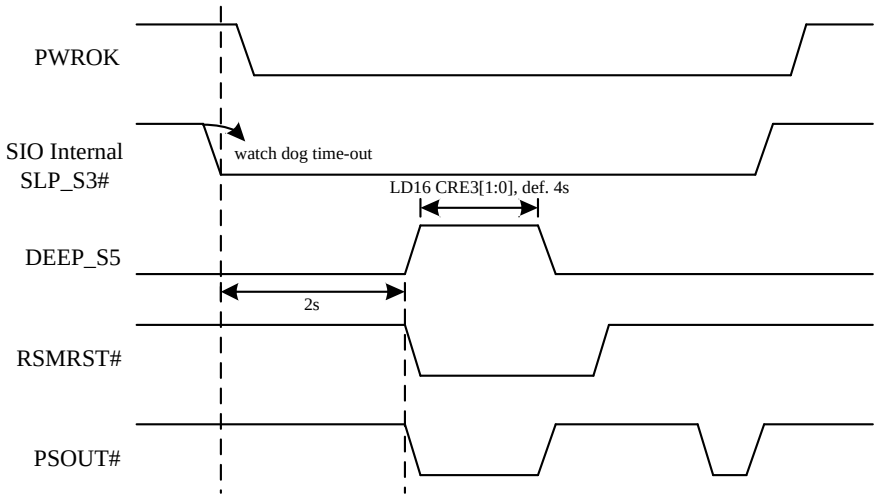


Figure 17-3 SLP_S3# Event When Logical Device D CRF0 Bit[7] and Bit[6] as 2'b11

18. GENERAL PURPOSE I/O

18.1 GPIO ARCHITECTURE

The NCT6122D / NCT6126D provides 72 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO port 0 ~ 7 is configured through control registers in Logical Device 7. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inverse). Port value is read/written through data register.

In addition, only GP63, GP64, GP44 and GP45 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has falling transitions. The following table gives more detailed register map on GP63, GP64, GP44 and GP45.

Table 18-1 Relative Control Registers of GPIO 63, 64, 44 and 45 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) **0: DISABLE** **1: ENABLE**	**EVENTROUTE II (PME#)** **0: DISABLE** **1: ENABLE**	**EVENT STATUS (PSOUT#, W1C)**	**EVENT STATUS (PME, W1C)**
GP63	LD9, CR E3h, Bit[7]	LD9, CR E3h, Bit[3]	LDE, CR E3h, Bit[7]	LDA, CRFAh, Bit[7]
GP64	LD9, CR E3h, Bit[6]	LD9, CR E3h, Bit[2]	LDE, CR E3h, Bit[6]	LDA, CRFAh, Bit[6]
GP44	LD9, CR E3h, Bit[5]	LD9, CR E3h, Bit[1]	LDE, CR E3h, Bit[5]	LDA, CRFAh, Bit[5]
GP45	LD9, CR E3h, Bit[4]	LD9, CR E3h, Bit[0]	LDE, CR E3h, Bit[4]	LDA, CRFAh, Bit[4]

Table 18-2 GPIO Group Programming Table

Equips maximum 72-pin GPIOs.

GPIO0 Group

Enable: Logical Device 7, CR30[0]
Data: Logical Device 7, E0h~E3h
Multi-function: YLW, GRN, WDTO#, SUSLED (Logical Device 8, CRE0[7-0])
Reset: Logical Device 9, CRE2[0]
OD/PP: Logical Device F, CRE0

Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP00	109	GP00	input	3VSB	
GP01	110	GP01	input	3VSB	
GP02	111	GP02	input	3VSB	
GP03	112	GP03	input	3VSB	
GP04	113	GP04	input	3VSB	
GP05	114	GP05	input	3VSB	
GP06	115	GP06	input	3VSB	
GP07	116	GP07	input	3VSB	

GPIO1 Group

Enable: Logical Device 7, CR30[1]
Data: Logical Device 7, E4h~E7h
Multi-function: YLW, GRN, BEEP, SMI (Logical Device 8, CRE1[7-0])
Reset: Logical Device 9, CRE2[1]
OD/PP: Logical Device F, CRE1

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP10	117	GP10	input	3VSB	
GP11	118	GP11	input	3VSB	
GP12	119	GP12	input	3VSB	
GP13	120	GP13	input	3VSB	
GP14	121	GP14	input	3VSB	
GP15	122	GP15	input	3VSB	
GP16	123	GP16	input	3VSB	
GP17	124	GP17	input	3VSB	

GPIO2 Group

Enable: Logical Device 7, CR30[2]
Data: Logical Device 7, E8h~Ebh
Multi-function: WDTO#, BEEP, SMI, PLED (Logical Device 8, CRE2[7-0])
Reset: Logical Device 9, CRE2[2]
OD/PP: Logical Device F, CRE2

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP20	125	GP20	input	3VSB	
GP21	126	GP21	input	3VSB	
GP22	127	GP22	input	3VSB	
GP23	128	GP23	input	3VSB	
GP24	1	GP24	input	3VSB	
GP25	2	GP25	input	3VSB	
GP26	3	GP26	input	3VSB	
GP27	4	GP27	input	3VSB	

GPIO3 Group

Enable: Logical Device 7, CR30[3]
Data: Logical Device 7, Ech~Efh
Multi-function: BEEP, SMI, WDTO#, SUSLED (Logical Device 8, CRE3[7-0])
Reset: Logical Device 9, CRE2[3]
OD/PP: Logical Device F, CRE3

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP30	32	GP30	input	3VSB	
GP31	33	GP31	input	3VSB	
GP32	34	GP32	input	3VSB	
GP33	35	GP33	input	3VSB	
GP34	36	GP34	input	3VSB	

GP35	37	GP35	input	3VSB	
GP36	38	GP36	input	3VSB	
GP37	39	GP37	input	3VSB	

GPIO4 Group
Enable: Logical Device 7, CR30[4]
Data: Logical Device 7, F0h~F3h
Multi-function: YLW, GRN, PLED, SMI (Logical Device 8, CRE4[7-0])
Reset: Logical Device 9, CRE2[4]
OD/PP: Logical Device F, CRE4

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP40	40	GP40	input	3VSB	
GP41	41	GP41	input	3VSB	
GP42	42	GP42	input	3VSB	
GP43	43	GP43	input	3VSB	
GP44	44	GP44	input	3VSB	
GP45	45	GP45	input	3VSB	
GP46	46	GP46	input	3VSB	
GP47	47	GP47	input	3VSB	

GPIO5 Group
Enable: Logical Device 7, CR30[5]
Data: Logical Device 7, F4h~F7h
Multi-function: YLW, GRN, BEEP, WDTO# (Logical Device 8, CRE5[7-0])
Reset: Logical Device 9, CRE2[5]
OD/PP: Logical Device F, CRE5

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP50	62	(KBC_EN)		(KBC_EN)		3VSB	CR1A[3] = 1
		0	SDA	0	output (OD)		
		1	KCLK	1	bi-direction		
GP51	63	(KBC_EN)		(KBC_EN)		3VSB	CR1A[3] = 1
		0	SCL	0	output (OD)		
		1	KDAT	1	bi-direction		
GP52	65	(KBC_EN)		(KBC_EN)		3VSB	
		0	GP52	0	input		
		1	MCLK	1	bi-direction		
GP53	66	{KBC_ EN}		{KBC_ EN}		3VSB	
		0	GP53	0	input		
		1	MDAT	1	bi-direction		
GP54	67	PSOUT#		output		3VSB	CR1A[1] = 1
GP55	68	PSIN#		input		3VSB	CR1A[0] = 1
GP56	70	SLP_S5#		input		3VSB	CR1B[7] = 1
GP57	71	PWROK		output (OD)		VRTC	CR1B[6] = 1

GPIO6 Group
Enable: Logical Device 7, CR30[6]
Data: Logical Device 7, F8h~FBh
Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logical Device 8, CRE6[7-0], CRE7[7-5])
Reset: Logical Device 9, CRE2[6]
OD/PP: Logical Device F, CRE6

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP60	72	PSON#	output (OD)	3VSB	CR1B[5] = 1
GP61	73	SLP_S3#	input	3VSB	CR1B[4] = 1
GP62	75	RSMRST#	output (OD)	VRTC	CR1B[3] = 1
GP63	94	SDA	input	3VSB	CR1B[1:0] = 2'b00, CR2A[1]=0
GP64	96	SCL	input	3VSB	CR1B[1:0] = 2'b00, CR2A[1]=0
GP65	106	SUSLED	output	3VSB	CR1C[6]=1
GP66	107	THERMTRIP#	input	3VSB	LD9_CRE1[4]=0, CR1C[5]=1
GP67	108	GP67	input	3VSB	LDA_CRF8[2:1]=01

GPIO7 Group
Enable: Logical Device 7, CR30[7]
Data: Logical Device 7, FCh~FFh
Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logical Device 8, CRE8[7-0])
Reset: Logical Device 9, CRE2[7]
OD/PP: Logical Device F, CRE7

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP70	5	GP70	input	3VSB	
GP71	17	GP71	input	3VSB	
GP72	7	GP72	input	3VSB	
GP73	8	GP73	input	3VSB	
GP74	9	GP74	input	3VSB	
GP75	10	GP75	input	3VSB	
GP76	11	GP76	input	3VSB	
GP77	13	GP77	input	3VSB	

GPIO8 Group
Enable: Logical Device 9, CR30[0]
Data: Logical Device 9, F0h~F3h
Multi-function: YLW, GRN, BEEP, SMI, WDTO#, SUSLED, PLED (Logical Device 8, CRE9[7-0])
Reset: Logical Device 9, CRE1[0]
OD/PP: Logical Device F, CRE8

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP80	14	AUXFANOUT0	output	3VSB	CR2B[4] = 1
GP81	6	AUXFANIN0	input	3VSB	CR2B[4] = 1
GP82	18	GP82	input	3VSB	CR2B[3] = 0
GP83	69	GP83	Input	3VSB	
GP84	77	WDTO#	output (OD)	3VSB	CR2A[3] = 1

GP85	86	PME#	output (OD)	3VSB	LDE_CRE6[7] = 1
GP86	87	GP86	Input	3VSB	
GP87	95	OVT#	Output(OD)	3VSB	CR1D[3:2] = 1x

GPIO9 Group
Enable: Logical Device 9, CR30[1]
Data: Logical Device 9, F4h~F7h
Multi-function: SUSLED, BEEP, SMI, WDT1, YLW, GRN,SMI, PLED (Logical Device 8, CREA[7-0])
Reset: Logical Device 9, CRE1[1]
OD/PP: Logical Device F, CRE9

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP90	78	CTSB#	input	3VSB	CR2C[3:2]=0x or 10
GP91	79	DSRB#	input	3VSB	CR2C[3:2]=0x or 10
GP92	80	RTSB#	input	3VSB	CR2C[3:2]=0x
GP93	81	DTRB#	Input	3VSB	CR2C[3:2]=0x or 10
GP94	82	SINB	input	3VSB	CR2C[3:2]=00
GP95	83	SOUTB#	input	3VSB	CR2C[3:2]=00
GP96	84	DCDB#	input	3VSB	CR2C[3:2]=0x or 10
GP97	85	RIB#	input	3VSB	CR2C[3:2]=0x or 10

GPIOA Group
Enable: Logical Device 9, CR30[2]
Data: Logical Device 9, F8h~FBh
Multi-function: SUSLED, BEEP, SMI, WDT1, YLW, GRN,SMI, PLED (Logical Device 8, CREB[7-0])
Reset: Logical Device 9, CRE1[2]
OD/PP: Logical Device F, CREA

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GPA0	49	CTSA#	input	3VSB	CR2C[1:0]=0x or 10
GPA1	50	DSRA#	input	3VSB	CR2C[1:0]=0x or 10
GPA2	51	RTSA#	input	3VSB	CR2C[1:0]=0x
GPA3	52	DTRA#	Input	3VSB	CR2C[1:0]=0x or 10
GPA4	53	SINA	input	3VSB	CR2C[1:0]=00
GPA5	54	SOUTA	input	3VSB	CR2C[1:0]=00
GPA6	56	DCDA#	input	3VSB	CR2C[1:0]=0x or 10
GPA7	57	RIA#	input	3VSB	CR2C[1:0]=0x or 10

GPIOB Group
Enable: Logical Device 9, CR30[3]
Data: Logical Device 9, FCh~FFh
Multi-function:BEEP (Logical Device 8, CREC[0])
Reset: Logical Device 9, CRE1[3]
OD/PP: Logical Device F, CREB

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GPB0	19	GPB0	input	3VSB	LDE_CRF4[3]

Table 18-3 GPIO Multi-Function Routing Table

GPIO Multi-Function Routing												
Bit	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8	GPIO9	GPIOA	GPIOB
7	0: GPIO07 1: YLW	0: GPIO17 1: YLW	0: GPIO27 1: WDTO#	0: GPIO37 1: BEEP	0: GPIO47 1: YLW	0: GPIO57 1: YLW	-	0: GPIO77 1: PLED	0: GPIO87 1: YLW	0: GPIO97 1: SUSLED	0: GPIOA7 1: SUSLED	-
6	0: GPIO06 1: GRN	0: GPIO16 1: GRN	0: GPIO26 1: BEEP	0: GPIO36 1: SMI	0: GPIO46 1: GRN	0: GPIO56 1: GRN	0: GPIO66 1: YLW	0: GPIO76 1: BEEP	0: GPIO86 1: SMI	0: GPIO96 1: BEEP	0: GPIOA6 1: BEEP	-
5	0: GPIO05 1: WDTO#	0: GPIO15 1: BEEP	0: GPIO25 1: SMI	0: GPIO35 1: WDTO#	0: GPIO45 1: PLED	0: GPIO55 1: BEEP	0: GPIO65 1: GRN	0: GPIO75 1: SMI	0: GPIO85 1: WDT1	0: GPIO95 1: SMI	0: GPIOA5 1: SMI	-
4	0: GPIO04 1: SUSLED	0: GPIO14 1: SMI	0: GPIO24 1: PLED	0: GPIO34 1: SUSLED	0: GPIO44 1: SMI	0: GPIO54 1: WDTO#	0: GPIO64 1: BEEP	0: GPIO74 1: WDT1	0: GPIO84 1: BEEP	0: GPIO94 1: WDT1	0: GPIOA4 1: WDT1	-
3	0: GPIO03 1: YLW	0: GPIO13 1: YLW	0: GPIO23 1: WDTO#	0: GPIO33 1: BEEP	0: GPIO43 1: YLW	0: GPIO53 1: YLW	0: GPIO63 1: SMI	0: GPIO73 1: PLED	0: GPIO83 1: YLW	0: GPIO93 1: YLW	0: GPIOA3 1: YLW	-
2	0: GPIO02 1: GRN	0: GPIO12 1: GRN	0: GPIO22 1: BEEP	0: GPIO32 1: SMI	0: GPIO42 1: GRN	0: GPIO52 1: GRN	0: GPIO62 1: WDTO#	0: GPIO72 1: BEEP	0: GPIO82 1: SMI	0: GPIO92 1: GRN	0: GPIOA2 1: GRN	-
1	0: GPIO01 1: WDTO#	0: GPIO11 1: BEEP	0: GPIO21 1: SMI	0: GPIO31 1: WDTO#	0: GPIO41 1: PLED	0: GPIO51 1: BEEP	0: GPIO61 1: SUSLED	0: GPIO71 1: SMI	0: GPIO81 1: WDT1	0: GPIO91 1: SMI	0: GPIOA1 1: SMI	-
0	0: GPIO00 1: SUSLED	0: GPIO10 1: SMI	0: GPIO20 1: PLED	0: GPIO30 1: SUSLED	0: GPIO40 1: SMI	0: GPIO50 1: WDTO#	0: GPIO60 1: PLED	0: GPIO70 1: WDT1	0: GPIO80 1: BEEP	0: GPIO90 1: PLED	0: GPIOA0 1: PLED	0: GPIOB0 1 :BEEP

18.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS strapping). The registers can be read / written only when the respective Logical Device ID and port number are selected.

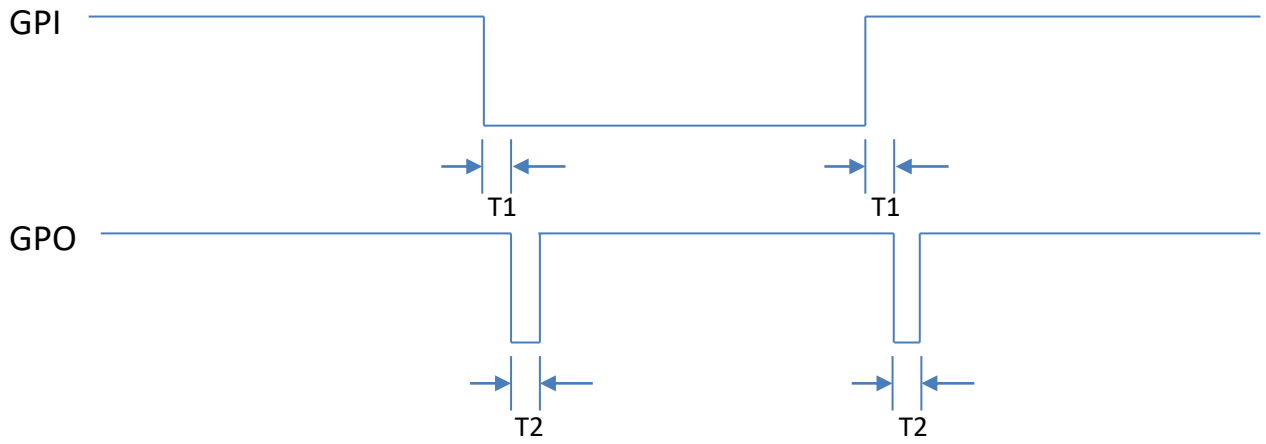
The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 18-4. Base address plus 0 to 4 are GPIO registers, base address plus 5 ,6 and 7 are watchdog registers. Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#7 for GPIO0 ~ GPIO7 respectively). Then the I/O register, the Data register, the Inversion register and the Status register are mapped to addresses Base+1, Base+2, Base+3 and Base+4 respectively. Only one GPIO can be accessed at one time.

Table 18-4 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer I(WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Counter Register							
Base + 7	Wdtsts	Watchdog Timer I (WDT1) Control & Status Register							

18.3 GPIO TRANSITION

NCT6122D / NCT6126D support GPIO transition function, CR[1A] bit[5:4] control GPIO transition pins from other function to this, when CR[1A] bit[5:4] set to 2'b10, two pins select to GPIO transition function, AFD# is GPI control pin, and STB# is GPO output pin. The GPIO transition timing chart shows as below, when GPI transition (high to low or low to high), after about 100ms (T1 delay), to issue about 10ms, 50ms, 100ms(default), or 200ms pulse (T2 delay) to trigger GPO pin, the pulse (T2 delay) controlled by LDF CR[F4] bit[7:6]. The GPIO transition function must be work under GPIO transition enable bit as one, which controlled by LDF CR[F4] bit[0].



19. SMBUS MASTER INTERFACE

19.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I²C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- SMBus and I²C compliant
- AMD-TSI
- PCH
- SMBus master

19.2 Introduction to the SMBus Master

19.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

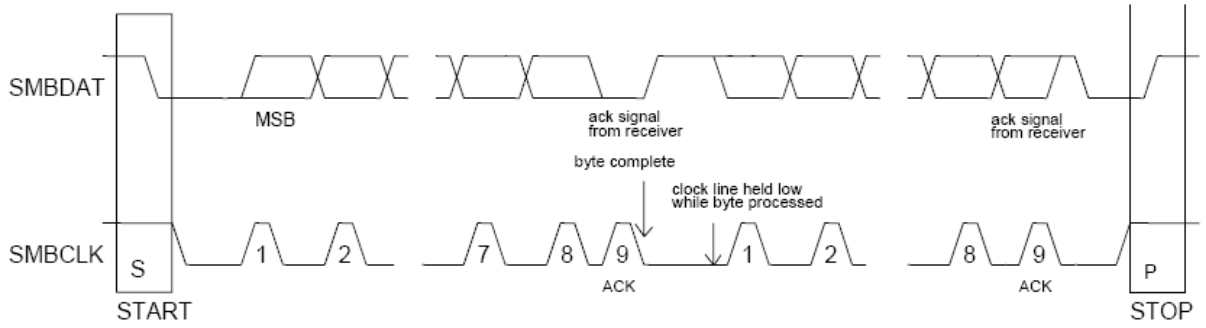


Figure 19-1 Data Transfer Format

19.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

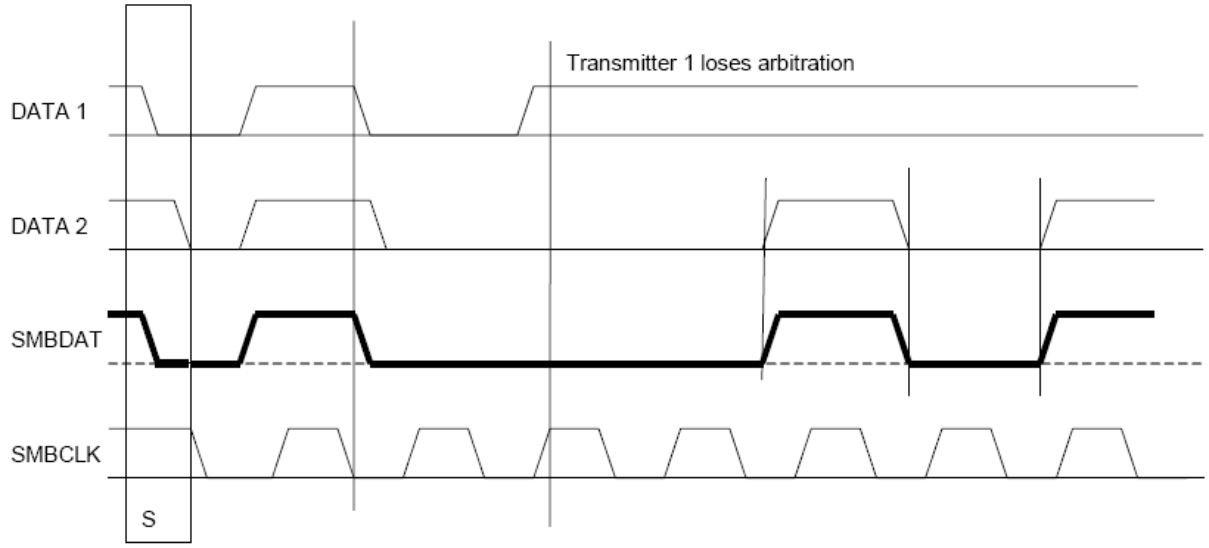


Figure 19-2 SMBus Arbitration

19.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore, the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

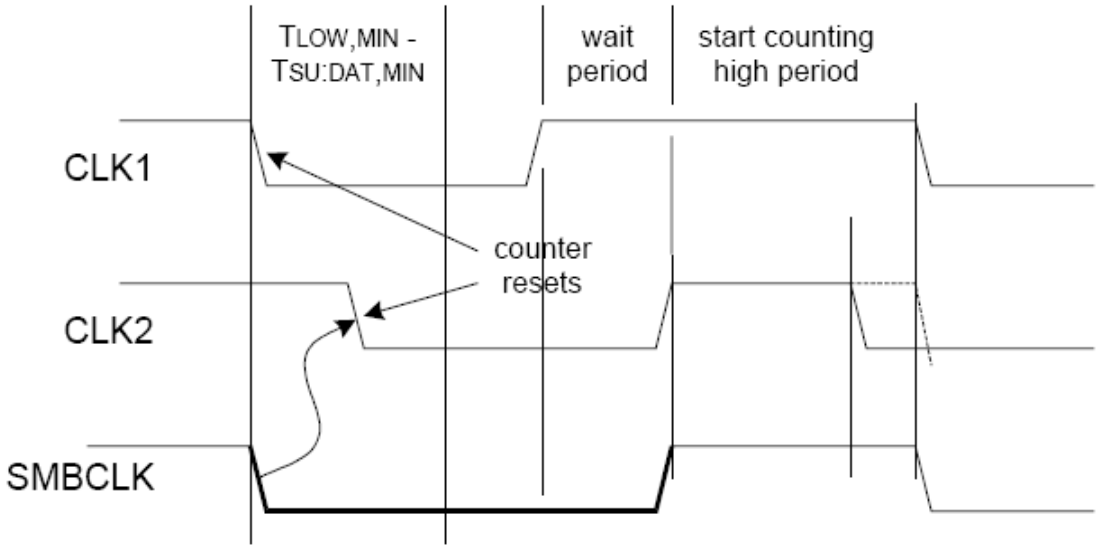


Figure 19-3 Clock synchronization

19.3 SB-TSI

The combined-format repeated start sequence is not supported in standard-mode and fast-mode.

- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

19.3.1 SB-TSI Address

The SMBus address is really 7 bits. The SB-TSI address is normally 98h or 4Ch. The address could vary with address select bits.

Table 19-1 SB-TSI Address Encoding

Address Select Bits	SB-TSI Address
000b	98h
001b	9Ah
010b	9Ch
011b	9Eh
100b	90h
101b	92h
110b	94h
111b	96h

19.4 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH and be programmed to alert the EC when a device has gone outside of its temperature limits.

19.4.1 Command Summary

Table 19-2 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Command	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		
Write MCH Temp Limits	I2C	0x43	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		

Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

19.5 SMBus Master

19.5.1 Block Diagram

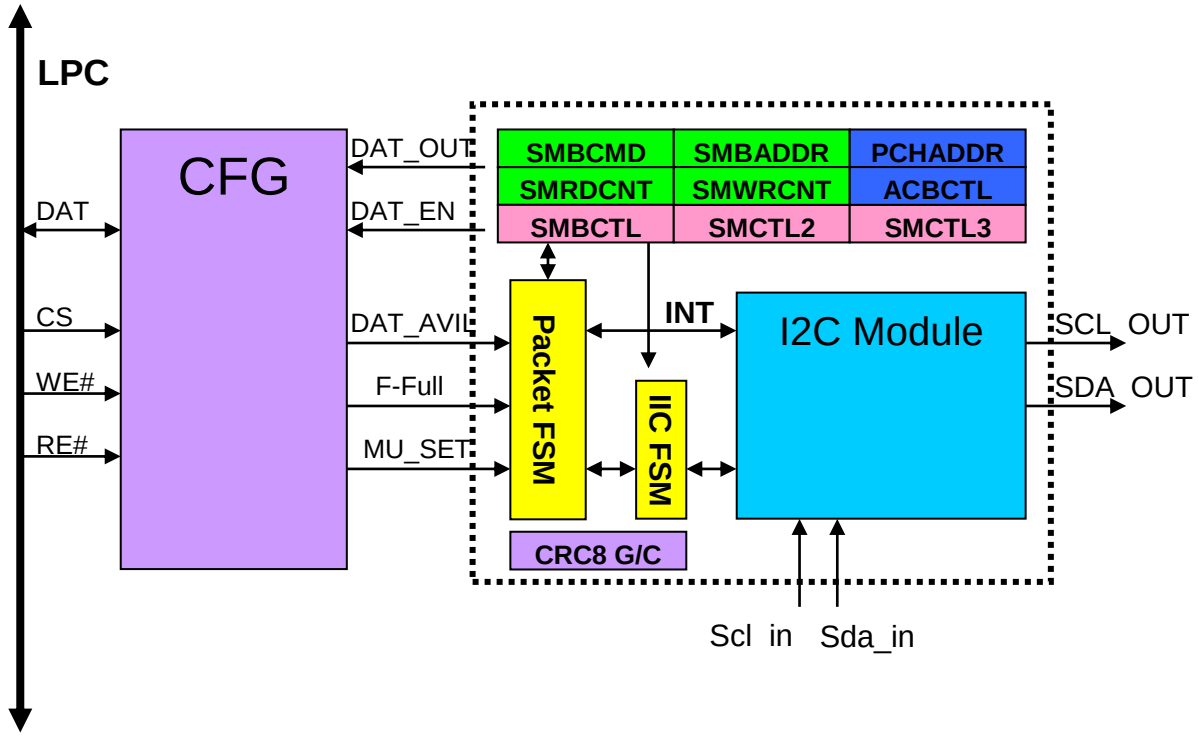


Figure 19-4 SMBus Master Block Diagram

.

19.5.2 Programming Flow

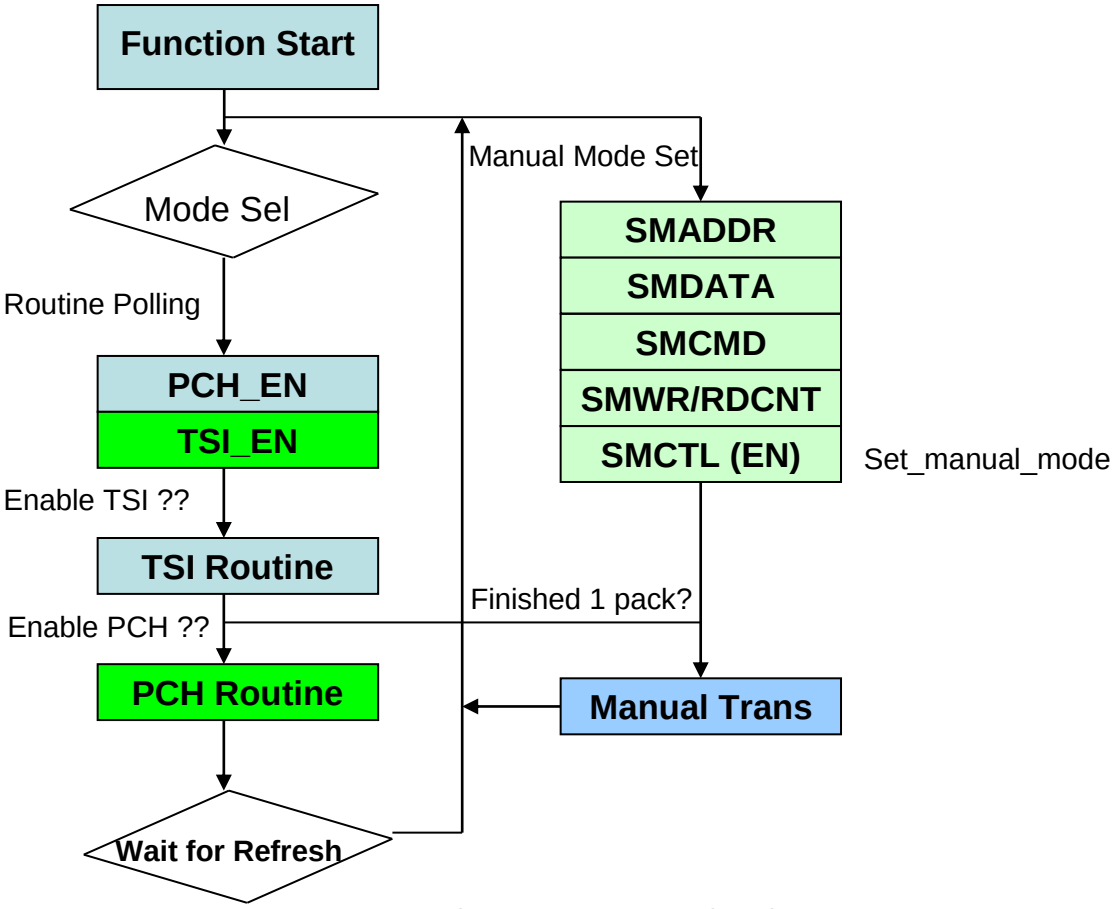


Figure 19-5 Programming Flow

19.5.3 TSI Routine

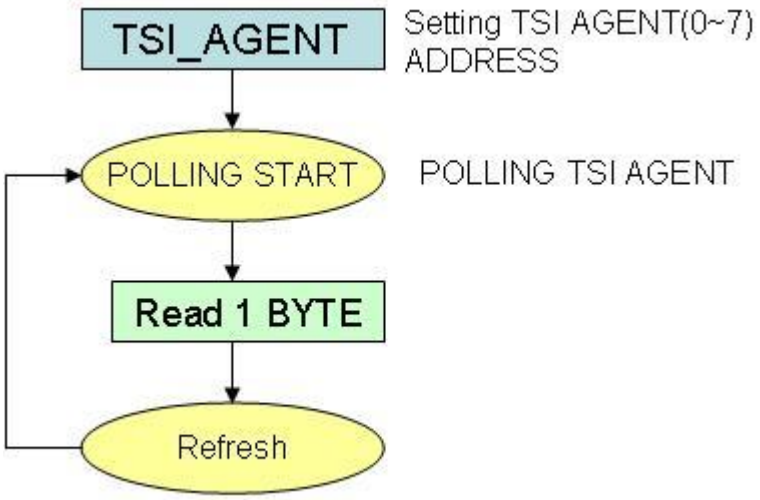


Figure 19-6 TSI Routine

19.5.4 PCH Routine

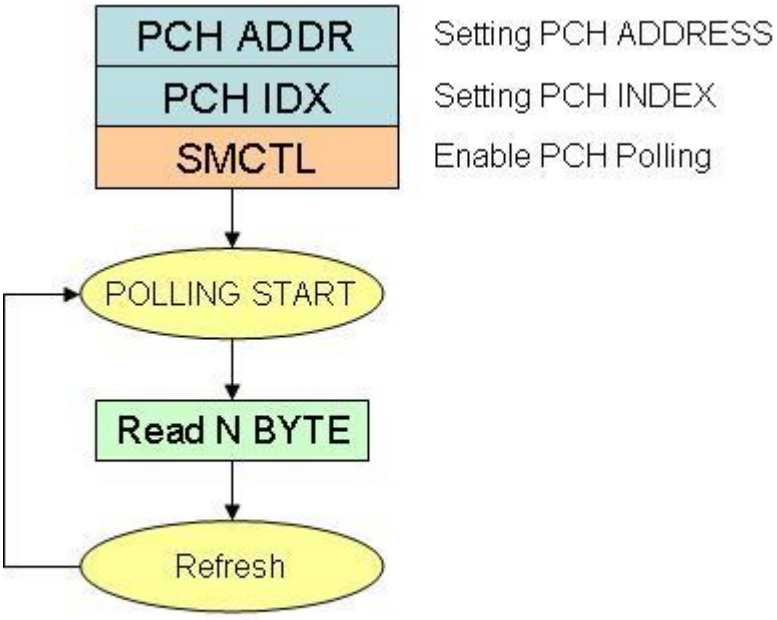


Figure 19-7 PCH Routine

19.5.5 BYTE Routine

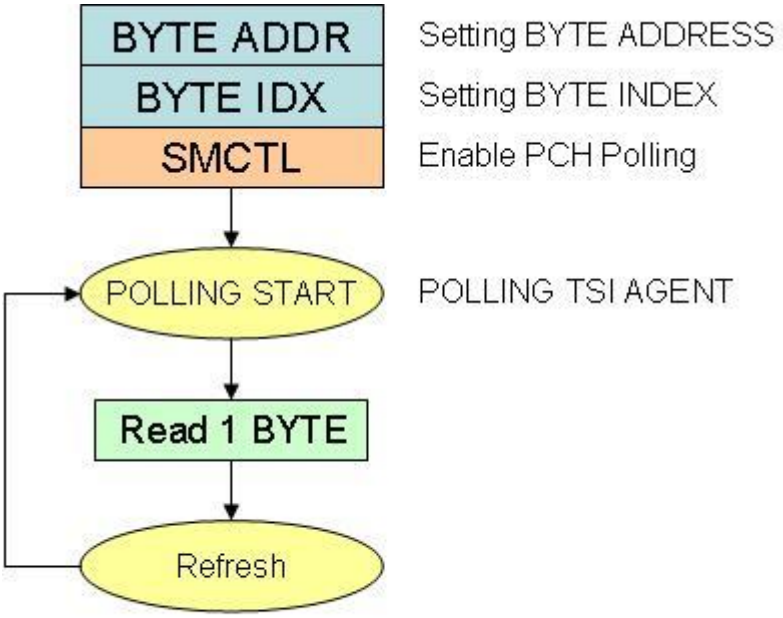


Figure 19-8 Byte Routine

19.5.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the SMBus slave. The timing diagrams below illustrate how to use the SMBus interface to write the data or read the data to the SMBus slave.

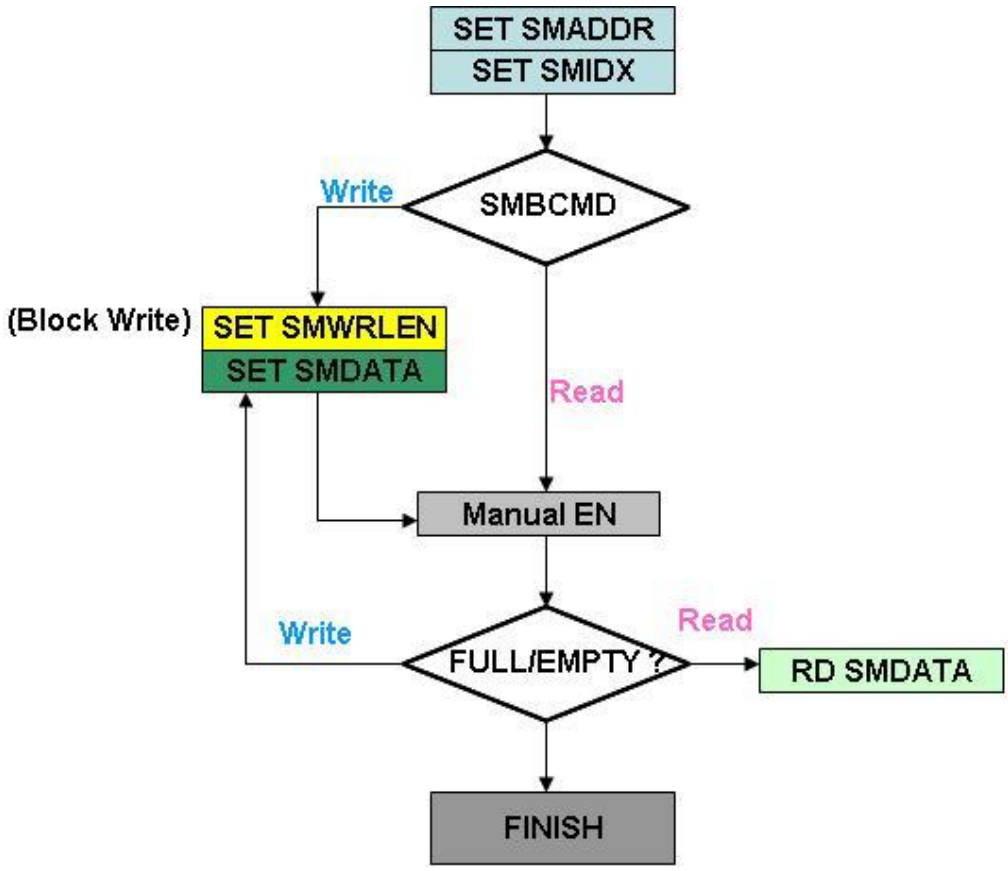


Figure 19-9 Manual Mode Programming Flow

19.6 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register.
- W = Write.
- RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

19.6.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

19.6.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

19.7 SMBus Master Register Set

19.7.1 SMBus Register Map

SMBus Master base address in register Logical Device B CR62h(MSB), CR63h(LSB).

Table 19-3 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	**SMDATA**	19.7.2
1	R/W	**SMWRSIZE**	19.7.3
2	R/W	**SMBCMD**	19.7.4
3	R/W	**SMIDX**	19.7.5
4	R/W	**SMCTL**	19.7.6
5	R/W	**SMADDR**	19.7.7
6	R/W	**SCLFREQ**	19.7.8
7	RO	**Reserved**	--
8	R/W	**PCHADDR**	19.7.9
9	R/W	**Error_status**	19.7.10
A	R/W	**Reserved**	19.7.11
B	R/W	**PCHCMD**	19.7.13
D	R/W	**TSI_AGENT**	19.7.12
E	R/W	**SMCTL3**	19.7.13
F	R/W	**SMCTL2**	19.7.14
10	R/W	**BYTE_ADDR0**	19.7.15
11	R/W	**BYTE_ADDR1**	19.7.16
12	R/W	**BYTE_IDX_H**	19.7.17
13	R/W	**BYTE_IDX_L**	19.7.18
14-15	R/W	**Reserved**	--
16	R/W	**TSI AGENT0 ADDR**	19.7.19
17	R/W	**TSI AGENT1 ADDR**	19.7.20

19.7.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Offset: 0h

Type: R/W

Byte	3	2	1	0
Name	**SMFIFO3**	**SMFIFO2**	**SMFIFO1**	**SMFIFO0**
Default	00h	00h	00h	00h

Byte	Description
3	**SMFIFO3 (SMBus FIFO 3).** This byte represents the high byte of the 32 bits SMBus data.
2	**SMFIFO2 (SMBus FIFO 2).** This byte represents the second byte of the 32 bits SMBus data.
1	**SMFIFO1 (SMBus FIFO 1).** This byte represents the first byte of the 32 bits SMBus data.
0	**SMFIFO0 (SMBus FIFO 0).** This byte represents the low byte of the 32 bits SMBus data.

19.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Offset: 1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMWRSIZE**				
Default	0	0	0	0	0	0	0	0

Bit	Descriptio
7-5	Reserved.
4-0	**SMWRSIZE (SMBus Write Byte Counter).** This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is bytes.

19.7.4 SMBus Command (SMCMD) – Bank 0

Offset: 2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**SMBCMD**			
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	Reserved.
3-0	**SMBCMD (SMBus Command).** This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

19.7.5 SMBus INDEX (SMIDX) – Bank 0

Offset: 3h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMIDX**							
Default	0	0	0	0	0	0	0	0

Bit	Description
7-0	**SMIDX (SMBus INDEX).** This field represents the index data of the SMBus.

19.7.6 SMBus Control (SMCTL) – Bank 0

Offset: 4h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**MMODE_S**	**S_RST**	**CRC8_EN**	**REFRESH_time**			**BYTE_EN**	**PCH_EN**
Default	0	0	0	0	0	0	0	0

Bit	Descriptio
7	**MMODE_S (Manual Mode Set).** 0: Disable. 1: Enable.
6	**S_RST (Soft Reset SMBus).** 0: Disable. 1: Enable..

5	**CRC8_EN (CRC8 Enable).** 0: Disable. 1: Enable.
4-2	**REFRESH_time (Refresh time length Select).** 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	**BYTE_EN (BYTE Enable).** 0: BYTE function is disabled. 1 : BYTE function is enabled.
0	**PCH_EN (PCH Enable).** 0: PCH function is disabled. 1 : PCH function is enabled.

19.7.7 SMBus Address (SMADDR) – Bank 0

Offset: 5h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMADDR**							**Reserved**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-1	**SMADDR (SMBus Address).** AMD-TSI only supports 7-bit SMBus address.
0	Reserved. 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

19.7.8 SCL FREQ (SCLFREQ) – Bank 0

Offset: 6h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**SCLFQ**			
Default	0	0	0	0	0	1	1	1

Bit	Description
7-4	Reserved

3-0	**SCLFQ (SMBCLK Frequency).** This field defines the SMBCLK period (low time and high time). The clock low time and high time ate defined as follows: 0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 91.5KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 70KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz

19.7.9 PCH Address (PCHADDR) – Bank 0

Offset: 8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHADDR**							**Reserved**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-1	**PCHADDR (PCH Address).** PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to “0”.

19.7.10 SMBus Error Status (Error_status) – Bank 0

Offset: 9h

Type: RO/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**ADNACK**	**Timeout**	**Reserved**	**BER**	**NACK**	**Reserved**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-6	Reserved.
5	**ADDR Non ACK.** This bit reflects SMBus occurring ADDRESS NON ACK in Manual mode..
4	**Timeout.** This bit reflects when SMBus occurring timeout.

3	Reserved.
2	**BER (Bus Error).** This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	**NACK (Negative acknowledge).** This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	Reserved.

19.7.11 PCH Command (PCHCMD) – Bank 0

Offset: Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHCMD**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**PCHCMD (PCH Command).** This field represents the command data of the PCH. The default command is block read (40h).

19.7.12 TSI Agent Enable Register (TSI_AGENT) – Bank0

Offset: Dh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						AG1	AG0
Default	0						0	0

Bit	Description
7-2	Reserved.
1	**TSI AGENT1 Enable. :** This bit reflects AMD-TSI Agent Select. 0: Disable 1: Enable
0	**TSI AGENT0 Enable. :** This bit reflects AMD-TSI Agent elect. 0: Disable 1: Enable

19.7.13 SMBus Control 3 Register (SMCTL3) – Bank 0

Offset: Eh

Type: W/R

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**CRC_CHK**	**M_MODE**	**F_FULL**	**F_EMPT**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	Reserved.
3	**CRC_CHK (CRC Check).** 0: incorrect 1 : correct
2	**M_MODE (Manual Mode).** 0 : Non-active 1 : Active
1	**F_FULL (fifo_full). :** This bit reflects SMBus data fifo is full. 0: Non-full 1 : Full
0	**F_EMPT (fifo empty). :** This bit reflects the SMBus data fifo is empty. 0: Non-empty 1 : Empty

19.7.14 SMBus Control 2 Register (SMCTL2) – Bank 0

Offset: Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**INT_LCH_E**	**Reserved**		**BYTE_SEL**	**BANKSEL**	
Default	0	0	0	0	0	0	0	0

Bit	Description
7-6	Reserved.
5	**INT_LCH_E (Interrupt Latch Enable). :** This bit will latch the I2CSTA register. 0: Disable. 1: Enable.
2	**BYTE_SEL :**This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	**BANKSEL (Bank Select).** 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

19.7.15 BYTE ADDRESS0 (BYTE ADDR) – Bank 0

Offset: 10h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS0**							**Reserved**
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**BYTE ADDRESS0 (BYTE ADDR).** This field represents the address data of the BYTE.

19.7.16 BYTE ADDRESS1 (BYTE ADDR) – Bank 0

Offset: 11h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS1**							**Reserved**
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**BYTE ADDRESS1 (BYTE ADDR).** This field represents the address data of the BYTE.

19.7.17 BYTE INDEX_H (BYTE_IDX_H) – Bank 0

Offset: 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_H**							
Default	0	0	0	0	0	0	0	1

Bit	Description
7-0	**BYTE_IDX_H (High BYTE INDEX).** This field represents the high byte index of the Byte polling. The default command is byte read (01h).

19.7.18 BYTE INDEX_L (BYTE_IDX_L) – Bank 0

Offset: 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_L**							
Default	0	0	0	1	0	0	0	0

Bit	Description
7-0	**BYTE_IDX_L (LOW BYTE INDEX).** This field represents the low byte index of the Byte polling. The default command is byte read (10h).

19.7.19 TSI AGENT0 ADDR (TSI0_ADDR) – Bank 0

Offset: 16h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**TSI_AGENT0_ADDR[7:1]**							**Reserved**
Default	1	0	0	1	1	0	0	0

Bit	Description
7-0	**TSI_AGENT0_ADDR[7:1].** This field represents the slave address of the TSI polling. The default command is byte read (98h).

19.7.20 TSI AGENT1 ADDR (TSI1_ADDR) – Bank 0

Offset: 17h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**TSI_AGENT1_ADDR[7:1]**							**Reserved**
Default	1	0	0	1	1	0	1	0

Bit	Description
7-0	**TSI_AGENT1_ADDR[7:1].** This field represents the slave address of the TSI polling. The default command is byte read (9Ah).

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address that the writes. The address must be different so that the IBX knows which target Is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

20. FADING LED

The NCT6122D / NCT6126D provide Fading LED interface that can be change LED speed of bright or dark througt different frequency or duty cycle. Furthermore, the constrast of LED bright or dark can be decided by maximum duty cycle, minimum duty cycle, and middle value.

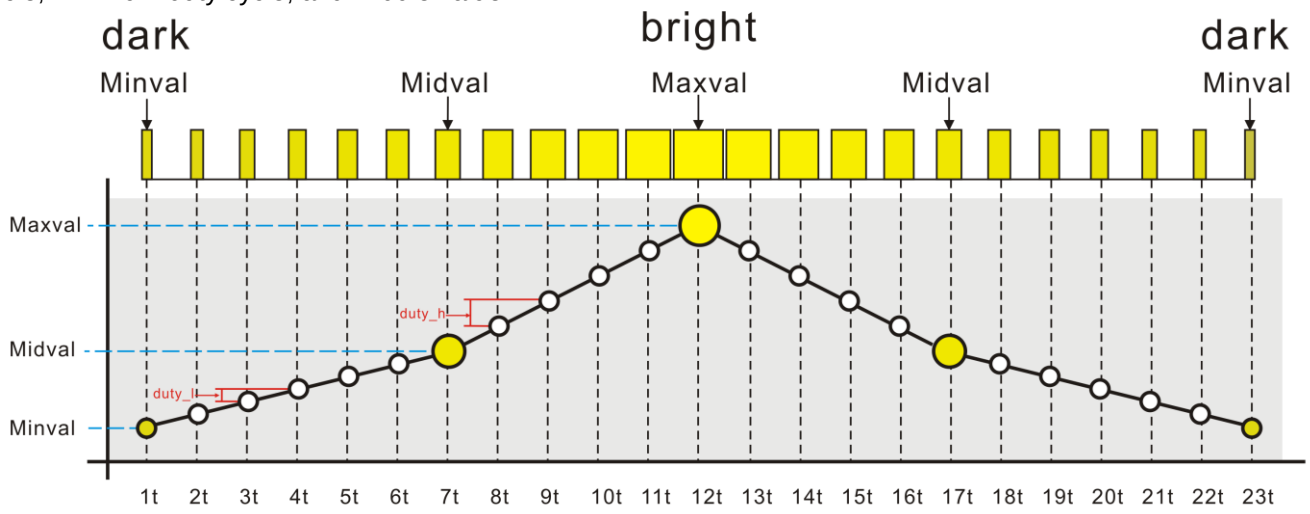


Figure 20-1 Example of Fading LED

NCT6122D / NCT6126D GRN/YLW, SUSLED and PLED supports fading LED function. The duty cycle can be increase and decrease contrl by LD15 CRE3 and CRE4, as table 20-1. Besides LD15 CRE6 and CRE7 also supports bright and dark extend control as table 20-2.

The Fading LED Frequency Divider Register (LD15 CRE8) and Fading_led_prgval repeat register (LD15 CRE5 B7-4) are set as 0x10 and as 0x1 in table 20-1 and table 20-2.

Table 20-1 Duty cycle increase/decrease time

LD15 CRE3	LD15 CRE4	Increase Time	Decrease Time
0x88	0x38	1.06 sec	1.93 sec
0x56	0x56	1.54 sec	1.54 sec
0x44	0x33	2.10 sec	2.79 sec

Table 20-2 Bright/Dark extend time

LD15 CRE6/CRE7	Bright/Dark Extend Time
0x0F	0.96 sec
0x17	1.47 sec
0x1E	1.92 sec

Use the ratio between two groups can quickly find out the setup value. It only suit for increase (or decrease) duty cycle value low and high register are equal. (The example time below is based on the Fading LED Frequency Divider Register (LD15 CRE8) is 0x10 and fading_led_prgval repeat register (LD15 CRE5 B7-4) is 0x1)

Time : Duty cycle value = 4.2 sec : 0x02 = 2.1 sec : 0x04 = 1.06 sec : 0x08 = 0.56 sec : 0x0F

21. RESETIC LOGIC

The ResetIC function controls the PWROK on/off. The PWROK is turned off for a period 140ms when detect pin RESETIC falling edge. If RESETIC low for a long while, PWROK will turn off again after a while. Please refer to the figure below.

The main function is enable by LDE_CRE6[1]

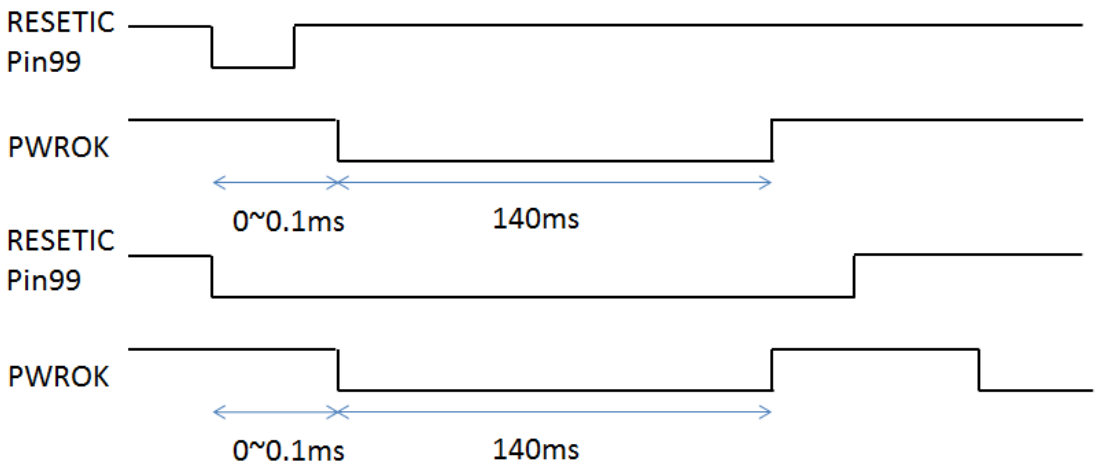


Figure 21-1 RESET IC Timing Chart

22. PORT80 TO UART

The NCT6122D / NCT6126D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be losing. But we make sure the last one would be send.

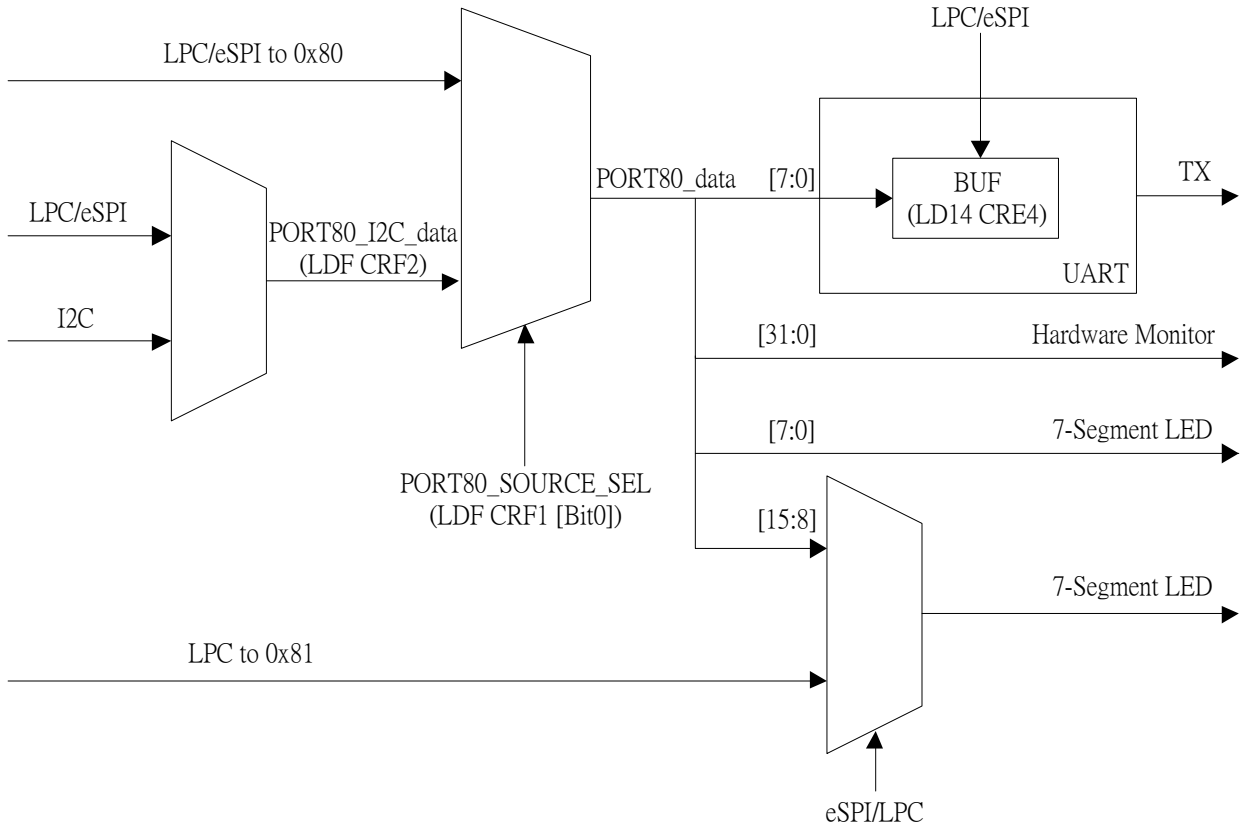


Figure 22-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

23. CONFIGURATION REGISTER

23.1 Chip (Global) Control Register

CR 02h. Software Reset Register

Location: Address 02h
Attribute: Write Only
Power Well: VSB
Reset by: LRESET#
Default :
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	Write “1” Only	Software RESET.

CR 07h. Logical Device Selection

Location: Address 07h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Location: Address 10h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

BIT	READ / WRITE	DESCRIPTION
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Location: Address 11h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : Feh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTD IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	UARTE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	UARTF IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

BIT	READ / WRITE	DESCRIPTION
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Location: Address 13h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Location: Address 14h
Attribute: Read/Write
Power Well: VAB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah. Multi-Function Selection

Location: Address 1Ah
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin87 function selection
<table>
<tr><th>LDE_CRFA[6]</th><th>CR1C [Bit7]</th><th>CR1A [Bit7]</th><th>CR1B [Bit2]</th><th>Pin87</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>PCH_PSON#</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>IRRX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP86</td></tr>
</table></td></tr>
<tr><td>6</td><td colspan="2">Reserved.</td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin31 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin31</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDA</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit1</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>PLED</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>SLCT</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>PLED</td></tr>
</table>
Pin32 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin32</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDB</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit2</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP30</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PE</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP30</td></tr>
</table>
Pin33 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin33</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDC</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit3</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP31</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>BUSY</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP31</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>
Pin34 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin34</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDD</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit4</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP32</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>ACK#</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP32</td></tr>
</table>
Pin35 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin35</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDE</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit5</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP33</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD7</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP33</td></tr>
</table>
Pin36 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin36</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDF</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit6</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP34</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD6</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP34</td></tr>
</table>
Pin37 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin37</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>LEDG</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit7</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP35</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD5</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP35</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>
Pin38 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin38</th></tr>
<tr><td>1</td><td>0</td><td>00</td><td>DGH0#</td></tr>
<tr><td>1</td><td>1</td><td>xx</td><td>Port80_Bit8</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP36</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD4</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP36</td></tr>
</table>
Pin39 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin39</th></tr>
<tr><td>1</td><td>0</td><td>xx</td><td>DGL0#</td></tr>
<tr><td>1</td><td>1</td><td>00</td><td>GP37</td></tr>
<tr><td>1</td><td>1</td><td>01</td><td>PD3</td></tr>
<tr><td>1</td><td>1</td><td>1x</td><td>GP37</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP37</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD3</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP37</td></tr>
</table>
Pin40 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin40</th></tr>
<tr><td>1</td><td>0</td><td>xx</td><td>DGH1#</td></tr>
<tr><td>1</td><td>1</td><td>00</td><td>GP40</td></tr>
<tr><td>1</td><td>1</td><td>01</td><td>PD2</td></tr>
<tr><td>1</td><td>1</td><td>1x</td><td>GP40</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP40</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD2</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP40</td></tr>
</table>
Pin41 function selection
<table>
<tr><th>GPIO_PORT80_SEL</th><th>LDB_CRF6[4]</th><th>CR1A [Bit5-4]</th><th>Pin41</th></tr>
<tr><td>1</td><td>0</td><td>xx</td><td>DGL1#</td></tr>
<tr><td>1</td><td>1</td><td>00</td><td>GP41</td></tr>
<tr><td>1</td><td>1</td><td>01</td><td>PD1</td></tr>
<tr><td>1</td><td>1</td><td>1x</td><td>GP41</td></tr>
<tr><td>0</td><td>x</td><td>00</td><td>GP41</td></tr>
<tr><td>0</td><td>x</td><td>01</td><td>PD1</td></tr>
<tr><td>0</td><td>x</td><td>1x</td><td>GP41</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-4</td><td>R / W</td><td>
Pin42 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin42</td></tr>
<tr><td>00</td><td>GP42</td></tr>
<tr><td>01</td><td>PD0</td></tr>
<tr><td>1x</td><td>GP42</td></tr>
</table>
Pin43 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin43</td></tr>
<tr><td>00</td><td>GP43</td></tr>
<tr><td>01</td><td>SLIN#</td></tr>
<tr><td>1x</td><td>GP43</td></tr>
</table>
Pin44 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin44</td></tr>
<tr><td>00</td><td>GP44</td></tr>
<tr><td>01</td><td>INIT#</td></tr>
<tr><td>1x</td><td>GP44</td></tr>
</table>
Pin45 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin45</td></tr>
<tr><td>00</td><td>GP45</td></tr>
<tr><td>01</td><td>ERR#</td></tr>
<tr><td>1x</td><td>GP45</td></tr>
</table>
Pin46 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin46</td></tr>
<tr><td>00</td><td>GP46</td></tr>
<tr><td>01</td><td>AFD#</td></tr>
<tr><td>10</td><td>GPI_TRANS</td></tr>
<tr><td>11</td><td>GP46</td></tr>
</table>
Pin47 function selection
<table>
<tr><td>CR1A [Bit5-4]</td><td>Pin47</td></tr>
<tr><td>00</td><td>GP47</td></tr>
<tr><td>01</td><td>STB#</td></tr>
<tr><td>10</td><td>GPO_TRANS</td></tr>
<tr><td>11</td><td>GP47</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin62 function selection
<table>
<tr><th>CR2F[4] (KBC_EN)</th><th>CR1A [3]</th><th>CR2A[0]</th><th>Pin62</th></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP50</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>KCLK</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MSDA</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SDA</td></tr>
</table>
Pin63 function selection
<table>
<tr><th>CR2F[4] (KBC_EN)</th><th>CR1A [3]</th><th>CR2A[0]</th><th>Pin63</th></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP51</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>KDAT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MSCL</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SCL</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin65 function selection
<table>
<tr><th>CR2F[4] (KBC_EN)</th><th>CR1A [2]</th><th>Pin65</th></tr>
<tr><td>0</td><td>0</td><td>GP52</td></tr>
<tr><td>1</td><td>x</td><td>MCLK</td></tr>
<tr><td>0</td><td>1</td><td>AUXFANIN1</td></tr>
</table>
Pin66 function selection
<table>
<tr><th>CR2F[4] (KBC_EN)</th><th>CR1A [2]</th><th>Pin66</th></tr>
<tr><td>0</td><td>0</td><td>GP53</td></tr>
<tr><td>1</td><td>x</td><td>MDAT</td></tr>
<tr><td>0</td><td>1</td><td>AUXFANOUT1</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin67 function selection
<table>
<tr><th>CR1A [1]</th><th>Pin67</th></tr>
<tr><td>0</td><td>PSOUT#</td></tr>
<tr><td>1</td><td>GP54</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin68 function selection
<table>
<tr><th>CR1A [0]</th><th>Pin68</th></tr>
<tr><td>0</td><td>PSIN#</td></tr>
<tr><td>1</td><td>GP55</td></tr>
</table></td></tr>
</table>

CR 1Bh. Multi-Function Selection

Location: Address 1Bh

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#
Default : 03h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin70 function selection
<table>
<tr><th>CR1B [7]</th><th>LDE_CRE6[6]</th><th>Pin70</th></tr>
<tr><td>0</td><td>0</td><td>SLP_S5#</td></tr>
<tr><td>1</td><td>0</td><td>GP56</td></tr>
<tr><td>x</td><td>1</td><td>SLP_S5# (out, OD)</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin71 function selection
<table>
<tr><th>CR1B [Bit6]</th><th>Pin71</th></tr>
<tr><td>0</td><td>PWROK</td></tr>
<tr><td>1</td><td>GP57</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin72 function selection
<table>
<tr><th>CR1B [Bit5]</th><th>Pin72</th></tr>
<tr><td>0</td><td>PSON#</td></tr>
<tr><td>1</td><td>GP60</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin73 function selection
<table>
<tr><th>CR1B [Bit4]</th><th>LDE_CRE6[6]</th><th>Pin73</th></tr>
<tr><td>0</td><td>0</td><td>SLP_S3#</td></tr>
<tr><td>1</td><td>0</td><td>GP61</td></tr>
<tr><td>0</td><td>1</td><td>SLP_S3#(out, OD)</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><th>CR1B [Bit3]</th><th>Pin75</th></tr>
<tr><td>0</td><td>RSMRST#</td></tr>
<tr><td>1</td><td>GP62</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin87 function selection
<table>
<tr><th>LDE_CRFA [6]</th><th>CR1C[7]</th><th>CR1A[7]</th><th>CR1B[2]</th><th>Pin87</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>PCH_PSON#</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>IRRX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP86</td></tr>
</table>
Pin88 function selection
<table>
<tr><th>CR1B [2]</th><th>Pin88</th></tr>
<tr><td>0</td><td>PECI</td></tr>
<tr><td>1</td><td>TSID</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin94 function selection
<table>
<tr><td>CR1B [Bit1-0]</td><td>CR2A[1]</td><td>Pin94</td></tr>
<tr><td>1x</td><td>x</td><td>SDA</td></tr>
<tr><td>00</td><td>0</td><td>GP63</td></tr>
<tr><td>01</td><td>x</td><td>MSDA</td></tr>
<tr><td>00</td><td>1</td><td>AUXFANIN2</td></tr>
</table>
Pin96 function selection
<table>
<tr><td>CR1B [Bit1-0]</td><td>CR2A[1]</td><td>Pin96</td></tr>
<tr><td>1x</td><td>x</td><td>SCL</td></tr>
<tr><td>00</td><td>0</td><td>GP64</td></tr>
<tr><td>01</td><td>x</td><td>MSCL</td></tr>
<tr><td>00</td><td>1</td><td>AUXFANOUT2</td></tr>
</table></td></tr>
</table>

CR 1Ch. Multi-Function Selection

Location: Address 1Ch
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin87 function selection
<table>
<tr><td>LDE_CRFA [6]</td><td>CR1C[7]</td><td>CR1A[7]</td><td>CR1B[2]</td><td>Pin87</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>PCH_PSON#</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>IRRX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP86</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin106 function selection
<table>
<tr><td>CR1C[6]</td><td>Pin106</td></tr>
<tr><td>0</td><td>SUSLED</td></tr>
<tr><td>1</td><td>GP65</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin107 function selection
<table>
<tr><td>LD9_CRE1[4]</td><td>CR1C[5]</td><td>Pin107</td></tr>
<tr><td>1</td><td>X</td><td>THERMTRIP#</td></tr>
<tr><td>0</td><td>1</td><td>GP66</td></tr>
<tr><td>0</td><td>0</td><td>THERMTRIP#</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td colspan="2">Reserved</td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin109-116 function selection
<table>
<tr><th>CR1D[4] (SOUTC_P80_SEL)</th><th>CR1C[3:2]</th><th>Pin109-116</th></tr>
<tr><td>1</td><td>xx</td><td>GP0x, SOUTC_P80</td></tr>
<tr><td>0</td><td>00</td><td>GP0x</td></tr>
<tr><td>0</td><td>10</td><td>SOUTC/SINC/RTSC (RS485), GP0x</td></tr>
<tr><td>0</td><td>01</td><td>SOUTC/SINC (RS422), GP0x</td></tr>
<tr><td>0</td><td>11</td><td>UARTC (RS232)</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Reserved.</td></tr>
<tr><td>0</td><td>R / W</td><td>Pin15-16 KBRST#/GA20M OD Select
1: Open Drain Type
0: Push-Pull Type</td></tr>
</table>

CR 1Dh. Multi-Function Selection

Location: Address 1Dh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 000s0000b
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-5</td><td colspan="2">Reserved</td></tr>
<tr><td>4</td><td>R / W</td><td>Pin109-116 function selection
<table>
<tr><th>CR1D[4] (SOUTC_P80_SEL)</th><th>CR1C[3:2]</th><th>Pin109-116</th></tr>
<tr><td>1</td><td>xx</td><td>GP0x, SOUTC_P80</td></tr>
<tr><td>0</td><td>00</td><td>GP0x</td></tr>
<tr><td>0</td><td>10</td><td>SOUTC/SINC/RTSC (RS485), GP0x</td></tr>
<tr><td>0</td><td>01</td><td>SOUTC/SINC (RS422), GP0x</td></tr>
<tr><td>0</td><td>11</td><td>UARTC (RS232)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin95 function selection
<table>
<tr><th>LDE_CRFA[6]</th><th>CR1D[3:2]</th><th>Pin95</th></tr>
<tr><td>1</td><td>x</td><td>S0_IDLE#</td></tr>
<tr><td>0</td><td>00</td><td>OVT#</td></tr>
<tr><td>0</td><td>01</td><td>SMI#</td></tr>
<tr><td>0</td><td>1x</td><td>GP87</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin117-124 function selection
<table>
<tr><th>CR1C[7]</th><th>CR1D[1:0]</th><th>Pin117-124</th></tr>
<tr><td>1</td><td>00</td><td>IRTX, GP1x</td></tr>
<tr><td>0</td><td>00</td><td>GP1x</td></tr>
<tr><td>x</td><td>10</td><td>SOUTD/SIND/RTSD (RS485), GP1x</td></tr>
<tr><td>x</td><td>01</td><td>SOUTD/SIND (RS422), GP1x</td></tr>
<tr><td>x</td><td>11</td><td>UARTD (RS232)</td></tr>
</table></td></tr>
</table>

CR 20h. Chip ID (High Byte)

Location: Address 20h
Attribute: Read Only
Power Well: VSB
Reset by: None
Default : D2h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = D2h (high byte).

CR 21h. Chip ID (Low Byte)

Location: Address 21h
Attribute: Read Only
Power Well: VSB
Reset by: None
Default : 81h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

7-0	Read Only	Chip ID number = X3h (A version) ; X4h (B version) (low byte).
		X= 8 // NCT6126
		X= A // NCT6122

CR 22h. Device Power Down

Location: Address 22h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : F8h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	DSIRLGRQ => = 0 Enable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
6	R / W	IR Power Down. 0: Powered down. 1: Not powered down.
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2	R/W	Select output type of AUXFANOUT2 =0 AUXFANOUT2 is Open-drain. (Default) =1 AUXFANOUT2 is Push-pull.
1	R / W	Select output type of AUXFANOUT1 =0 AUXFANOUT1 is Open-drain. (Default) =1 AUXFANOUT1 is Push-pull.
0	R / W	Reserved.

CR 24h. Multi-Function Selection & Global Option
Location: Address 24h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. (Default) =1 SYSFANOUT is Push-pull.
5	R / W	Select output type of CPUFANOUT =0 CPUFANOUT is Open-drain. (Default) =1 CPUFANOUT is Push-pull.
4	R / W	Select output type of AUXFANOUT0 =0 AUXFANOUT0 is Open-drain. (Default) =1 AUXFANOUT0 is Push-pull.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Pin14 AUXFANOUT0 Function Output Enable =0 Disable =1 Enable
2	Reserved	
1	R / W	Pin18 BEEP Function Output Enable =0 Disable =1 Enable
0	R / W	PNPCVS => = 0 The compatible PNP address-select registers have default values. = 1 The compatible PNP address-select registers have no default values.

CR 25h. Interface Tri-state Enable

Location: Address 25h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTFTRI 1: enable, 0: disable
6	R / W	UARTETRI 1: enable, 0: disable
5	R / W	UARTDTRI 1: enable, 0: disable
4	R / W	UARTCTRI 1: enable, 0: disable
3	R / W	UARTBTRI 1: enable, 0: disable
2	R / W	UARTATRI 1: enable, 0: disable
1	R / W	PRTTRI 1: enable, 0: disable
0	Reserved.	

CR 26h. Global Option s: value by strapping

Location: Address 26h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 0s000000b
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	

BIT	READ / WRITE	DESCRIPTION
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	R / W	= 0 Disable the access to CR10h, CR11h (Device IRQ Type) and CR13h, CR14h (Device IRQ Polarity). = 1 Enable the access to CR10h, CR11h (Device IRQ Type) and CR13h, CR14h (Device IRQ Polarity).
4-3	Reserved.	
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable URAT B legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Global Option

Location: Address 27h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	Pin31 PLED Function Output Enable =0 Disable =1 Enable

CR 28h. Global Option

Location: Address 28h
Attribute: Read/Write

Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-4	R / W	0 0 : LPC or I2C to 80PORT switch 0 1: CPU temperature to 80PORT switch 1 0: SYS temperature to 80PORT switch 1 1: AUX temperature to 80PORT switch
3	Reserved.	
2-0	R / W	PRTMODS2 ~ 0 => **Bits** **2 1 0** = 0 x x Parallel Port Mode. = 1 x x Reserved.

CR 29h. Global Option
Location: Address 29h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : F0h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTF Power Down. 0: Powered down. 1: Not powered down.
6	R / W	UARTE Power Down. 0: Powered down. 1: Not powered down.
5	R / W	UARTD Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTC Power Down. 0: Powered down. 1: Not powered down.
3	R / W	DSUFLGRQ => = 0 Enable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART F legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
2	R / W	DSUELGRQ => = 0 Enable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART E legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
1	R / W	DSUDLGRQ => = 0 Enable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART D legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

BIT	READ / WRITE	DESCRIPTION
0	R / W	DSUCLGRQ => = 0 Enable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART C legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 2Ah. Global Option

Location: Address 2Ah
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R/W	Enable Over Temperature shutdown Protection (OVT#) = 0 The thermal shutdown function is disabled. (Default) = 1 Enable thermal shutdown function. If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.
4	R/W	IRTX output enable 1: Enable 0: Disable (Default)
3	R/W	Pin77 Function Selection CR2A[3] = 1 → GP84 CR2A[3] = 0 → WDTO#
2	R/W	OVT# Power Down Selection =0 Disable =1 Enable

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>R/W</td><td>Pin94 function selection
<table>
<tr><td>CR1B [Bit1-0]</td><td>CR2A[1]</td><td>Pin94</td></tr>
<tr><td>1x</td><td>x</td><td>SDA</td></tr>
<tr><td>00</td><td>0</td><td>GP63</td></tr>
<tr><td>01</td><td>x</td><td>MSDA</td></tr>
<tr><td>00</td><td>1</td><td>AUXFANIN2</td></tr>
</table>
Pin96 function selection
<table>
<tr><td>CR1B [Bit1-0]</td><td>CR2A[1]</td><td>Pin96</td></tr>
<tr><td>1x</td><td>x</td><td>SCL</td></tr>
<tr><td>00</td><td>0</td><td>GP64</td></tr>
<tr><td>01</td><td>x</td><td>MSCL</td></tr>
<tr><td>00</td><td>1</td><td>AUXFANOUT2</td></tr>
</table></td></tr>
<tr><td>0</td><td>R/W</td><td>Pin62 function selection
<table>
<tr><td>CR2F[4] (KBC_EN)</td><td>CR1A [3]</td><td>CR2A[0]</td><td>Pin62</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP50</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>KCLK</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MSDA</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SDA</td></tr>
</table>
Pin63 function selection
<table>
<tr><td>CR2F[4] (KBC_EN)</td><td>CR1A [3]</td><td>CR2A[0]</td><td>Pin63</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP51</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>KDAT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MSCL</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SCL</td></tr>
</table></td></tr>
</table>

CR 2Bh. Global Option

Location: Address 2Bh
Attribute: Read/Write
Power Well: VSB
Reset by: CR2B[7:2]: PWROK CR2B[1:0] : LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R/W</td><td>Pin125-4 function selection
<table>
<tr><th>CR2B[7]</th><th>CR2C [5:4]</th><th>Pin125-4</th></tr>
<tr><td>1</td><td>xx</td><td>GP2x,
AUXFANIN1,
AUXFANIN2,
AUXFANOUT1,
AUXFANOUT2</td></tr>
<tr><td>0</td><td>00</td><td>GP2x</td></tr>
<tr><td>0</td><td>10</td><td>SOUTE/SINE/RTSE
(RS485), GP2x</td></tr>
<tr><td>0</td><td>01</td><td>SOUTE/SINE (RS422),
GP2x</td></tr>
<tr><td>0</td><td>11</td><td>UARTE (RS232)</td></tr>
</table></td></tr>
<tr><td>6-5</td><td colspan="2">Reserved.</td></tr>
<tr><td>4</td><td>R/W</td><td>Pin6 AUXFANIN0 function selection
<table>
<tr><th>CR2B [Bit4]</th><th>Pin6</th></tr>
<tr><td>0</td><td>AUXFANIN0</td></tr>
<tr><td>1</td><td>GP81</td></tr>
</table>
Pin14 AUXFANOUT0 function selection
<table>
<tr><th>CR2B [Bit4]</th><th>Pin14</th></tr>
<tr><td>0</td><td>AUXFANOUT0</td></tr>
<tr><td>1</td><td>GP80</td></tr>
</table></td></tr>
<tr><td>3</td><td>R/W</td><td>Pin18 BEEP function selection
<table>
<tr><th>CR2B [Bit3]</th><th>Pin18</th></tr>
<tr><td>1</td><td>BEEP</td></tr>
<tr><td>0</td><td>GP82</td></tr>
</table></td></tr>
<tr><td>2</td><td colspan="2">Reserved</td></tr>
<tr><td>1</td><td>R / W</td><td>HM IO space lock enable
0 : Disable (Unlock)
1 : Enable (Lock)</td></tr>
<tr><td>0</td><td>R / W</td><td>CLKRUN_EN
0: Disable CLKRUN function.
1: Enable CLKRUN function.</td></tr>
</table>

CR 2Ch. UART Option

Location: Address 2Ch
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 0Fh

Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R/W</td><td>Pin5, Pin7-11, Pin13 and Pin17 function selection
<table>
<tr><td>CR2C [7:6]</td><td>Pin5, Pin7-11, Pin13 and Pin17</td></tr>
<tr><td>00</td><td>GP7x</td></tr>
<tr><td>10</td><td>SOUTF/SINF/RTSF (RS485), GP7x</td></tr>
<tr><td>01</td><td>SOUTF/SINF (RS422), GP7x</td></tr>
<tr><td>11</td><td>UARTF (RS232)</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R/W</td><td>Pin125-4 function selection
<table>
<tr><td>CR2B[7]</td><td>CR2C [5:4]</td><td>Pin125-4</td></tr>
<tr><td>1</td><td>xx</td><td>GP2x, AUXFANIN1, AUXFANIN2, AUXFANOUT1, AUXFANOUT2</td></tr>
<tr><td>0</td><td>00</td><td>GP2x</td></tr>
<tr><td>0</td><td>10</td><td>SOUTE/SINE/RTSE (RS485), GP2x</td></tr>
<tr><td>0</td><td>01</td><td>SOUTE/SINE (RS422), GP2x</td></tr>
<tr><td>0</td><td>11</td><td>UARTE (RS232)</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R/W</td><td>Pin78-85 function selection
<table>
<tr><td>CR2C [3:2]</td><td>Pin78-85</td></tr>
<tr><td>00</td><td>GP9x</td></tr>
<tr><td>10</td><td>SOUTB/SINB/RTSB (RS485), GP9x</td></tr>
<tr><td>01</td><td>SOUTB/SINB (RS422), GP9x</td></tr>
<tr><td>11</td><td>UARTB (RS232)</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R/W</td><td>Pin49-57 function selection
<table>
<tr><td>CR2C [1:0]</td><td>Pin49-57</td></tr>
<tr><td>00</td><td>GPAx</td></tr>
<tr><td>10</td><td>SOUTA/SINA/RTSA (RS485), GPAx</td></tr>
<tr><td>01</td><td>SOUTA/SINA (RS422), GPAx</td></tr>
<tr><td>11</td><td>UARTA (RS232)</td></tr>
</table></td></tr>
</table>

CR 2Fh. Strapping Function Result

Location: Address 2Fh

Attribute: Read/Write

Power Well: VSB
Reset by: PWROK(Bit1), RSMRST#
Default : by ssss_0sss
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	PLAT_SEL Strapping result reading.
6	R / W	ATX mode / AT mode Power sequence select.
5	R / W	eSPI and LPC interface switch.
4	R / W	KBC_EN Strapping result reading. It can enable KB/MS pins function.
3	Reserved.	
2	R / W	ESPI_OWN_SEL Strapping result reading.
1	R / W	GPIO_PORT80_SEL Strapping result reading.
0	R / W	Entry Key Strapping result reading.

Note . All Strapping results can be programming by LPC Interface. There are two conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#
2) VCC Strapping result can be programming by LPC, and reset by PWROK

23.2 Logical Device 1 (PRT)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, 78h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 07h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.

Location: Address 74h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 3Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

23.3 Logical Device 2 (UARTA)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTA 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.

BIT	READ / WRITE	DESCRIPTION
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to “logic 0” by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to “logic 0” by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1’b1.)

CR F3h. UARTA 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTA 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTA 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB

Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTA 9bit-mode Interrupt Control Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bit-mode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bit-mode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTA 9bit-mode IRQ output. 1: Enable UARTA 9bit-mode IRQ output.

CR F7h. UARTA 9bit-mode IRQ Status Register

Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)

BIT	READ / WRITE	DESCRIPTION
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved.	
0	R / W	**UARTA 9bit-mode Status Bit** 0: UARTA 9bit-mode IRQ have not been triggered. 1: UARTA 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTA Control Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartAB_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

5	Reserved.
4	uartAB_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

23.4 Logical Device 3 (UARTB)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h, F8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 2 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1-0	R / W	**Bits** **1 0** 0 0: UART B clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART B clock source is 24 MHz (24 MHz / 1). 1 1: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTB 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.

BIT	READ / WRITE	DESCRIPTION
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTB 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTB 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTB 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTB 9bit-mode Interrupt Control Register

Location: Address F6h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTB 9bit-mode IRQ output. 1: Enable UARTB 9bit-mode IRQ output.

CR F7h. UARTB 9bit-mode IRQ Status Register

Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved	
0	R	**UARTB 9bit-mode Status Bit** 0: UARTB 9bit-mode IRQ have not been triggered. 1: UARTB9bit-mode IRQ have been triggered.

CR F8h. Extending UARTB Control Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

23.5 Logical Device 5 (KBC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Location: Address 62h, 63h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.
Location: Address 72h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.
Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 83h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved.	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

23.6 Logical Device 6 (CIR)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 08h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R/W	CIR wide band filter select 0: Low-pass filter 1: Band-pass filter
2-1	R/W	Timeout margin selection of CIR wide band band-pass filter 00: 200% recording carrier period 01: 100% recording carrier period 10: 50% recording carrier period 11: 25% recording carrier period
0	R/W	Carrier recording mode CIR wide band band-pass filter 0: Second carrier 1: Every carrier

CR F1h.
Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 09h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Highest input period of CIR wide band band-pass filter (unit : us)

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 32h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Lowest input period of CIR wide band band-pass filter (unit : us)

CR F3h.
Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Recording carrier period of CIR wide band band-pass filter (unit : us)

23.7 Logical Device 7 (GPIO)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, LRESET# (Bit7, 2)
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION	
7	R / W	0: GPIO7 is inactive.	1: GPIO7 is active.
6	R / W	0: GPIO6 is inactive.	1: GPIO6 is active.
5	R / W	0: GPIO5 is inactive.	1: GPIO5 is active.
4	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
3	R / W	0: GPIO3 is inactive.	1: GPIO3 is active.
2	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.
1	R / W	0: GPIO1 is inactive.	1: GPIO1 is active.
0	R / W	0: GPIO0 is inactive.	1: GPIO0 is active.

CR E0h. GPIO0 I/O Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.

BIT	READ / WRITE	DESCRIPTION
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Location: Address E3h
Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP07-GP00, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO1 I/O Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

CR E5h. GPIO1 Data Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO1 Inversion Register
Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO1 Status Register
Location: Address E7h
Attribute: Read Only
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E8h. GPIO2 I/O Register
Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST

Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

CR E9h. GPIO2 Data Register
Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR EAh. GPIO2 Inversion Register
Location: Address EAh
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR EBh. GPIO2 Status Register
Location: Address EBh
Attribute: Read Only
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR ECh. GPIO3 I/O Register

Location: Address ECh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR EDh. GPIO3 Data Register

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR EEh. GPIO3 Inversion Register

Location: Address EEh
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR EFh. GPIO3 Status Register

Location: Address EFh
Attribute: Read Only
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F0h. GPIO4 I/O Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read/written and produced to pins.

BIT	READ / WRITE	DESCRIPTION
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO4 Inversion Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO4 Status Register

Location: Address F3h
Attribute: Read Only
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F4h. GPIO5 I/O Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR F5h. GPIO5 Data Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO5 Inversion Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO5 Status Register

Location: Address F7h
Attribute: Read Only
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 I/O Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB

Reset by: GP6X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F9h. GPIO6 Data Register
Location: Address F9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FAh. GPIO6 Inversion Register
Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FBh. GPIO6 Status Register
Location: Address FBh
Attribute: Read Only
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR FCh. GPIO7 I/O Register

Location: Address FCh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.

CR FDh. GPIO7 Data Register

Location: Address FDh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FEh. GPIO7 Inversion Register

Location: Address FEh
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FFh. GPIO7 Status Register

Location: Address FFh
Attribute: Read Only
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit clears it to 0.

23.8 Logical Device 8 (GPIO, WDT1)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 8 byte boundary.

CR E0h. GPIO0 Multi-function Select Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → YLW
6	R / W	0: GPIO06 1: GPIO06 → GRN
5	R / W	0: GPIO05 1: GPIO05 → WDTO#
4	R / W	0: GPIO04 1: GPIO04 → SUSLED

BIT	READ / WRITE	DESCRIPTION
3	R / W	0: GPIO03 1: GPIO03 → YLW
2	R / W	0: GPIO02 1: GPIO02 → GRN
1	R / W	0: GPIO01 1: GPIO01 → WDTO#
0	R / W	0: GPIO00 1: GPIO00 → SUSLED

CR E1h. GPIO1 Multi-function Select Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW
6	R / W	0: GPIO16 1: GPIO16 → GRN
5	R / W	0: GPIO15 1: GPIO15 → BEEP
4	R / W	0: GPIO14 1: GPIO14 → SMI
3	R / W	0: GPIO13 1: GPIO13 → YLW
2	R / W	0: GPIO12 1: GPIO12 → GRN
1	R / W	0: GPIO11 1: GPIO11 → BEEP
0	R / W	0: GPIO10 1: GPIO10 → SMI

CR E2h. GPIO2 Multi-function Select Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → WDTO#
6	R / W	0: GPIO26 1: GPIO26 → BEEP
5	R / W	0: GPIO25 1: GPIO25 → SMI
4	R / W	0: GPIO24 1: GPIO24 → PLED
3	R / W	0: GPIO23 1: GPIO23 → WDTO#
2	R / W	0: GPIO22 1: GPIO22 → BEEP
1	R / W	0: GPIO21 1: GPIO21 → SMI
0	R / W	0: GPIO20 1: GPIO20 → PLED

CR E3h. GPIO3 Multi-function Select Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → BEEP
6	R / W	0: GPIO36 1: GPIO36 → SMI
5	R / W	0: GPIO35 1: GPIO35 → WDTO#
4	R / W	0: GPIO34 1: GPIO34 → SUSLED
3	R / W	0: GPIO33 1: GPIO33 → BEEP
2	R / W	0: GPIO32 1: GPIO32 → SMI
1	R / W	0: GPIO31 1: GPIO31 → WDTO#
0	R / W	0: GPIO30 1: GPIO30 → SUSLED

CR E4h. GPIO4 Multi-function Select Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → YLW
6	R / W	0: GPIO46 1: GPIO46 → GRN
5	R / W	0: GPIO45 1: GPIO45 → PLED
4	R / W	0: GPIO44 1: GPIO44 → SMI
3	R / W	0: GPIO43 1: GPIO43 → YLW
2	R / W	0: GPIO42 1: GPIO42 → GRN
1	R / W	0: GPIO41 1: GPIO41 → PLED
0	R / W	0: GPIO40 1: GPIO40 → SMI

CR E5h. GPIO5 Multi-function Select Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → YLW
6	R / W	0: GPIO56 1: GPIO56 → GRN
5	R / W	0: GPIO55 1: GPIO55 → BEEP
4	R / W	0: GPIO54 1: GPIO54 → WDTO#

BIT	READ / WRITE	DESCRIPTION
3	R / W	0: GPIO53 1: GPIO53 → YLW
2	R / W	0: GPIO52 1: GPIO52 → GRN
1	R / W	0: GPIO51 1: GPIO51 → BEEP
0	R / W	0: GPIO50 1: GPIO50 → WDTO#

CR E6h. GPIO6 Multi-function Select Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: GPIO66 1: GPIO66 → YLW
5	R / W	0: GPIO65 1: GPIO65 → GRN
4	R / W	0: GPIO64 1: GPIO64 → BEEP
3	R / W	0: GPIO63 1: GPIO63 → SMI
2	R / W	0: GPIO62 1: GPIO62 → WDTO#
1	R / W	0: GPIO61 1: GPIO61 → SUSLED
0	R / W	0: GPIO60 1: GPIO60 → PLED

CR E7h. GPIO67 Multi-function Select Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST (Bit7-5)
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	000: GPIO67 001: GPIO67 → YLW 010: GPIO67 → GRN 011: GPIO67 → BEEP 100: GPIO67 → SMI 101: GPIO67 → WDTO# 110: GPIO67 → SUSLED 111: GPIO67 → PLED
4-0	Reserved.	

CR E8h. GPIO7 Multi-function Select Register

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO77 1: GPIO77 → PLED
6	R / W	0: GPIO76 1: GPIO76 → BEEP
5	R / W	0: GPIO75 1: GPIO75 → SMI
4	R / W	0: GPIO74 1: GPIO74 → WDTO#
3	R / W	0: GPIO73 1: GPIO73 → PLED
2	R / W	0: GPIO72 1: GPIO72 → BEEP
1	R / W	0: GPIO71 1: GPIO71 → SMI
0	R / W	0: GPIO70 1: GPIO70 → WDTO#

CR E9h. GPIO8 Multi-function Select Register

Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → YLW
6	R / W	0: GPIO86 1: GPIO86 → SMI
5	R / W	0: GPIO85 1: GPIO85 → WDTO#
4	R / W	0: GPIO84 1: GPIO84 → BEEP
3	R / W	0: GPIO83 1: GPIO83 → YLW
2	R / W	0: GPIO82 1: GPIO82 → SMI
1	R / W	0: GPIO81 1: GPIO81 → WDTO#
0	R / W	0: GPIO80 1: GPIO80 → BEEP

CR EAh. GPIO9 Multi-function Select Register

Location: Address EAh
Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO97 1: GPIO97 → SUSLED
6	R / W	0: GPIO96 1: GPIO96 → BEEP
5	R / W	0: GPIO95 1: GPIO95 → SMI
4	R / W	0: GPIO94 1: GPIO94 → WDT1
3	R / W	0: GPIO93 1: GPIO93 → YLW
2	R / W	0: GPIO92 1: GPIO92 → GRN
1	R / W	0: GPIO91 1: GPIO91 → SMI
0	R / W	0: GPIO90 1: GPIO90 → PLED

CR EBh. GPIOA Multi-function Select Register

Location: Address EBh
Attribute: Read/Write
Power Well: VSB
Reset by: GPAX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIOA7 1: GPIOA7 → SUSLED
6	R / W	0: GPIOA6 1: GPIOA6 → BEEP
5	R / W	0: GPIOA5 1: GPIOA5 → SMI
4	R / W	0: GPIOA4 1: GPIOA4 → WDT1
3	R / W	0: GPIOA3 1: GPIOA3 → YLW
2	R / W	0: GPIOA2 1: GPIOA2 → GRN
1	R / W	0: GPIOA1 1: GPIOA1 → SMI
0	R / W	0: GPIOA0 1: GPIOA0 → PLED

CR ECh. GPIOB Multi-function Select Register

Location: Address ECh
Attribute: Read/Write
Power Well: VSB
Reset by: GPBX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
1-7	Reserved.	
0	R / W	0: GPIOB0 1: GPIOB0 → BEEP

CR F0h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET# or PWROK
Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin (Pin15) 0: Disable. 1: Enable.
0	R / W	Watchdog Timer I Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F1h. Watchdog Timer I(WDT1) Counter Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to the register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchdog timer I about one cycle deviation. If CR F2h, bits 7 and 6 are set, any Interrupt event comes from Mouse or Keyboard both cause the previously-loaded. Non-zero value will be reloaded to the Watch Dog Counter and the countdown resumes. Reading the register returns the current value in the Watch Dog Counter but not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is based on LD8 CRF0, bit[3], by analogy.

CR F2h. Watchdog Timer I (WDT1) Control & Status Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET# or PWROK
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by mouse interrupt. 1: Watchdog Timer I is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by keyboard interrupt. 1: Watchdog Timer I is reset by keyboard interrupt.
5	Write “1” Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

23.9 Logical Device 9 (GPIO)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	4 second PSIN# with thermtrip mode select 0: Keep DeepS5 210ms and back to S5 state 1: Stay at DeepS5 state
6-5	R / W	4 second PSIN# with thermtrip mode DEEPS5 timing select 00: 210 ms (default) 01: 500 ms 10: 1000 ms 11: 1500 ms
4	Reserved	
3	R / W	0: GPIOB is inactive. 1: GPIOB is active.
2	R / W	0: GPIOA is inactive. 1: GPIOA is active.
1	R / W	0: GPIO9 is inactive. 1: GPIO9 is active.
0	R / W	0: GPIO8 is inactive. 1: GPIO8 is active.

CR E1h. GPIOs Reset Source Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 90h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSMRST# reset source select. 0: VSB and PSOUT# 1: VSB and PSOUT# and Deep_S5_Ctrl
6	R / W	PSOUT# 3.8 second block 0: Disable 1: Limit PSOUT# maximum pulse about 3.8 second
5	Reserved	

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>Pin107 function selection
<table>
<tr><td>LD9_CRE1[4]</td><td>CR1C[5]</td><td>Pin107</td></tr>
<tr><td>1</td><td>X</td><td>THERMTRIP#</td></tr>
<tr><td>0</td><td>1</td><td>GP66</td></tr>
<tr><td>0</td><td>0</td><td>THERMTRIP#</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>GPBX_MRST
0: GPBX reset by RSMRST#.
1: GPBX reset by SLP_S5#.</td></tr>
<tr><td>2</td><td>R / W</td><td>GPAX_MRST
0: GPAX reset by RSMRST#.
1: GPAX reset by SLP_S5#.</td></tr>
<tr><td>1</td><td>R / W</td><td>GP9X_MRST
0: GP9X reset by RSMRST#.
1: GP9X reset by SLP_S5#.</td></tr>
<tr><td>0</td><td>R / W</td><td>GP8X_MRST
0: GP8X reset by RSMRST#.
1: GP8X reset by SLP_S5#.</td></tr>
</table>

CR E2h. GPIOs Reset Source Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	GP7X_MRST 0: GP7X reset by LRESET#. 1: GP7X reset by PWROK.
6	R / W	GP6X_MRST 0: GP6X reset by RSMRST#. 1: GP6X reset by SLP_S5#.
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLP_S5#.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLP_S5#.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLP_S5#.

BIT	READ / WRITE	DESCRIPTION
2	R / W	GP2X_MRST 0: GP2X reset by LRESET#. 1: GP2X reset by PWROK.
1	R / W	GP1X_MRST 0: GP1X reset by RSMRST#. 1: GP1X reset by SLP_S5#.
0	R / W	GP0X_MRST 0: GP0X reset by RSMRST#. 1: GP0X reset by SLP_S5#.

CR E3h. GPIO63, 64, 44 & 45 Event Route Selection Register

Location: Address E3h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable GP63 event route to PSOUT#. 1: Enable GP63 event route to PSOUT#.
6	R / W	0: Disable GP64 event route to PSOUT#. 1: Enable GP64 event route to PSOUT#.
5	R / W	0: Disable GP44 event route to PSOUT#. 1: Enable GP44 event route to PSOUT#.
4	R / W	0: Disable GP45 event route to PSOUT#. 1: Enable GP45 event route to PSOUT#.
3	R / W	0: Disable GP63 event route to PME#. 1: Enable GP63 event route to PME#.
2	R / W	0: Disable GP64 event route to PME#. 1: Enable GP64 event route to PME#.
1	R / W	0: Disable GP44 event route to PME#. 1: Enable GP44 event route to PME#.
0	R / W	0: Disable GP45 event route to PME#. 1: Enable GP45 event route to PME#.

CR E4h.

Location: Address E4h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 30h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	**WDT3_EN** 0: disable WDT3 1: enable WDT3
1-0	R / W	**ACLOSS_PSOUT_DLY** (Default= 00) (This bit affect power loss and set always on function) 00: 0.5 ~ 0.75sec 01: 1 ~ 1.25sec 10: 1.5 ~ 1.75sec 11: 2 ~ 2.25sec

CR E6h. Port80 Programmable Address Low byte

Location: Address E6h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Low byte of programmable Port80 address

CR E7h. Port80 Programmable Address High byte

Location: Address E7h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	High byte of programmable Port80 address

CR F0h. GPIO8 I/O Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

CR F1h. GPIO8 Data Register

Location: Address F1h

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h (The default value is for output data. It can be read when the corresponding GPIO group is activated in CR30h and set to output mode.)

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Data register For output ports, the respective bits can be read/ written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO8 Inversion Register

Location: Address F2h

Attribute: Read/Write

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO8 Status Register

Location: Address F3h

Attribute: Read Only

Power Well: VSB

Reset by: GP8X_MRST

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit will clear it to 0.

CR F4h. GPIO9 I/O Register

Location: Address F4h

Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 I/O register 0: The respective GPIO9 PIN is programmed as an output port 1: The respective GPIO9 PIN is programmed as an input port.

CR F5h. GPIO9 Data Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 Data register For output ports, the respective bits can be read/ written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO9 Inversion Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO9 Status Register

Location: Address F7h
Attribute: Read Only
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO9 Event Status Bit 7-0 corresponds to GP97-GP90, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit will clear it to 0.

CR F8h. GPIOA I/O Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: GPAX_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOA I/O register 0: The respective GPIOA PIN is programmed as an output port 1: The respective GPIOA PIN is programmed as an input port.

CR F9h. GPIOA Data Register

Location: Address F9h
Attribute: Read/Write
Power Well: VSB
Reset by: GPAX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOA Data register For output ports, the respective bits can be read/ written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FAh. GPIOA Inversion Register

Location: Address Fah
Attribute: Read/Write
Power Well: VSB
Reset by: GPAX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOA Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FBh. GPIOA Status Register

Location: Address FBh
Attribute: Read Only
Power Well: VSB
Reset by: GPAX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIOA Event Status Bit 7-0 corresponds to GPA7-GPA0, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit will clear it to 0.

CR FCh. GPIOB I/O Register

Location: Address FCh
Attribute: Read/Write
Power Well: VSB
Reset by: GPBX_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOB I/O register 0: The respective GPIOB PIN is programmed as an output port 1: The respective GPIOB PIN is programmed as an input port.

CR FDh. GPIOB Data Register

Location: Address FDh
Attribute: Read/Write
Power Well: VSB
Reset by: GPBX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOB Data register For output ports, the respective bits can be read/ written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR FEh. GPIOB Inversion Register

Location: Address Feh
Attribute: Read/Write
Power Well: VSB
Reset by: GPBX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIOB Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR FFh. GPIOB Status Register

Location: Address FFh
Attribute: Read Only
Power Well: VSB
Reset by: GPBX_MRST
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIOB Event Status Bit 7-0 corresponds to GPB7-GPB0, respectively. 0: No active edge (rising/falling) has been detected 1: An active edge (rising/falling) has been detected Read the status bit will clear it to 0.

23.10 Logical Device A (ACPI)

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 01h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN# is wire-AND and connected to PSOUT#.
1: PSIN# is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Enable CIR wake-up
0: Disable CIR wake-up function via PSOUT#.
1: Enable CIR wake-up function via PSOUT#.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.

CR E1h. KBC Wake-Up Index Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Location: Address E3h
Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.

BIT	READ / WRITE	DESCRIPTION
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN#_STS 0: No PSIN# event issued. 1: PSIN# event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Location: Address E4h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control bits => (VBAT) **Bits** **6 5** 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logical Device A, CRE6[4])
4	R / W	3VSBSW Enable bit => (Reset by 3VCC) 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. (this bit is reset by LRESET#) (Note. This bit is to generate PSOUT# via KB or MS under S1.) 0: Disable. 1: Enable.
1-0	Reserved.	

CR E5h. PWROK Option Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	PWROK source selection. 0: PSON#. 1: SLP_S3#.
0	R / W	ATXPGD signal to control PWROK 0: Enable. 1: Disable.

CR E6h.

Location: Address E6h
Attribute: Read/Write
Power Well: VRTC
Reset by: RSMRST#(Bit5, Bit3-1), Battery reset(Bit7, Bit4), VCC reset(Bit0)
Default : 0Ch
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. Write 1 to this bit to clear CASEOPEN status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF.

BIT	READ / WRITE	DESCRIPTION
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS 1 1 1: 420 ~ 560mS
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger the PWROK signal from low to high.

CR E7h.

Location: Address E7h
Attribute: Read/Write
Power Well: VRTC
Reset by: RSMRST#, Battery reset (Bit0, 1, 4)
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.

BIT	READ / WRITE	DESCRIPTION
4	R / W	EN_ONPSOUT Disable/Enable to issue a 0.5s(Default) delay PSOUT# level when system returns from power loss state. The PSOUT# delay time refer to Logical Device 9, CR E4[1:0] 0: Disable. 1: Enable.
3	R / W	Select WDT1 reset source 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2-1	Reserved.	
0	R / W	Hardware Monitor RESET source select 0: PWROK. 1: LRESET#.

CR EDh.

Location: Address EDh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Reserved.	Reserved.
3-2	Reserved.	
1	R / W	Keyboard souce select for PME# wake-up 0: KDAT falling edge event 1: Any key or Password event (reference LDA CRE0 [Bit0])
0	R / W	Mouse souce select for PME# wake-up 0: MDAT falling edge event 1: Mouse button event (reference LDA CRE0 [Bit4])

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Pin64 function selection LDA_CRF0[7:6] = 1x → DEEP_S5_2 LDA_CRF0[7:6] = 00 → 3VSBSW LDA_CRF0[7:6] = 01 → LATCH_BKFD_CUT
5-0	Reserved.	

CR F1h.
Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME# status of the RIA event. Write 1 to clear this status.
6	R / W-Clear	PME# status of the RIB event. Write 1 to clear this status.
5	R / W-Clear	PME# status of the RIC event. Write 1 to clear this status.
4	R / W-Clear	PME# status of the RID event. Write 1 to clear this status.
3	R / W-Clear	PME# status of the RIE event. Write 1 to clear this status.
2	R / W-Clear	PME# status of the RIF event. Write 1 to clear this status.
1-0	Reserved.	

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : C4h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable

BIT	READ / WRITE	DESCRIPTION
4-3	Reserved.	
2	R / W	VHIF Debounce Enable bit 0 : Disable 1 : Enable
1	Reserved.	
0	R / W	EN_PME# => 0 : Disable PME#. 1 : Enable PME#.

CR F3h.

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W-Clear	PME# status of the Mouse event. Write 1 to clear this status.
4	R / W-Clear	PME# status of the KBC event. Write 1 to clear this status.
3	R / W-Clear	PME# status of the PRT IRQ event. Write 1 to clear this status.
2	Reserved	
1	R / W-Clear	PME# status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME# status of the URB IRQ event. Write 1 to clear this status.

CR F4h.

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME# status of the URC IRQ event. Write 1 to clear this status.

BIT	READ / WRITE	DESCRIPTION
6	R / W-Clear	PME# status of the URD IRQ event. Write 1 to clear this status.
5	R / W-Clear	PME# status of the URE IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME# status of the URF IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME# status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME# status of the WDT1 event. Write 1 to clear this status.
1	R / W-Clear	PME# status of the RIA event. Write 1 to clear this status.
0	R / W-Clear	PME# status of the RIB event. Write 1 to clear this status.

CR F5h.
Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable PME# interrupt of the URC IRQ event. 1: Enable PME# interrupt of the URC IRQ event.
6	R / W	0: Disable PME# interrupt of the URD IRQ event. 1: Enable PME# interrupt of the URD IRQ event.
5	R / W	0: Disable PME# interrupt of the URE IRQ event. 1: Enable PME# interrupt of the URE IRQ event.
4	R / W	0: Disable PME# interrupt of the URF IRQ event. 1: Enable PME# interrupt of the URF IRQ event.
3-2	Reserved.	
1	R / W	0: Disable PME# interrupt of the RIA event. 1: Enable PME# interrupt of the RIA event.
0	R / W	0: Disable PME# interrupt of the RIB event. 1: Enable PME# interrupt of the RIB event.

CR F6h.
Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#

Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC event. 1: Enable KB, MS interrupt of the KBC event.
6	R / W	0: Disable PME# interrupt of the RIA event. 1: Enable PME# interrupt of the RIA event.
5	R / W	0: Disable PME# interrupt of the Mouse event. 1: Enable PME# interrupt of the Mouse event.
4	R / W	0: Disable PME# interrupt of the KBC event. 1: Enable PME# interrupt of the KBC event.
3	R / W	0: Disable PME# interrupt of the PRT IRQ event. 1: Enable PME# interrupt of the PRT IRQ event.
2	Reserved	
1	R / W	0: Disable PME# interrupt of the URA IRQ event. 1: Enable PME# interrupt of the URA IRQ event.
0	R / W	0: Disable PME# interrupt of the URB IRQ event. 1: Enable PME# interrupt of the URB IRQ event.

CR F7h.
Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable PME# interrupt of the RIC event. 1: Enable PME# interrupt of the RIC event.
6	R / W	0: Disable PME# interrupt of the RID event. 1: Enable PME# interrupt of the RID event.
5	R / W	0: Disable PME# interrupt of the RIE event. 1: Enable PME# interrupt of the RIE event.
4	R / W	0: Disable PME# interrupt of the CIRWAKEUP event. 1: Enable PME# interrupt of the CIRWAKEUP event.
3	R / W	0: Disable PME# interrupt of the HM IRQ event. 1: Enable PME# interrupt of the HM IRQ event.
2	R / W	0: Disable PME# interrupt of the WDT1 event. 1: Enable PME# interrupt of the WDT1 event.
1	R / W	0: Disable PME# interrupt of the RIF event. 1: Enable PME# interrupt of the RIF event.

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: Disable PME# interrupt of the RIB event. 1: Enable PME# interrupt of the RIB event.

CR F8h.

Location: Address F8h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-1	R / W	Pin108 function selection LDA_CRF8 [2:1] / Pin108 00 / 14.7456MHZ_CLKIN 01 / GP67 1x / ATXPGD
0	R / W	0: Disable RSMRST# always monitor PSOUT# 1: Enable RSMRST# always monitor PSOUT#

CR FAh. GPIO Wakeup Status

Location: Address FAh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME# status of the GP63 event. Write 1 to clear this status.
6	R / W-Clear	PME# status of the GP64 event. Write 1 to clear this status.
5	R / W-Clear	PME# status of the GP44 event. Write 1 to clear this status.
4	R / W-Clear	PME# status of the GP45 event. Write 1 to clear this status.
3-0	Reserved.	

CR FFh. ACPI Pin Type

Location: Address FFh

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	PWROK Push-Pull / OD select 0: Push-Pull 1: Open Drain (Default)
3-0	Reserved.	

23.11 Logical Device B (HM, LED)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Location: Address 62h, 63h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 64h, 65h.

Location: Address 64h, 65h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the read-only HM base address <100h : FFEh> along a two-byte boundary.

CR 70h.
Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register
Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register
Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN0 Duty Cycle Register
Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN0 Duty Cycle Register

CR E3h. AUXFAN1 Duty Cycle Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN1 Duty Cycle Register

CR E4h. AUXFAN2 Duty Cycle Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN2 Duty Cycle Register

CR F0h. FANIN de-bouncer Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	1: Enable AUXFANIN0 input de-bouncer. 0: Disable AUXFANIN0 input de-bouncer.
6	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
5	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
4	R / W	1: Enable AUXFANIN1 input de-bouncer. 0: Disable AUXFANIN1 input de-bouncer.
3	R / W	1: Enable AUXFANIN2 input de-bouncer. 0: Disable AUXFANIN2 input de-bouncer.
2-0	Reserved.	

CR F1h. SMI IRQ Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	SMI IRQ Enable
6	Reserved.	
5-4	R / W	HM_TEM_SEL 00: PORT80 data from LPC or I2C 01: CPU temperature 10: SYS temperature 11: AUX temperature
3	Reserved.	
2-0	R / W	Bank Selection

CR F2h. SMBus de-bouncer Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: Enable SCL input de-bouncer 80 ~ 120ns. 1: Disable SCL input de-bouncer.
0	R / W	0: Enable SDA input de-bouncer 80 ~ 120ns. 1: Disable SDA input de-bouncer.

CR F3h. Deep S5 Front Panel Green & Yellow LED control register

Location: Address F3h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**DEEPS5_YLW_BLK_FREQ** bits (This function affects by LDB CRF7 Bit 5) 1xxx : Fading LED. 0111 : YLW_LED will drive low. 0110 : YLW_LED will output 2Hz , 50% duty-cycle signal. 0101 : YLW_LED will output 1Hz , 50% duty-cycle signal. 0100 : YLW_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : YLW_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : YLW_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : YLW_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : YLW_LED will output High-Z. (since YLW_LED pin is open-drain).
3-0	R / W	**DEEPS5_GRN_BLK_FREQ** bits (This function affects by LDB CRF7 Bit 4) 1xxx : Fading LED. 0110 : GRN_LED will output 2Hz , 50% duty-cycle signal. 0101 : GRN_LED will output 1Hz , 50% duty-cycle signal. 0100 : GRN_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : GRN_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : GRN_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : GRN_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : GRN_LED will output High-Z. (since GRN_LED pin is open-drain).

CR F4h.

Location: Address F4h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved.	

CR F5h. Front panel green LED control register

Location: Address F5h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 87h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	**AUTO_EN** bit Set to 0, the GRN_LED and YLW_LED are controlled by GRN_ LED_ RST, GRN_BLK_FREQ and YLW_LED_RST, YLW_BLK_FREQ bits. Set to 1, the GRN_LED and YLW_LED are controlled by SLP_S5#, SLP_S3# pins and GRN_BLK_FREQ, YLW_BLK_FREQ bits.
6	R / W	**GRN_LED_RST#** Set to 0, GRN_BLK_FREQ will be reset to 000 when (SLP_S3# & internal PWROK) = 0, which means when in S3~S5 states, GRN_LED will output High-Z. Set to 1, GRN_BLK_FREQ will be kept when (SLP_S3# & internal PWROK) = 0.
5	R / W	**GRN_LED_POL** Set to 0 , GRN_LED output is active low. Set to 1 , GRN_LED output is active high.
4	Reserved.	
3-0	R / W	**GRN_BLK_FREQ** bits 1xxx : Fading LED. 0111 : GRN_LED will drive low. 0110 : GRN_LED will output 2Hz , 50% duty-cycle signal. 0101 : GRN_LED will output 1Hz , 50% duty-cycle signal. 0100 : GRN_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : GRN_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : GRN_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : GRN_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : GRN_LED will output High-Z. (since GRN_LED pin is open-drain).

CR F6h.Front panel yellow LED control register

Location: Address F6h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 47h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	**YLW_LED_RST#** Set to 0, YLW_BLK_FREQ will be reset to 000 when (SLP_S3# & internal PWROK) = 0, which means when in S3~S5 states, YLW_LED will output High-Z. Set to 1, YLW_BLK_FREQ will be kept when (SLP_S3# & internal PWROK) = 0.

BIT	READ / WRITE	DESCRIPTION
5	R / W	**YLW_LED_POL** Set to 0, YLW_LED output is active low. Set to 1, YLW_LED output is active high.
4	R / W	**P80_Binary_Sel** Set to 0 : Port80 Binary output disable. (Default) Set to 1 : Port80 Binary output enable.
3-0	R / W	**YLW_BLK_FREQ bits** 1xxx : Fading LED. 0111 : YLW_LED will drive low. 0110 : YLW_LED will output 2Hz , 50% duty-cycle signal. 0101 : YLW_LED will output 1Hz , 50% duty-cycle signal. 0100 : YLW_LED will output 0.5Hz , 50% duty-cycle signal. 0011 : YLW_LED will output 0.25Hz , 50% duty-cycle signal. 0010 : YLW_LED will output 0.125Hz , 50% duty-cycle signal. 0001 : YLW_LED will output 0.0625Hz , 50% duty-cycle signal. 0000 : YLW_LED will output High-Z. (since YLW_LED pin is open-drain).

CR F7h.YLW & GRN Enable register

Location: Address F7h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	**YLW_DEEPS5_SET** 1: YLW_LED always output high-Z. (YLW_LED pin is open-drain) 0: YLW_LED output by DEEPS5_YLW_BLK_FREQ.(CRF4, bit[7:4])
4	R / W	**GRN_DEEPS5_SET** 1: GRN_LED always output high-Z. (GRN_LED pin is open-drain) 0: GRN_LED output by DEEPS5_GRN_BLK_FREQ.(CRF4, bit [3:0])
3-0	Reserved.	

23.12 Logical Device D (WDT2)

CR E0h. Watchdog Timer II (WDT2) Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-2	R / W	Clock select of 5 second Watchdog Timer II **Bits** **3 2** = 0 0, clock rate 4Hz = 0 1, clock rate 1Hz = 1 0, cloak rate 1/2Hz = 1 1, clock rate 1MHz
1-0	R / W	Clock select of 100ms Watchdog Timer II **Bits** **1 0** = 0 0, clock rate 512Hz, WDT will generate 100mS low pulse after 5S = 0 1, clock rate 256Hz, WDT will generate 200mS low pulse after 5S = 1 0, clock rate 1KHz, WDT will generate 50mS low pulse after 5S = 1 1, clock rate 1MHz, WDT will generate 50uS low pulse after 5S

CR E1h. Watchdog Timer II 100ms counter Register

Location: Address E1h
Attribute: Read only
Power Well: VSB
Reset by: RSMRST#
Default : 32h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R	Setting of 100mS watch dog time out counter. Default is 8'h32. **Note. If CRE0[1:0] is 2'b00, then Watchdog Timer II 100ms counter will be 1.95ms(512Hz) * 50(8'h32) = 100m sec**

CR E2h. Watchdog Timer II 5s counter Register

Location: Address E2h
Attribute: Read only
Power Well: VSB
Reset by: RSMRST#
Default : 14h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R	Setting of 5 second watch dog time out counter. Default is 8'h14. **Note. If CRE0[3:2] is 2'b00, then Watchdog Timer II counter will be 0.25s(4Hz) * 20(8'h14) = 5 sec**

CR E3h. Watchdog Timer II Software Reset Register

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R/W	This bit is used to start Watchdog Timer II counter 0: Disable 1: Start the counter. When the time is up, it will clear itself to 0.

CR E4h. Watchdog Timer II Status Register

Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	Watchdog Timer II status. When this bit is set to 1, it means timeout event occurs.
6-0	Reversed.	

CR E5h. KBC Control Register

Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed.	

BIT	READ / WRITE	DESCRIPTION
0	R/W	Keyboard-Mouse short enable. 0: Disable (Default) 1: Enable

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	Mask Watchdog Timer 1 to affect PWROK, then enter Deep_S5 Watchdog Timer chapter has description in detail. 0: Mask enable. (WDT1 not affect PWROK) 1: Mask disable. (WDT1 default affect PWROK)
6	R/W	Mask Watchdog Timer 1 to affect RSMRST# Watchdog Timer chapter has description in detail. 0: Mask enable. (WDT1 not affect RSMRST#) 1: Mask disable. (WDT1 default affect RSMRST#)
5-3	Reversed.	
2	R/W	DIS WAKEUP ESPI ESPI virtual wire WAKE# is controlled by SIO glue logic. 0: Disable. 1: Enable.
1	R/W	Enable Watchdog Timer II.
0	Reversed.	

23.13 Logical Device E (CIR WAKE-UP)

CR 30h.

Location: Address 00h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 19h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Clock 1M to 40K divider register

CR E1h.
Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
2	R/W	Clock 1M to 40K divider number flush. Write 1 then auto-clear.
1	R/W1C	CIR Wake-up clock calibration done status bit. .
0	R/W	CIR Wake-up clock calibration enable. Cleaned once calibration is done.

CR E3h. GPIO, RI PSOUT Wake-Up Status Register
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PSOUT# status of the GP63 event. Write 1 to clear this status.
6	R / W-Clear	PSOUT# status of the GP64 event. Write 1 to clear this status.
5	R / W-Clear	PSOUT# status of the GP44 event. Write 1 to clear this status.
4	R / W-Clear	PSOUT# status of the GP45 event. Write 1 to clear this status.
3	R / W-Clear	PSOUT# status of the RIA# event. Write 1 to clear this status.
2	R / W-Clear	PSOUT# status of the RIB# event. Write 1 to clear this status.
1-0	Reserved.	

CR E4h. GPIO, RI# PSOUT# Wake-Up Control Register
Attribute: Read/Write
Power Well: VRTC

Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	GPIO and RI# PSOUT# Wake-Up Group Select. 0: GPIO 1: GPIO+RI#
0	R / W	GPIO and RI# PSOUT# Wake-Up Mode Select 0: Sleep 1: Sleep+Deep

CR E6h.
Location: Address E6h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R/W	Pin86 function selection LDE_CRE6 [7] / Pin86 0 / PME# 1 / GP85
6	R/W	ESPI OUT SEL 0: Pin70 and Pin73 will be input pins 1: Pin70 and Pin73 will be output pins that drive by eSPI internal signal of SLP_S5# and SLP_S3# .
5	R/W	ESPI SUSWARN# SEL 0: Pin87 will be GP86 or other functions. 1: Pin87 will be output pin that drive by eSPI internal signal of SUSWARN#

BIT	READ / WRITE	DESCRIPTION
4	R/W	ESPI S5 / S4 SEL For Version A : If LDE_CRE6[6]=1 0: Pin70 will drive SLP_S5# by eSPI internal signal 1: Pin70 will drive SLP_S4# by eSPI internal signal If LDE_CRE6[6]=0 0: SLP_S5# as internal SLP_S5# logic 1: SLP_S4# as internal SLP_S5# logic For Version B : (The internal SLP_S5# logic is decided by LD16_CR30[6]) 0: Pin70 will drive SLP_S5# by eSPI internal signal 1: Pin70 will drive SLP_S4# by eSPI internal signal
3	R/W	Enable RIA# for wake up event. 0: Disable RIA# wake up function via PSOUT# (Default) 1: Enable RIA# wake up function via PSOUT#
2	R/W	Enable RIB# for wake up event. 0: Disable RIB# wake up function via PSOUT# (Default) 1: Enable RIB# wake up function via PSOUT#
1	R/W1C	RESETIC Enable bit 1: Enable RESETIC 0: Disable (Default) .
0	R/W	ATX5VSB Enable bit 1: Enable ATX5VSB 0: Disable (Default)

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-1	R / W	OOB Destination Slave Address. (Default: 01h for PCH Temperature)
0	Reserved (always 0)	

CR F1h.

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 0Fh

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-1	R / W	OOB Source Slave Address. (Default: 07h)
0	Reserved (always 1)	

CR F2h.
Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#(Bit5-4,1-0), RSMRST#(Bit3-2)
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-6	R	ESPI OOB polling status: 00: No request 01: Polling CPU Temperature 10: Polling PCH Temperature 11: Reserved
5-4	R / W	ESPI OOB polling time: 00: 0.5 second 01: 1 second (Default) 10: 2 second 11: 4 second
3	R / W	Switch to ESPI PCH reading 0: Read SMBus PCH Temperature (Default) 1: Read ESPI PCH Temperature
2	R / W	Switch to ESPI CPU reading (only for Agent0, Domain0) 0: Read PECI CPU Temperature (Default) 1: Read ESPI CPU Temperature
1	R / W	ESPI polling PCH Temperature Enable.
0	R / W	ESPI polling CPU Temperature Enable. (only for Agent 0, Domain0)

CR F3h.
Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Mask eSPI OOB polling under S0ix state (Monitor S0_IDLE#) 0: Disable 1: Enable
3-0	Reserved.	

CR F4h.
Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST
Default : 49h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td colspan="2">Reserved.</td></tr>
<tr><td>5</td><td>R / W</td><td>Port81 function enable bit.
0: Disable
1: Enable</td></tr>
<tr><td>4</td><td colspan="2">Reserved.</td></tr>
<tr><td>3</td><td>R / W</td><td>Pin19 function selection
<table>
<tr><th>CR 2F[5] (LPC_ESPI_SEL)</th><th>LDE_CRF4[3]</th><th>Pin 19 w/ PU / PD</th><th>Pin19</th></tr>
<tr><td>0 (LPC)</td><td>0</td><td>x</td><td>CLKRUN#</td></tr>
<tr><td>0 (LPC)</td><td>1</td><td>x</td><td>GPB0</td></tr>
<tr><td>1 (eSPI)</td><td>x</td><td>Pull-Up</td><td>ESPI_ALERT_HNSK</td></tr>
<tr><td>1 (eSPI)</td><td>x</td><td>Pull-Down</td><td>GPB0</td></tr>
</table></td></tr>
<tr><td>2-0</td><td colspan="2">Reserved.</td></tr>
</table>

CR F7h.
Location: Address F7h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 0Bh

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4-2	R / W	MAXFREQ (Maximum Frequency Supported) 000: 20MHz 001: 25MHz 010: 33MHz (Default) 011: 50MHz Others: Reserved
1-0	Reserved.	

CR FAh. S0ix Control Register
Location: Address FAh
Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST
Default : 20h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Reserved</td></tr>
<tr><td>6</td><td>R / W</td><td>Pin87 function selection
<table>
<tr><th>LDE_CRFA [Bit6]</th><th>CR1C[Bit7]</th><th>CR1A[Bit7]</th><th>CR1B[Bit2]</th><th>Pin 87</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>PCH_PSON#</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>IRRX</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP86</td></tr>
</table>
Pin95 function selection
<table>
<tr><th>LDE_CRFA[6]</th><th>CR1D[3:2]</th><th>Pin 95</th></tr>
<tr><td>1</td><td>xx</td><td>S0_IDLE#</td></tr>
<tr><td>0</td><td>01</td><td>SMI#</td></tr>
<tr><td>0</td><td>00</td><td>OVT#</td></tr>
<tr><td>0</td><td>1x</td><td>GP87</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin16 function selection
<table>
<tr><th>LDE_CRFA [Bit5]</th><th>Pin16</th></tr>
<tr><td>0</td><td>GA20M</td></tr>
<tr><td>1</td><td>SLPS0#</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>PCH_PSON# invert enable
0: Disable
1: Enable (invert the PCH_PSON# from pin)</td></tr>
<tr><td>3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>S0ix channel menchanism enable bit.
0: Disable
1: Enable</td></tr>
<tr><td>1</td><td>R / W</td><td>S0ix input debounce enable
0: SLPS0# and PCH_PSON# will debounce 10us.
1: SLPS0# and PCH_PSON# won’t debounce.</td></tr>
<tr><td>0</td><td>R / W</td><td>S0ix Enable bit
0: Disable (Default)
1: Enable modern standby function</td></tr>
</table>

CR FBh.
Location: Address FBh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST

Default : 48h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Mask PME# wakeup event under S0ix state (Monitor PSON#) 0: Disable 1: Enable
5	R / W	Mask SMIOVT event under S0ix state (Monitor S0_IDLE) 0: Disable 1: Enable
4	R / W	Isolation UARTA~F and SOUT_P80 pin type (tri-state) under S0ix state (Monitor PSON#) 0: Disbale 1: Enable
3	R / W	Mask PSOUT# wakeup event under S0ix state (Monitor PSON#) 0: Disable 1: Enable
2	R / W	Isolation PRT pin type (tri-state) under S0ix state (Monitor PSON#) 0: Disbale 1: Enable
1	Reserved.	
0	R / W	Mask PECI detection under S0ix state (Monitor SLP_S0#) 0: Disable 1: Enable

23.14 Logical Device F (GPIO)

CR E0h.

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E1h.

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E2h.

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E3h.

Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP3 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E4h.
Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E5h.
Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E6h.
Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E7h.
Location: Address E7h
Attribute: Read/Write

Power Well: VSB
Reset by: GP7X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP7 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E8h.
Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP8 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR E9h.
Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP9 Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR EAh.
Location: Address EAh
Attribute: Read/Write
Power Well: VSB
Reset by: GPAX_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPA Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR EBh.

Location: Address EBh
Attribute: Read/Write
Power Well: VSB
Reset by: GPBX_MRST
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPB Push-Pull/OD select 0: Push-Pull 1: Open Drain

CR F0h. I2C Control & Address Register

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 9Dh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register

Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	LPC or I2C to 80PORT switch 0: LPC 1: I2C

CR F2h. I2C to 80PORT Data Register

Location: Address F2h

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

CR F3h. I2C to 81PORT Data Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 81PORT Data

CR F4h. GPIO Transition Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 40h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	GPO pulse width control bits, default value is 100ms (2'b01) 00: 200ms 01: 100ms 10: 50ms 11: 10ms
5-1	Reserved	
0	R / W	GPIO Transition Enable 0: Disable 1: Enable

23.15 Logical Device 10 (UARTC)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 3 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 3.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART C clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART C clock source is 24 MHz (24 MHz / 1). 1 1: UART C clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTC 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.

BIT	READ / WRITE	DESCRIPTION
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTC 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTC 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTC 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTC 9bit-mode Interrupt Control Register

Location: Address F6h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTC 9bit-mode IRQ output. 1: Enable UARTC 9bit-mode IRQ output.

CR F7h. UARTC 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved	
0	R	**UARTC 9bit-mode Status Bit** 0: UARTC 9bit-mode IRQ have not been triggered. 1: UARTC 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTC Control Register
Location: Address F8h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartCD_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5	Reserved.
4	uartCD_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

23.16 Logical Device 11 (UARTD)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h, E0h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 4 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 4.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART D clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART D clock source is 24 MHz (24 MHz / 1). 1 1: UART D clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTD 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.

BIT	READ / WRITE	DESCRIPTION
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTD 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTD 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTD 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTD 9bit-mode Interrupt Control Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTD 9bit-mode IRQ output. 1: Enable UARTD 9bit-mode IRQ output.

CR F7h. UARTD 9bit-mode IRQ Status Register

Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved	
0	R	**UARTD 9bit-mode Status Bit** 0: UARTD 9bit-mode IRQ have not been triggered. 1: UARTD 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTD Control Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register Bit7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

23.17 Logical Device 12 (UARTE)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, E8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 5 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 5.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART E clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART E clock source is 24 MHz (24 MHz / 1). 1 1: UART E clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTE 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.

BIT	READ / WRITE	DESCRIPTION
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTE 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTE 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTE 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTE 9bit-mode Interrupt Control Register

Location: Address F6h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTE 9bit-mode IRQ output. 1: Enable UARTE 9bit-mode IRQ output.

CR F7h. UARTE 9bit-mode IRQ Status Register

Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved.	
0	R	**UARTE 9bit-mode Status Bit** 0: UARTE 9bit-mode IRQ have not been triggered. 1: UARTE 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTE Control Register

Location: Address F8h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved	uartEF_switch _enable	Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5	Reserved.
4	uartEF_switch_enable (Bypass mode) 0: switch disable 1: switch enable
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

23.18 Logical Device 13 (UARTF)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h, E8h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 6 I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 6.

CR F0h.

Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART F clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: UART F clock source is 24 MHz (24 MHz / 1). 1 1: UART F clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h. UARTF 9bit-mode Config Register

Location: Address F2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_auto_RX_ctrl** 0: 9bit-mode RX block function will pass all data or address byte and not compare any address byte. 1: 9bit-mode RX block function could only receive address byte and compare the address bytes. (The address matched or not will issue IRQ. Refer to CRF6 description)
6	R / W	**En_auto_only_addr_comp** 0: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will compare the address byte and update the RX_ctrl Bit automatically. 1: When setting en_auto_RX_ctrl =1'b1, 9bit-mode RX block function will only compare the address byte. But the RX_ctrl Bit will not be updated automatically by 9bit-mode RX block function.
5	R / W	**RTS_low_time_sel** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 2 bit time before inverting the driving signal.
4	R / W	**RS485_RTS_inv_sel** 0: Automatic drive RTS# high when receiving data. Automatic drive RTS# low when transmitting data. 1: Automatic drive RTS# low when receiving data. Automatic drive RTS# high when transmitting data.
3	R / W	**En_auto_TX_ctrl** 0: En_address_byte bit will not be automatic updated to "logic 0" by hardware after TX block sent address byte. 1: En_address_byte bit will be automatic updated to "logic 0" by hardware after TX block sent address byte.
2	R / W	**En_auto_RX_ctrl** 0: the address byte will be ignored by the receiver. 1: the address byte will be received into RX FIFO by the receiver.

BIT	READ / WRITE	DESCRIPTION
1	R / W	**En_RS485_RTS** 0: RS232 driver 1: RS485 driver The 9bit-mode TX block function will drive RTS_L to high when transmit data automatically
0	R / W	**En_9bit_mode** 0: normal UART function. 1: enable 9-bit mode function. (9bit-TX block use parity bit as address/Data bit when setting En_9bit_mode = 1'b1.)

CR F3h. UARTF 9bit-mode Slave Address Register

Location: Address F3h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave address**

CR F4h. UARTF 9bit-mode Slave Mask Address Register

Location: Address F4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Slave mask address**

CR F5h. UARTF 9bit-mode Broadcast Address Register

Location: Address F5h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	**Broadcast Address**

CR F6h. UARTF 9bit-mode Interrupt Control Register

Location: Address F6h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	**IRQ_type_sel** 0: 9bitemode RX block function will issue an IRQ when receive any address byte. (when **IRQ_addr_Enable** bit = 1) 1: 9bitemode RX block function will issue an IRQ when only receive the matched address byte. (when **IRQ_addr_Enable** bit = 1)
0	R / W	**IRQ_addr_Enable** 0: Disable UARTF 9bit-mode IRQ output. 1: Enable UARTF 9bit-mode IRQ output.

CR F7h. UARTF 9bit-mode IRQ Status Register
Location: Address F7h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	R / W	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5	R / W	**RTS485_no_delay** 0: TX block will keep 1 bit time before inverting the driving signal. 1: TX block will keep 0 bit time before inverting the driving signal. (When RTS485_no_delay CRF7 Bit5=1 and RTS_low_time_sel CRF2 Bit5=1, TX block will keep 0 bit time before inverting the driving signal.)
4-1	Reserved	
0	R	**UARTF 9bit-mode Status Bit** 0: UARTF 9bit-mode IRQ have not been triggered. 1: UARTF 9bit-mode IRQ have been triggered.

CR F8h. Extending UARTF Control Register
Location: Address F8h

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	fifo_level _mode		Reserved		Reserved (All should be set to 0)			Enable_128 bytes_fifo
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	fifo_level_mode: (Also check UFR register B7-6 definition)
5-4	Reserved.
3-1	Reserved. (All should be set to 0)
0	Extending fifo enable bit: 0: Disable 128 bytes TX and RX FIFO. 1: Enable 128 bytes TX and RX FIFO.

UFR_ BIT 7	UFR_ BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)			
		FIFO_LEVEL_ MODE (CRF8_B7:6 = 00)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 01)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 10)	FIFO_LEVEL_ MODE (CRF8_B7:6 = 11)
0	0	01	16	80	112
0	1	04	32	88	116
1	0	08	48	96	120
1	1	14	64	104	124

23.19 Logical Device 14 (PORT80, IR)

CR 30h.

Location: Address 30h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: IR is inactive. 1: IR is active.

CR 60h, 61h.

Location: Address 60h, 61h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h
Size: 16 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Location: Address 70h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for IR.

CR E0h. PORT80 UART Control Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 80h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved.	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length selection) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved.	

CR E1h. PORT80 UART Status Register

Location: Address E1h
Attribute: Read Only
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte

Location: Address E3h
Attribute: Read/Write

Power Well: VSB
Reset by: LRESET#
Default : 10h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer
Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

CR F0h.
Location: Address F0h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: Reserved. 1 0: IR clock source is 24 MHz (24 MHz / 1). 1 1: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h.
Location: Address F1h
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	

BIT	READ / WRITE	DESCRIPTION
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into IRRX
100	ASK-IR	Inverting IRTX pin	Routed to IRRX
101	ASK-IR	Inverting IRTX & 500 KHZ clock	Routed to IRRX
110	ASK-IR	Inverting IRTX	Demodulation into IRRX
111*	ASK-IR	Inverting IRTX & 500 KHZ clock	Demodulation into IRRX

Note: The notation is normal mode in the IR function.

23.20 Logical Device 15 (FADING LED)

CR E0h. Fading Maximum Duty Cycle Value Register

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-0</td><td>R / W</td><td>Fading_led_maxval
This byte reference LED frequency select, CRE5 bit[1] and fading LED enable, CRE5 bit[0], LED frequency select bit has higher priority, the combination of LED frequency select and fading LED enable describe below. When solid LED mode, this byte is duty cycle control register, and frequency control by CRE8.

Led frequency before divider select = 1 and fading led enable = 1 is fading LED
The maximum duty cycle value.

Led frequency before divider select = 0 or fading led enable = 0 is solid LED
<table>
<tr><th>maxval</th><th>ratio</th><th></th><th>Duty cycle</th></tr>
<tr><td>0x01</td><td>1/255</td><td>=</td><td>0.3%</td></tr>
<tr><td>0x02</td><td>2/255</td><td>=</td><td>0.7%</td></tr>
<tr><td colspan="4">…</td></tr>
<tr><td>0x40</td><td>64/255</td><td>=</td><td>25.1%</td></tr>
<tr><td colspan="4">…</td></tr>
<tr><td>0xFF</td><td>255/255</td><td>=</td><td>100%</td></tr>
</table>
</td></tr>
</table>

CR E1h. Fading Middle Duty Cycle Value Register

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 3Fh
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_midval This byte is the turning point duty cycle value between minimum and maximum duty cycle value.

CR E2h. Fading Minimum Duty Cycle Value Register

Location: Address E2h
Attribute: Read/Write
Power Well: VSB

Reset by: RSMRST#
Default : 01h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_minval This byte is the minimum duty cycle value.

CR E3h. Fading Increase Duty Cycle Value Register
Location: Address E3h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 11h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_led_duty_inc_h The increased duty cycle value between the turning point and the maximum duty cycle value.
3-0	R / W	Fading_led_duty_inc_l The increased duty cycle value between the minimum duty cycle value and turning point.

CR E4h. Fading Decrease Duty Cycle Value Register
Location: Address E4h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 11h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_led_duty_dec_h The decreased duty cycle value between the maximum duty cycle value and the turning point.
3-0	R / W	Fading_led_duty_dec_l The decreased duty cycle value between the turning point and the minimum duty cycle value.

CR E5h. Fading Configure Register
Location: Address E5h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_led_prgval Repeat each duty cycle value for a few times.

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3-2</td><td>R / W</td><td>Fading LED extend enable bits
00: No extend.
01: Only extend the minimum duty cycle.
10: Only extend the maximum duty cycle.
11: Both extend the minimum and the maximum duty cycle.</td></tr>
<tr><td>1</td><td>R / W</td><td>LED frequency before frequency divider select
Fading LED is only allowed when this bit select 1 (1kHz). When this bit turns to 0 (4Hz). It forces to solid LED mode regardless Fading LED enable bit (LD15 CRE5 Bit0).
0: 4Hz
1: 1kHz (default)</td></tr>
<tr><td>0</td><td>R / W</td><td>Fading LED enable
0: Solid LED
1: Fading LED
<table>
<tr><th>LD15 CRE5 bit[1:0]</th><th>Led mode</th></tr>
<tr><td>00</td><td>Solid LED and 4Hz before divider</td></tr>
<tr><td>01</td><td>Solid LED and 4Hz before divider</td></tr>
<tr><td>10</td><td>Solid LED and 1kHz before divider</td></tr>
<tr><td>11</td><td>Fading LED and 1kHz before divider</td></tr>
</table></td></tr>
</table>

CR E6h. Fading Light extend Register

Location: Address E6h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the maximum duty cycle value. The extend time reference to fading LED frequency: Extend time = (extend value * 4) / fading LED frequency

CR E7h. Fading Dark extend Register

Location: Address E7h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the minimum duty cycle value. The extend time reference to fading LED frequency: Extend time = (extend value * 4) / fading LED frequency

CR E8h. Fading Frequency Divide Register

Location: Address E8h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-0</td><td>R / W</td><td>Fading LED frequency divide factor
when fading frequency before divider select = 1
(It can select fading or solid mode depend on LD15 CRE5 bit0)
<table>
<tr><td></td><td></td><td></td><td>LED frequency</td><td></td></tr>
<tr><td>0x01:</td><td>1kHz/1</td><td>=</td><td>1kHz</td><td></td></tr>
<tr><td>0x02:</td><td>1kHz/2</td><td>=</td><td>500Hz</td><td></td></tr>
<tr><td colspan="4">…</td><td></td></tr>
<tr><td>0x10:</td><td>1kHz/16</td><td>=</td><td>62Hz</td><td></td></tr>
<tr><td colspan="4">…</td><td></td></tr>
<tr><td>0xFF:</td><td>1kHz/255</td><td>=</td><td>4Hz</td><td></td></tr>
</table>
When fading LED frequency before divider select = 0
(It force to solid LED mode)
<table>
<tr><td></td><td>Solid LED frequency</td></tr>
<tr><td>0x00:</td><td>Output low</td></tr>
<tr><td>0x01:</td><td>High-z</td></tr>
<tr><td>0x02:</td><td>4Hz</td></tr>
<tr><td>0x03:</td><td>2Hz</td></tr>
<tr><td>0x04:</td><td>1Hz</td></tr>
<tr><td>0x05:</td><td>1/2Hz</td></tr>
<tr><td>0x06:</td><td>1/4Hz</td></tr>
<tr><td>0x07:</td><td>Output low</td></tr>
<tr><td>others</td><td>High-z</td></tr>
</table></td></tr>
</table>

CR E9h. Suspend LED S5 Enable Register

Location: Address E9h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	SUSLED only follows fading LED in S5 state 0: SUSLED works in S5, S3 and S0 state. 1: SUSLED only works in S5 state.

23.21 Logical Device 16 (DEEP SLEEP)

CR 30h. Deep Sleep configuration register

Location: Address 30h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : A0h
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	Interal SLP_S5# logic seclection (For ESPI mode / Version B only) 0: Interal SLP_S5# logic is driven by eSPI internal signal of SLP_S5#. 1: Interal SLP_S5# logic is driven by eSPI internal signal of SLP_S4#.
5-1	R / W	Reserved
0	R / W	Deep S5 Enable Set to 0, If SLP_S5# state, will not enter Deep S5 state. Set to 1, If SLP_S5# state, will enter Deep S5 state.

CR E0h. Deep Sleep wake up PSOUT# delay time

Location: Address E0h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 20h (Default: 512ms)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Location: Address E1h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 04h (Default: 128 ms)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R/W	Deep_S5_2 signal status. 0: Deep_S5_2 signal always keep low. 1: Deep_S5_2 signal follow Deep_S5_1 signal.
6	Reserved.	
5	R/W	SUSLED Enable 0: Disable (default and output low) 1: Enable
4	Reserved.	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control

Location: Address E2h
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 05h (Default: 5 sec)
Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

CR E3h. WDT1 to Deep Sleep Delay Time Control

Location: Address E3h
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	Watchdog Timer 1 wake up auto mode. 0: SIO will not wake up system after RSMRST# release 1: SIO will wake up system after RSMRST# release.

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	Deep Sleep Watchdog Timer 1 Delay Time Control. When system will enter Deeps5 by watchdog timer 1, SIO will set a delay time to control. Delay time: 2, 4, 6, 8 sec = register: 0, 1, 2, 3

24. SPECIFATIONS

24.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	-40 to +85	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

24.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VSB Quiescent Current	IVSB			25	mA	VCC = 3.3 V VSB (AVSB)= 3.3 V LRESET = High CASEOPEN Pull-Up to VBAT
VCC Quiescent Current	IVCC			1	mA	
Vtt Quiescent Current	IVTT			1	mA	VCC = 3.3 V VSB (AVSB)= 3.3 V VTT = 1.2V LRESET = High CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						
In_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	

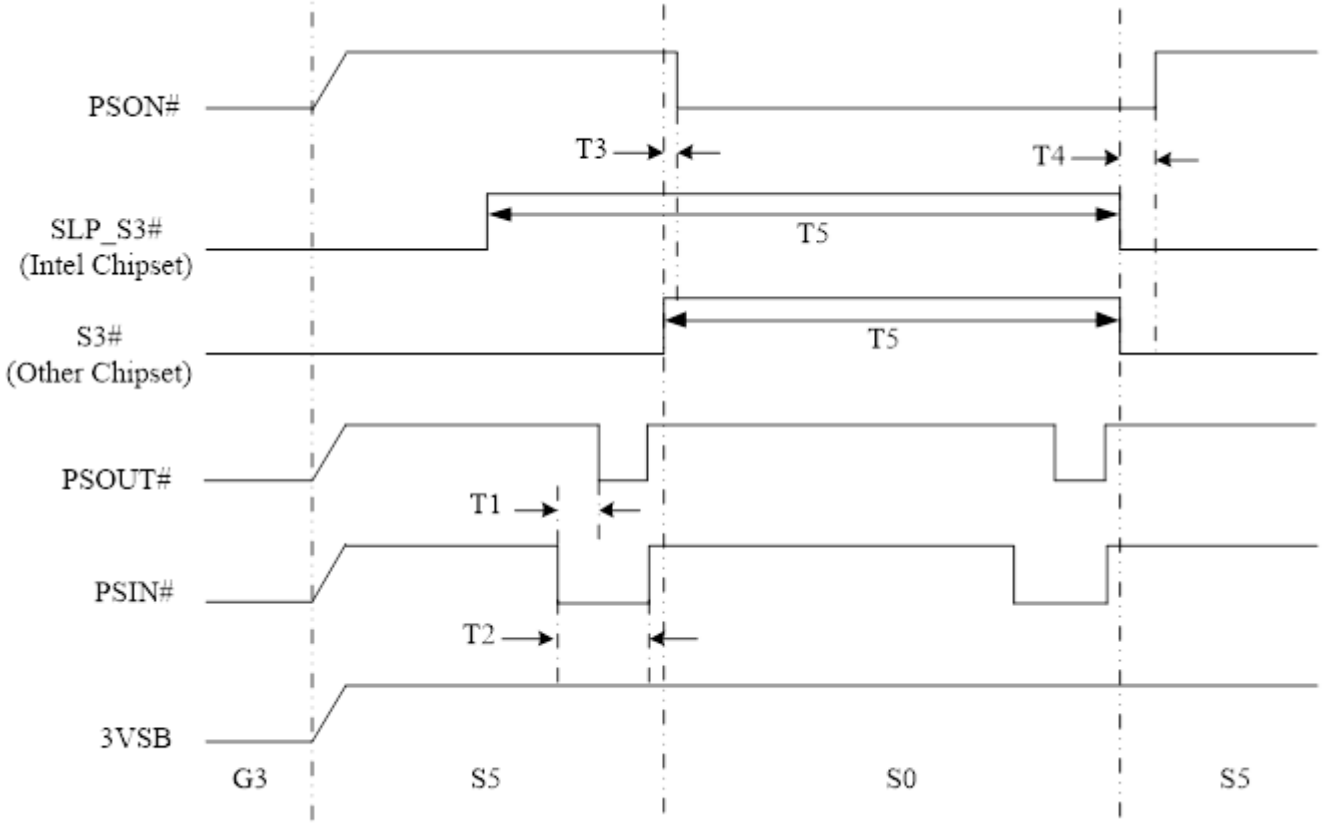
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}			0.8	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	2.0			V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{sp318} – 3.3V/1.8V Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}			0.8	V	
Input High Threshold Voltage	V_{t+}	1.1			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tp318} – 3.3V/1.8V input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{gp5} – 5V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
In_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD_8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O_{12} – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24} – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O_{48} – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD_{48} – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275*V_{tt}		0.5*V_{tt}	V	
Input High Voltage	V_{IH}	0.55*V_{tt}		0.725*V_{tt}	V	
Output Low Voltage	V_{OL}			0.25*V_{tt}	V	
Output High Voltage	V_{OH}	0.75*V_{tt}			V	
Hysterisis	V_{Hys}	0.1*V_{tt}			V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
O12cu – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD12cu – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA
OX8 – Output pin with 8mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA, LPC_ESPI_VDD=3.3V
Output High Voltage	VOH	1.31			V	IOH = -8 mA, LPC_ESPI_VDD=1.8V
OD8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
ODX8 – Output pin with 8mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA

25. AC CHARACTERISTICS

25.1 Power On / Off Timing

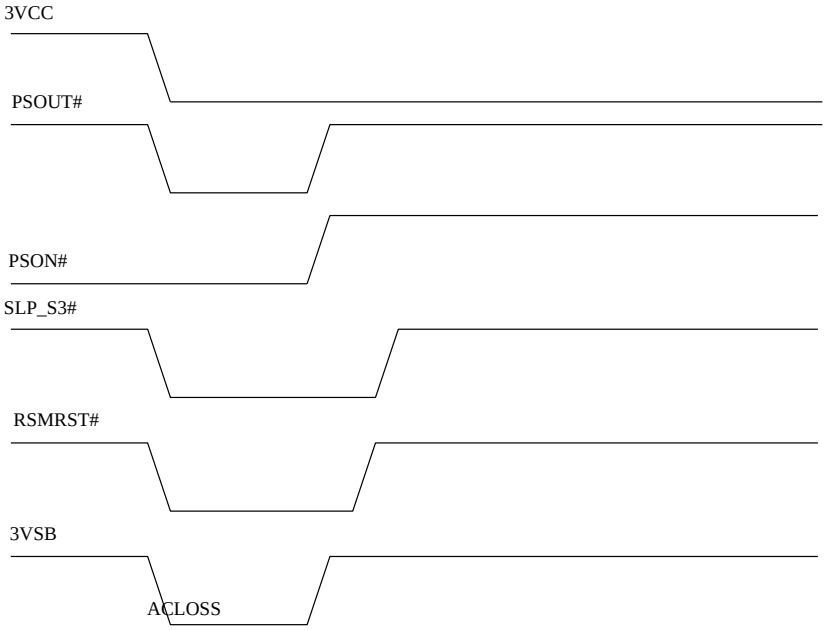


	T1	T2	T3	T4	T5
IDEAL TIMING	64ms	Over 64ms at least	< 10ns	32ms	Over 32ms at least

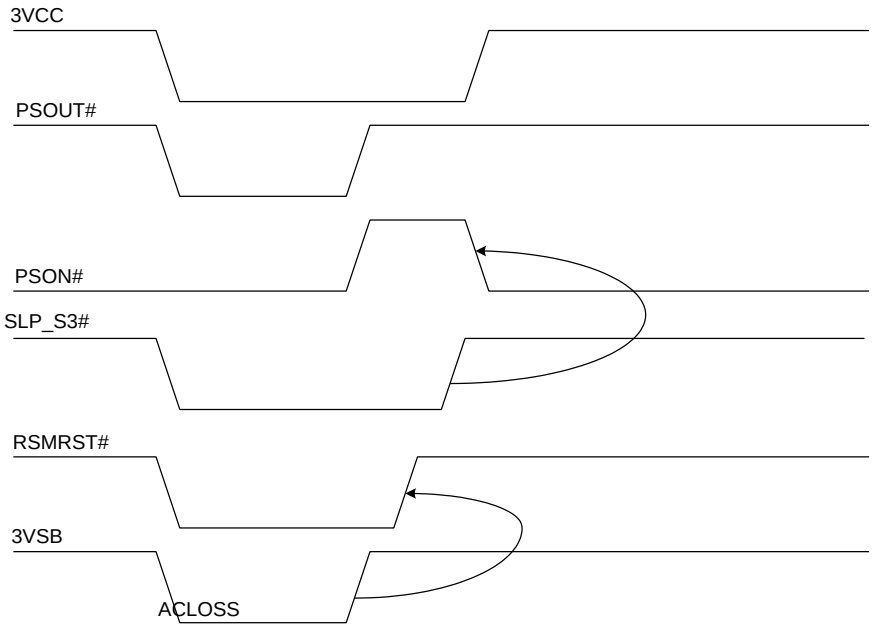
25.2 AC Power Failure Resume Timing

i. Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



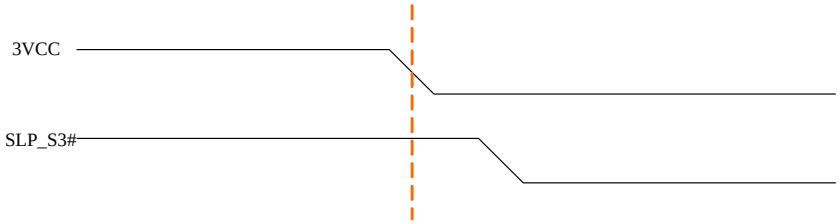
ii. Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

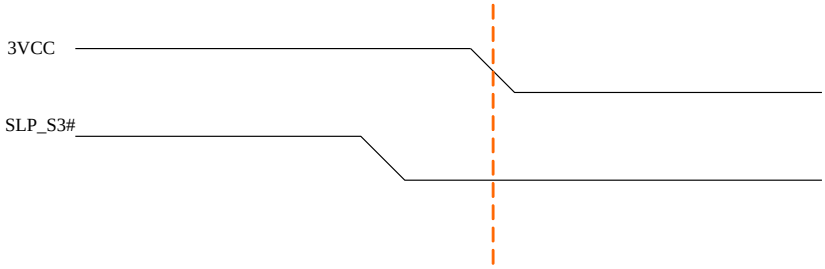
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



SLP_S3# was implemented 30mS de-bounce internally, so the interval between VCC and SLP_S3# must be over 30mS.

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6122D / NCT6126D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6-5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

BIT	READ/WRITE	DESCRIPTION
6-5	R / W	Power-loss control bits => (VBAT) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the resuming state before power loss.(refer to Logical Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

25.3 LPC Timing

PCI_CLK AC Specification					
Symbol	**Parameter**	**MIN**	**Typical**	**MAX**	**Units**
T_{CYC}	PCI_CLK cycle	30		42	ns
T_{per}	PCI_CLK period	35	50	65	%

LPC AC Specification (24MHz / 3.3V)					
Symbol	**Parameter**	**MIN**	**Typical**	**MAX**	**Units**
T_{CO}	Tx Rising Clock to Data Output Delay	3.3		7.8	ns
T_{SU}	Rx Data Setup Time to CLK Rising Edge	10.4			ns
T_{HD}	Rx Data Hold Time to CLK Rising Edge	0			ns
T_R	Input Rise Time (0.8V to 2.0V)			8.4	ns
T_F	Input Fall Time (2.0V to 0.8V)			8.4	ns

LPC AC Specification (33MHz / 3.3V)					
Symbol	**Parameter**	**MIN**	**Typical**	**MAX**	**Units**
T_{CO}	Tx Rising Clock to Data Output Delay	3.3		7.8	ns
T_{SU}	Rx Data Setup Time to CLK Rising Edge	8			ns
T_{HD}	Rx Data Hold Time to CLK Rising Edge	0			ns
T_R	Input Rise Time(0.8V to 2.0V)			6	ns
T_F	Input Fall Time(2.0V to 0.8V)			6	ns

25.4 eSPI Interface Timing

The eSPI interface meets the eSPI specification for 33 MHz.

Symbol	Figure	Description	Conditions		Min	Typ	Max	Units
Clock (Input) Requirements								
t_{CK}	25-4-1	ESPI_CLK Cycle Time	From RE to RE		30[1]			ns
t_{CKH}	25-4-1	ESPI_CLK High Time	From V_{IH} to V_{IH}, at t_{CK} = 30 ns		0.4 * t_{CK}[2]			–
t_{CKL}	25-4-1	ESPI_CLK Low Time	From V_{IL} to V_{IL}, at t_{CK} = 30 ns		0.4 * t_{CK}[2]			–
Signal Timing								
t_{DVCH}	25-4-2	ESPI_IO[3:0] Input Setup Time	Before RE of ESPI_CLK		7 [2]			ns
t_{CHDX}	25-4-2	ESPI_IO[3:0] Input Hold Time	After RE of ESPI_CLK		7 [2]			ns
t_{CLQV}	25-4-2, 25-4-3	ESPI_IO[3:0] Output Valid Time	After FE of ESPI_CLK	C_L = 20 pF			9	ns
t_{CLQX}	25-4-2	ESPI_IO[3:0] Output Hold Time	After FE of ESPI_CLK	C_L = 20 pF	0[3]			ns
t_{SHQZ}	25-4-3	ESPI_IO[3:0] Output Disable Time after ESPI_CS#	After RE of ESPI_CS#	C_L = 20 pF			9[4]	ns
t_{CLQZ}	25-4-2	ESPI_IO[3:0] Output Disable Time after ESPI_CLK	After FE of ESPI_CLK	C_L = 20 pF			9[4]	ns
t_{SLCH}	25-4-3	ESPI_CS# Input Setup Time	Before RE of ESPI_CLK		1.5 * t_{CK}[5]			–
t_{CLSH}	25-4-3	ESPI_CS# Input Hold Time	After FE of ESPI_CLK		1 * t_{CK}[6]			–
t_{SHSL}	25-4-3	ESPI_CS# Deassertion Time	From RE to FE of ESPI_CS#		1 * t_{CK}[6]			–
t_{SLAZ}	25-4-3	eSPI_IO[1] / ESPI_ALERT# Output Disable Time	After FE of ESPI_CS#				9	ns
t_{SHAA}	25-4-3	eSPI_IO[1] / ESPI_ALERT# Output Enable Time	After RE of ESPI_CS#		9			ns
t_{INIT}		ESPI_RST# Deassertion Time	Before FE of ESPI_CS#		1[7]			µs

1. The maximum eSPI clock frequency is 66 MHz. Because the limitation for internal clock frequence, the NCT6126D's eSPI only support the eSPI_CLK 20~33MHz.
2. Not tested; guaranteed by characterization guardband.

3. Not fully tested; characterized only.
4. This parameter is 9 ns in eSPI Spec for 33 MHz eSPI_CLK frequency.
5. This parameter is 45 in eSPI Spec for 33 MHz eSPI_CLK frequency.
6. This parameter is 30 in eSPI Spec for 33 MHz eSPI_CLK frequency.
7. Not tested; based on design simulation.

[Device Specifications]

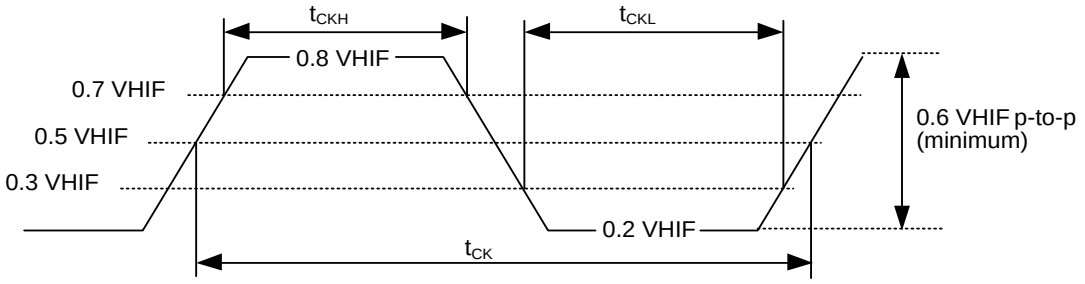


Figure 25-4-1 eSPI Clock Timing

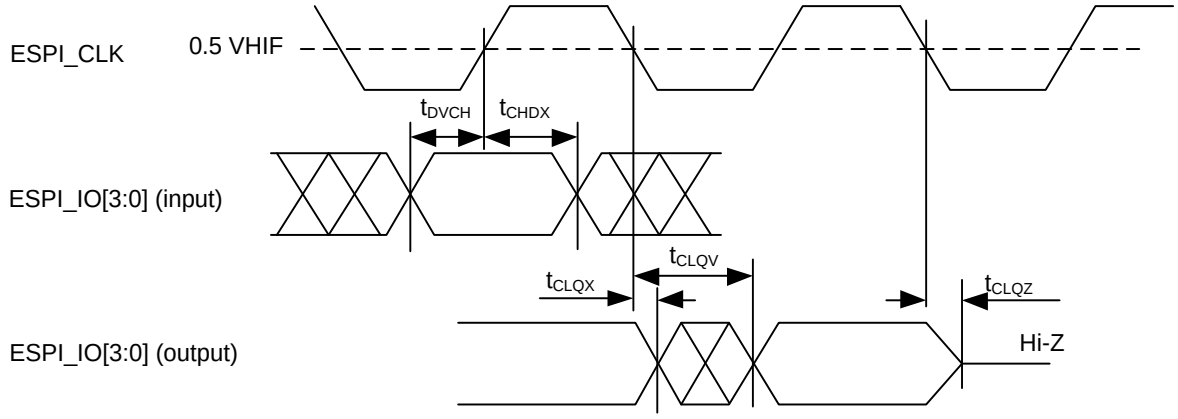


Figure 25-4-2 eSPI Data Signals Timing

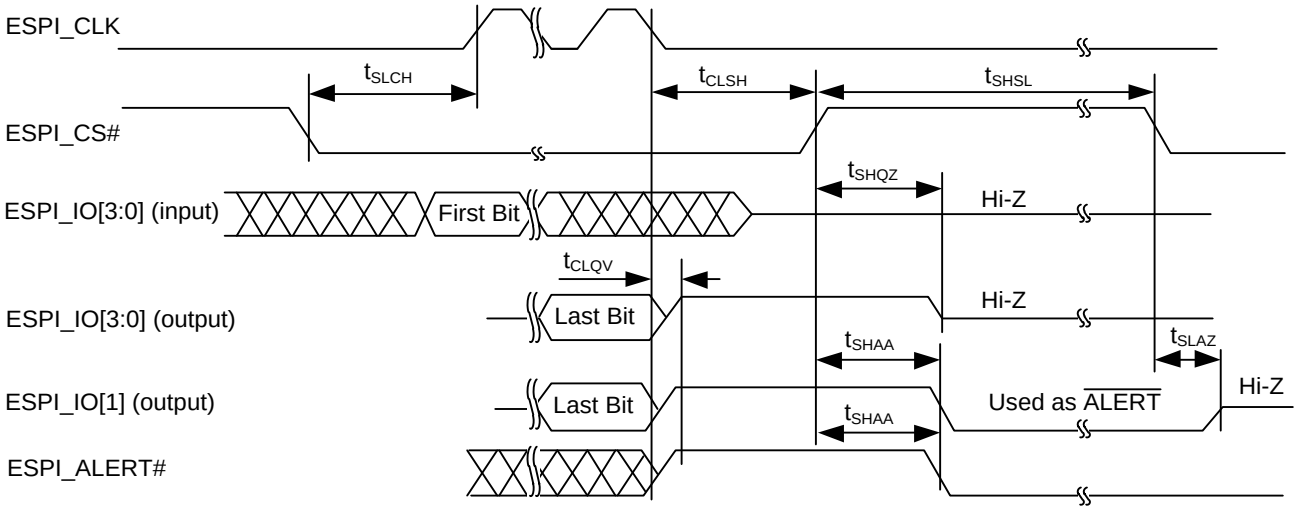
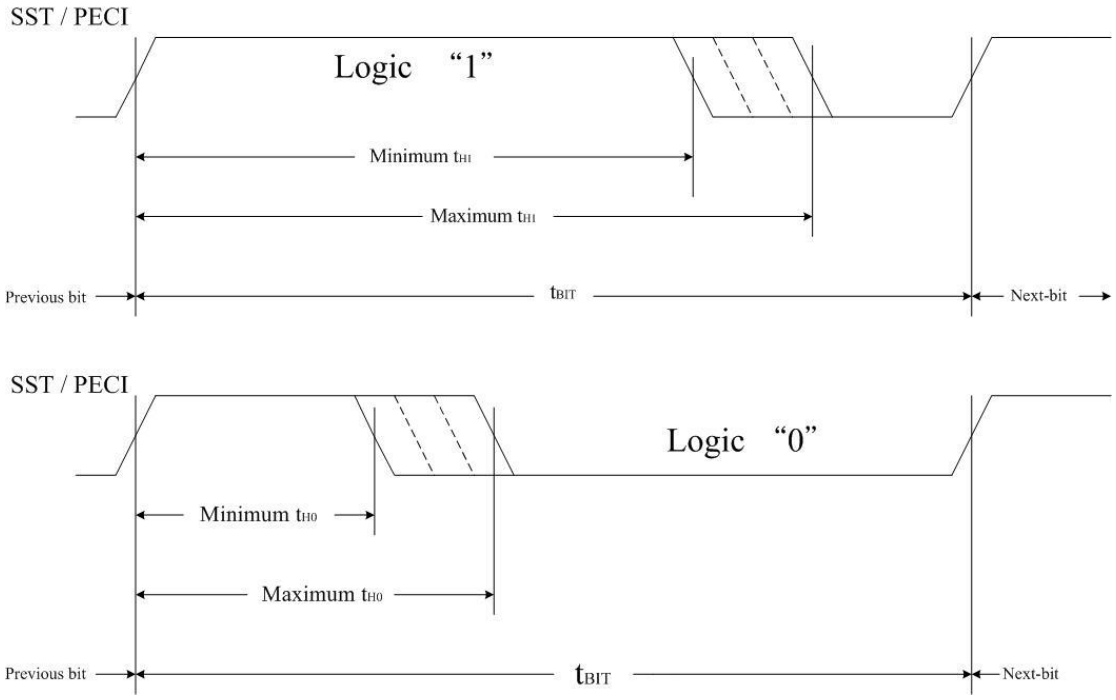


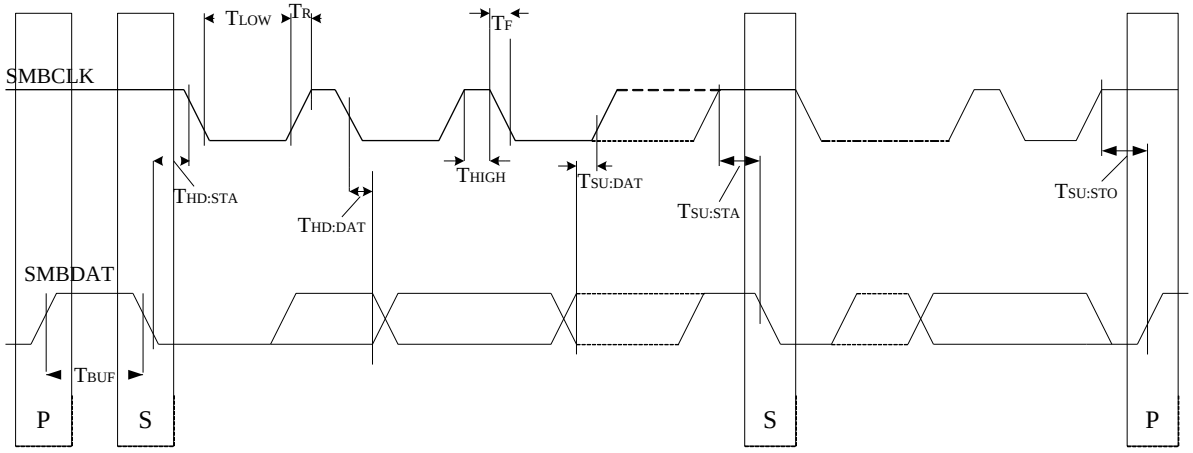
Figure 25-4-3 eSPI ESPI_CS# and ESPI_ALERT# Signals Timing

25.5 PECI Timing



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μS
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

25.6 SMBus Timing



PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Bus Free time between stop and start command	TBUF	4.7	-	-	µS
Hold time after start command	THD.STA	4	-	-	µS
Data hold time	THD.DAT	0	-	-	nS
Data setup time	TSU.DAT	250	-	-	nS
Stop condition setup time	TSU.STO	4			µS
Repeat start condition setup time	TSU.STA	4			µS

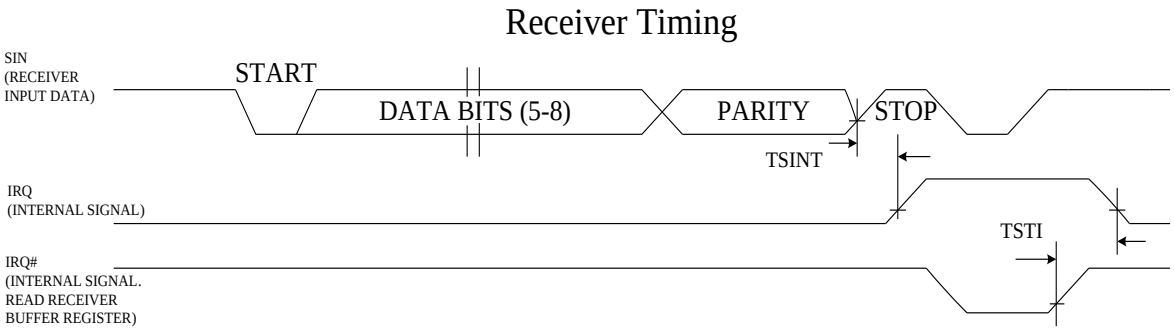
Note: TCLK = 100KHz

25.7 UART Parameters

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

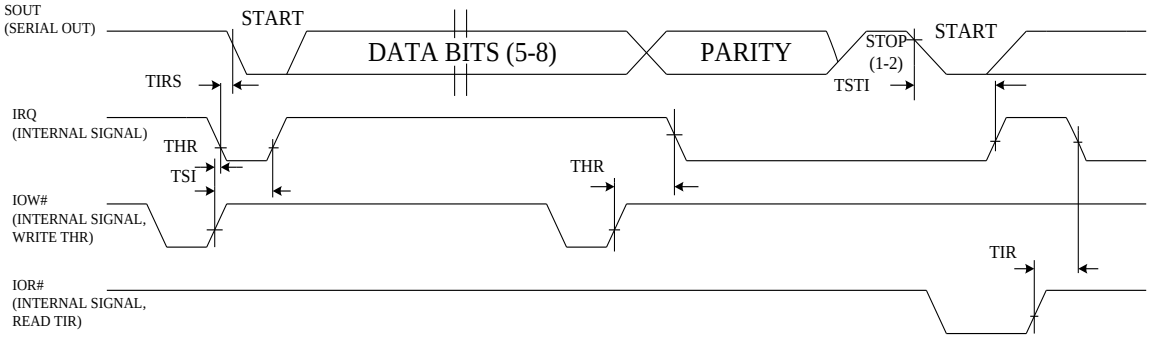
25.7.1 UART Receiver Timing

UART Receiver Timing



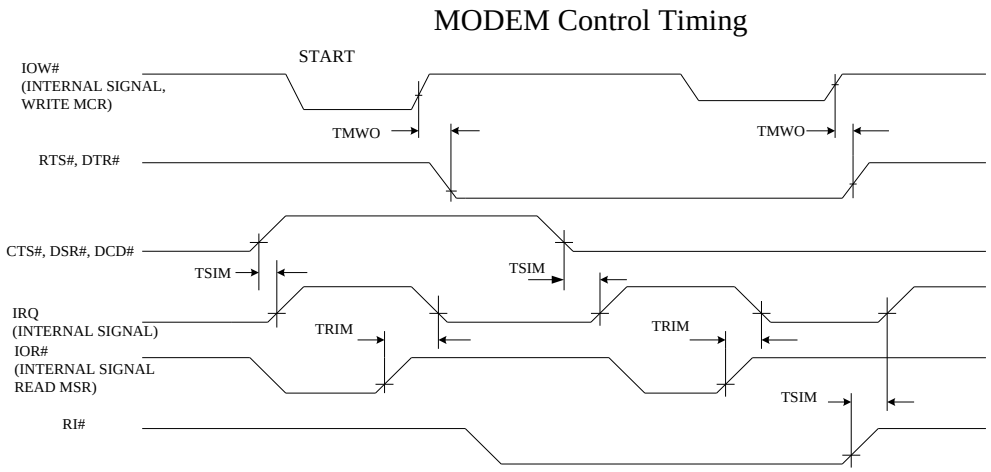
25.7.2 UART Transmitter Timing

UART Transmitter Timing



25.7.3 Modem Control Timing

Modem Control Timing

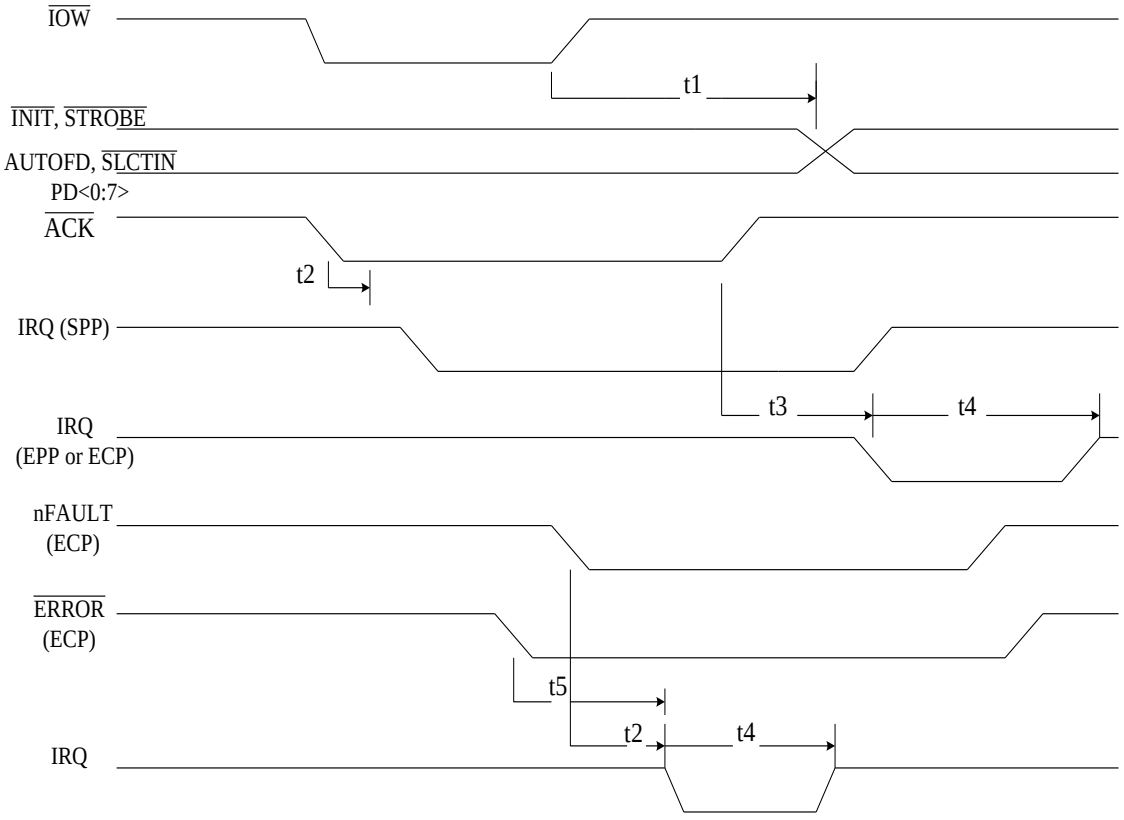


25.8 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

25.8.1 Parallel Port Timing

Parallel Port Timing

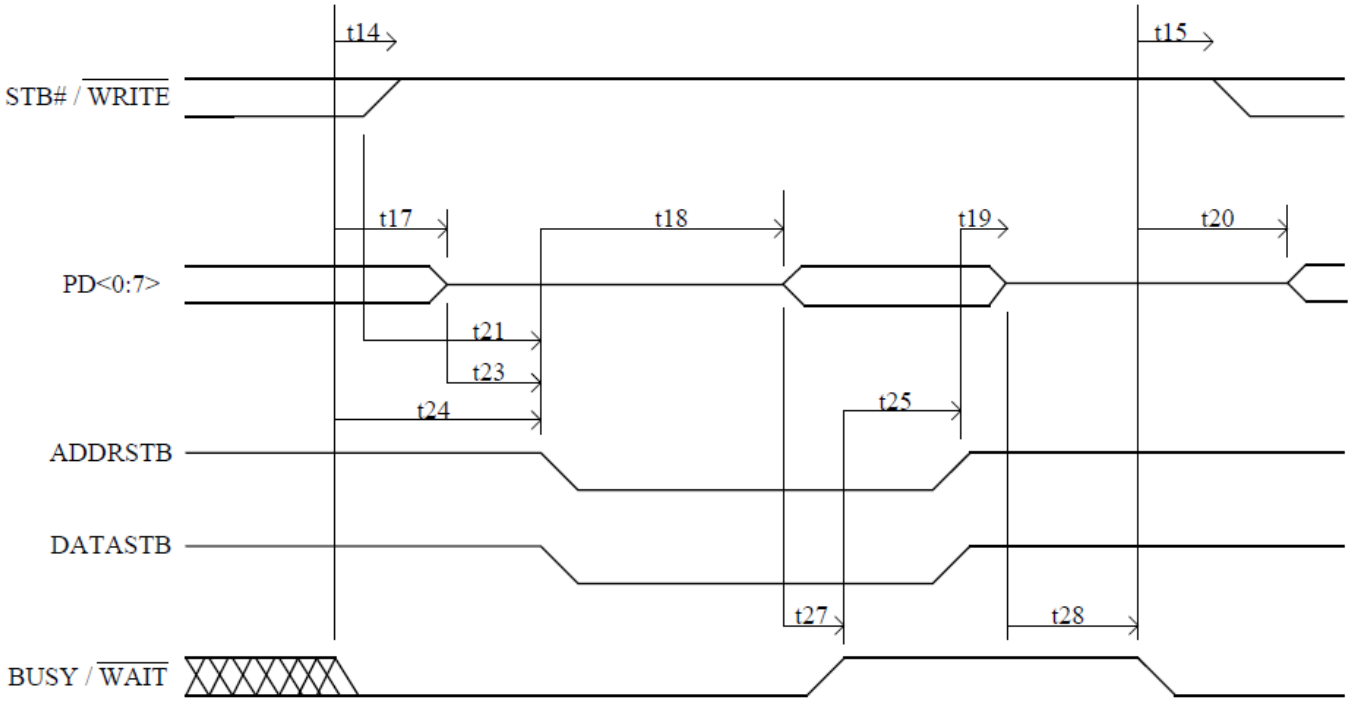


25.8.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS

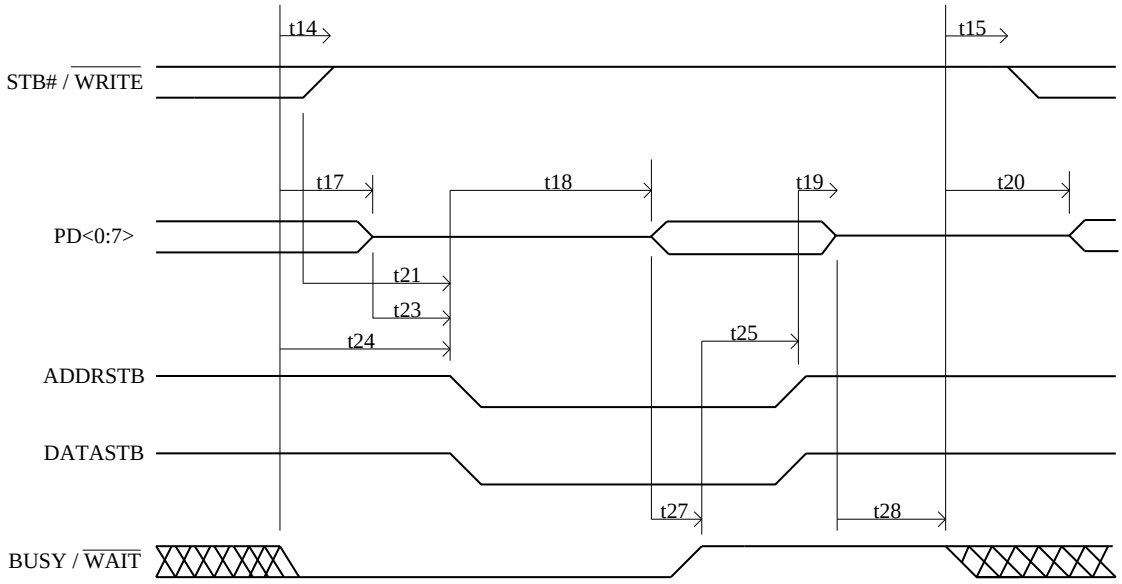
PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

25.8.3 EPP Data or Address Read Cycle (EPP Version 1.9)



25.8.4 EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



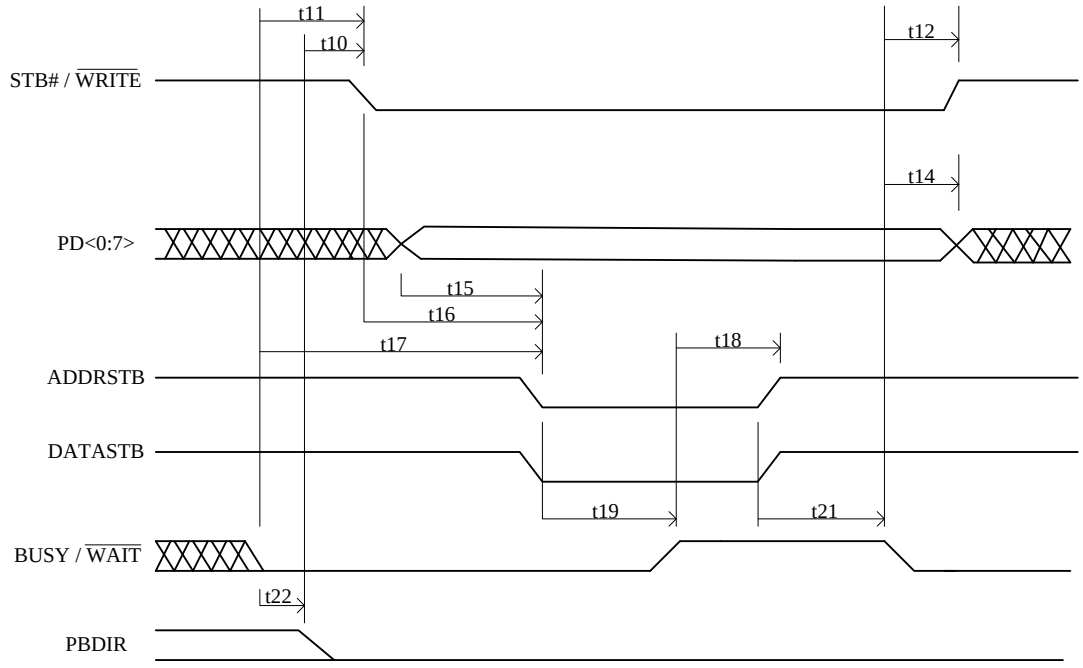
25.8.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS
$\overline{WRITE}$ to Command Asserted	t16	5	35	nS

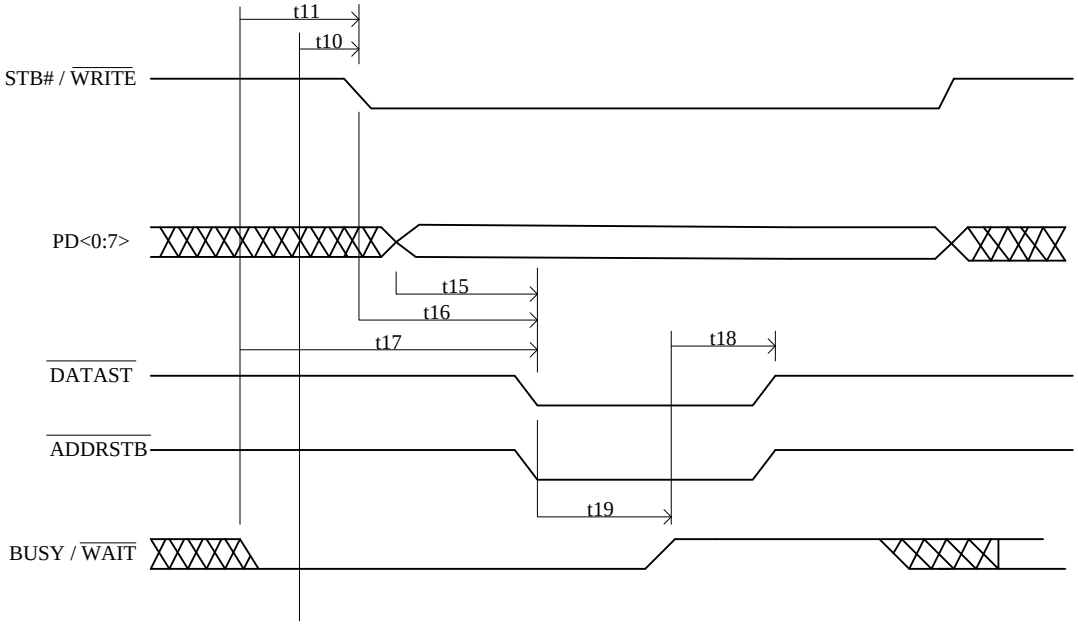
25.8.6 EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



25.8.7 EPP Data or Address Write Cycle (EPP Version 1.7)

EPP Data or Address Write Cycle (EPP Version 1.7)

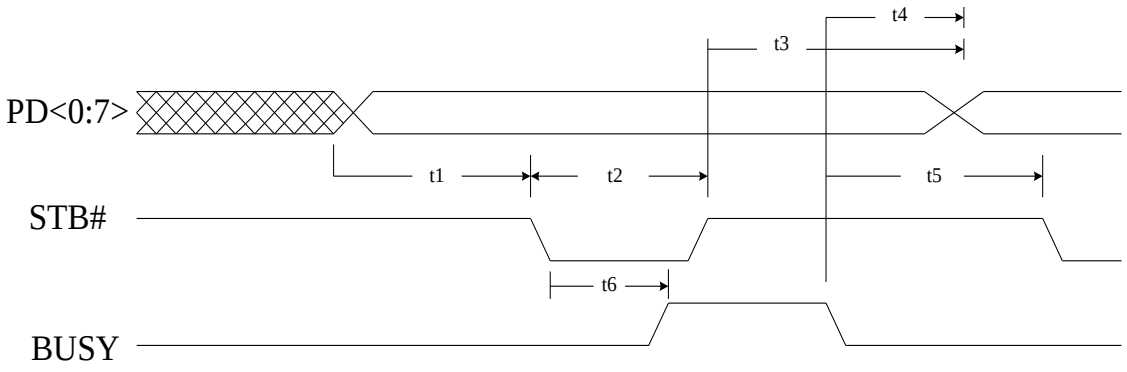


25.8.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

25.8.9 Parallel FIFO Timing

Parallel FIFO Timing

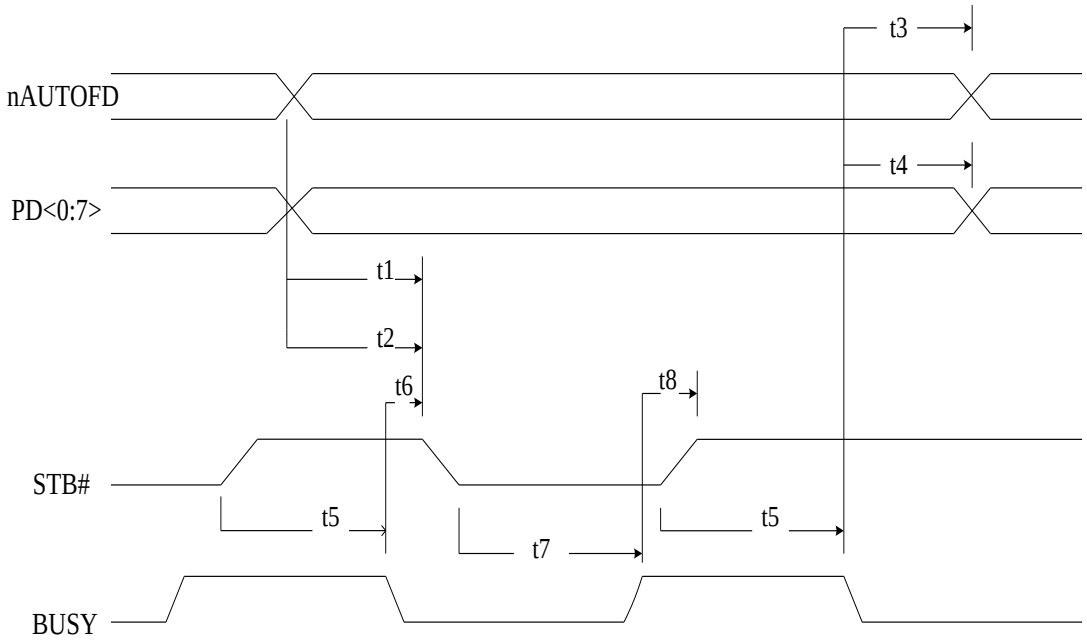


25.8.10 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

25.8.11 ECP Parallel Port Forward Timing

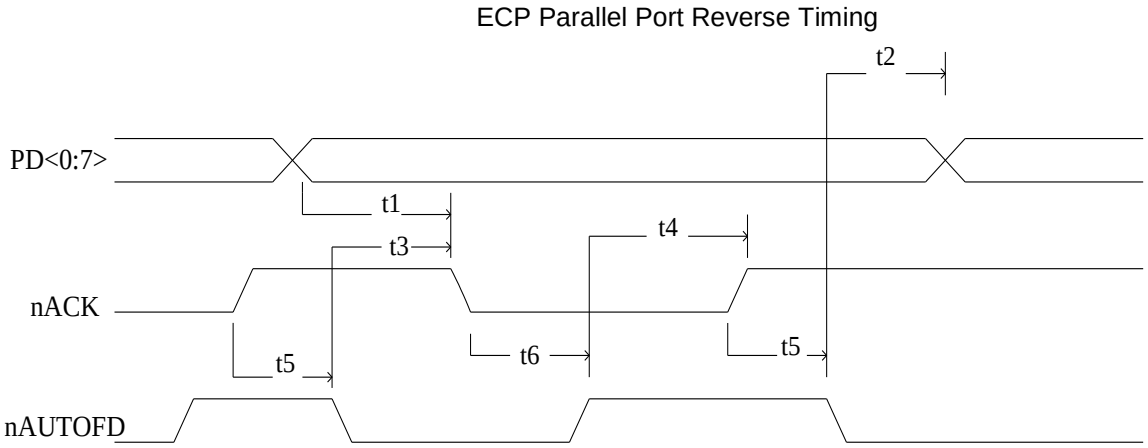
ECP Parallel Port Forward Timing



25.8.12 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

25.8.13 ECP Parallel Port Reverse Timing

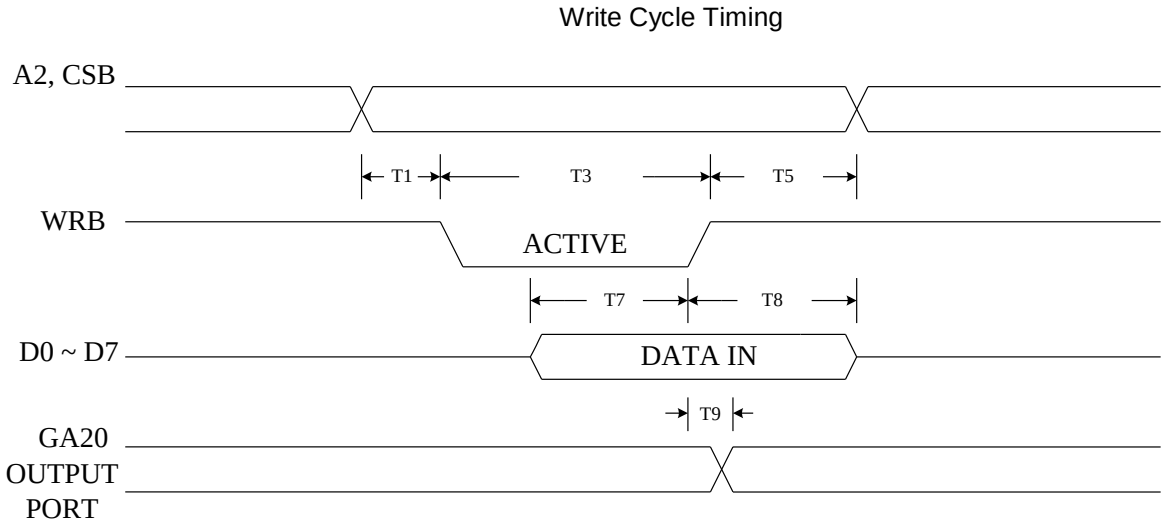


25.8.14 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 MHz)	63	167	nS
T22	Duration of CLK inactive	30	50	µS

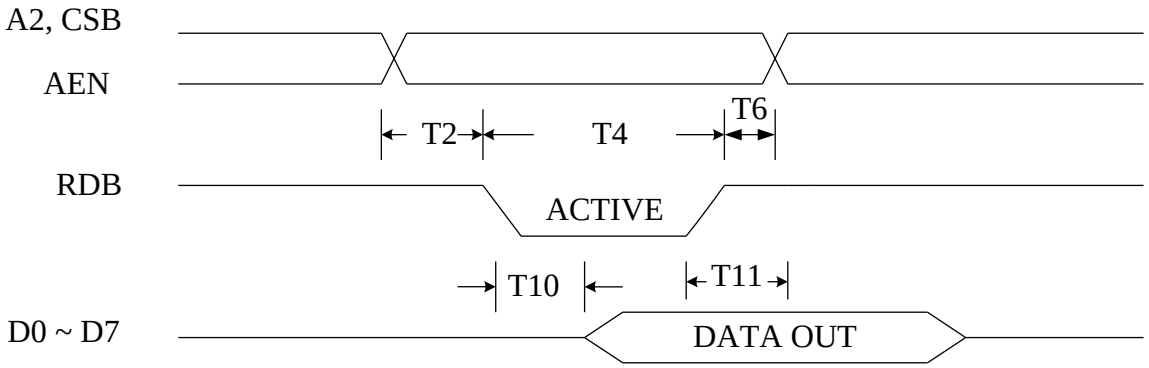
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the AUXiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

25.8.15 Writing Cycle Timing



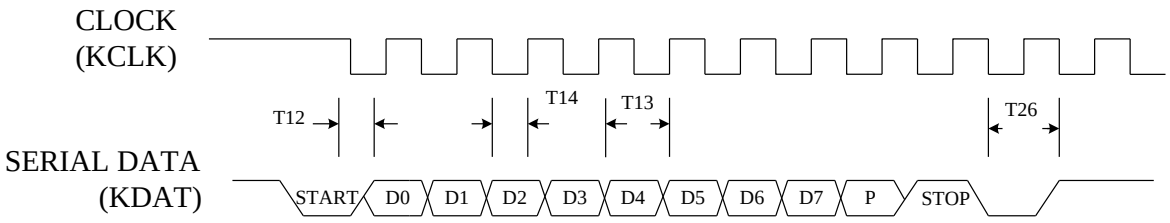
25.8.16 Read Cycle Timing

Read Cycle Timing



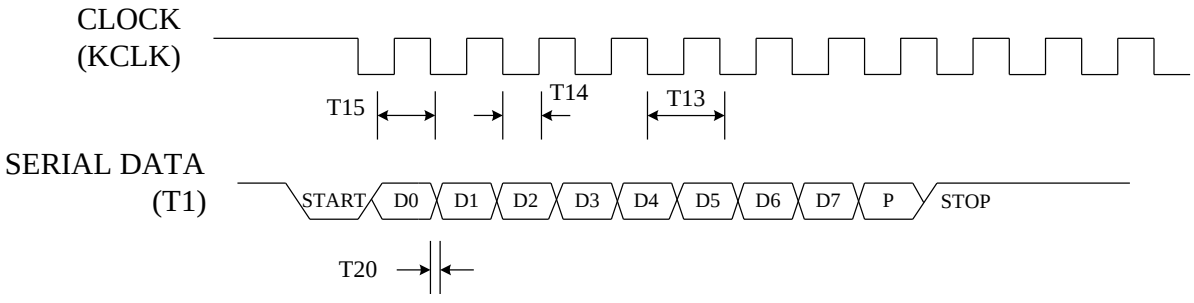
25.8.17 Send Data to K/B

Send Data to K/B



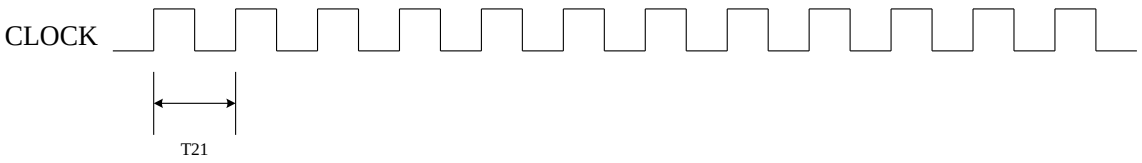
25.8.18 Receive Data from K/B

Receive Data from K/B



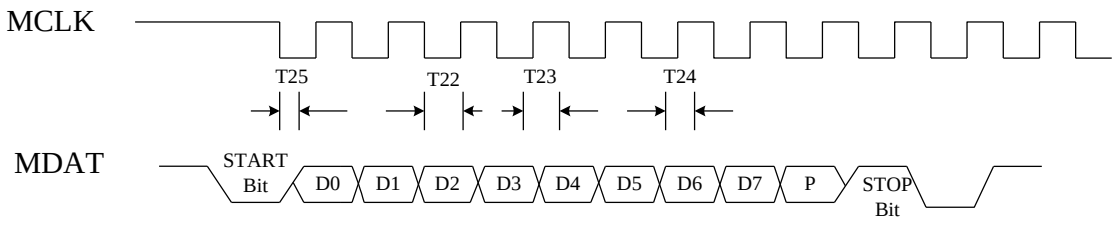
25.8.19 Input Clock

Input Clock



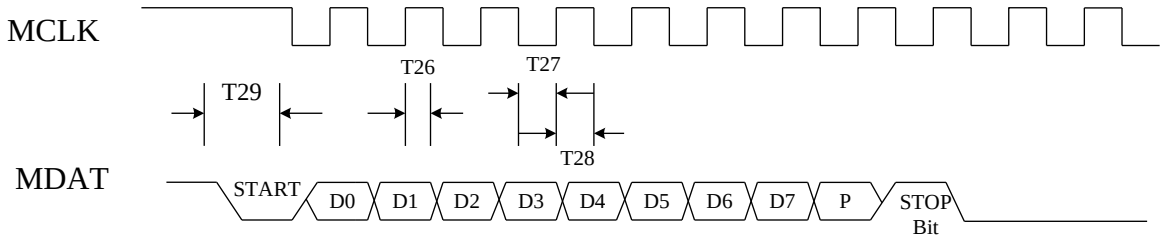
25.8.20 Send Data to Mouse

Send Data to Mouse



25.8.21 Receive Data from Mouse

Receive Data from Mouse



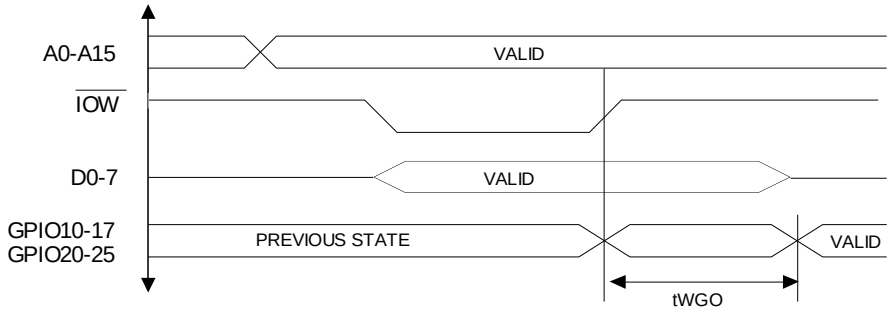
25.9 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300 (Note)	ns

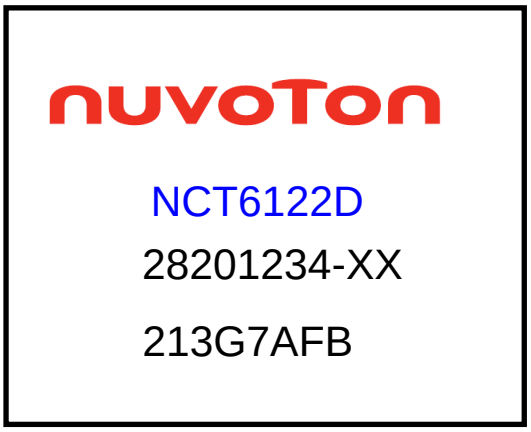
Note: Refer to Microprocessor Interface Timing for Read Timing.

25.9.1 GPIO Write Timing

GPIO Write Timing diagram



26. TOP MARKING SPECIFICATIONS



1st line: Nuvoton logo

2nd line: part number NCT6122D

3rd line: wafer production series lot number. It could be 8 characters, such as 28201234, or 11 characters, such as 28201234-XX.

4th line: tracking code 213G7AFB

213: packages made in 2022, week 13

G: assembly house ID; G means GR, A means ASE, etc

7: code version; 7 means code 007

A: IC revision; A means version A; B means version B, and C means version C

FB: Nuvoton internal use

1st line: Nuvoton logo

2nd line: part number NCT6126D

3rd line: wafer production series lot number. It could be 8 characters, such as 28201234, or 11 characters, such as 28201234-XX.

4th line: tracking code 213G7AFB

213: packages made in 2022, week 13

G: assembly house ID; G means GR, A means ASE, etc

7: code version; 7 means code 007

A: IC revision; A means version A; B means version B, and C means version C

FB: Nuvoton internal use

27. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6122D	128Pin LQFP (Green package)	**-40℃~+85℃**
NCT6126D	128Pin LQFP (Green package)	**-40℃~+85℃**

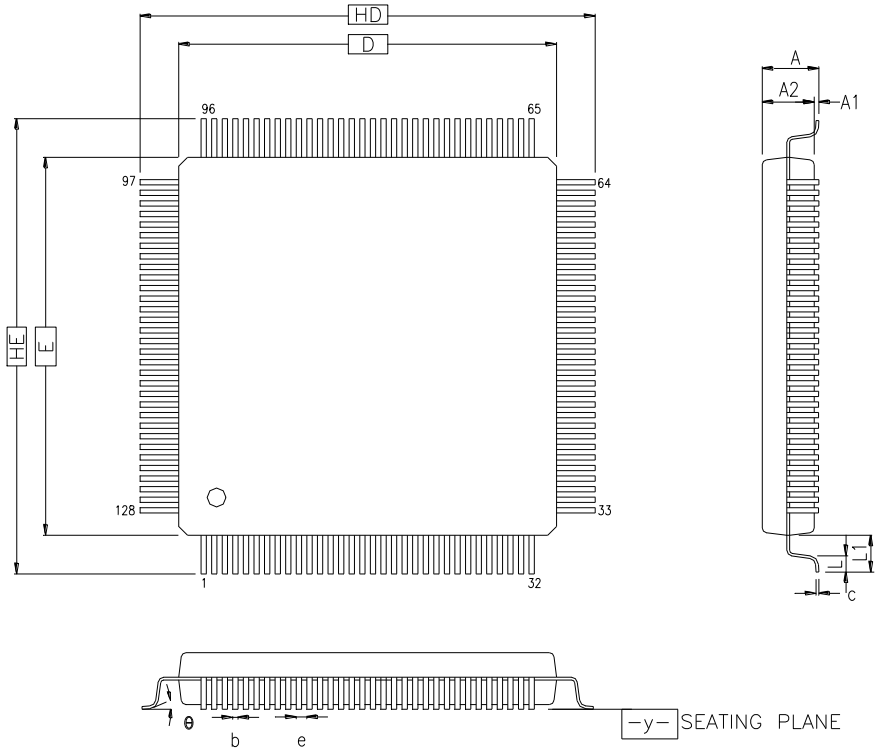
NCT6122D/NCT6126D Version Change Notice 1

Function		Description	
		A version	**B version**
1	Chip ID	D2A3/D283	D2A4/D284
2	S0_IDLE# pin type.	Push pull type output.	Open drain type output.
3	ASSC function in eSPI mode	SLP_S5# event is selected by Logical device E Index E6 Bit 4 (ESPI S5/S4 SEL).	SLP_S5# event is selected by Logical device 16 Index 30 Bit 6. (Source of internal SLP_S5# logic)
4	PSON#	When PLAT_SEL =1 (ATOM platform), PSON# sometimes gets a low pulse glitch in the first time of battery power up.	Fixed.
5	UART	When LPC clock > 24MHz or eSPI clock > 33MHz, the UART error status may not be read clear.	Fixed.
6	Extended Function Data Register	When the interface is eSPI, user must read the EFDR at the end programming of SIO.	Fixed.

NCT6122D / NCT6126D Version Change Notices List

	Date	Version	Revision	Remark
1	11/30/2021	VCN1	0.1	Version Change Notice for A version to B version.
2	4/20/2022	VCN1	0.2	Updated the typo and item.4 description.

28. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin LQFP (14x14x1.4mm)

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	11/14/2018	N.A.	Draft datasheet
0.6	05/13/2019	N.A.	Add part number NCT6122D
0.7	07/10/2019	33 35 152.153.208.209 450 51 25, 28, 29 300~439 18 46	1. Add RSMRST# monitor 3VSB/VHIF timing 2. Modify LATCH_BKFD_CUT description. 3. Modify Ch. 9 hardware monitor register 4. Add LPC timing 5. Added the description for exit the Extended Function Mode with 0xBB when entry key is 0x88. 6. Modify GPIO description. 7. Modify register description 8. Modify the description for PAD_CAP. (External Filter Capacitor 1uF) 9. Modify 6.9 Thermtrip# function description.
0.8	08/12/2019	207, 208	1. Corret the information in bank 0 Index 46. 2. Modify the entry key strapping descrition. 3. Update Chapter 9.353 BEEP Control Register1 – Index C0h (Bank 3) 4. Modify the thermtrip imformation. 5. Modify the 3VSBSW in the GLUE LOGIC.
0.9	02/21/2020	262,31,39,47,438	1. Correct the PME# imformation. 2. Delete the SMART FAN™ IV has stepping information. 3. Modify PLAT_SEL condition. 4. Correct the LPC_ESPI_SEL pin from 16 to 54. 5. Add Chapter 6.6 AT / ATX mode 6. Modify the thermtrip function diagram 7. Modify the description of LD15, CR[E9] bit 0 (SUSLED in S5 stste)

1.0	04/10/2020	15 312 219 225	1. Add pin 107 THERMTRIP# description 2. Motify the pin 19 function. 3. Modify CR 1Dh default value 4. Modify the registors of the FAN Enable Critical Duty. 5. Correct the description of the Set Silence Enable register in UART function. 6. Add BAUD RATE colum from pre-divider = 1.625 7. Add pin 23 ESPI_ALERT# description 8. Modify chip ID. 9. Correct the GPIO_PORT80 strapping power well. 10. Remove the LDX CR F0 bit 6 description.
1.1	07/21/2020	31 312	0 Modify pin 107 PLAT_SEL strapping condition and description 1 Modify the SOUTC_P80_SEL to CR1D[4]
1.2	09/16/2020	2 381 319-320	1. Add feature about Oscillator free and remove Clock input timing, 2. Revise the default vaule of LDA CRE5 bit 1. 3. Revise CR2B and CR2C UART pins function selection.
1.3	11/16/2020	19 32 48 61 16	1. Modify Pin31 PLED buffer type 2. Add SIO needs one more read EFDR step at the end programming when the interface is eSPI 3. Modify Thermtrip# function diagram (PLAT_SEL=1 case). 4. Modify 8.6.2 Voltage Data Format 5. Add AUXFAN2 pin description
1.4	12/18/2020	398 6,7	1. Add the descrption at LDE, CRF7 bit[4:2] for eSPI frequency selection. 2. Correct NCT6122D / NCT6126D pin layout on pin 27
1.5	06/02/2021	435 9 397 350 312	1. Modify DC CHARACTERISTICS. 2. Added ESPI_ALERT_HNSK into pin description. 3. Corrected the pin 19 function selection. 4. Removed clock source is 2 MHz of UART / IR. 5. Corrected the typo.
1.6	07/12/2021	60,82,87	1. Update Figure 8-6 in Chapter 8.6 2. Modify SMI# / OVT# description. 3. Remove the LD2, LD3, LD10-14 CR F0 bit 5 description.

1.7	11/12/2021	53 61 81	1. Modify 7.15 Software Programming Example. 2. Modify the VTT reading formula 3. Add 8.10.5 Max Duty Compare Source
1.8	02/11/2022	394 381 395, 434	1. Modify Logical Device E, CR E6h, bit4 description 2. Add PWROK Push-Pull / OD type selection bit at Logical Device A, CR FFh, bit4 3. Add LD16, CR30h bit6 for the internal SLP_S5# selection
1.9	03/22/2022	463	Add VCN in Chapter 27.ORDERING INFORMATION
2.0	04/29/2022	13~17, 21, 22, 25, 26, 30, 31, 275~279, 462	1. Modify power well to VSB at pin 1-11, 13-18, 69 and 125-128 in Chapter 5. Pin Description and Table 18-2 GPIO Group Programming Table 2. Update Chapter 26. TOP MARKING SPECIFICATIONS
2.1	08/12/2022	58 281 433 463 303	1. Modify Logical Device 15, CR E9h, bit0 description 2. Modify VCN in Chapter 27. ORDERING INFORMATION 3. Fixed the typo of Table 18-4. 4. Update Exit Deeper Sleeping State figure in Chapter 6.8.3. 5. Add Logical Device B, CR 64h and CR65h description 6. Modify Figure 22-1. 7. Add Index 47h-49h Bank 0 registers. 8. Update description of Chapter 8.4 ESPI interface
2.2	04/14/2023	9, 30 438 73, 144, 149, 155, 175, 181	1. Remove the description of multiple eSPI slave system 2. Modify pin19 ESPI_ALERT_HNSK, pin 80 ESPI_OWN_SEL description 3. Update 24.2 DC CHARACTERISTICS 4. Modify Speed Cruise™ Mode tolerance registers.
2.3	06/12/2023	447,448	1. Add 25.4 eSPI interface timing
2.4	09/12/2023	45, 46, 47 49 113, 117 451	1. Modify the figures and update description of section 6.8.2 and 6.8.3 2. Modify the description of section 6.10 3. Modify the description of Bank 0, index 76h and index 7Dh. 4. Update 25.6 SMBUS timing

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.