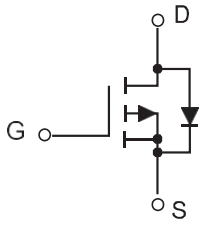
-40V/-40A P-Channel Enhancement Mode Power MOSFET

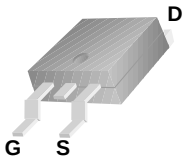
Description

The PTD40P40 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



General Features

- V_{DS} =-40V,I_D =-40A
  $R_{DS(ON)}$ < 13m Ω @ V_{GS}=-10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



TO-252

Application

- Battery and loading switching

Order Information

Product	Package	Marking	Packing
PTD40P40	TO-252	PTD40P40	2500PCS/REF

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous(T_C=25℃)	I_D (25℃)	-40	A
Pulsed Drain Current	I_{DM}	-160*	A
Maximum Power Dissipation	P_D	42.7	W
Derating factor		0.9	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	245	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55To +150	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.435	℃/W

* Drain current limited by maximum junction temperature

-40V/-40A P-Channel Enhancement Mode Power MOSFET

Electrical Characteristics (T_C=25℃unless otherwise noted)

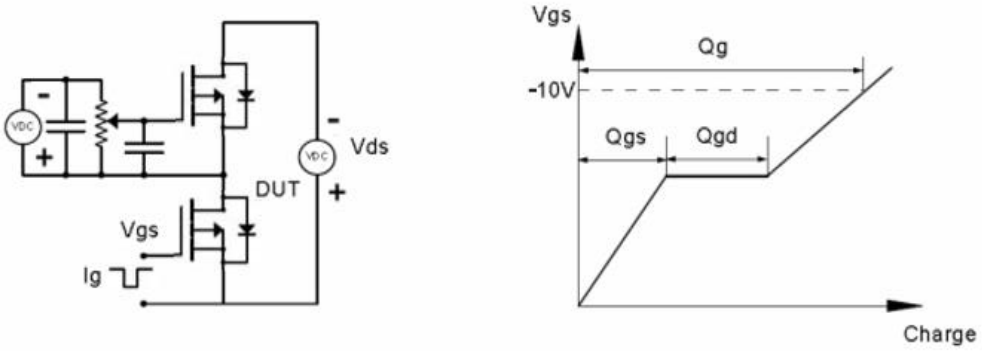
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-100	nA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.1	-1.6	-2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)1}$	V_{GS}=-10V, I_D=-12A	-	10.5	13	mΩ
Drain-Source On-State Resistance	$R_{DS(ON)2}$	V_{GS}=-4.5V, I_D=-10A	-	13.5	17.5	mΩ
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -20 A (Note 6)	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	3230	-	PF
Output Capacitance	C_{oss}		-	262	-	PF
Reverse Transfer Capacitance	C_{rss}		-	3.8	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -20 V, ID = -20 A, V_{GS} = -10 V, R_G = 2.5 Ω (Note 6, 7)	-	11.4	-	nS
Turn-on Rise Time	t_r		-	27.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	92.4	-	nS
Turn-Off Fall Time	t_f		-	20.6	-	nS
Total Gate Charge	Q_g	V_{DD} = -20 V, ID = -20 A, V_{GS} = -10 V (Note 6, 7)	-	67.4		nC
Gate-Source Charge	Q_{gs}		-	11.1		nC
Gate-Drain Charge	Q_{gd}		-	12.4		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-30A	-0.5		-1.2	V
Diode Forward Current (Note 2)	I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	-40	A
Reverse Recovery Time	t_{rr}	V_{GS}= 0 V, I_S = -20 A, di/dt=100A/μs	-	14.9		nS
Reverse Recovery Charge	Qrr		-	5.15		nC

Notes:

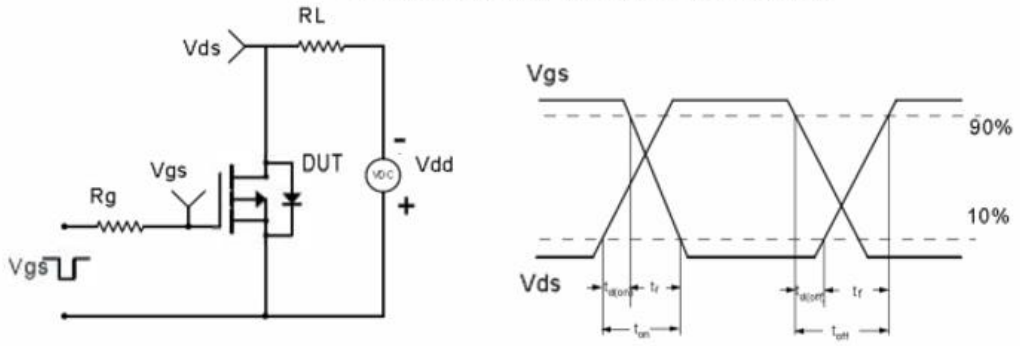
1. L = 0.5 mH, V_{DD} = -20V, R_G = 25 Ω, Starting T_j = 25°C.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-20V,V_G=-10V,L=1mH,Rg=25Ω,I_{AS}=33A
6. $_{SD}$ ≤ -40A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_j=25°C
7. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤2%

Test Circuit & Waveform

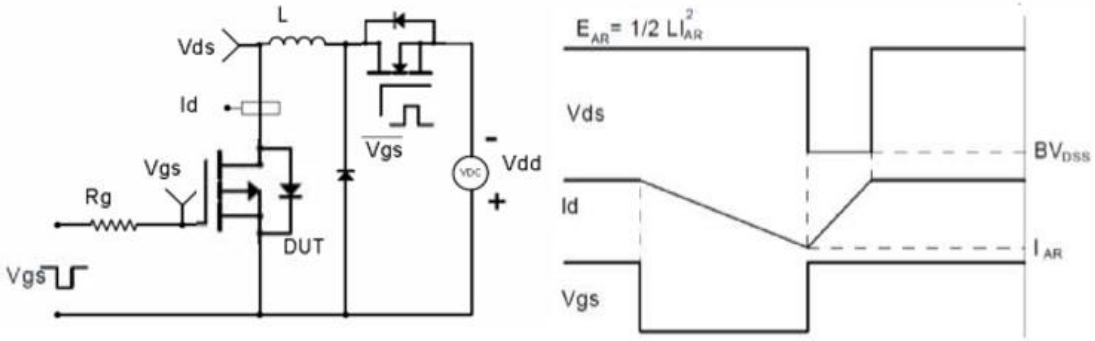
Gate Charge Test Circuit & Waveform



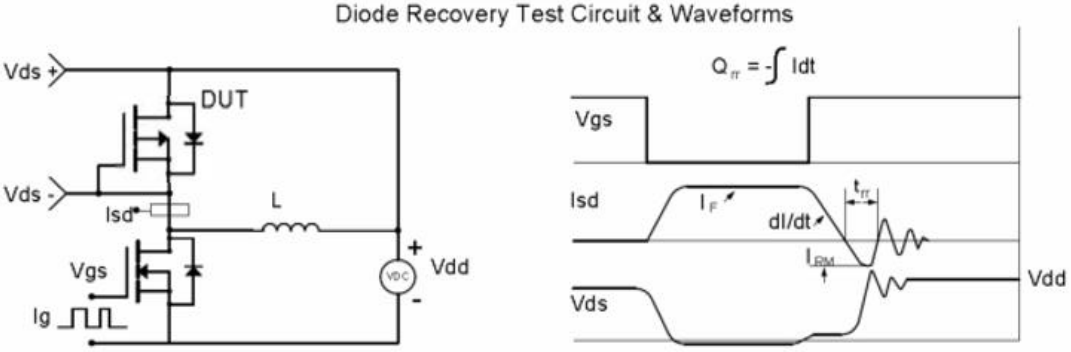
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



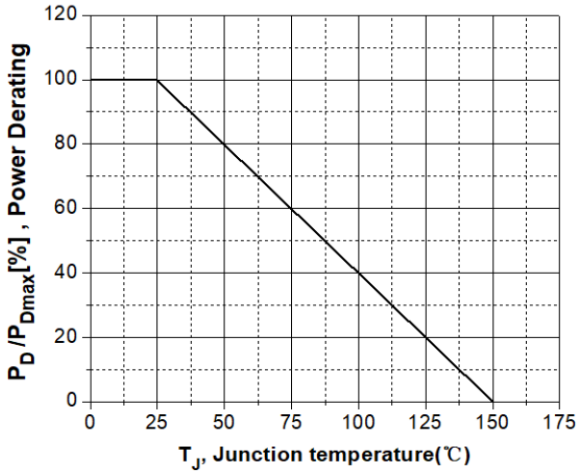


Fig1. Power Dissipation Derating Curve

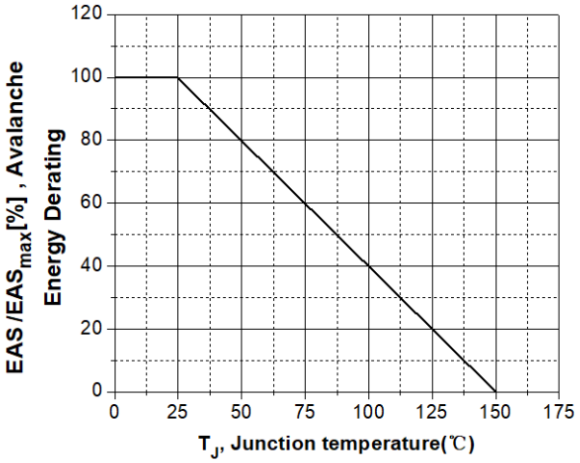


Fig2. Avalanche Energy Derating Curve vs. Junction Temperature

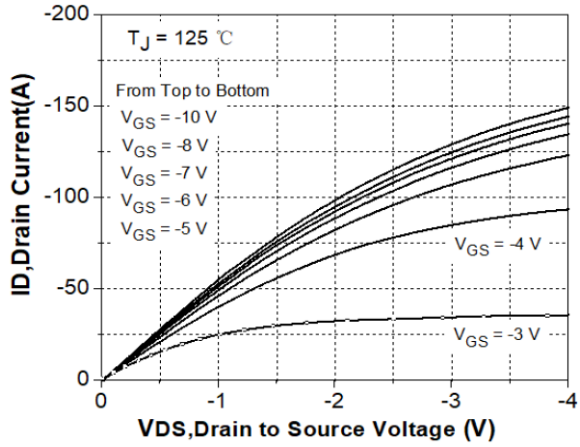


Fig3. Typical Output Characteristics@Tj= 125℃

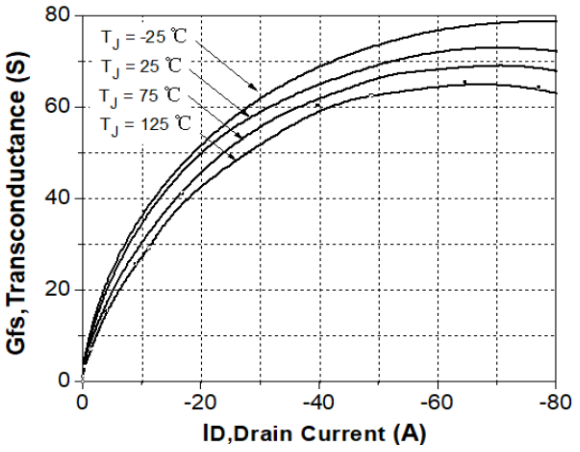


Fig4. Transconductance vs. Drain Current @Tj= -25/25/75/125℃

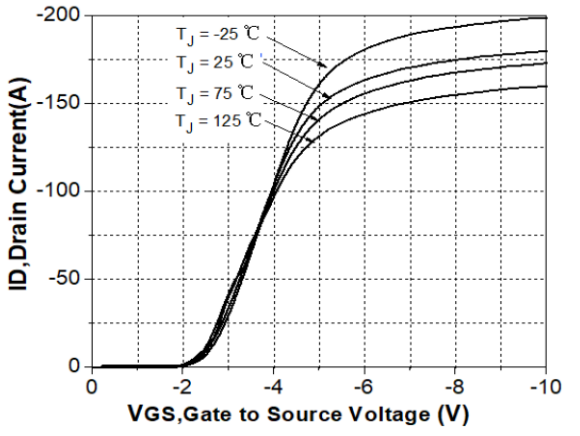


Fig5. Typical Transfer Characteristics @Tj= -25/25/75/125℃

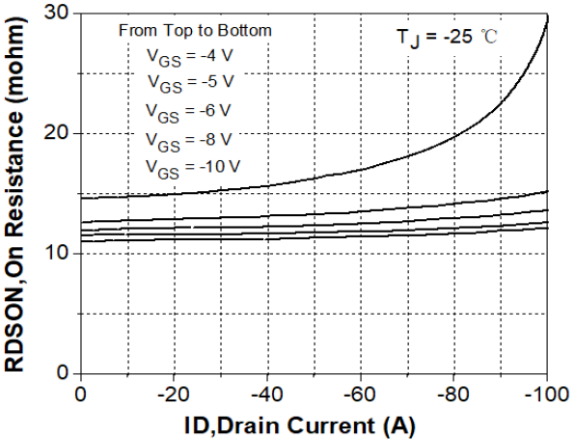


Fig6. Static Drain - Source On - State Resistance vs. Drain Current @Tj= -25℃

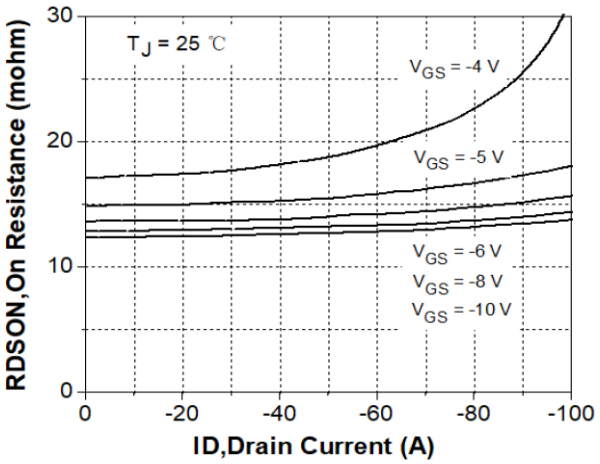


Fig7. Static Drain - Source On - State Resistance vs. Drain Current @Tj= 25℃

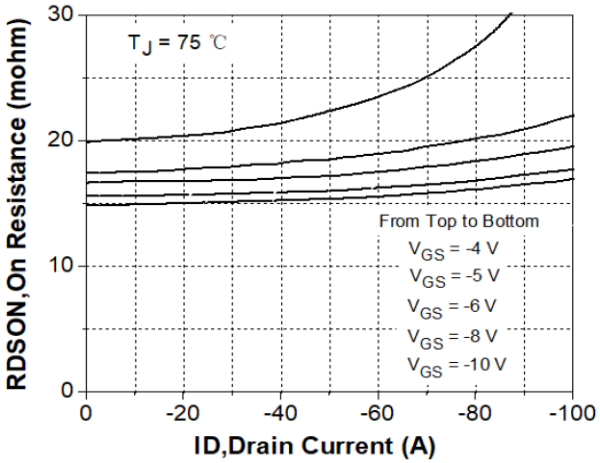


Fig8. Static Drain - Source On - State Resistance vs. Drain Current @Tj= 75℃

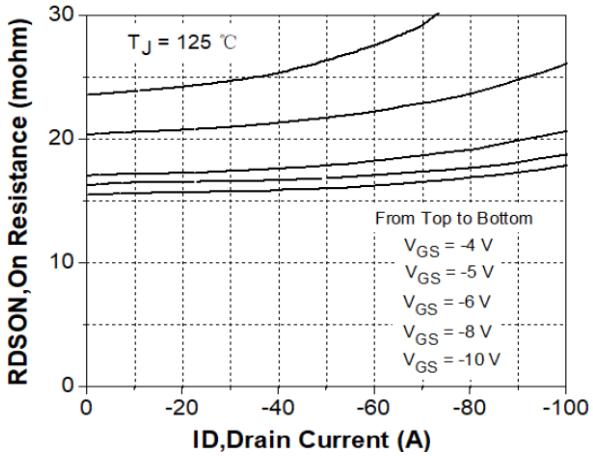


Fig9. Static Drain - Source On - State Resistance vs. Drain Current @Tj= 125℃

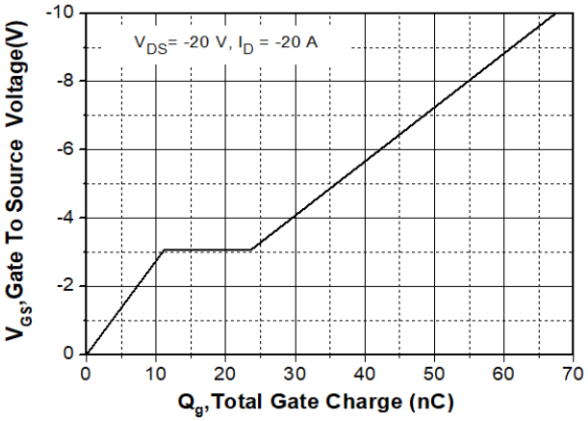


Fig10. Gate Charge Characteristics

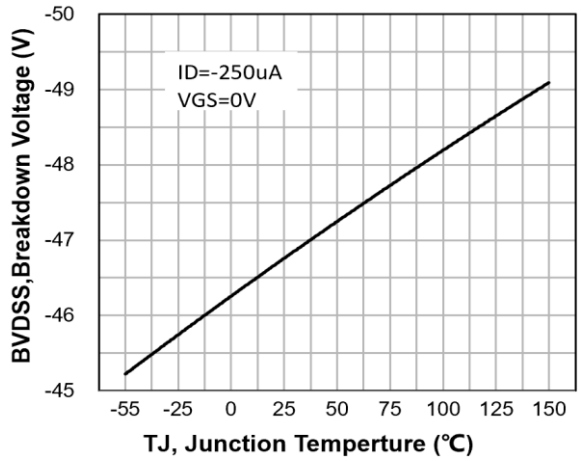


Fig11. Breakdown Voltage vs. Junction Temperature

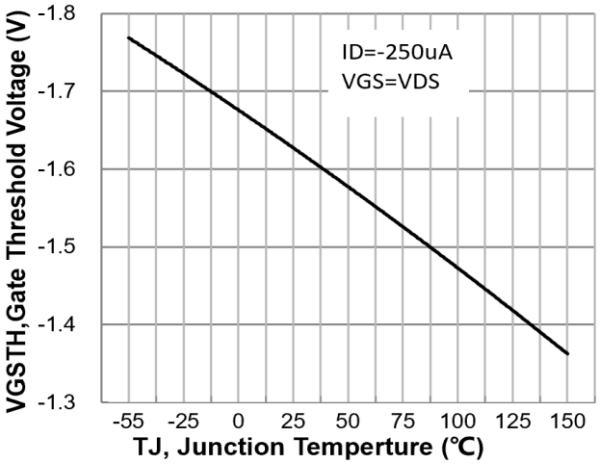


Fig12. Gate Threshold Voltage vs. Junction Temperature

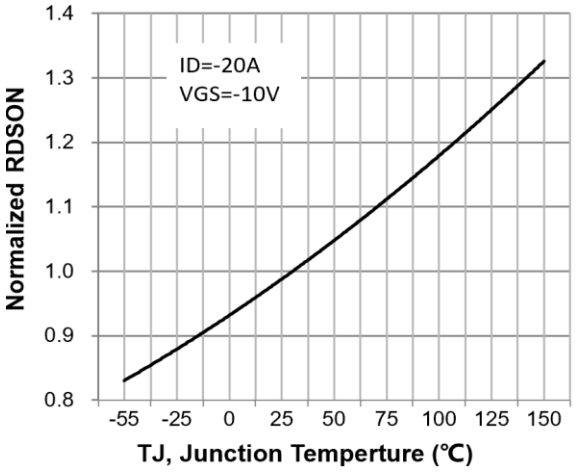


Fig13. On-Resistance Variation vs. Junction

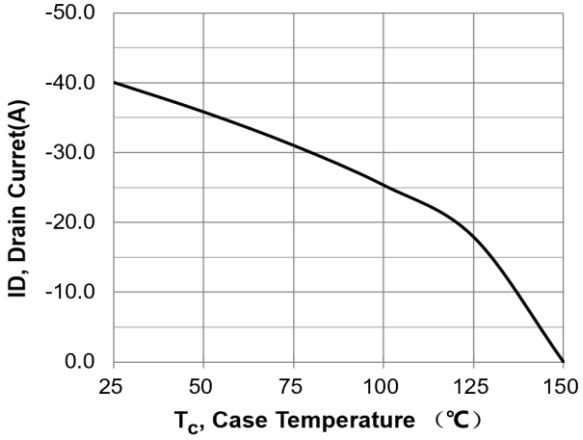


Fig14. Maximum Drain Current vs. Case Temperature

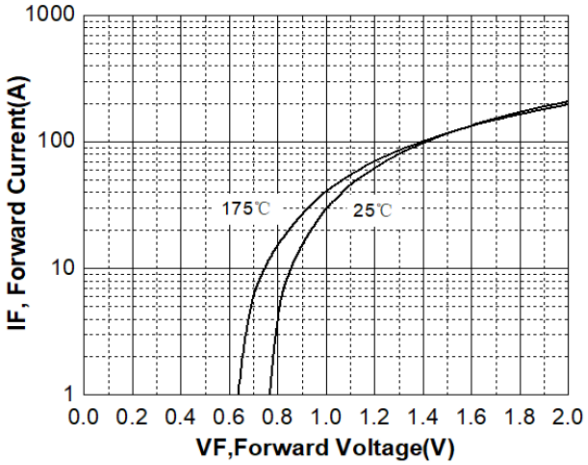


Fig15. Body Diode Forward Voltage vs. Reverse Drain Current

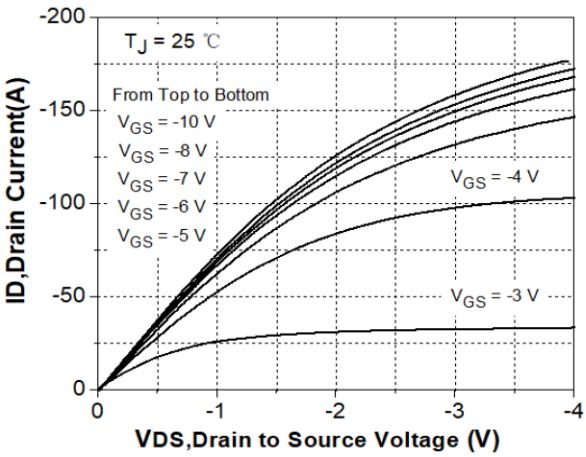


Fig16. Typical Output Characteristics@Tj= 25℃

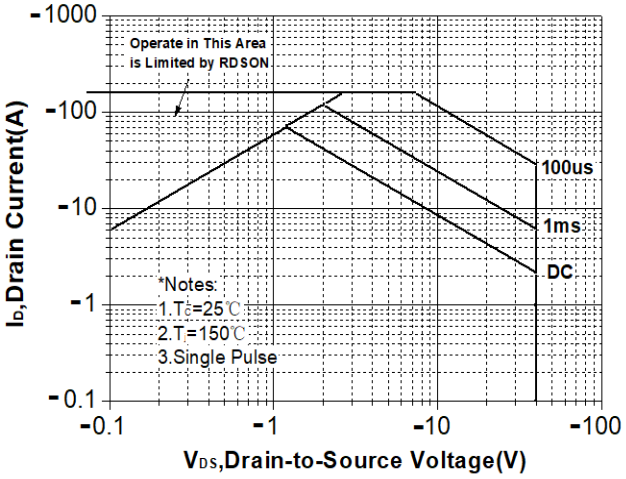


Fig17. Safe Operating Area

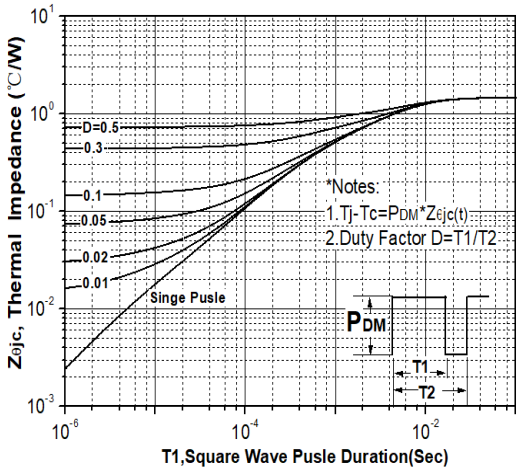
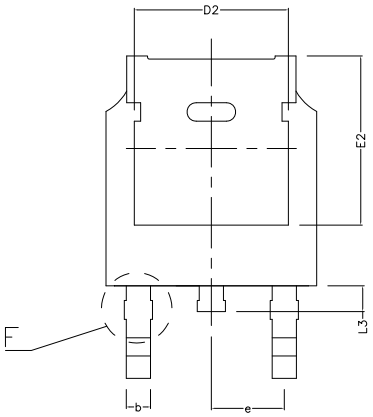


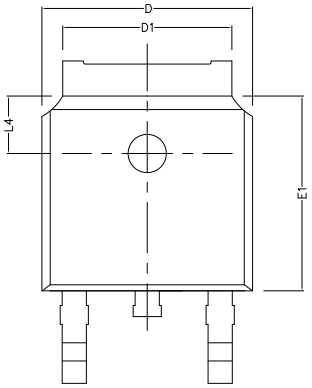
Fig18. Transient Thermal Response Curve

TO-252 **Package Outline Dimensions (Units: mm)**

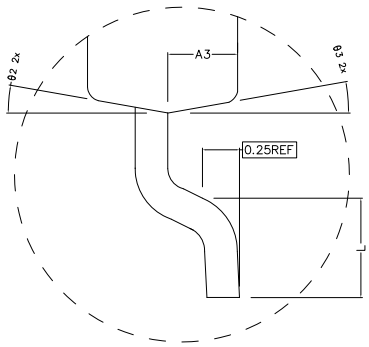
Package Outline Dimensions



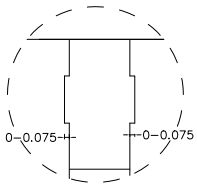
BOTTOM VIEW



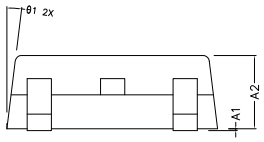
TOP VIEW



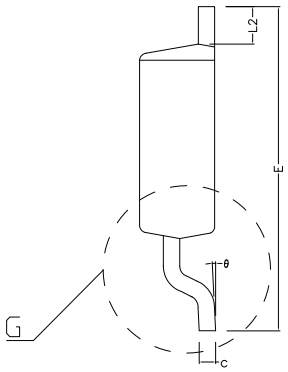
DETAIL G



DETAIL F



SIDE VIEW



SIDE VIEW

COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
	MIN	NORMAL	MAX
A1	0.000	0.100	0.150
A2	2.200	2.300	2.400
A3	1.020	1.070	1.120
b	0.710	0.760	0.810
c	0.460	0.508	0.550
D	6.500	6.600	6.700
D1	5.330REF		
D2	4.830REF		
E	9.900	10.100	10.300
E1	6.000	6.100	6.200
E2	5.600REF		
e	2.286TYPE		
L	1.400	1.550	1.700
L2	1.10REF		
L3	0.80REF		
L4	1.80REF		
θ	0~8°		
θ1	7° TYPE		
θ2	10° TYPE		
θ3	10° TYPE		