20V/5A Synchronous step-down regulator

Check for Samples: LGS53605A

Features

- High Efficiency: Up to 96%
- 5A Output Current
- 4V to 20V VIN Range
- Integrated Power N-Channel MOSFETs
- Adjustable DCM and FCCM under light load conditions
- Adjustable Frequency 800kHz to 2MHz
- Multiphase Operation（Up to 12 Phases）
- Adjustable soft-start time and Output voltage tracking capability
- Shutdown Mode Draws Less Than 11μA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Available in 24-Pin (4mm × 4mm) QFN Package

Applications

- Point of Load Power Supply
- Portable Instruments
- Distributed Power Systems
- Battery-Powered Equipment

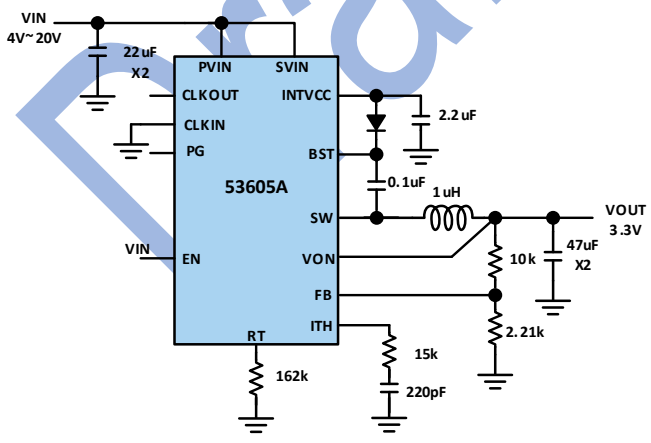
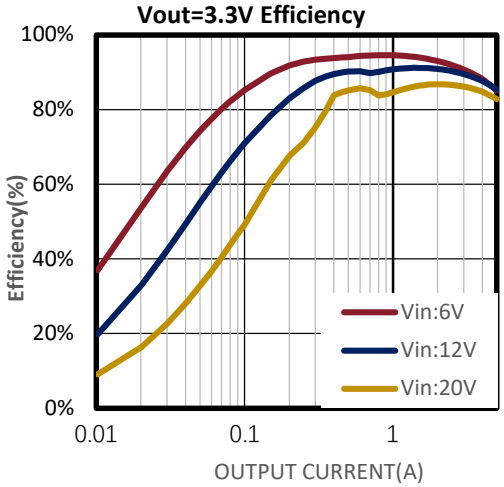


Figure 1. Typical Application Circuit

Description

LGS53605A is a step-down DC/DC regulator with an internal switch, The operating supply voltage range is from 20V down to 4V, making it suitable for dual, triple or quadruple lithium-ion battery inputs as well as point of load power supply applications from a 12V or 5V rail. LGS53605A using a phase lockable controlled on-time constant frequency, current mode architecture. Multiphase operation allows multiple LGS53605A regulators to run out of phase while using minimal input and output capacitance.

The operating frequency is programmable from 800kHz to 2MHz with an external resistor. The high frequency capability allows the use of small surface mount inductors. For switching noise sensitive applications, it can be externally synchronized from 800kHz to 2MHz. The PHMODE pin allows user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that are operating at high frequency while demanding fast transient response. Two internal phase-lock loops synchronize the internal oscillator to the external clock and also servos the regulator on-time to lock on to either the internal clock or the external clock if it's present.



Historical revision record (†)

Rev.A V0.1 May.2022	The page number
※ A version of the original.	
The parameters in this manual only describe and acknowledge the indicators in version A.	ALL

Rev.A V0.2 Nov.2022	The page number
※ A version of the original. Update the application information part of version A.	ALL

RevA V0.3 Mar.2023	The page number
※ A version of the modified.Updated for version A technical specifications, typical application waveform and recommended PCB layout information.	ALL

† NOTE: Page numbers of previous editions may differ from those of the current edition.

Absolute Maximum Ratings (†)

Table 2.1

Parameter	Range
Pin to GND Voltage (PVIN,SVIN,SW,EN)	-0.3V~22.5V
Pin to GND Voltage (SW Transient)	-2V~24.5V
Pin to GND Voltage (BST)	-0.3V ~PVIN+INTVCC
Pin to GND Voltage (VON)	-0.3V~SVIN
Pin to GND Voltage (INTVCC)	-0.3V~3.6V
Pin to GND Voltage (ITH,RT,PG,CLKIN,CLKOUT)	-0.3V~INTVCC
Pin to GND Voltage (PHMODE,MODE,TRACK/SS,FB)	-0.3V~INTVCC
Operating junction temperature	-40℃ to 125℃
Storage temperature	-65℃ to 150℃
ESD Value（HBM）	±2KV
ESD Value（CDM）	±1KV

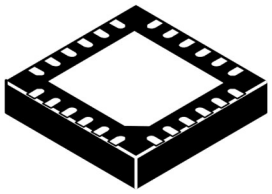
† NOTE：If the operating conditions of the device exceed the absolute maximum, the device may be permanently damaged. This is only a limit parameter and it is not recommended that the device operate at or above the limit value. The reliability of devices may be affected by long time operation in limiting conditions.

ESD warning

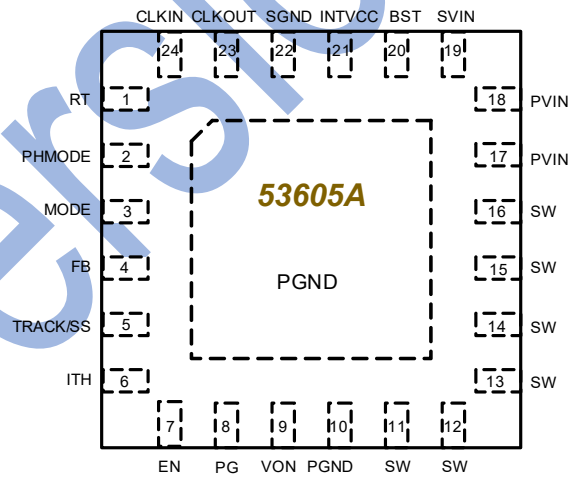
ESD(Electro static discharge)Sensitive devices.

Electric devices and circuit boards can be electrically charged without being noticed. Although this product has a patented or proprietary protection circuit, the device may be damaged in the event of high energy ESD. Therefore, appropriate ESD preventive measures should be taken to avoid device performance degradation or function loss.

Pin arrangement



QFN4X4-24 Package



Top View

T_{JMAX}=125℃,θ_{JA}=37℃/W

Figure 2. Encapsulation and pin arrangement

Table 2.2 Description of pin function

Pin number	pin name	Description
1	RT	Oscillator Frequency Programming Pin. Connect an external resistor (between 200k to 80k) from RT to SGND to program the frequency from 800kHz to 2MHz. Since the synchronization range is ±30% of set frequency, be sure that the set frequency is within this percentage range of the external clock to ensure frequency lock.
2	PHMODE	Control Input to Phase Selector. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to INTINTVCC for 2-phase operation, tie it to SGND for 3-phase operation, and tie it to INTINTVCC/2 for 4-phase operation
3	MODE	Operation Mode Select. Tie this pin to INTINTVCC to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous mode operation at light loads. Do not float this pin.
4	FB	Output Feedback Voltage. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the output voltage.
5	TRACK/SS	Output Tracking and Soft-Start Pin. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5μA pull-up current from INTINTVCC on this pin, so putting a capacitor here provides soft-start function.
6	ITH	Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage.
7	EN	Regulator output enable pin, set high enable output. The undervoltage protection of VIN can be set by configuring the external resistor divider.
8	PG	Output Power Good with Open-Drain Logic. PG is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.
9	V_{ON}	On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to VOUT and keeps the switching frequency constant at different VOUT.
10,EP	PGND	Power Ground. Return path of internal power MOSFETs. Connect this pin to the negative terminals of the input capacitor and output capacitor. The exposed pad must be soldered to the PCB ground for electrical contact and rated thermal performance.
11~16	SW	Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PVIN.
17,18	PVIN	Regulator power input. Use a ceramic capacitor of 22μF or larger as close as possible to the bypass PVIN to PGND.
19	SVIN	Signal VIN. Filtered input voltage to the on-chip 3.3V regulator. Connect a (1Ω to 10Ω) resistor between SVIN and PVIN and bypass to GND with a 0.1μF capacitor.

20	BST	Bootstrap drive power supply. High quality 100nF ceramic capacitors need to be connected between the BST and SW to bias the internal high voltage side gate driver.
21	INTVCC	A power supply to supply power to the internal control circuit. A 1uF~4.7uF ceramic decoupling capacitor must be connected between INTVCC and PGND, as close as possible to the chip pin.
22	SGND	Signal Ground Connection.
23	CLKOUT	Output Clock Signal for Multiphase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is INTVCC to GND.
24	CLKIN	External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 20k. The phase-locked loop will force the top power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal.

Electrical Characteristics

Limits apply to operating junction temperatures (T_J) ranging from -40℃ to +125℃ unless otherwise specified. Minimum and maximum limits are specified by test, design or statistical correlation. Typical values represent the most likely parameter specifications when T_J=25℃, for reference only. All voltages are relative to GND.

Table3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SVIN	SVIN Input Voltage Range		4		20	V
PVIN	PVIN Input Voltage Range		0.9		20	V
I_Q	No-load input current	Mode = 0, R_T = 130k		600		uA
Isd	Shutdown current	V_{IN} = 12V, EN = 0		11		uA
V_{FB}	Feedback Reference Voltage		0.594	0.6	0.606	V
$\Delta V_{FB(LINE)}$	Feedback Voltage Line Regulation	V_{IN} = 4V to 20V		0.001	0.03	%
$\Delta V_{FB(LOAD)}$	Feedback Voltage Load Regulation			0.1	0.3	%
I_{FB}	Feedback Pin Input Current			10	100	nA
g_m(EA) (1)	Error Amplifier Transconductance		1.253		1.670 V	mS
$t_{ON(MIN)}$ (1)	Minimum On-Time			50		ns
$t_{OFF(MIN)}$ (1)	Minimum Off-Time			130		ns
I_{LIM}	Positive Inductor Valley Current Limit			6		A
	Negative Inductor Valley Current Limit			-6		A
R_{TOP}	Top Power NMOS On-Resistance	INTVCC = 3.3V		85	150	mΩ
R_{BOTTOM}	Bottom Power NMOS On-Resistance	INTVCC = 3.3V		42	60	mΩ
V_{UVLO}	INTVCC Undervoltage Lockout Threshold	INTVCC Rising		2.6		V
		INTVCC Falling		2.8		V
V_{EN}	EN Threshold 2(I_Q≥1mA)	EN Rising		1.1		V
	EN Threshold 1(I_Q≥100uA)	EN Rising		0.5		V
INTVCC	Internal VCC Voltage	4V < VIN < 20V		3.3		V
ΔINTVCC	INTVCC Load Regulation	I_{LOAD} = 0mA to 20mA		0.3		%
OV	Output Overvoltage Threshold	V_{FB} Rising		110		%
UV	Output Undervoltage Threshold	V_{FB} Falling		91		%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning		1		%
R_{PG}	PGOOD Pull-Down Resistance			38		Ω

I_{PG}	PGOOD Leakage	0.54V<V_{FB}<0.66V			2	uA
$I_{TRACK/SS}$	TRACK Pull-Up Current			2.5	4	uA
fs	Oscillator Frequency	RT = 162kΩ	0.8	1	2	MHz
CLKIN	CLKIN Threshold	CLKIN V_{IL}			0.3	V
		CLKIN V_{IH}	1			V
V_{VIN_OV}	VIN Overvoltage Lockout Threshold	VIN Rising		23		V
		VIN Falling		21		V

(1) Design Guarantee. Not production tested.

Typical Characteristics

Unless otherwise specified , VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

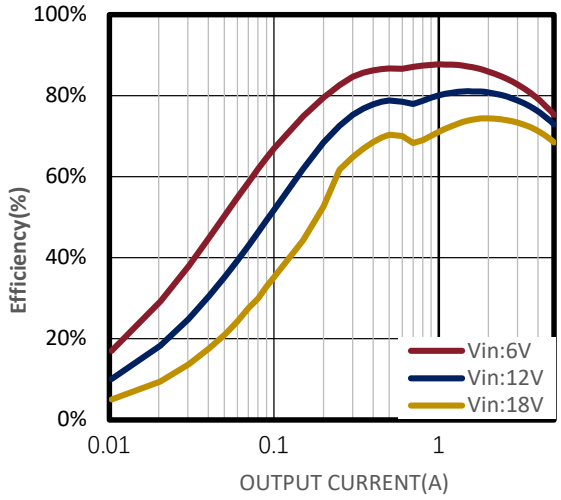


Figure 3.1 Vout=1.2V,FCCM Mode Efficiency

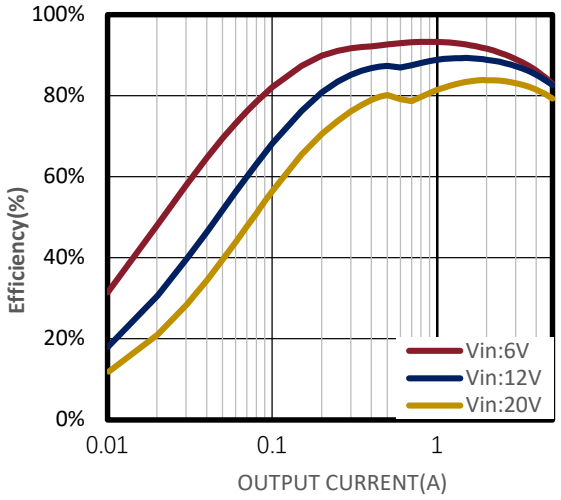


Figure3.2 Vout=2.5V,FCCM Mode Efficiency

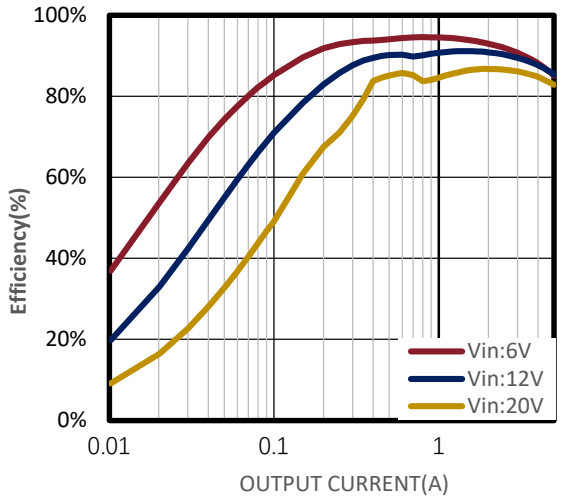


Figure 3.3 Vout=3.3V,FCCM Mode Efficiency

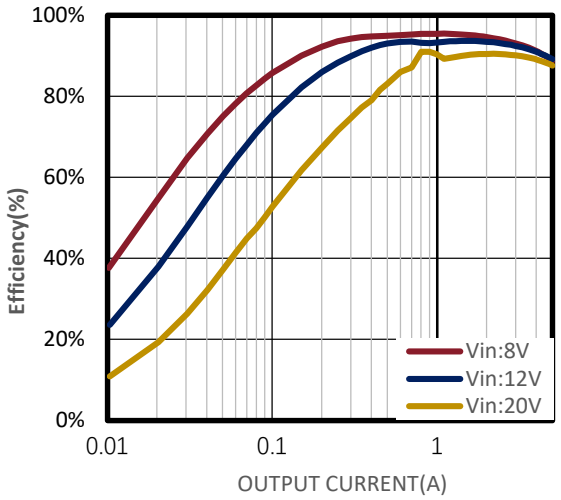


Figure 3.4 Vout=5V,FCCM Mode Efficiency

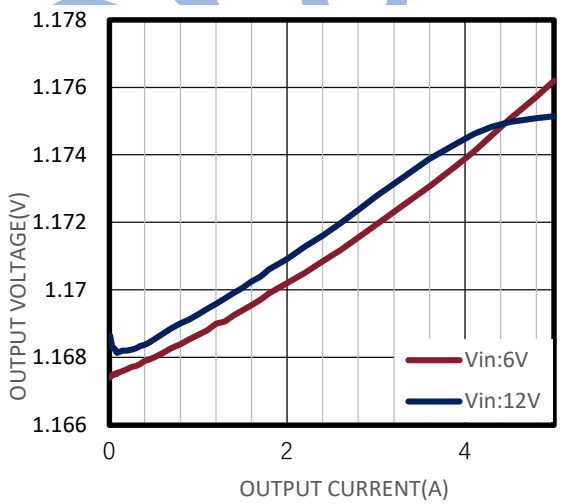


Figure 3.5 Vout=1.2V, FCCM Mode Load Regulation

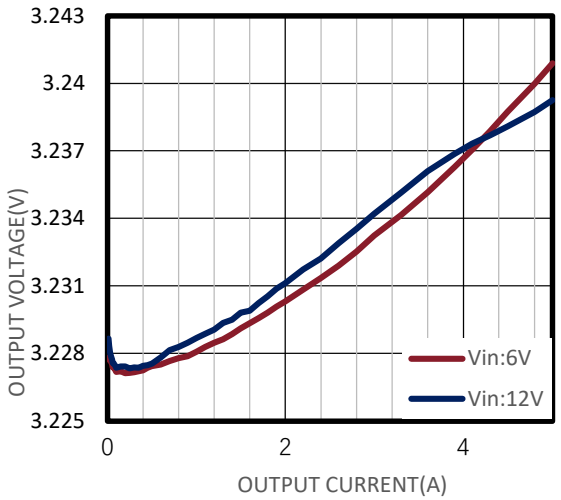


Figure3.6 Vout=3.3V, FCCM Mode Load Regulation

Typical Characteristics

Unless otherwise specified ,VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

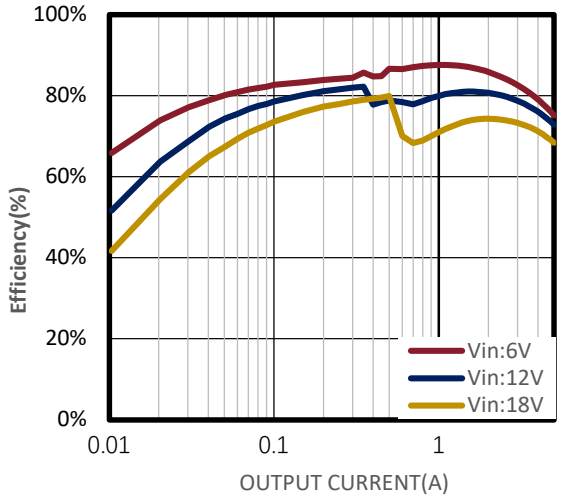


Figure 3.7 Vout=1.2V,PFM Mode Efficiency

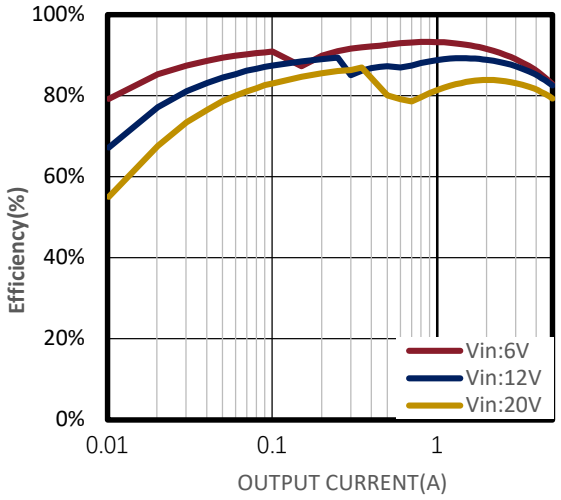


Figure3.8 Vout=2.5V,PFM Mode Efficiency

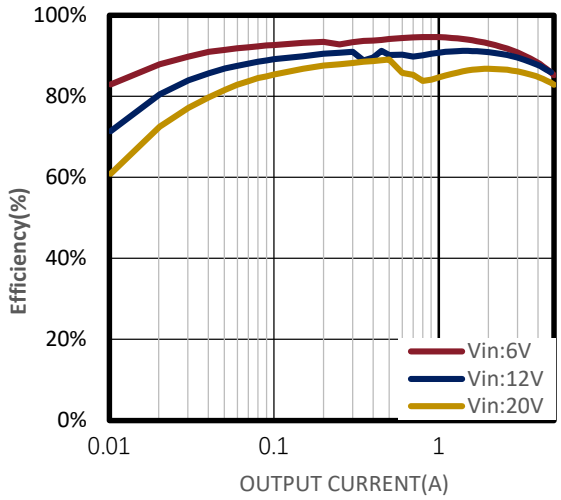


Figure 3.9 Vout=3.3V,PFM Mode Efficiency

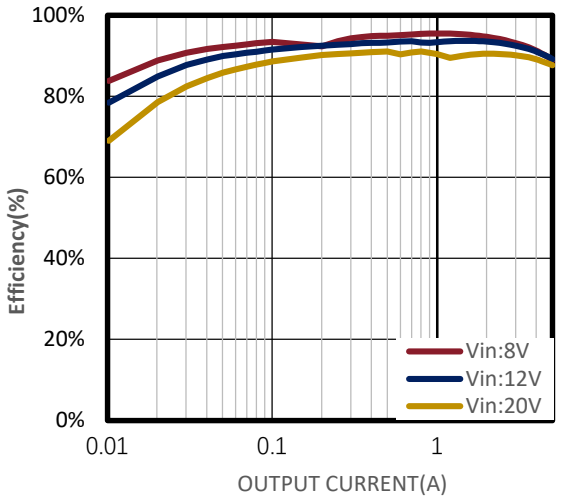


Figure 3.10 Vout=5V,PFM Mode Efficiency

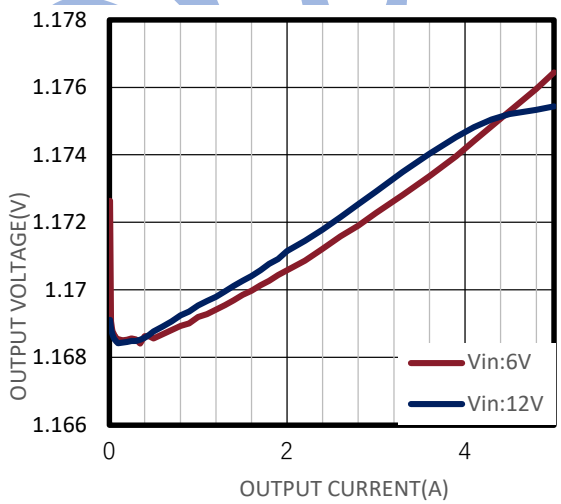


Figure 3.11 Vout=1.2V, PFM Mode Load Regulation

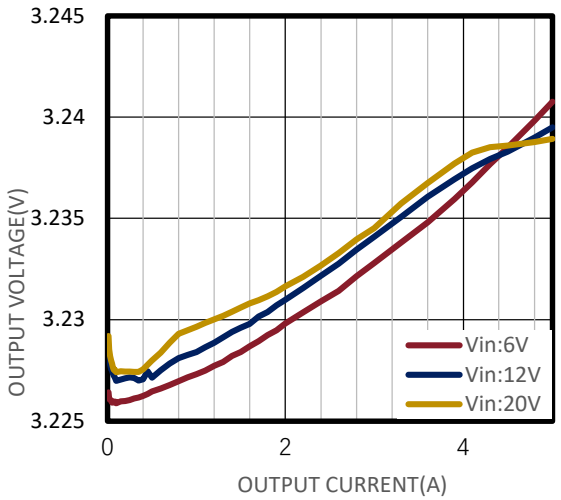
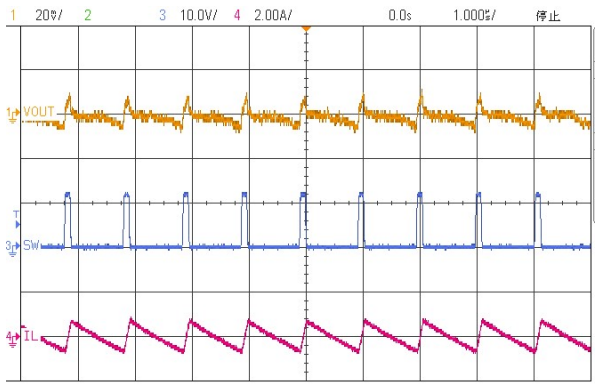


Figure3.12 Vout=3.3V, PFM Mode Load Regulation

Typical Characteristics

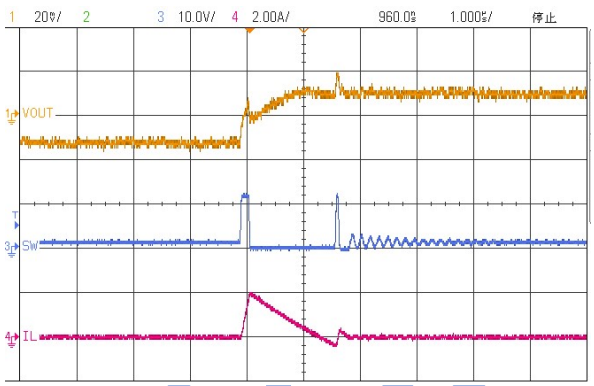
Unless otherwise specified ,VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

Figure 3.13 FCCM Mode Switching Waveform



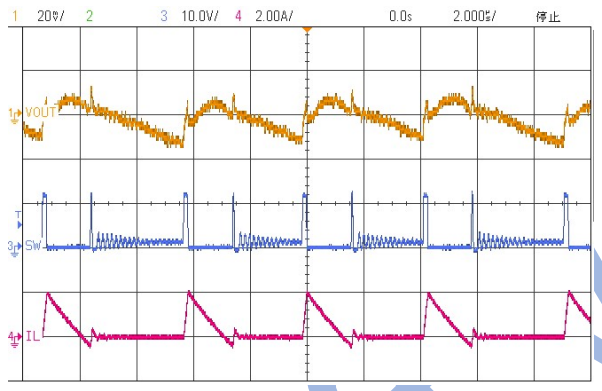
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.14 PFM Mode Switching Waveform



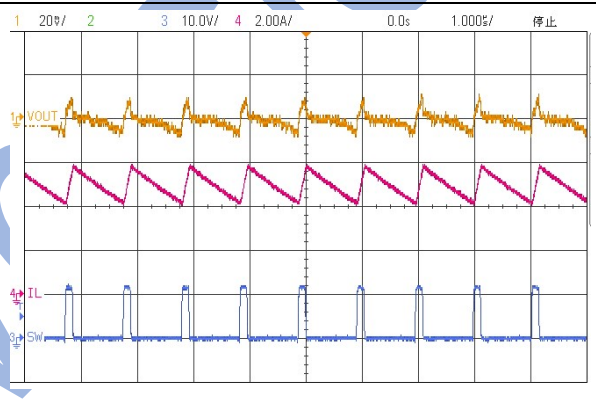
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.15 PFM Mode Switching Waveform



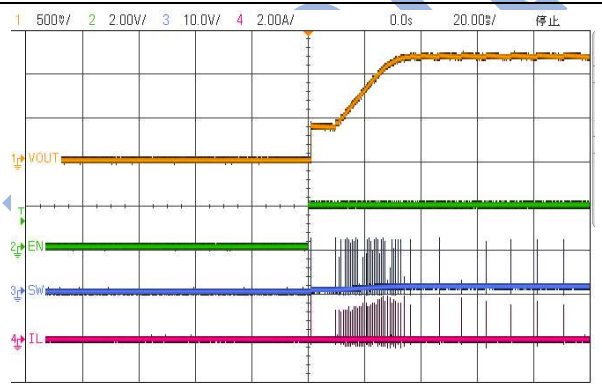
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=300mA

Figure 3.16 PFM Mode Switching Waveform



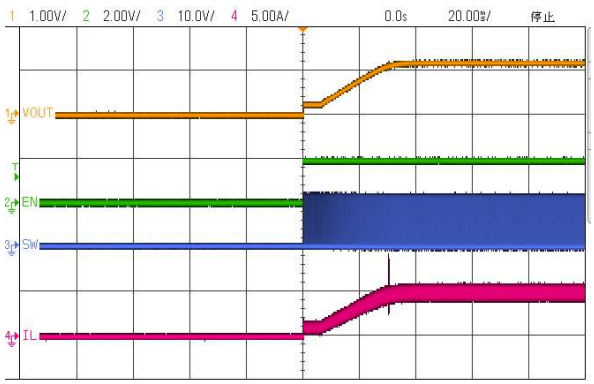
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5A

Figure 3.17 PFM Mode EN StartUp



VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.18 PFM Mode EN StartUp

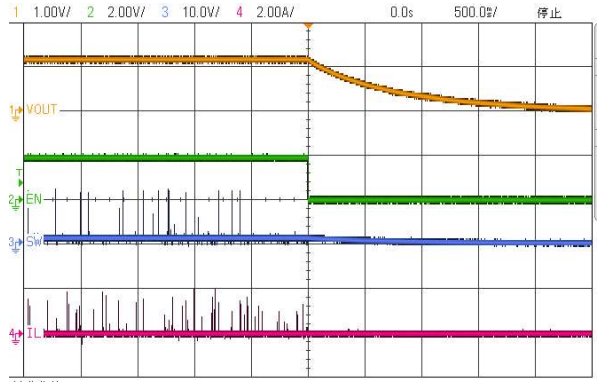


VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5A

Typical Characteristics

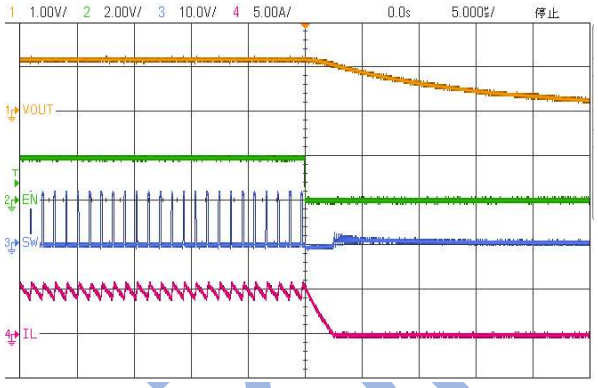
Unless otherwise specified ,VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

Figure 3.19 PFM Mode EN ShutDown



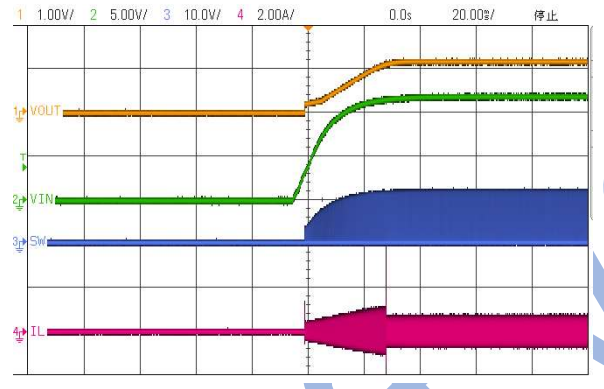
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.20 PFM Mode EN ShutDown



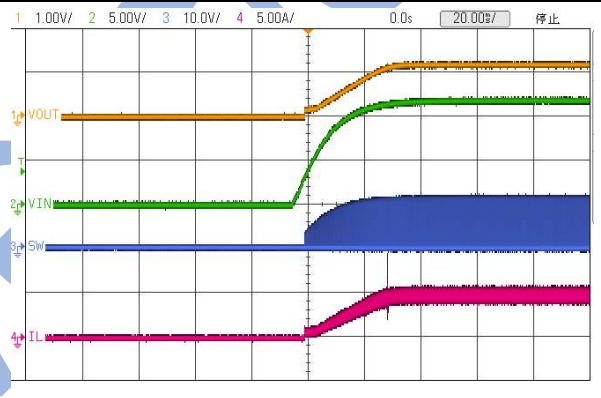
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5A

Figure 3.21 FCCM Mode VIN StartUp



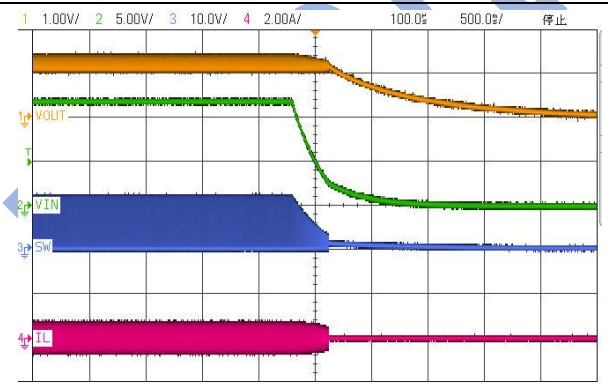
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.22 FCCM Mode VIN StartUp



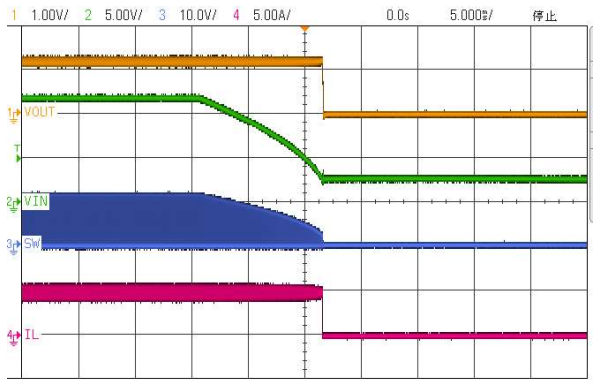
VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5A

Figure 3.23 FCCM Mode VIN ShutDown



VIN=12V,VOUT=1.2V,FS=1MHz,Iout=0A

Figure 3.24 FCCM Mode VIN ShutDown

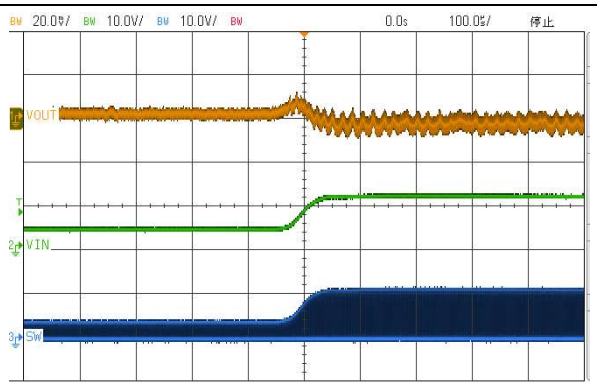


VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5A

Typical Characteristics

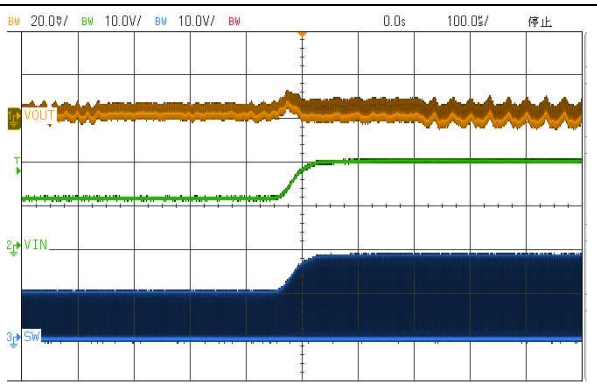
Unless otherwise specified ,VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

Figure 3.25 FCCM Mode VIN Transient



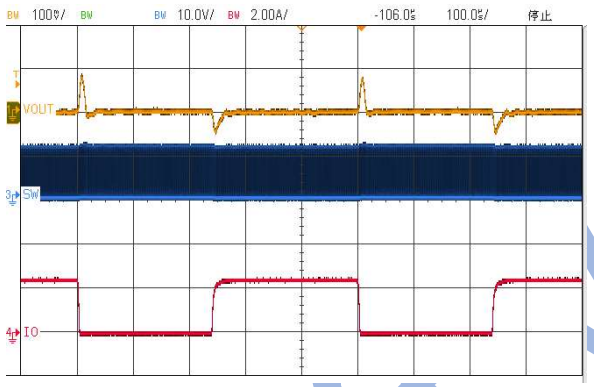
VIN=4V-12V,VOUT=1.2V,FS=1MHz, Iout=5A

Figure 3.26 FCCM Mode VIN Transient



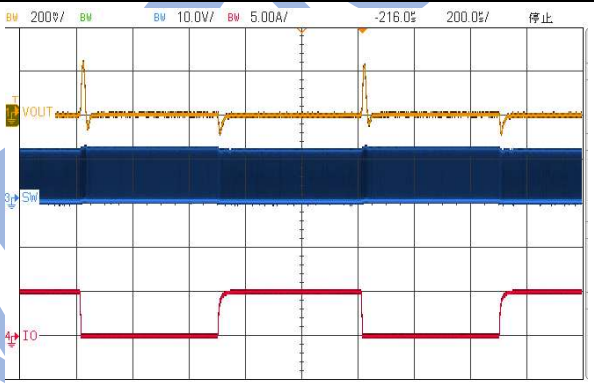
VIN=12V-20V,VOUT=1.2V,FS=1MHz, Iout=5A

Figure 3.27 FCCM Mode Load Transient



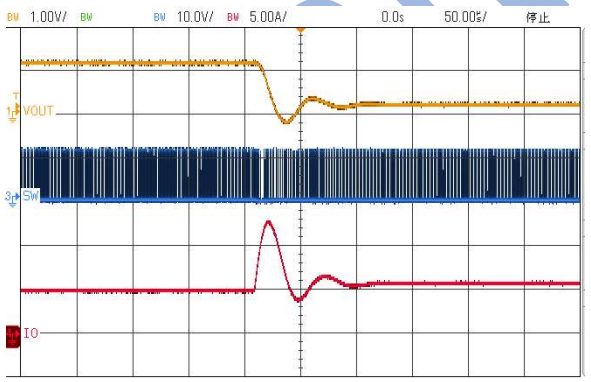
VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=0-2.5A

Figure 3.28 FCCM Mode Load Transient



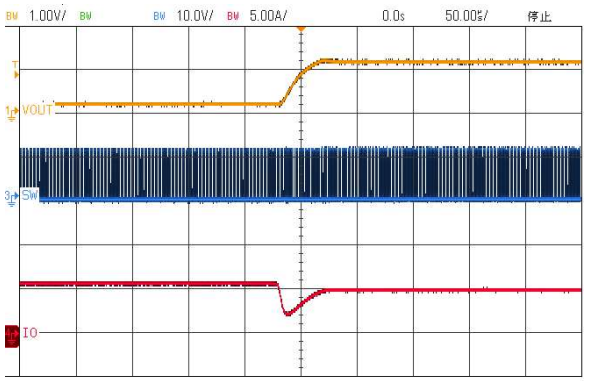
VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=0-5A

Figure 3.29 FCCM Mode SCP



VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=5A

Figure 3.30 FCCM Mode SCP Recovery

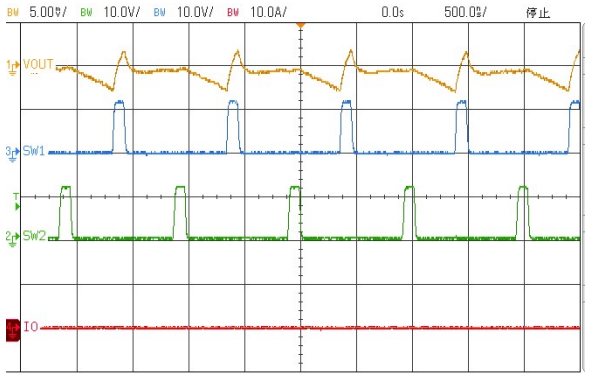


VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=5A

Typical Characteristics

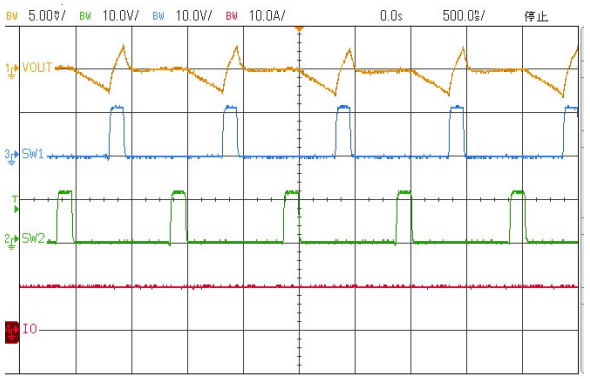
Unless otherwise specified ,VIN=12V, VOUT=1.2V, FS=1MHz, L=0.68μH, CIN=47μF, COUT=100μF.

Figure 3.31 2-phase FCCM Mode Switching Waveform



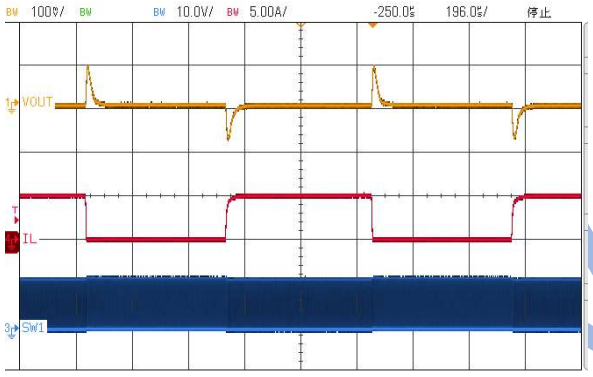
VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=0A

Figure 3.32 2-phase PFM Mode Switching Waveform



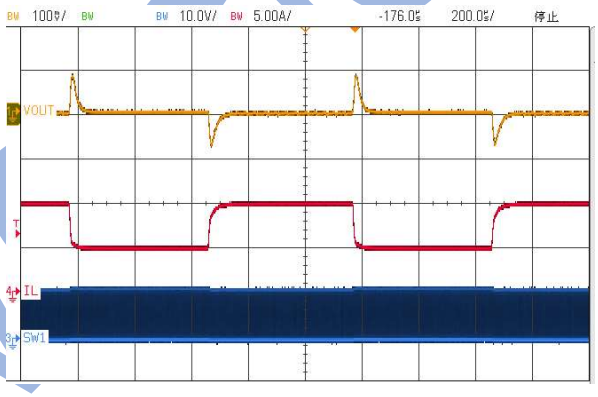
VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=10A

Figure 3.33 2-phase FCCM Mode Load Transient



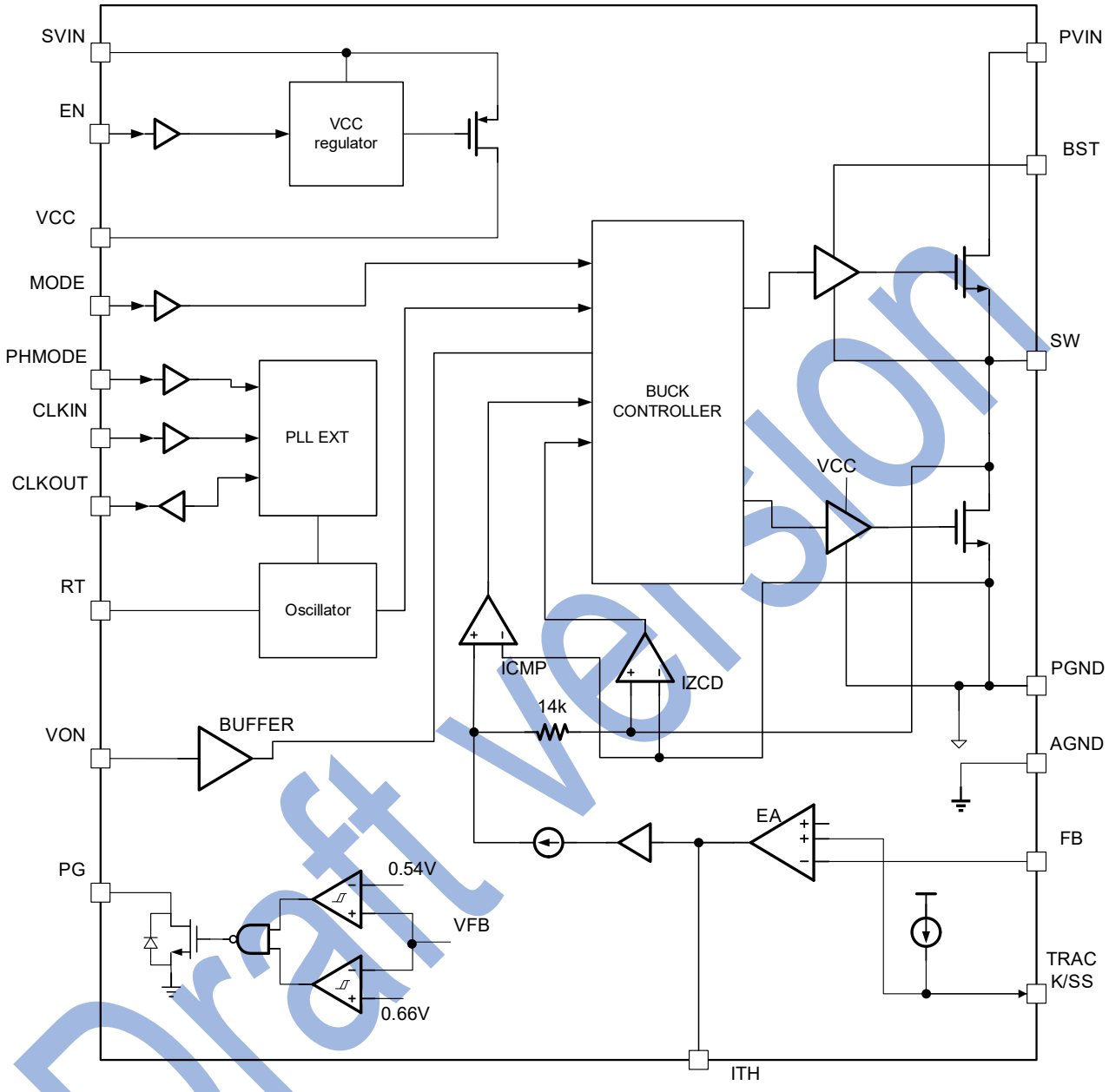
VIN=12V,VOUT=1.2V,FS=1MHz,IOUT=0-5A

Figure 3.34 2-phase FCCM Mode Load Transient



VIN=12V,VOUT=1.2V,FS=1MHz,Iout=5-10A

Functional block diagram



Application information: Feature Description

Overview

LGS53605A is a step-down DC/DC regulator with an internal switch, The operating supply voltage range is from 20V down to 4V, making it suitable for dual, triple or quadruple lithium-ion battery inputs as well as point of load power supply applications from a 12V or 5V rail.

LGS53605A using a phase lockable controlled on-time constant frequency, current mode architecture. Multiphase operation allows multiple LGS53605A regulators to run out of phase while using minimal input and output capacitance. The operating frequency is programmable from 800kHz to 2MHz with an external resistor. The high frequency capability allows the use of small surface mount inductors. For switching noise sensitive applications, it can be externally synchronized from 800kHz to 2MHz. The PHMODE pin allows user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that are operating at high frequency while demanding fast transient response. Two internal phase-lock loops synchronize the internal oscillator to the external clock and also servos the regulator on-time to lock on to either the internal clock or the external clock if it's present.

EN Threshold

Pulling the EN pin to ground forces the LGS53605A into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the EN pin above 0.6V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the EN voltage above 1.2V turns on the entire chip.

INTVCC Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the drivers and the internal bias circuitry. The INTVCC can supply up to 100mA RMS and must be bypassed to ground with a minimum of 1μF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to the INTVCC pin is not recommended since it will further push the LDO into its RMS current rating while increasing power dissipation and die temperature.

VIN Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LGS53605A constantly monitors the VIN pin for an overvoltage condition. When VIN rises above 23V, the regulator suspends operation by shutting off both power MOSFETs. Once VIN drops below 21V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

PVIN/SVIN Voltage Differential

PVIN is an internal power circuit input pin, and SVIN supply the internal logic circuit power pins. To ensure that internal logic circuits are not disturbed by noise, SVIN is recommended to connect to PVIN with a low - pass filter of 1Ω to 10Ω and 0.1 μF. Both the chip PVIN and SVIN pins include an internal underwriter locking circuit. When the pins voltage is lower than the decrease threshold of UVLO, the UVLO protection will be triggered and the voltage output will be turned off. The rising threshold of PVIN UVLO is about 0.9V, and the rise threshold of SVIN UVLO is about 2.8V. After the pin voltage reaches the UVLO above this voltage, the controller will enter the soft startup process.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$VOUT = 0.6V \times (1 + \frac{R2}{R1})$$

The resistive divider allows the VFB pin to sense a fraction of the output voltage as shown in Figure 5.

Application information: Feature Description

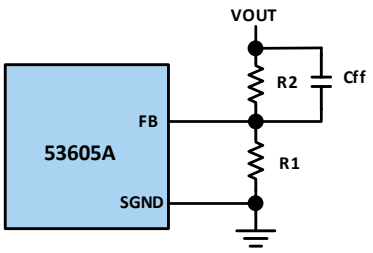


Figure 5. Setting the Output Voltage

Fixed R2 to calculate the required resistance value R1, assuming that R2 fixed value is 10K. The following table gives several appropriate R1 values of common output voltage:

Vout (V)	R1 (Ω)	R2 (Ω)
1.2	4.99k	4.99k
2.5	3.16k	10k
3.3	2.21k	10k
5	1.37k	10k

Programming Switching Frequency

Connecting a resistor from the RT pin to SGND programs the switching frequency from 800kHz to 2MHz according to the following formula:

$$f_s(Hz) = \frac{1.6e^{11}}{RT(\Omega)}$$

Output Voltage Tracking and Soft-Start

The LGS53605A allows the user to program its output voltage ramp rate by means of the TRACK/SS pin. An internal 2μA pulls up the TRACK/SS pin to INTVCC. Putting an external capacitor on TRACK/SS enables soft starting the output to prevent current surge on the input supply. For output tracking applications, TRACK/SS can be externally driven by another voltage source. From 0V to 0.6V, the TRACK/SS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of TRACK/SS pins. During this start-up time, the LGS53605A will operate in discontinuous mode. When TRACK/SS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage

Output Power Good

When the LGS53605A's output voltage is within the ±10% window of the regulation point, which is reflected back as a VFB voltage in the range of 0.54V to 0.66V, the output voltage is good and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pull-down device (38Ω) will pull the PGOOD pin low.

Multiphase Operation

For output loads that demand more than 5A of current, multiple LGS53605A can be cascaded to run out of phase to provide more output current. The CLKIN pin allows the LGS53605A to synchronize to an external clock (±30% of frequency programmed by RT) and the internal phase locked-loop allows the LGS53605A to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following LGS53605A stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to INTVCC, SGND or INTVCC/2 generates a phase difference (between CLKIN and CLKOUT) of 180 degrees, 120 degrees, or 90 degrees respectively, which corresponds to 2-phase, 3-phase or 4-phase operation. A total of 12 phases can be cascaded to run simultaneously out of phase with respect to each other by programming the PHMODE pin of each LGS53605A to different levels.

ITH Compensation

ITH is an internal error amplifier compensation pin, and its internal is used to connect to the output of an error amplifier with a 65K resistor with a 60PF capacitor in series (internal ITH compensation points).

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LGS53605A is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 160ns. The minimum off-

Application information: Feature Description

time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON}+t_{OFF(MIN)})$.If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \times \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its “on” state. This time is typically 50ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$D_{MIN} = f \times t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input Operation and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the VIN input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, VDROOP, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} \cong 2.5 \frac{\Delta I_{OUT}}{f_0 \cdot V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22μF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PVIN pins as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OU}}{f \cdot L}(1 - \frac{V_{OUT}}{V_{IN(MAX)}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor.

Application information: Feature Description

There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 2.5A. This is especially important at low VOUT operation where VOUT is 1.8V or below. Care must be given to choose an inductance value that will generate a big enough current ripple (1.5A to 2.5A) so that the chip's valley current comparator has enough signal-to-noise ratio to force constant switching frequency. Meanwhile, also note that the largest ripple current occurs at the highest VIN. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \cdot \Delta I_{L(MAX)}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

However, the inductor ripple current must not be so large that its valley current level (–ΔIL/2) can exceed the negative current limit, which can be as low as –3.5A. If the negative current limit is exceeded in forced continuous mode of operation , VOUT can get charged to above the regulation level until the inductor current no longer exceeds the negative current limit. In such instances, choose a larger inductor value to reduce the inductor ripple current. The alternative is to reduce the RT resistor value to increase the switching frequency in order to reduce the inductor ripple current.

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current Operation is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

Application information: Typical Applications

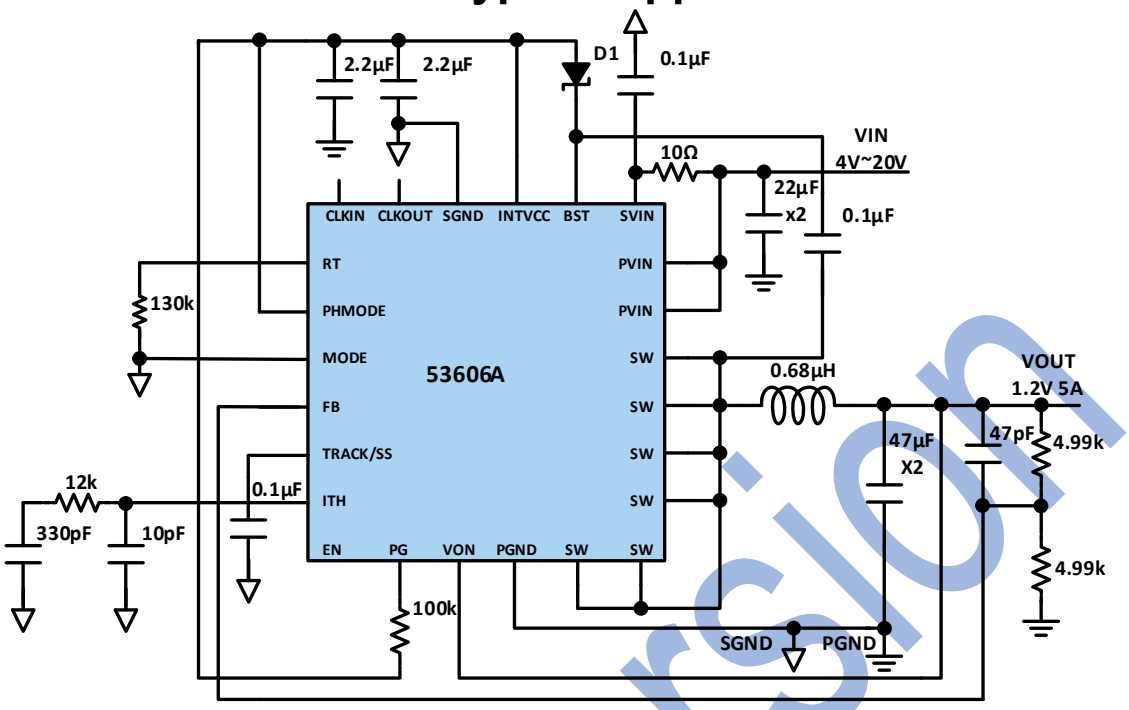


Figure 6 12V to 1.2V 1MHz Buck Regulator

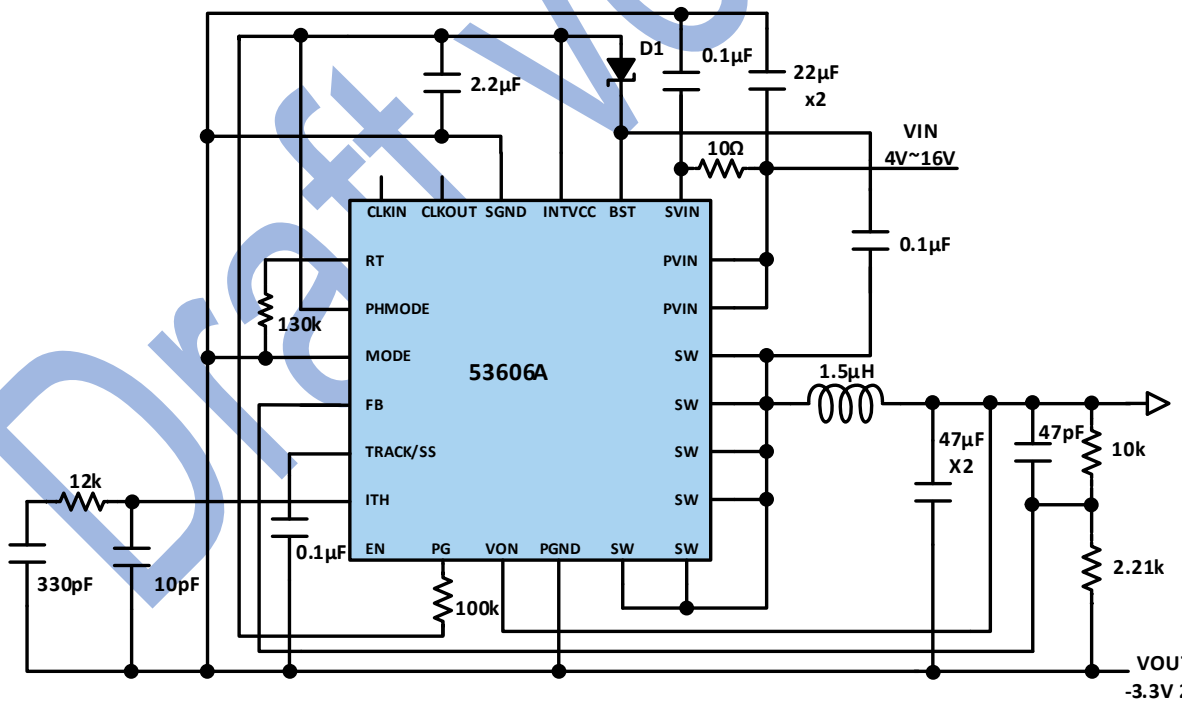


Figure 7 -3.3V Negative Converter

Application information: Typical Applications

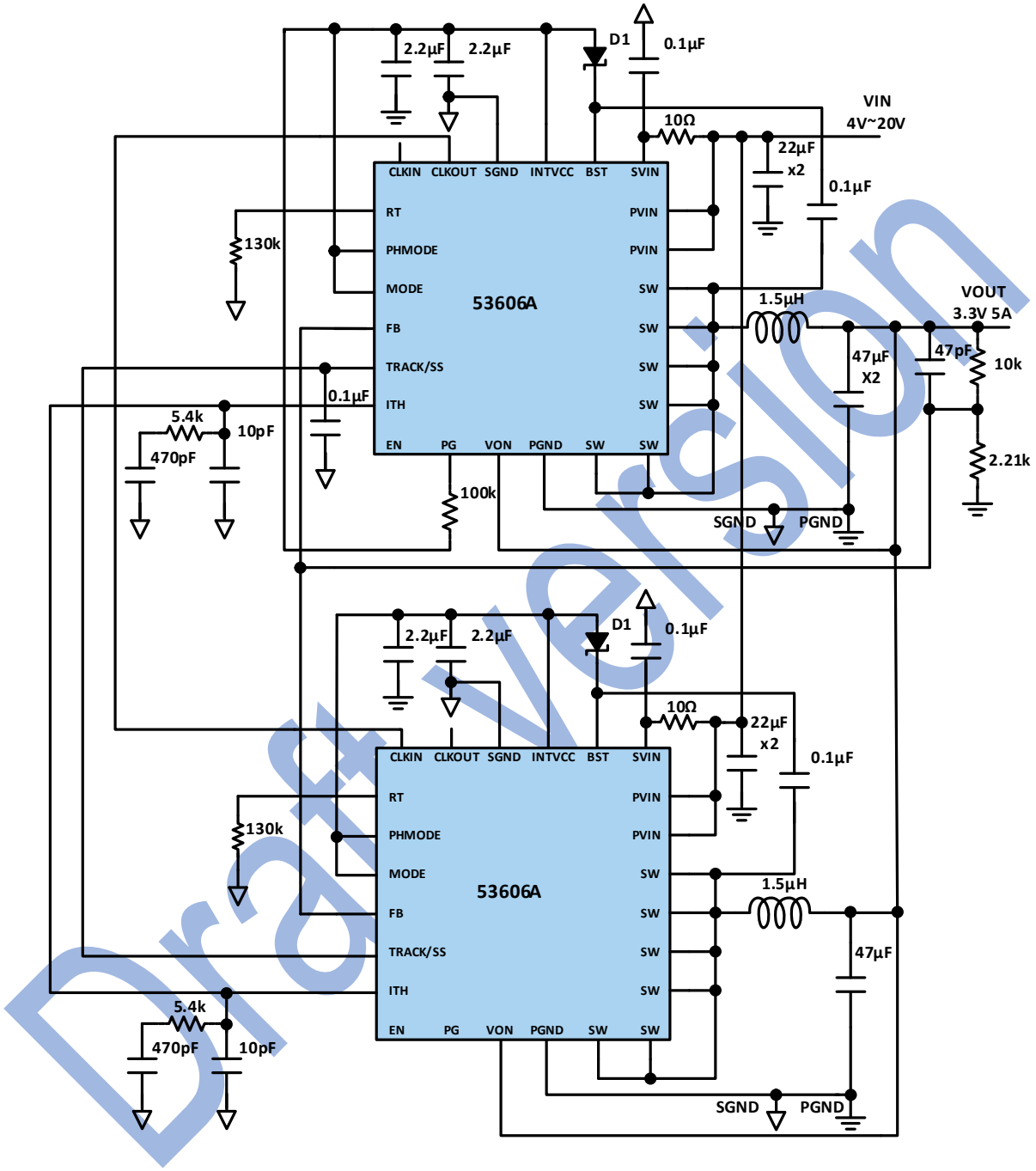


Figure 8 12V, 10A 2-Phase Single Output Regulator

Application information: PCB layout

LGS53605A's high integration makes PCB board layout very simple and easy. A poor layout affects the performance of LGS53605A, resulting in poor electromagnetic interference (EMI), electromagnetic compatibility (EMC), and voltage loss, affecting voltage regulation and stability. In order to optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and wiring to ensure optimal performance:

- The high frequency ceramic input capacitor C_{IN} must be placed near the PVIN and PGND pins as close as possible to reduce the high frequency noise.
- Resistance dividers R_{FBH} and R_{FBL} must be connected between the positive end of C_{OUT} and SGND. Feedback signal V_{FB} should be kept away from noisy elements and routing, such as SW lines, and its routing should be minimized. Keep the R_{FBH} and R_{FBL} close to the IC.
- Solder the bare pad (pin EP) at the bottom of the package to the PGND plane. Connect this PGND plane to other layers with thermal through-holes to help dissipate heat from LGS53605A.
- Keep the sensor away from the SW pin. RT resistors, compensation capacitors CC and C_{ITH} and all R_{FBH}, R_{FBL} and R_C resistors and INTVCC bypass capacitors should be kept away from SW wiring and inductor L1. In addition the SW pin pad should be as small as possible.
- Keep the signal and power grounded isolated, the small signal component returns to the SGND pin and then connects to the PGND pin at the negative terminal of the output capacitor C_{OUT}.
- Cover all unused areas on all layers with copper to reduce the temperature rise of the power element. These copper areas should be connected to PGND.

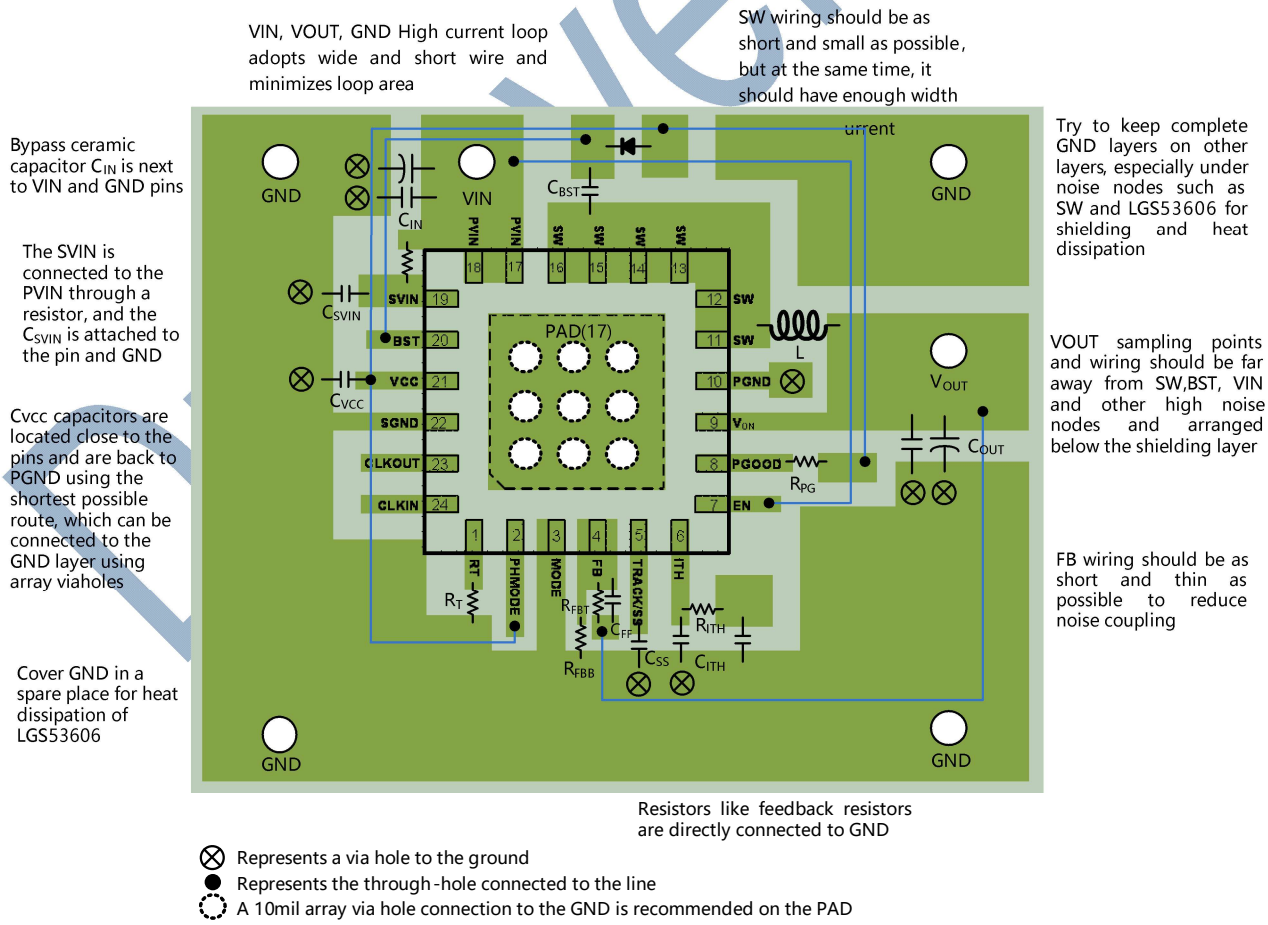
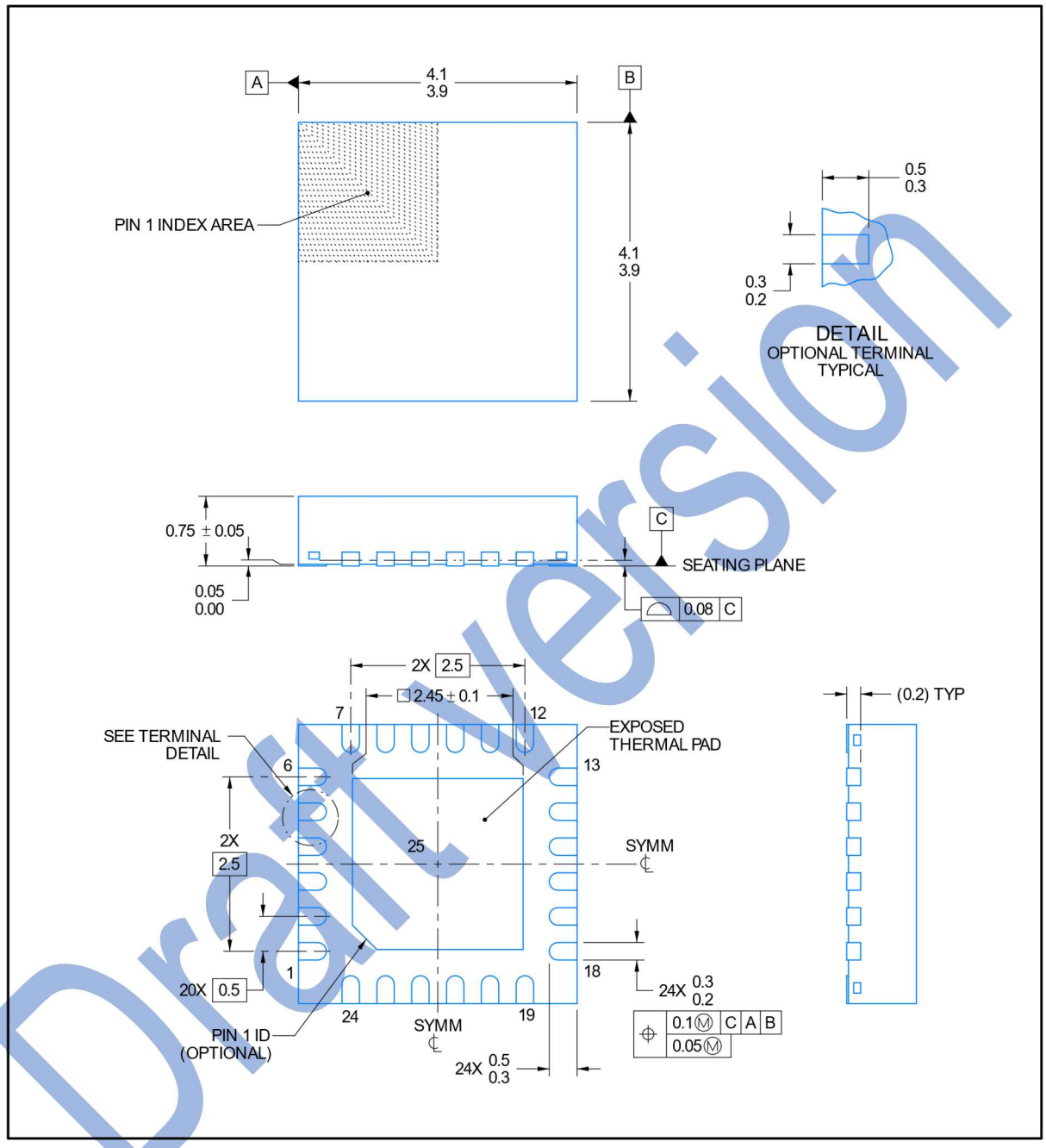


Figure9. QFN24(4*4) package typical application PCB recommendation

Package Outline Description (QFN4x4-24)

24-Pin Plastic QFN with Bottom EPAD



NOTE:

(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

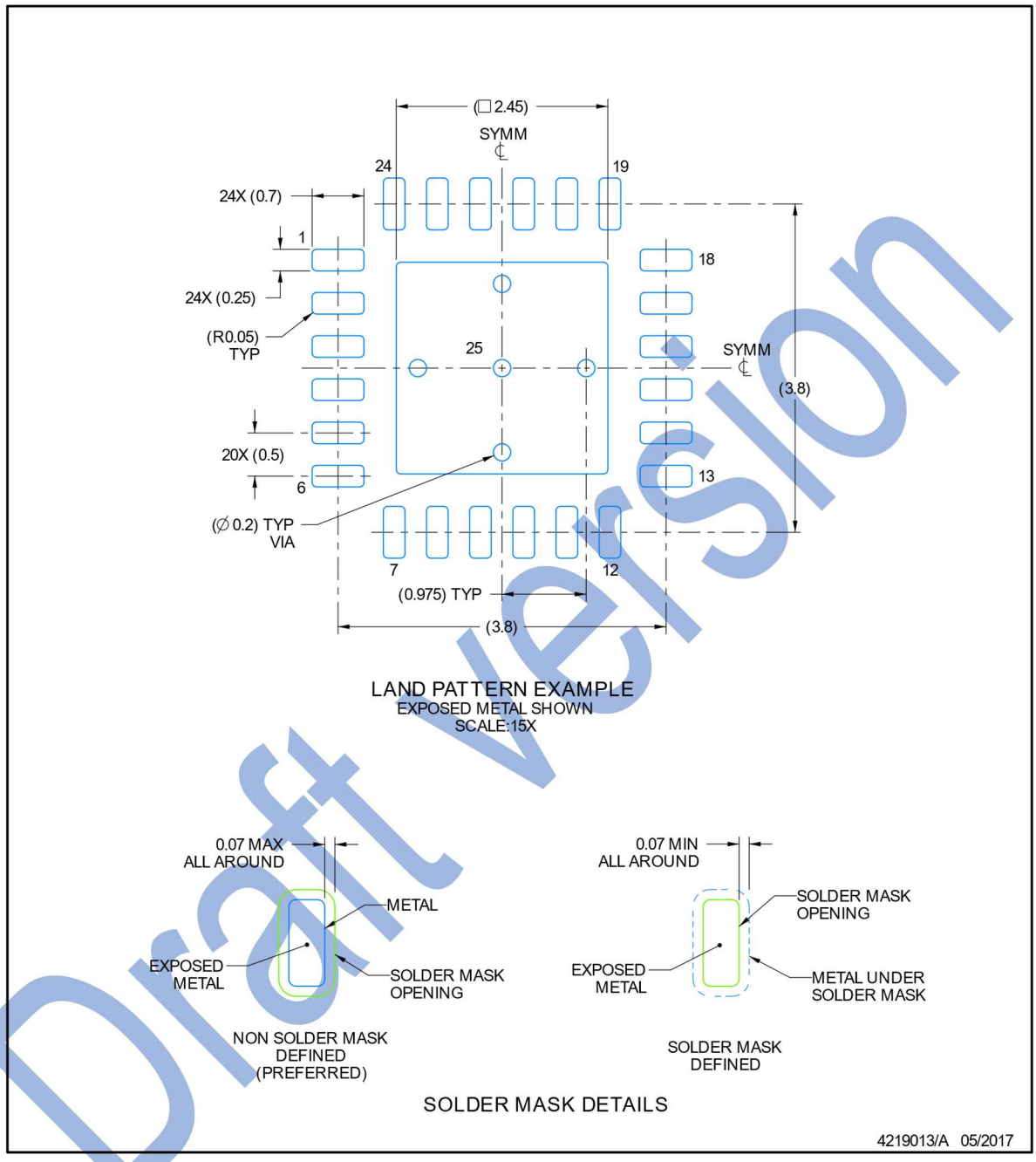
(2) This drawing is subject to change without notice.

(3) This dimension does not include mold burrs, protrusions, or nozzle burrs. The burrs or protrusions on each side of the mold shall not exceed 0.15mm.

(4) This dimension does not include mold burrs, and the burrs or protrusions on each side of the mold do not exceed 0.25 mm.

Package Outline Description (QFN4x4-24)

24-Pin Plastic QFN with Bottom EPAD



NOTE:

(1) Based on IPC-7351, which relies on proven mathematical algorithms, and comprehensively considers manufacturing, assembly, and component tolerances, the pad pattern is accurately calculated.

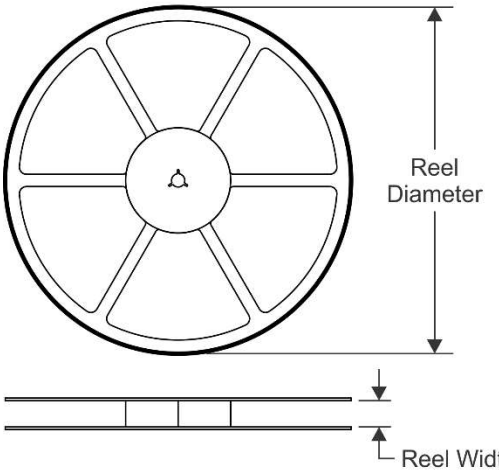
(2) Solder mask tolerances between and around signal pads may vary due to board fabrication.

(3) The size of the metal pad may vary due to creepage requirements.

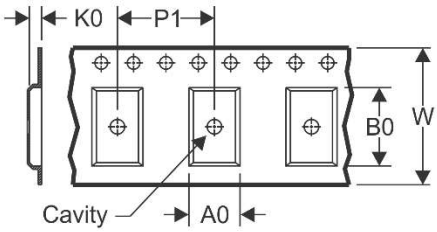
(4) Through holes are optional, depending on application, see device data sheet. If vias are used, refer to the via locations shown in this view. It is recommended to fill or cover the vias under the pads with solder paste.

TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

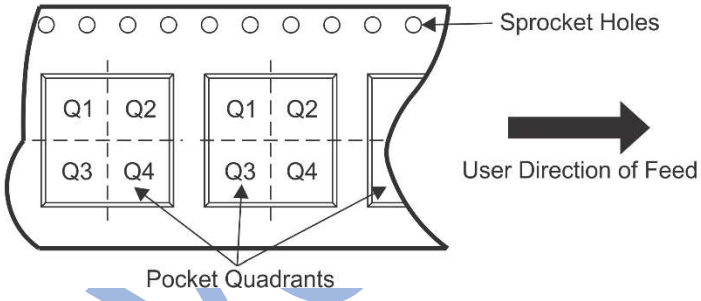


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LGS53605A	QFN-24	QF	24	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

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