65V, 3A wide output range, low ripple, synchronous buck converter

Check for Samples: LGS54360

Characteristic

- Supports transient voltage of 80V
- Working input voltage range: 4.5V-65V
- Equipped with FM and EN enable functions
- Output voltage range: 1V-VIN
- Integrated upper and lower power transistors, maximum output current 3A
- Configurable operating frequency: 200KHz~2MHz
- Adaptive switching between CCM/DCM/PFM modes
- Internal loop compensation simplifies system design
- Support high load capacitor startup
- Protection function: UVLO/OCP/SCP/OTP
- The junction temperature range is -40 ℃ to+125 ℃
- All ports have ± 2000V (HBM) ESD protection
- Provide enhanced heat dissipation ESOP-8 package

Application

- Industrial control system power supply
- Wide voltage input range power supply
- Low ripple and low-noise power supply

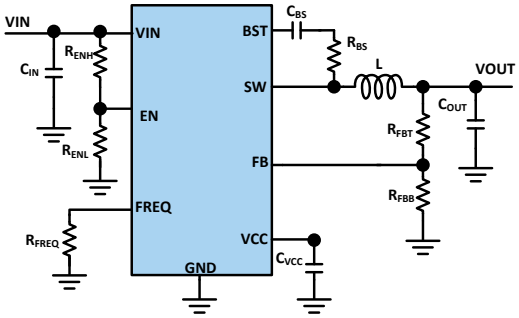


Figure 1 Typical Application Topology

Description

LGS54360 is a step-down DC/DC regulator with integrated upper and lower power Mos transistors, featuring SKIP control mode. It combines low static current with high switching frequency to achieve efficient voltage regulation over a wide range of load currents. SKIP mode uses short "burst" cycles to switch inductor current through internal power MOSFETs, followed by a sleep cycle in which the power switch is turned off and the load current is provided by the output capacitor. At light loads, the sudden cycle accounts for a small portion of the total cycle time, minimizing the average power supply current and greatly improving efficiency at light loads.

The LGS54360 has a wide input voltage range of 4.5V-65V, minimizing the need for external surge suppression components. Make it an ideal choice for industrial and high cell count battery pack applications with a wide input power range.

LGS54360 has a low resistance 130m Ω high side and 95m Ω low side power transistor, which can provide a maximum output current of 3A and has excellent load and line transient response.

LGS54360 can adjust a wider range of output voltages, making it suitable for various application environments. This voltage regulator is very suitable for the 48V power bus range. Additional features include: soft start, hot shutdown, UVLO undervoltage lock, maximum duty cycle limit timer, and intelligent current limit shutdown timer. And integrates output short-circuit protection, providing HICCUP mode when FB voltage is low to avoid overheating during short circuit.

Purchase Guide

Part	Package	Top Mark
LGS54360	ESOP-8	54360 YW

YW: Factory Version

Application Information: Typical Application Circuits

Full functional application circuit diagram

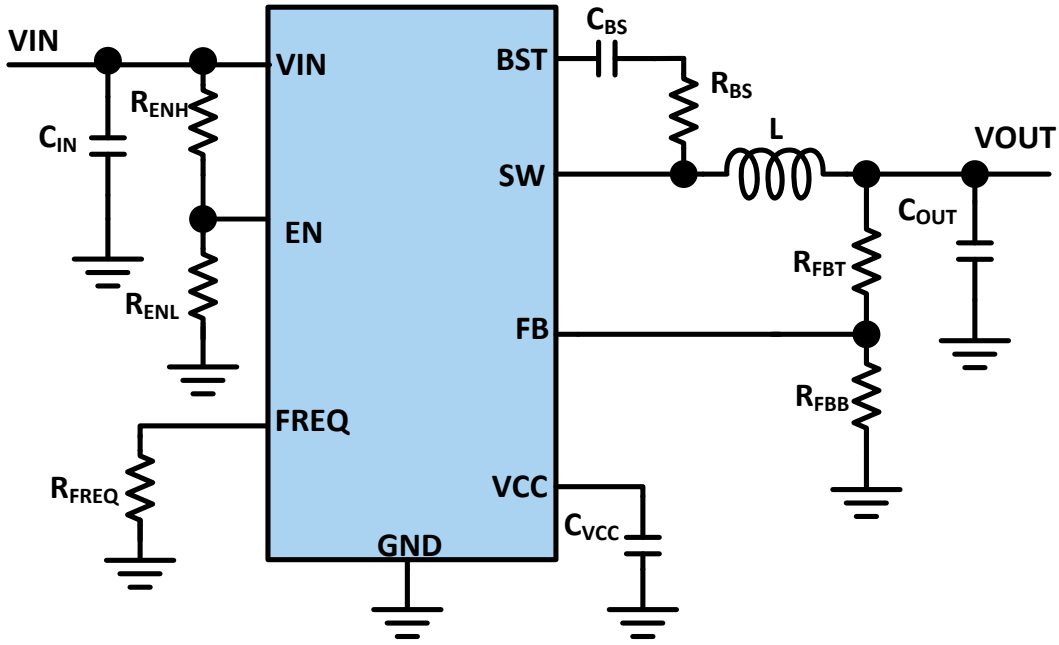


Figure 2 Typical application topology of DC-DC buck mode

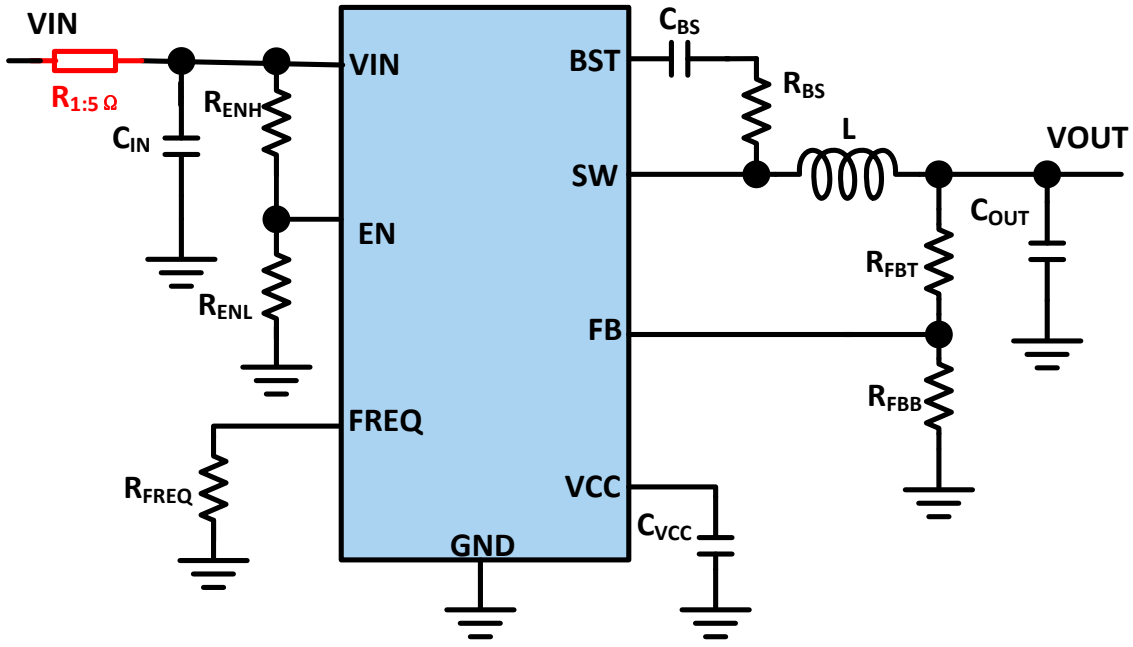


Figure 3: Topology of DC-DC buck mode hot swappable application

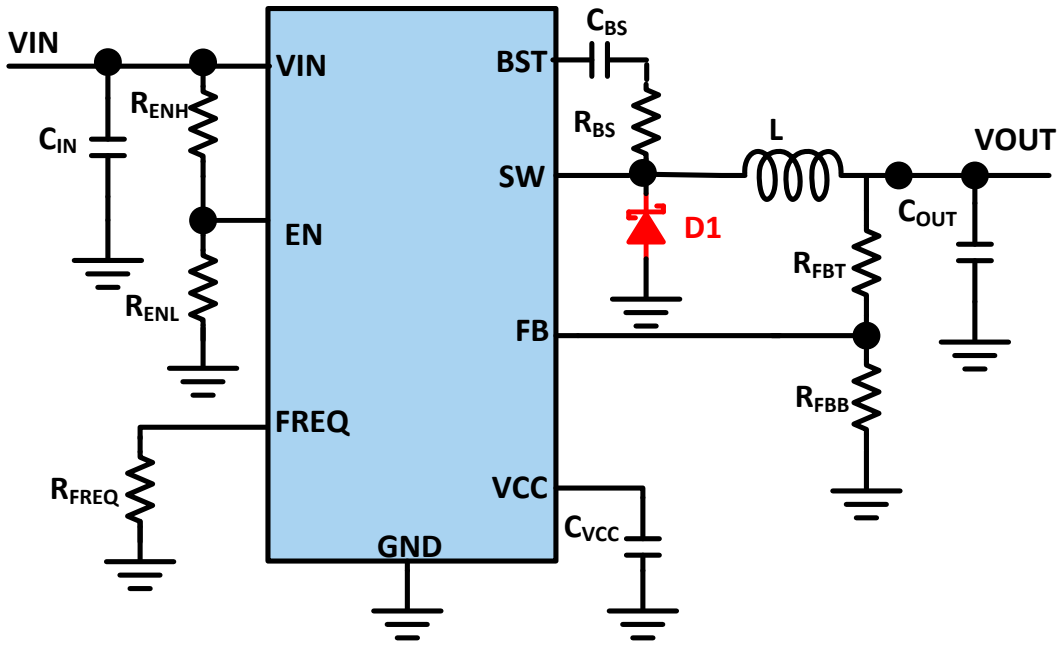


Figure 4: Topology of DC-DC Input High Voltage and High Current Application

NOTE:

(1) It is recommended to use X7R or X5R ceramic capacitors with a capacitance of 10uF or higher for input, and try to be as close as possible to the power input VIN and GND.

(2) C_{BST}, please choose ceramic capacitors with a withstand voltage of 16V or higher, and try to be as close as possible to the SW and BST pins.

(3) C_{VCC}, please choose ceramic capacitors with a withstand voltage of 10V or above, and try to be as close as possible to the VCC and GND pins.

(4) RBS recommends selecting resistors above 0.5 Ω, with a maximum resistance not exceeding 1 Ω.

(5) D1 recommends selecting Schottky diodes with low conduction voltage drop to further reduce chip heating in response to the issue of chip heating under high input voltage and high current conditions.

Reference Material List

Table 2

Reference number	descriptions	Manufacturer's serial number	Manufacturer	illustration
C_{IN}	4.7uF/100V, 1206, X7S	GRM31CC72A475KE11L	muRata	Please refer to Table 3 for the use of output inductors and capacitors
C_{OUT}	47uF/16V, 1210, X5R	GRM32ER61C476KE15L	muRata	
C_{BS}	470nF/50V, 0805, X7R	CC0805KKX7R8BB474	YAGEO	
C_{VCC}	2.2uF/16V, 0603, X5R	CL10A225KO8NNNC	SAMSUNG	
R_{FBT}	1MΩ			
R_{FBB}	432kΩ			
R_{ENH}, R_{ENL}	100kΩ			
R_{FREQ}	162kΩ			
L	10μH			
D1	60V 3A 420mV@3A	PMEG6030EVPX		

Application Information: Typical Application Circuits

Table 3. Typical Application External Device Table

R_{FREQ}(kΩ)	V_{OUT}(V)	V_{IN_Range} (V)	C_{OUT}(uF)(3)	L(uH)(2)	R_{FBT}(kΩ)	R_{FBB}(kΩ)
Fs=2MHz						
18.7kΩ	3.3	4-15(1)	47	2.2	1000	432
	5	5-24(1)	47	2.2	1000	249
	12	12-65(4)	22	8.2	1000	90.9
	24	24-65(4)	22	15	1000	43.2
Fs=1MHz						
64.9kΩ	1	4-9(1)	100	2.2	Short	Open
	3.3	4-30(1)	100	6.8	1000	432
	5	5-65	100	8.2	1000	249
	12	12-65	22	18	1000	90.9
	24	24-65	22	27	1000	43.2
Fs=400kHz						
200kΩ	1	4-21(1)	200	4.7	Short	Open
	3.3	4-65	100	10	1000	432
	5	5-65	100	10	1000	249
	12	12-65	22	22	1000	90.9
	24	24-65	22	47	1000	43.2

Note:

(1) The maximum input voltage is limited by the minimum conduction time T_{ON_SIN}.

(2) The calculation of inductance value is based on the typical value VIN=24V.

(3) All C_{OUT} capacitance values are after derating, and more capacitors need to be added when using ceramic capacitors.

(4) At high frequencies, due to temperature protection limitations, it may not be possible to provide full load current at higher voltages.

Absolute maximum (†)

Table 4.1

Parameter	range
Pin to GND voltage (VIN, SW, EN)	-0.3V~80V
Pin to SW voltage (BST)	-0.3V~5.5V
Pin to GND voltage (FB, FREQ, VCC)	-0.3V~5.5V
storage temperature	-65℃ to 150℃
Work completion temperature	-40℃ to 150℃

† Note: If the operating conditions of the device exceed the "absolute maximum value" mentioned above, it may cause permanent damage to the device. This is only a limit parameter, and it is not recommended for the device to operate at or beyond the limit values mentioned above. Long term operation of the device under extreme conditions may affect its reliability.

ESD level

Table 4.2

Parameter	Range
ESD rating (HBM)	±2KV
ESD rating (CDM)	±1KV

ESD warning

ESD (electrostatic discharge) sensitive devices.
Charged components and circuit boards may discharge without being noticed. Although this product has patented or proprietary protection circuits, the device may be damaged in the event of high-energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid device performance degradation or functional loss.

Recommended operating conditions

Table 4.3

Parameter	Range
VIN	4.5V~65V
EN	-0.3V~65V
FB	-0.3V~1.1V
Output voltage VOUT	1V~VIN
Output current IOUT	0A~3A
Work completion temperature	-40℃ to 125℃

Pin arrangement

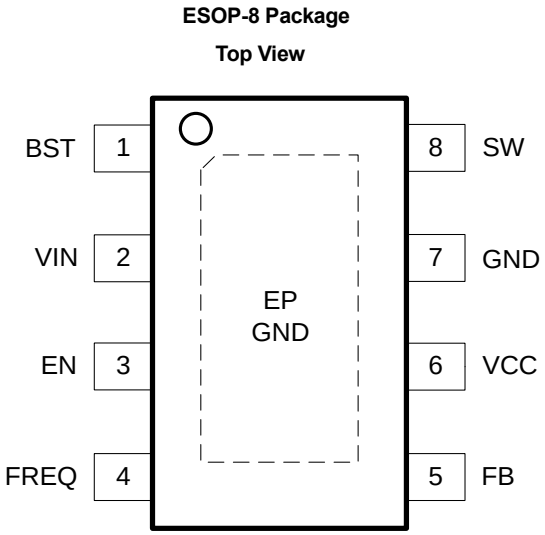


Figure 5 Packaging and Pin Arrangement

Pin function

Table 5 Pin Function Description

Pin Numbering	Pin Name	Description
1	BST	Self driving power supply. A high-quality ceramic capacitor with a capacitance of at least 100nF needs to be connected between BST and SW to bias the internal high-voltage side gate driver.
2	VIN	Input power pin. Internally connected to the upper bridge power MOSFET and VIN linear power supply. One or more decoupling ceramic capacitors must be connected between VIN and GND, as close as possible to the pins.
3	EN	Voltage regulator output enable pin, set high enable output. VIN can be set for undervoltage protection by configuring external resistor voltage divider.
4	FREQ	The working frequency setting pin of the voltage regulator is connected to a suitable resistor between FREQ and GND, which can adjust the switching frequency from 200KHz to 2MHz.
5	FB	Output voltage feedback pin. By configuring the voltage divider ratio between VOUT and GND, the output voltage can be adjusted.
6	VCC	To provide power supply for internal control circuits, a 1uF~4.7uF ceramic decoupling capacitor must be connected between VCC and GND, as close as possible to the chip pins.
8	SW	Internal power switch node. External connection of power inductor and CBST capacitor.
7,EP	GND	Metal heat sink, used as GND.

Technical specifications

Unless otherwise specified, the limit values apply to the working junction temperature (TJ) range of -40 ℃ to+125 ℃. The minimum and maximum limits are specified through experimentation, design, or statistical correlation. The typical value represents the most likely parameter specification at TJ=25 ℃, for reference only. All voltages are relative to GND.

Table 6 Parameter Indicators

Parameter		**Test conditions**	MIN	TYP	MAX	Unit
Input Characteristic						
V_{IN}	Recommended input voltage range		4.5		65	V
V_{IN_GD}	VIN undervoltage protection threshold	Rising		4		V
		Falling		3.6		V
I_Q	VIN equivalent static current	V_{IN}=24V, V_{FB}=1.2V No switch		130		uA
VCC characteristics						
V_{CC}	VCC output voltage	VIN=24V	4.8	5.0	5.2	V
V_{CC_GD}	VCC undervoltage protection	Rising		3.5		V
		Falling		3.2		V
I_{SC_VCC}	VCC short-circuit current (VIN power supply)	VIN=24V		20		mA
FB pin						
V_{FB_acc}	FB feedback voltage		0.99	1.0	1.01	V
V_{FB_skip}	FB jump cycle threshold			1.003		V
I_{FB_leak}	FB leakage current			80		nA
PWM related						
R_{DS_HS} (1)	Upper pipe RDSON	T_J= 25℃		130	160	mΩ
R_{DS_LS} (1)	Lower pipe RDSON	T_J= 25℃		95	130	mΩ
I_{Peak_HS}	Upper tube current limit			3.7		A
I_{Peak_LS}	Lower tube current limit			3.3		A
I_{ZCD}	Zero crossing of lower tube current			50		mA
$I_{SW.LKG}$	SW leakage current				1	uA
F_{SW}	Switching frequency accuracy	PWM Operation R_{FREQ} = 162k	0.9	1.0	1.1	MHz
F_{SW_range}	Switching frequency range	with 1% R_{FREQ}	0.2		2.0	MHz
$T_{HSON.MIN}$ (2)	Minimum conduction time of upper tube			90		ns
$T_{LSON.MIN}$ (2)	Minimum conduction time of the lower tube			160		ns
T_{SCP_HOLD}	Short circuit protection triggering time			5		ms
T_{SCP_HICCUP}	Short circuit protection hiccup waiting time			4		ms
EN pin						
V_{EN_H}	EN high logic threshold		1.1			V
V_{EN_L}	EN low logic threshold				0.5	V
$V_{EN\_UV\_R}$	EN undervoltage protection rising edge		1.19	1.2	1.21	V
$V_{EN\_UV\_F}$	EN undervoltage protection falling edge		1.14	1.15	1.16	V
I_{LKG-EN}	EN input current	EN < 65V			1	uA
Global thermal protection characteristics (2)						
T_{OTP-R}	Over Temperature Protection	T_J Rising		160		℃
T_{OTP-F}	Over temperature protection released	T_J Falling		145		℃
Thermal resistance coefficient (2)						

θ_{JA}	Thermal resistance coefficient from silicon core to surrounding air	0 LFPM Air Flow		42.9		℃/W
θ_{JB}	Thermal resistance coefficient from silicon core to PCB board surface			13.6		℃/W
θ_{JCtop}	Thermal resistance coefficient from silicon core to packaging surface			54		℃/W
Ψ_{JB}	Thermal resistance coefficient from silicon core to PCB board surface			13.8		℃/W

(1) Test on the packaging pins.

(2) Design assurance. Without production testing.

Typical characteristics

Unless otherwise specified, the testing condition is VIN=24V, VOUT=5V, FS=400kHz, L=10μH, COUT=100μF.

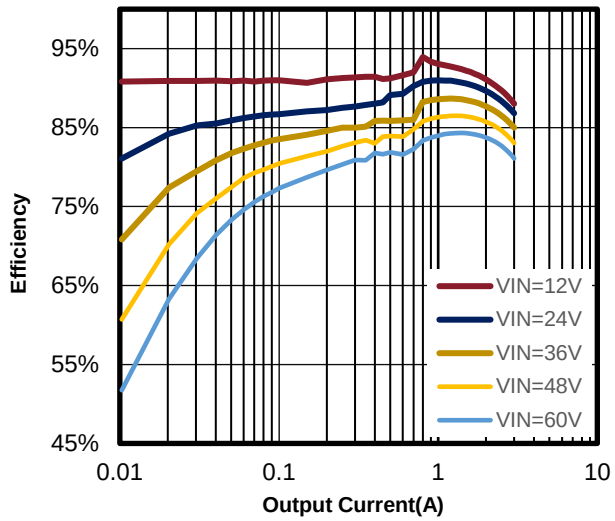


Figure 6 Fs=400kHz efficiency

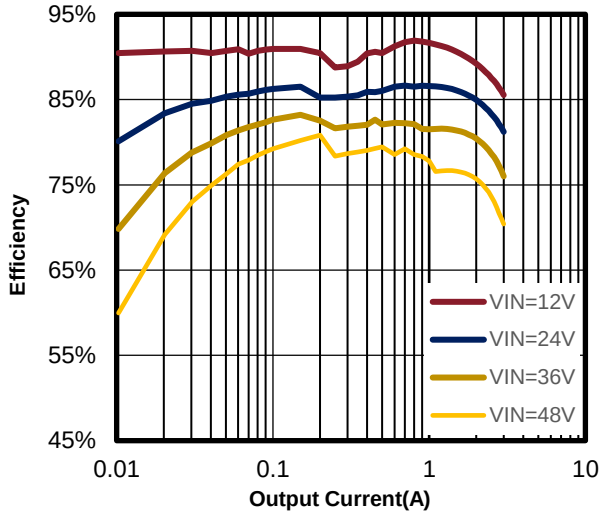


Figure 7. Fs=1MHz efficiency

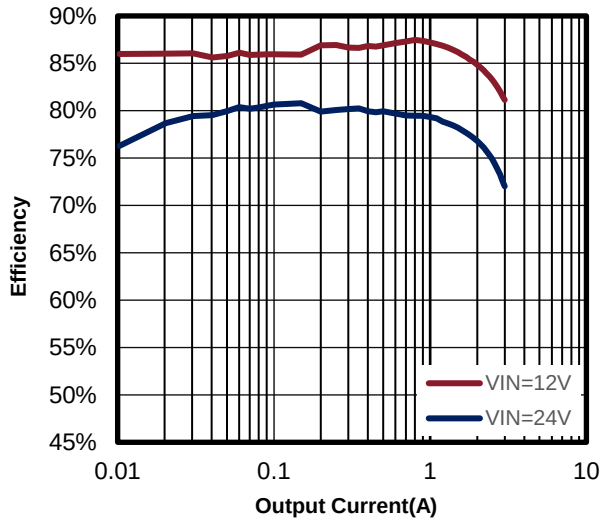


Figure 8 Fs=2MHz efficiency

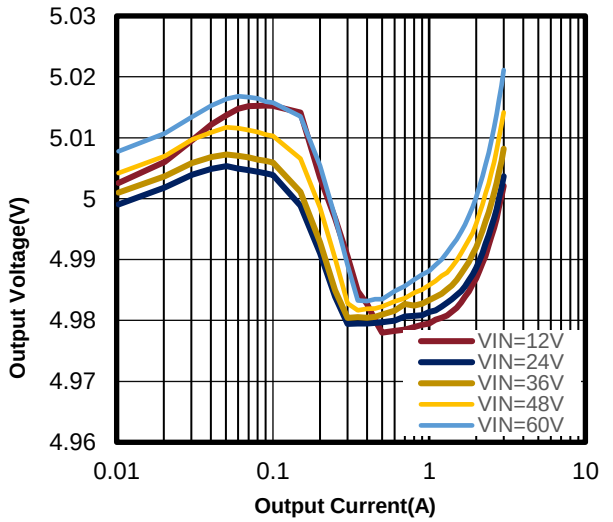


Figure 9 Fs=400kHz VOUT characteristics

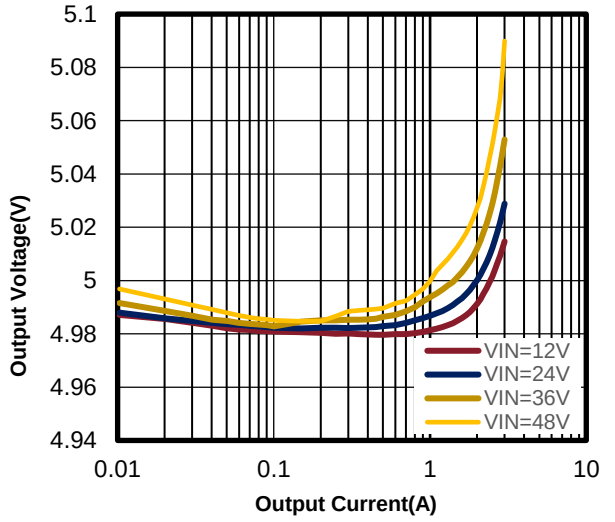


Figure 10 Fs=1MHz VOUT characteristics

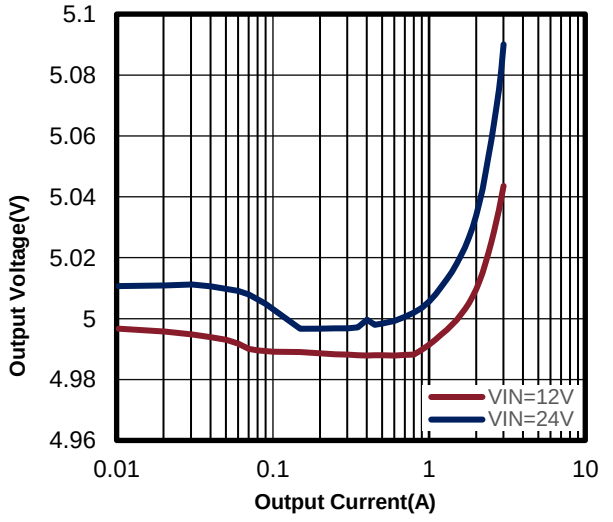
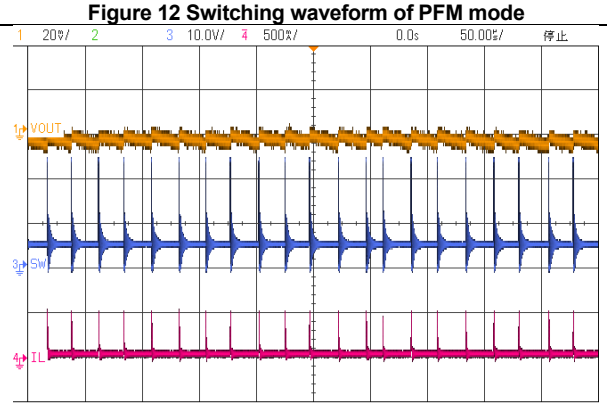


Figure 11. Characteristics of Fs=2MHz VOUT

Typical characteristics

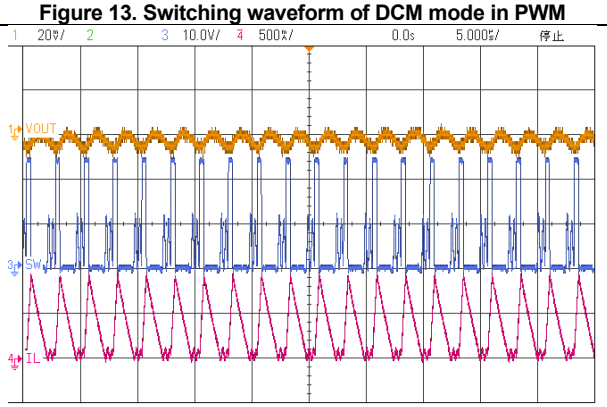
Unless otherwise specified, the testing condition is VIN=24V, VOUT=5V, FS=400kHz, L=10μH, COUT=100μF.

Figure 12 Switching waveform of PFM mode



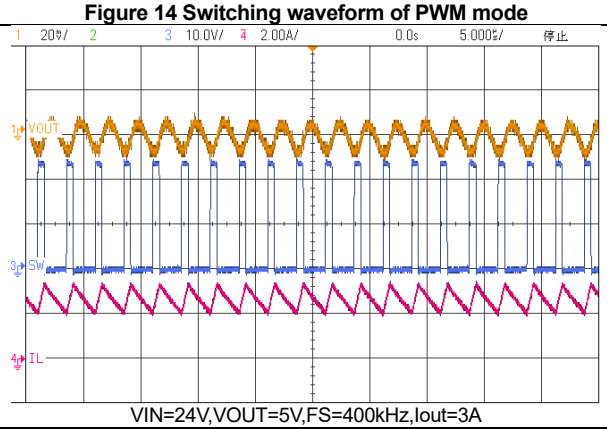
VIN=24V,VOUT=5V,FS=400kHz,Iout=10mA

Figure 13. Switching waveform of DCM mode in PWM



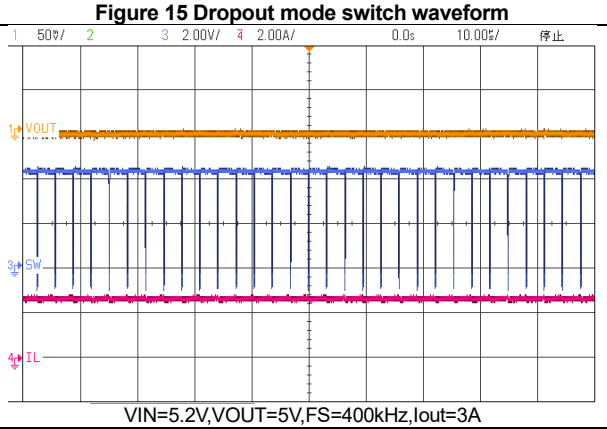
VIN=24V,VOUT=5V,FS=400kHz,Iout=300mA

Figure 14 Switching waveform of PWM mode



VIN=24V,VOUT=5V,FS=400kHz,Iout=3A

Figure 15 Dropout mode switch waveform

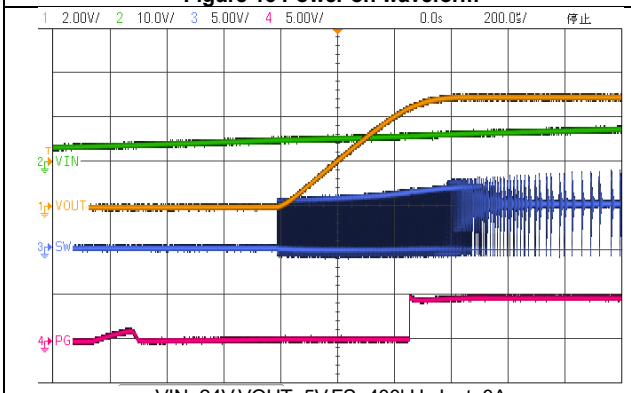


VIN=5.2V,VOUT=5V,FS=400kHz,Iout=3A

Typical characteristics

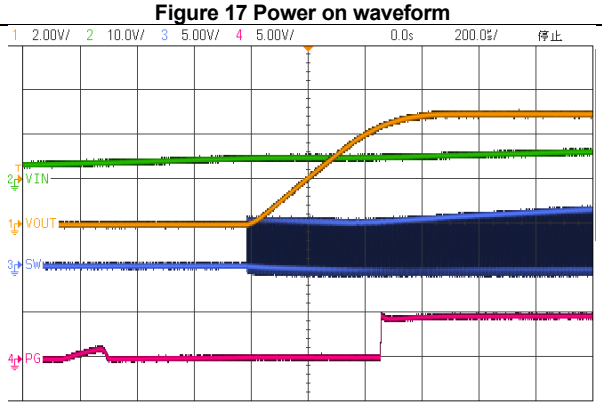
Unless otherwise specified, the testing condition is VIN=24V, VOUT=5V, FS=400kHz, L=10μH, COUT=100μF.

Figure 16 Power on waveform



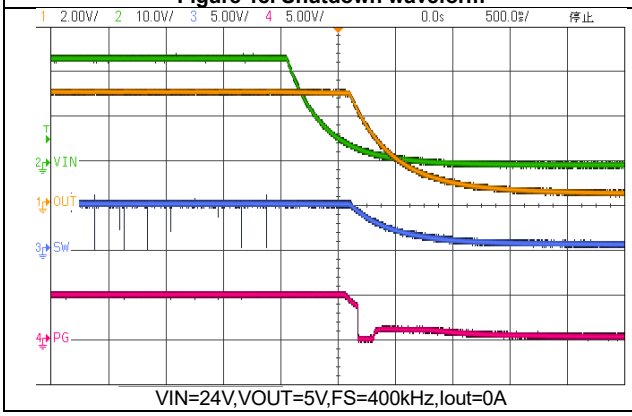
VIN=24V,VOUT=5V,FS=400kHz,Iout=0A

Figure 17 Power on waveform



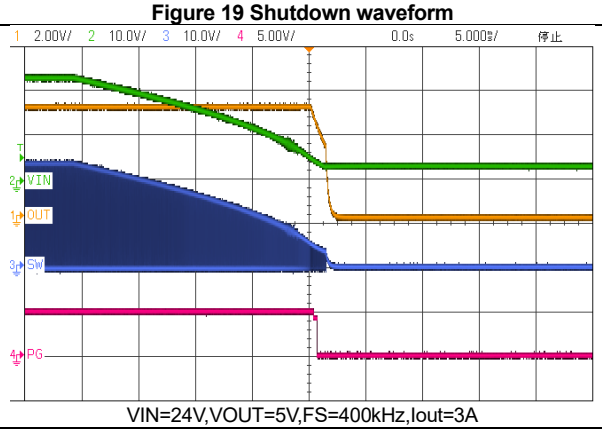
VIN=24V,VOUT=5V,FS=400kHz,Iout=3A

Figure 18. Shutdown waveform



VIN=24V,VOUT=5V,FS=400kHz,Iout=0A

Figure 19 Shutdown waveform



VIN=24V,VOUT=5V,FS=400kHz,Iout=3A

Typical characteristics

Unless otherwise specified, the testing condition is VIN=24V, VOUT=5V, FS=400kHz, L=10μH, COUT=100μF.

Figure 20. Pre charging voltage startup

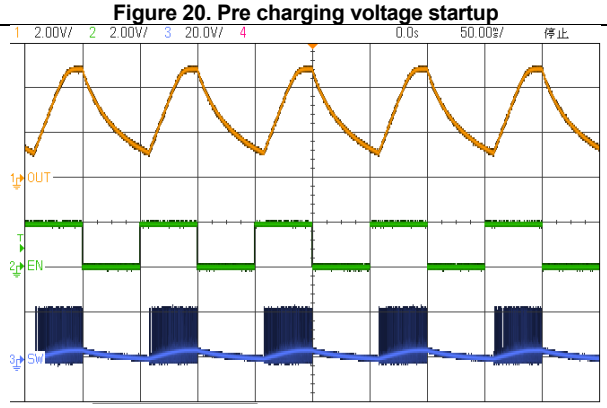
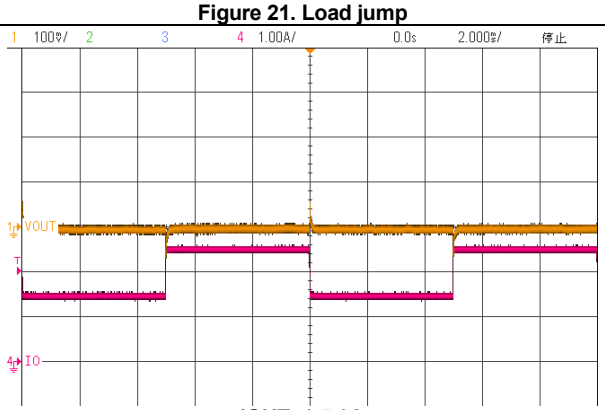
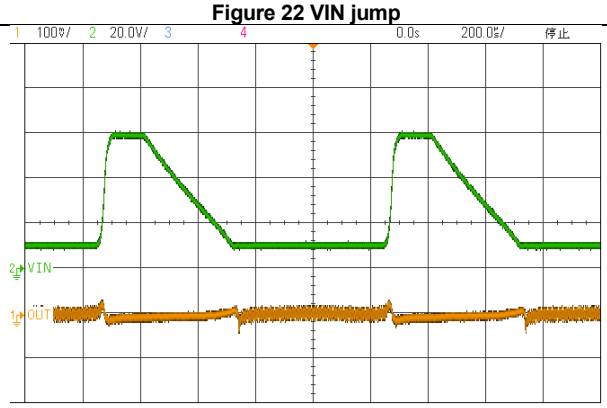


Figure 21. Load jump



IOUT=1.5-3A

Figure 22 VIN jump



VIN=12V-60V

Figure 23 Output short circuit and Hiccup mode

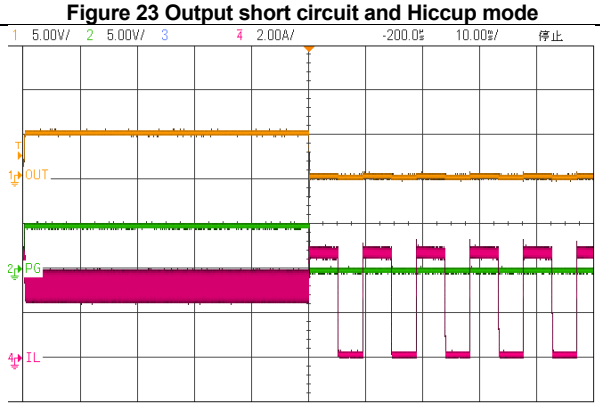
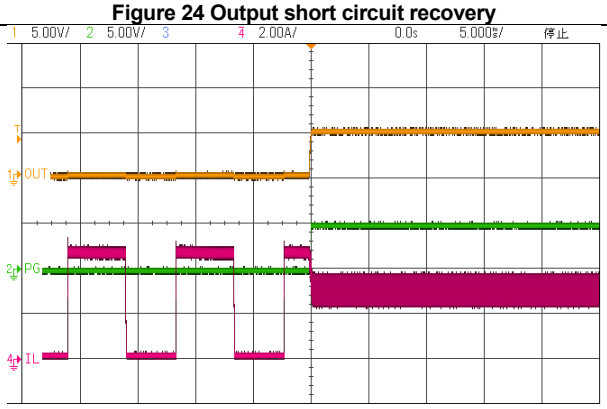


Figure 24 Output short circuit recovery



Functional Block Diagram

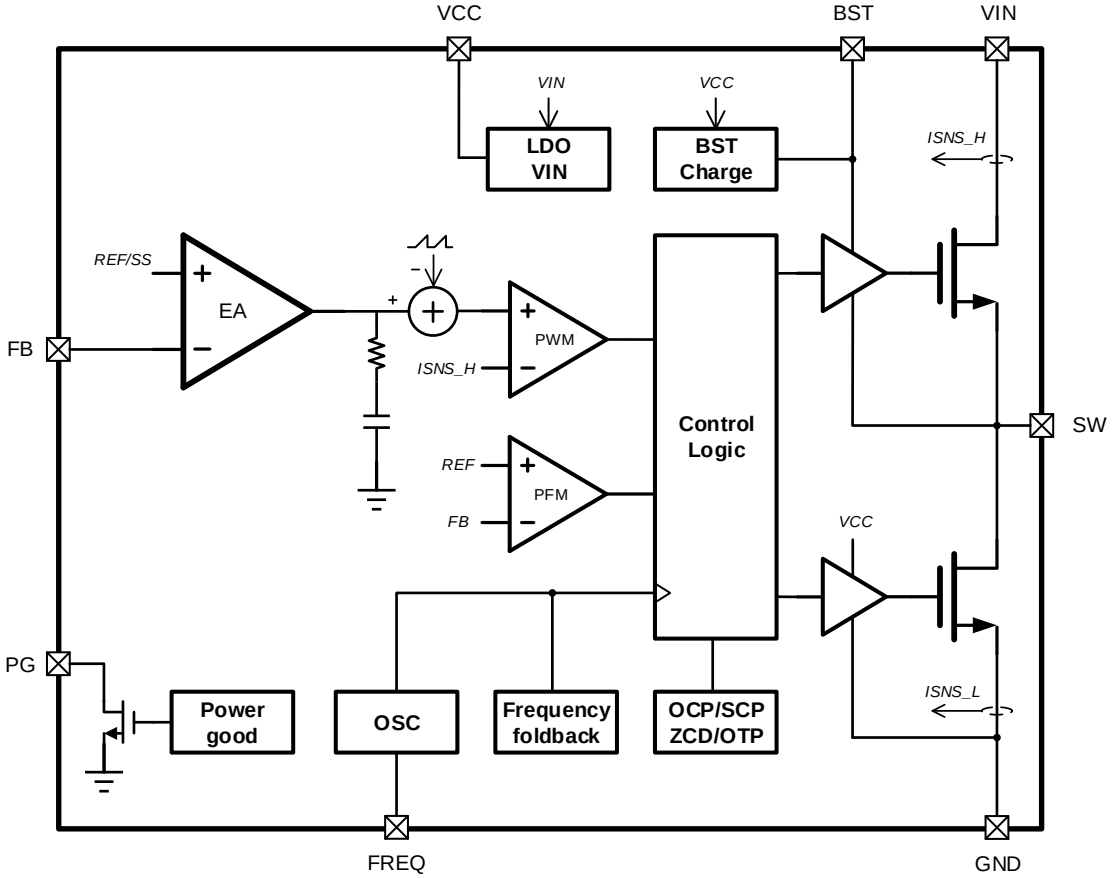


Figure 25 Internal functional block diagram

Application information: High efficiency step-down switching regulator

Overview

LGS54360 is a high-efficiency, high power density synchronous buck converter. The input voltage range of this chip is 4.5V to 65V, and it integrates upper and lower power MOS transistors internally, which can output a load current of up to 3A. And it can provide a stable output voltage from 1V to VIN.

The LGS54360 features SKIP control mode, which combines low static current with high switching frequency to achieve high efficiency over a wide range of load currents. Adopting a fixed frequency peak current control mode with integrated internal compensation to shorten design time and require fewer external components. LGS54360 adjusts the switching frequency through an external resistor, with a range of 200kHz~2MHz. The wide switching frequency range allows the chip to be optimized according to different needs, adapting to small volume requirements at higher frequencies or high-efficiency power supplies at lower frequencies. In addition, LGS54360 can operate at nearly 100% maximum duty cycle to achieve maximum input-output pressure difference as much as possible.

LGS54360 also provides various other functions, including external resistor regulation of output voltage and a good power indicator. The protection functions include periodic peak current and valley current limits, output short-circuit protection in hiccup mode, thermal shutdown and self recovery, and precise input undervoltage protection.

Internal LDO linear power supply

LGS54360 integrates an LDO linear power supply internally, providing VCC power for control circuits and MOSFET drivers. The nominal voltage of VCC is 5V, and this pin must be connected to GND as close as possible through a 1uF-4.7uF ceramic decoupling capacitor.

Output voltage VOUT and FB pin

The voltage regulation circuit of LGS54360 will adjust the FB voltage to be the same as the internal reference voltage. The output voltage can be adjusted by changing the resistance ratio between the upper voltage divider resistor R_{FBT} and the lower voltage divider resistor R_{FBB}. Please connect the resistive voltage divider between the output node and ground, with the midpoint connected to the FB pin. The steady-state voltage of V_{FB} is usually 1V. R_{FBB} can be calculated using the following formula:

$$R_{FBB} = (\frac{V_{FB}}{V_{OUT} - V_{FB}}) \times R_{FBT}$$

The choice of R_{FBB} depends on the application environment. A larger voltage divider resistor can reduce the current flowing through the voltage divider network, but an excessively large resistance value can make the feedback loop more susceptible to noise. It is recommended that the maximum R_{FBB} value not exceed 1M Ω. Large precision errors and temperature coefficients can affect the control accuracy of output voltage. It is recommended to use resistors with precision errors not exceeding 1% and temperature coefficients less than 100ppm.

The feedback loop should be kept away from PCB noise interference, and the PCB layout reference can be referred to in the following text.

BST and SW pins

LGS54360 requires a small ceramic capacitor to be added between the BST and SW pins to provide gate driving voltage for the high side MOSFET. When the high side MOSFET is turned off and the low side MOSFET is turned on, the C_{BST} capacitor charges. The ceramic capacitor is recommended to use 0.47uF and be connected between BST and SW for normal operation. It is recommended to use X7R or X5R grade dielectric ceramic capacitors as they have stable temperature and voltage characteristics. The rated voltage of ceramic capacitors should be 16V or higher.

Application information: High efficiency step-down switching regulator

Switching frequency and FREQ pin

The switching frequency of LGS54360 can be determined by the external resistor R_{FREQ} connected between the FREQ pin and GND, with an adjustment range between 200kHz and 2.5MHz. R_{FREQ} can be calculated using the following formula:

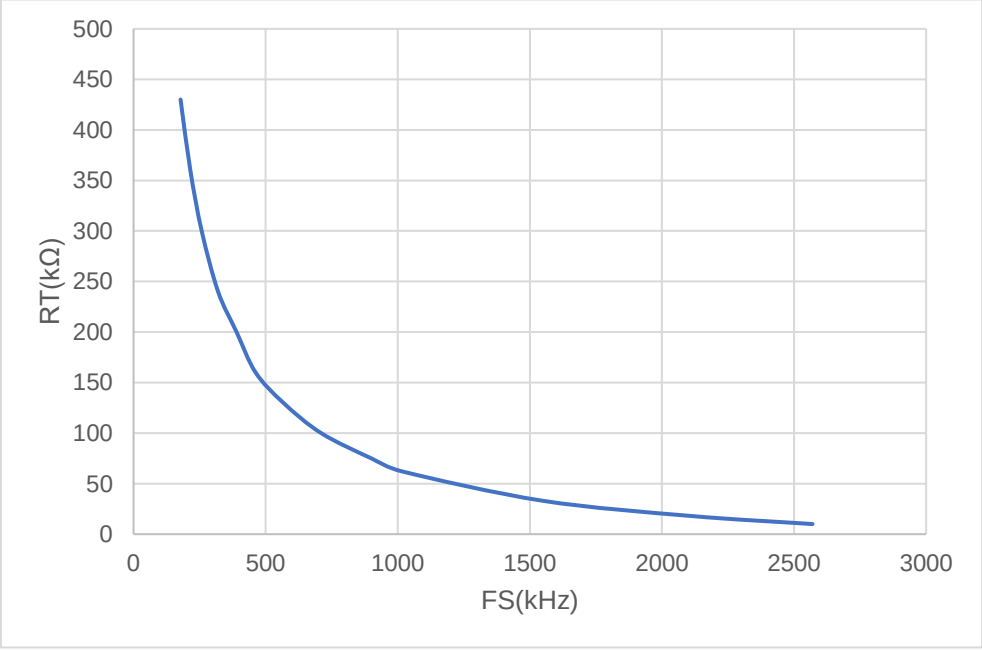
$$R_{FREQ}(k\Omega) = \frac{81053}{Fs(kHz)} - 21$$

For common switching frequencies, the setting of R_{FREQ} can refer to the following table

Table 7

R_{FREQ}(kΩ)	Fs(kHz)
10	2500
18.7	2000
33	1500
64.9	1000
160	500
200	400
470	200

The relationship curve between RFREQ resistance and switching frequency is shown in the following figure



Low Drop Out mode

When the input voltage approaches the set output voltage, LGS54360 will enter Low Drop Out mode. At this time, the single cycle conduction time of the high side power transistor is allowed to exceed the set switching period, and the conduction time will automatically adjust with the input voltage to maintain control over the output voltage. When the input voltage is lower than the set output voltage, the maximum conduction time of the high side power transistor is limited to $T_{HSON\ MAX}$， At this time, the low side power transistor will briefly conduct $T_{LSON\ MIN}$ is used to charge C_{BST}. Ensure that CBST has sufficient voltage to maintain the normal operation of the high side power transistor drive circuit.

Application information: High efficiency step-down switching regulator

Overcurrent protection and short circuit protection

LGS54360 prevents overcurrent situations by limiting the peak and valley values of inductor current on a periodic basis. If the overcurrent situation persists, it will trigger the hiccup mode to prevent the chip from overheating.
The overcurrent protection of high side MOSFET is achieved through the characteristics of peak current control mode. The output of the error amplifier is compared with the sampled high side power transistor current after subtracting the ramp compensation for each switching cycle. Please refer to the functional block diagram for details. Therefore, the peak current of the high side power transistor is constrained by the maximum output of the error amplifier, thereby achieving the ability to limit the peak current cycle by cycle.
During the conduction period of the low side MOSFET, LGS54360 detects the current of the low side power transistor and compares it with the valley current limit threshold. When the current of the low side power transistor exceeds the valley current limit threshold, the high side power transistor will not be allowed to conduct until the low side power transistor is below the valley current limit threshold.
When the high side power transistor current triggers the error amplifier limit and the power supply normal indicator flag is pulled down, LGS54360 will enter Hiccup mode. At this point, the chip will turn off the output and maintain it for 5ms before attempting to restart. If the overcurrent or short-circuit fault state still exists, repeat hiccups until the fault state ends. Hiccup mode reduces power consumption under severe overcurrent or short circuit conditions, preventing damage to the chip caused by overheating.

Over Temperature Protection

The thermal overload protection circuit limits the junction temperature to below 160 ℃ (typical value). Under extreme conditions (high ambient temperature and/or high power consumption), when the junction temperature starts to rise above 160 ℃, the over temperature protection is activated and the system will forcibly shut down the regulator output. When the junction temperature drops below 145 ° C, the OTP state will be unlocked, the regulator output will restart, and the output current will return to normal operating value. Thermal overload protection aims to protect devices from the effects of momentary accidental overload conditions.
The guaranteed operating junction temperature range of this device is -40 ° C to 125 ° C. High junction temperature will reduce the working life; When the junction temperature remains high at 125 ° C for a long time, the lifespan of the device will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions, circuit board layout, rated package thermal resistance, and other environmental factors.

The junction temperature (T_J, unit: ℃) is calculated based on the ambient temperature (T_A, unit: ℃) and power consumption (P_D, unit: W), using the following formula:

$$\boldsymbol{T_J = T_A + (P_D \times \theta_{JA})}$$

Among them, θ_{JA} (unit: ℃/W) is the thermal resistance of the package.

Input undervoltage lock

There is an internal undervoltage lockout circuit on the VIN pin of the device. When the VIN voltage drops below the threshold of UVLO, UVLO protection will be triggered and the regulator output will be turned off. The rising threshold of UVLO is about 4V, and when VIN reaches this voltage and UVLO is removed, the chip will enter the soft start process.

SKIP pulse skipping mode

LGS54360 has a built-in pulse circuit; When under light load, the circuit is turned on; Only switch when necessary to maintain the output voltage within the specified range. This can reduce switch losses and allow the driver to maintain high efficiency under light load conditions.

In pulse skipping mode, when the output voltage drops below the specified value, LGS54360 enters PWM mode and stays for several oscillator cycles to raise the output voltage to the specified range. During the waiting time between sudden pulses, the power switch is turned off and all load currents are provided by the output capacitor. Due to the periodic sudden drops and recovery of the output voltage, the ripple of the output voltage in this mode is greater than that in the PWM working mode.

Application information: High efficiency step-down switching regulator

Hot dip safety

Ceramic capacitors have the advantages of small size, good stability, and low impedance, making them an ideal choice for input bypass capacitors in the LGS54360 circuit. But if LGS54360 is plugged into a live power source, these capacitors may cause problems. Ceramic capacitors with low ESR characteristics and stray inductance connected in series with the power supply form an "underdamped slot circuit". The voltage at the VIN pin of LGS54360 may reach twice the nominal input voltage, exceeding the rated value of LGS54360 and damaging the parts. If the input power control is improper or the user needs to plug the LGS54360 into a power source, the design of the input network should prevent this overshoot.

Figure 26A shows the waveform generated when the LGS54360 circuit is connected to a 65V power supply via a 6-foot (2m) 24AW twisted pair cable. The first figure shows the instantaneous response of a ceramic capacitor with a 10 μ input terminal. The input voltage is as high as 100V, and the peak input current is 10A.

One way to improve and prevent the impact of this problem is to add an RC absorption network in the circuit. Added a series resistor of 1 Ω and a 47 μ F input aluminum electrolytic capacitor in Figure 8c. The damping generated by the high equivalent series resistance of this capacitor can eliminate voltage overshoot. The additional capacitance improves the input ripple and can slightly increase the efficiency of the circuit, although it may be the largest component in the circuit.

Another solution is shown in Figure 6b. A 5 Ω resistor is connected in series with the input to eliminate voltage overshoot (which also reduces peak input current). This solution is smaller and cheaper than electrolytic capacitors. It is not recommended to add this circuit to prevent resistance damage caused by excessive current when the input current is higher than 0.5A, and the efficiency is low.

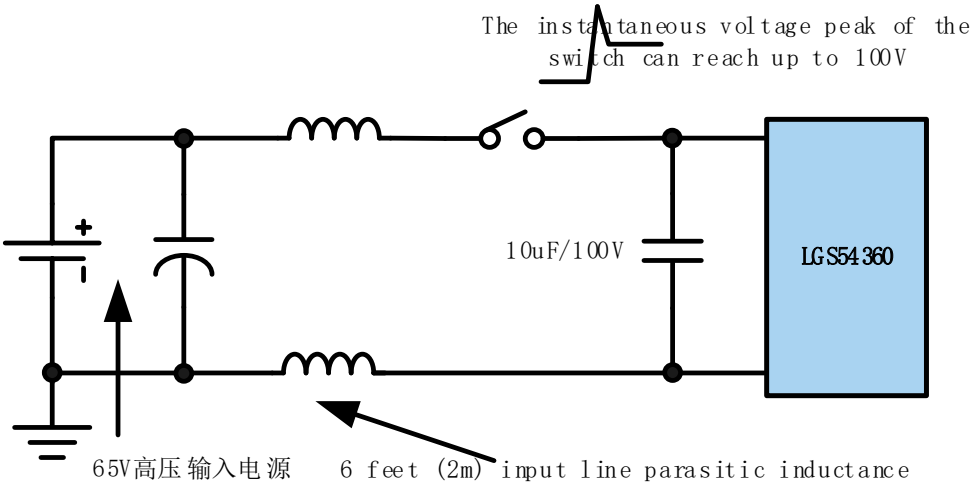


Figure 26 a. Schematic diagram of high-voltage hot plugging without filtering circuit

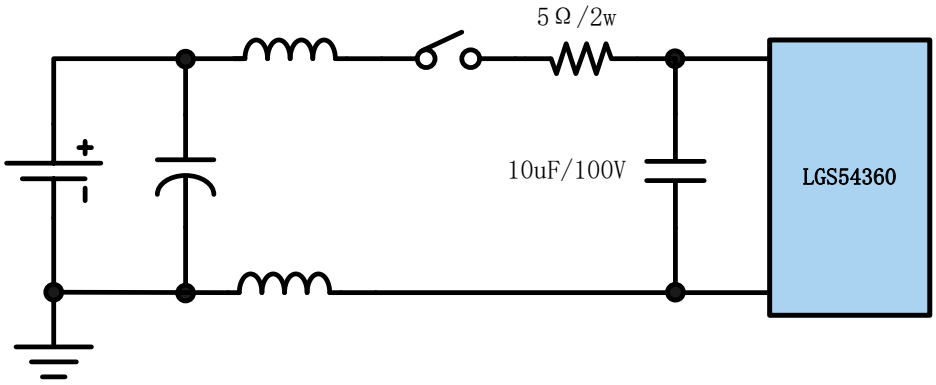


Figure 26 b. Schematic diagram of hot plugging in the case of a single resistor filter circuit

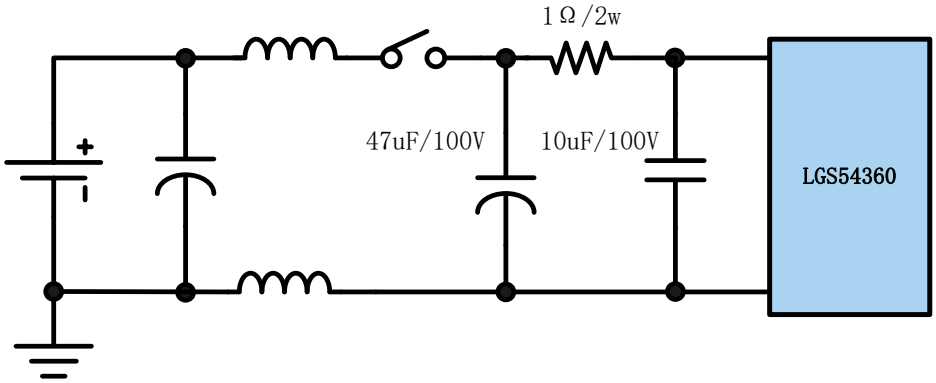


Figure 26 c. Schematic diagram of hot plugging under RC absorption network conditions

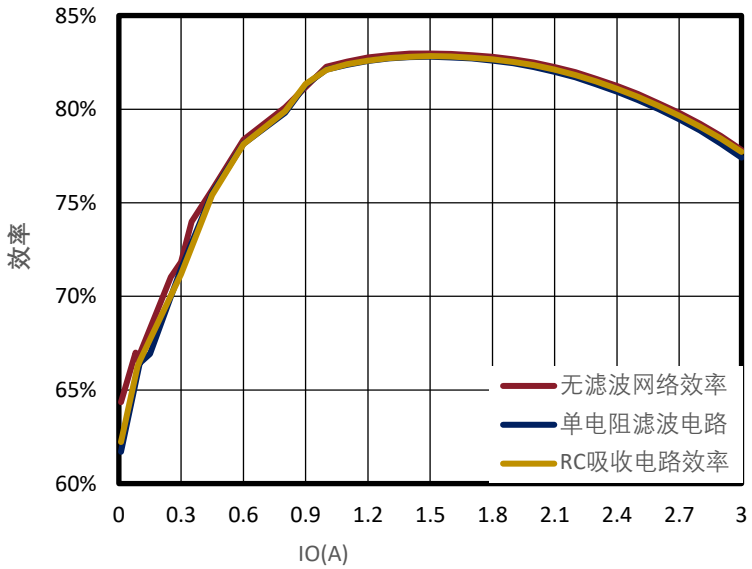


Figure 26 d. Comparison of 65V Input to 5V Efficiency

Application Information: Device Selection Suggestions and Calculations

Output setting voltage

The output voltage VOUT is determined by the dividing resistor between VOUT and GND on the FB pin, and the resistance value can be selected according to the following equation:

$$R_{FBB} = (\frac{V_{FB}}{V_{OUT} - V_{FB}}) \times R_{FBT}$$

VFB is the internal reference voltage. The upper voltage divider resistor R_{FBT} is generally selected with a resistance not greater than 1M Ω. A resistance value that is too large will weaken the anti-interference ability of the feedback circuit, while a resistance value that is too small will increase the static current and reduce the light load efficiency.

Set switch frequency resistor

The switching frequency Fs is determined by the external resistance RT between the FREQ pin and GND. The RT resistance can be calculated using the following formula, and it is recommended to use a 1% precision resistor.

$$R_T(k\Omega) = \frac{81053}{Fs(kHz)} - 21$$

Input capacitor selection

In typical application scenarios, it is recommended to use ceramic capacitors made of 4.7uF-10uF X7R or X5R materials, which need to have sufficient rated voltage. To compensate for the derating caused by the DC bias of ceramic capacitors, it is recommended that the rated voltage be twice the maximum input voltage. It is also recommended to use small packaged capacitors as close as possible to the VIN and GND pins to absorb high-frequency switching noise, such as 0603 packaging and 0.1uF ceramic capacitors.

Inductance selection

The selection of inductance needs to consider the following aspects:

(1) Choose an inductor to provide the required current ripple. It is recommended to choose a current ripple of about 20% -40% of the current maximum output current, and the inductance calculation formula is as follows:

$$L = \frac{V_{OUT} \times \left(1 - V_{OUT}/V_{IN,MAX}\right)}{f_{SW} \times I_{OUT(MAX)} \times K}$$

Where $F_{\_SW}$ is the switching frequency, $I_{OUT\,(MAX)}$ is the LED current, and the constant K is the percentage of inductor current ripple.

For the majority of typical application circuits of LGS54360, the optimal selection range for inductance is 2.2 μ H to 15 μ H.

(2) To ensure circuit safety, it is necessary to choose an inductor with a saturation current rating greater than the peak current under full load conditions. It is recommended to choose an inductor with a saturation current that exceeds the peak current of the inductor by 30% to 40% during normal operation. The peak current of an inductor can be calculated according to the following formula:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(1 - V_{OUT}/V_{IN,MAX}\right)}{2 \times f_{SW} \times L}$$

Output capacitor selection

The LGS54360 allows for a wide range of output capacitor values. To ensure cost and small size, it is recommended to choose the appropriate output capacitor. In practical applications, the output capacitance directly affects the voltage overshoot/undershoot and output voltage ripple during the transient response of the output current. When the load undergoes transient changes, the output capacitor needs to provide charge before the loop regulation is completed. The transient voltage change value ΔV_{OUT} can be calculated by the following formula:

$$\Delta V_{OUT} = \Delta I_{OUT} * ESR$$

Where ΔI_{OUT} represents the jump value of the load current, and ESR is the equivalent series resistance value of the output capacitor.

The output voltage ripple is mainly composed of two parts: one is caused by the inductance current ripple flowing through the ESR of the output capacitor, and the other is caused by the inductance current ripple on the charging and discharging of the output capacitor.$\Delta V_{OUT-ripple} = \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}} + \Delta I_L \times ESR$

Where ΔI_L represents the inductor ripple current, and $F_{\_SW}$ represents the MOSFET switching frequency

In order to maintain a small output voltage overshoot or undershoot and reduce output ripple during transient changes, capacitors with large capacitance and small ESR are required, which also increases costs and volume. Choosing the appropriate output capacitor is crucial.

CVCC capacitor

The VCC pin is the output of the internal LDO of LGS54360, used for powering the internal control circuit of LGS54360 and driving two internally integrated MOSFETs. The input of this LDO comes from VIN (please refer to the internal functional diagram for details). To ensure voltage stability, it is recommended to place a 1uF-4.7uF ceramic capacitor as close as possible to the VCC and GND pins, with a recommended rated voltage of 10V or higher.

CBST capacitor

C_{BST} capacitor is a bootstrap capacitor used in LGS54360 applications for driving high side power transistors. To ensure voltage stability, it is recommended to place a 0.1uF-1uF ceramic capacitor with a rated voltage of 16V or higher in close proximity to the BST and SW pins.

PCB layout

Wiring principles

The performance of switch mode power supplies is closely related to PCB wiring. LGS54360 fully considers the optimization requirements of PCB wiring in the allocation of pin positions, such as placing VIN and GND pins adjacent to each other for convenient placement of VIN bypass capacitors. As shown in the figure below, the input current of the step-down switching power supply has a high di/dt change rate. This part of the current flows into the chip through the VIN pin during transient changes, passes through the upper bridge arm switch tube, passes through the lower bridge arm switch tube, and flows out of the chip through the GND pin. Placing high-frequency bypass capacitors closest to the VIN and GND pins to reduce the derivative inductance of this current loop is the most effective way to improve the performance of switching power supplies and reduce EMI pollution. In addition, the voltage on SW has a high dv/dt change rate, so when making PCB layouts, it is necessary to shorten the SW wiring as much as possible; Sensitive signal lines should be avoided from being too close to SW.

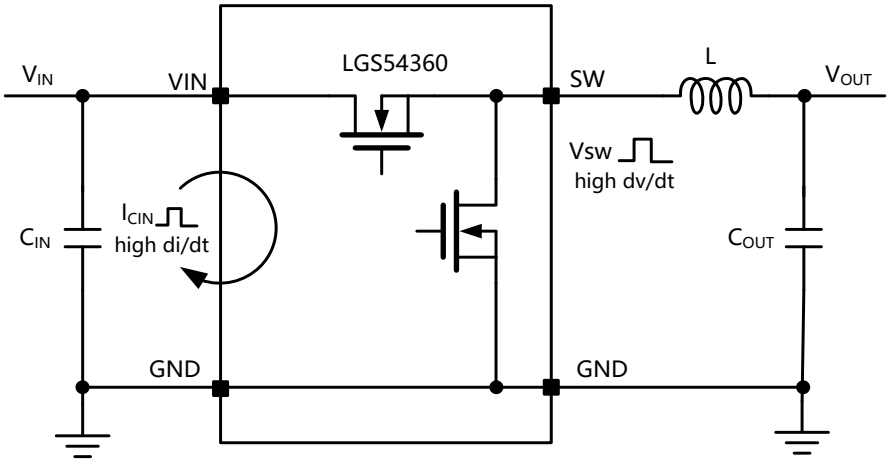


Figure 27. LGS54360 Simplified Application Circuit

To achieve optimal work efficiency, heat dissipation, and EMI performance, we recommend following the following basic rules on PCB wiring.

(1) High frequency bypass ceramic capacitors CIN are crucial and need to be placed near the VIN and GND pins of LGS54360 to minimize the loop area of high-frequency input current; According to the filtering requirements, if multiple input capacitors are needed, placing ceramic capacitors in small packages (such as 0603) closest to the pins can achieve the best effect of reducing high-frequency noise;

(2) The high current circuits of VIN, VOUT, and GND should be connected as wide and short as possible;

(3) The bypass capacitor of VCC should be arranged close to the pin and connected back to the GND pin of the chip with the shortest possible wire;

(4) It is recommended to use a 4-layer board, and the heat dissipation pads of LGS54360 are connected to each layer through array vias. And using the first intermediate layer as a geological layer can simultaneously serve the functions of heat dissipation and shielding; Each layer adopts the largest possible GND copper coating to achieve sufficient heat dissipation;

(5) The SW network contains a large amount of high-frequency noise, so the pin connections should be as short as possible and have sufficient width to conduct current;

(6) Sensitive analog signals, such as FB and FREQ, need to be kept away from SW and BST networks, and avoid being too close to inductors. It may be considered to arrange the wiring in shielding

(7) The way of signal layer below the layer;

(8) The feedback resistor connected to FB should be as close to the pin as possible, and the wiring length of FB should be shortened as possible to reduce the introduction of noise;

Wiring Example

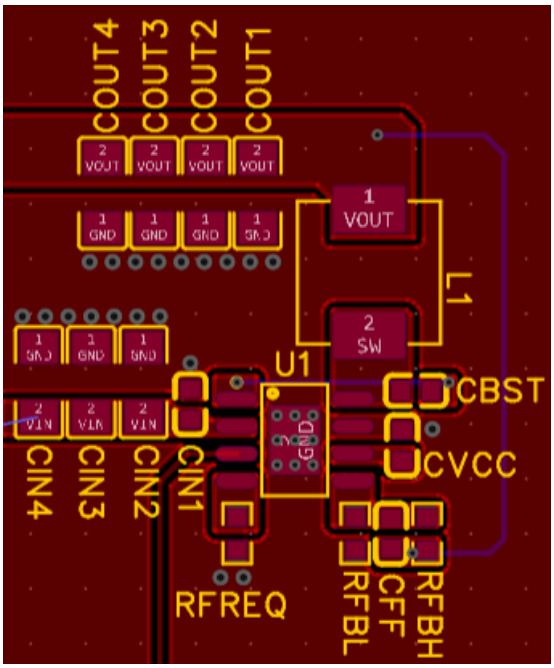
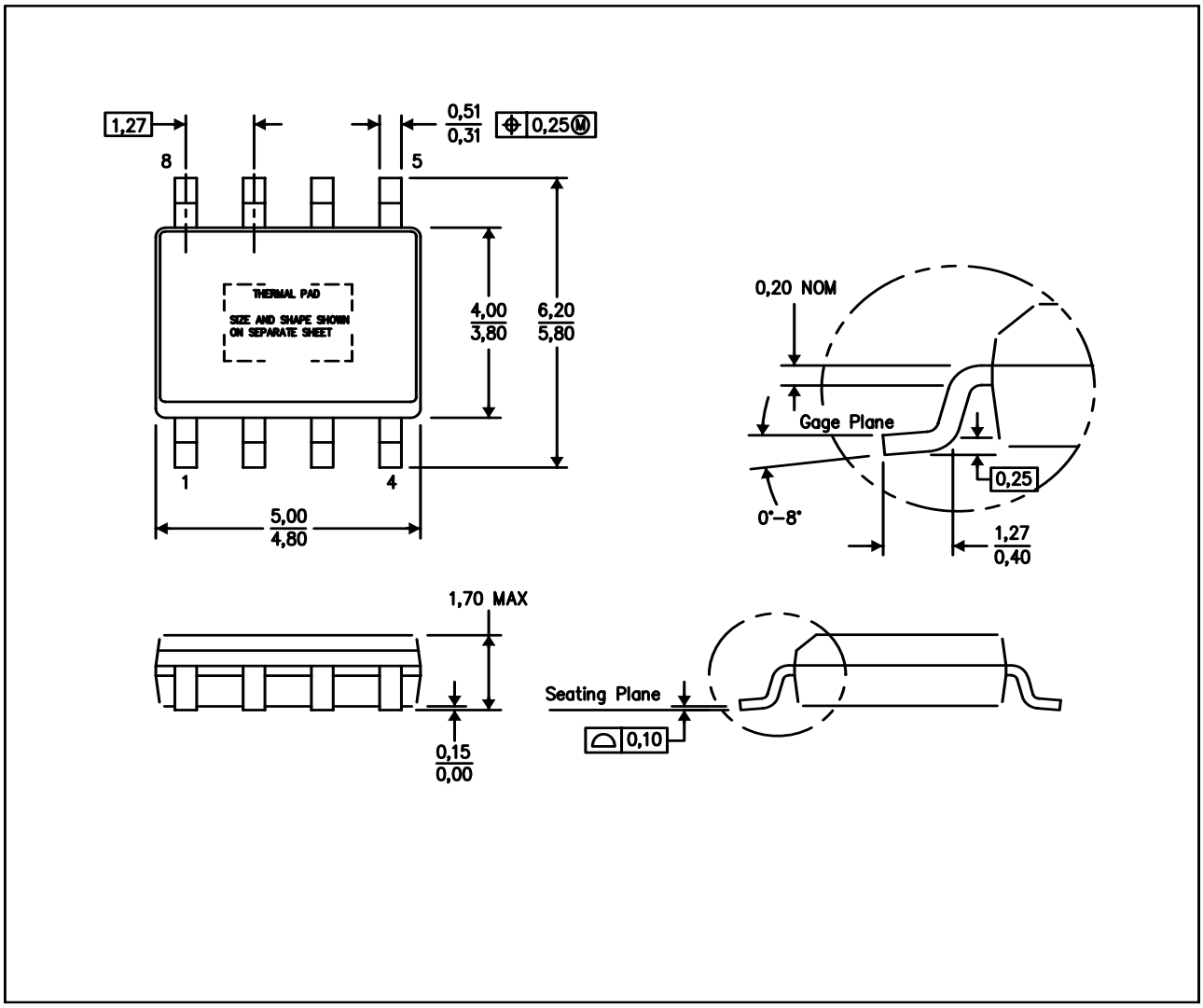


Figure 28. Typical Application PCB Layout of ESOP8 Packaging

Package Description (ESOP8)

8-pin plastic encapsulated SOIC with bottom EPAD



Note:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only.

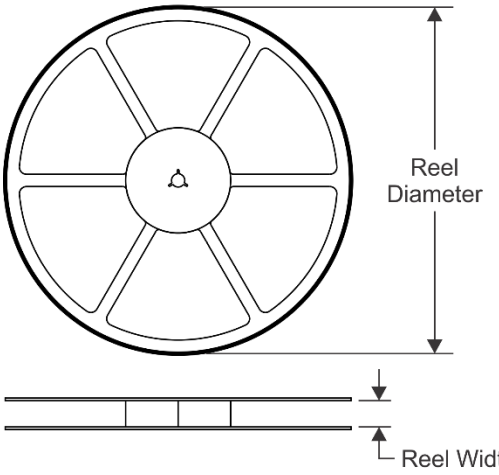
(2) This image is subject to change without prior notice.

(3) This size does not include mold burrs, protrusions, or nozzle burrs.

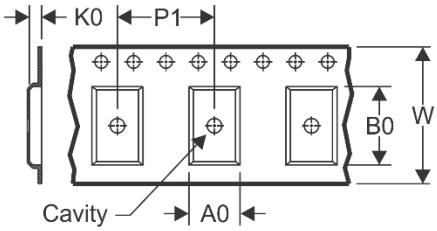
(4) This size does not include mold burrs.

TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

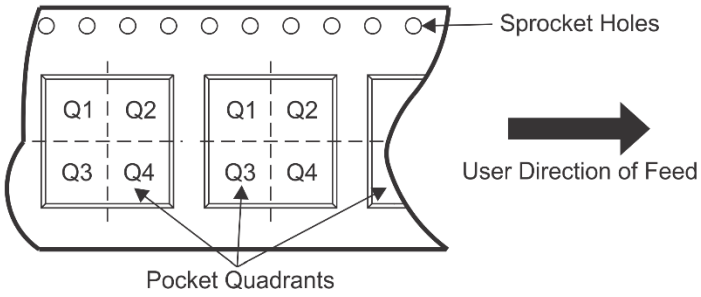


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LGS54360	ESOP8	EP	8	4000	330	6.5	5.3	2.1	8	12	Q1

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