18V 2A high-efficiency synchronous buck converter

Check for Samples: LGS5116B

Characteristic

- Wide input voltage range: 4.5V to 18V
- Output voltage range: 0.6V-12V
  - Provide adjustable output voltage options
- Working temperature range:- 40°C - + 125°C
- Provide a fixed switching frequency of 500KHz
- Maximum continuous output current of 2A
- Up to 96% system conversion efficiency
- Cycle by cycle current limiting protection
- Safe and reliable operating characteristics
  - Internal soft start
  - Overheating and overcurrent protection
  - Output short circuit protection
  - Input overvoltage protection
- Ultra small solution size
  - ——Small SOT23-6 package
- High efficiency and low power dissipation throughout the entire load range

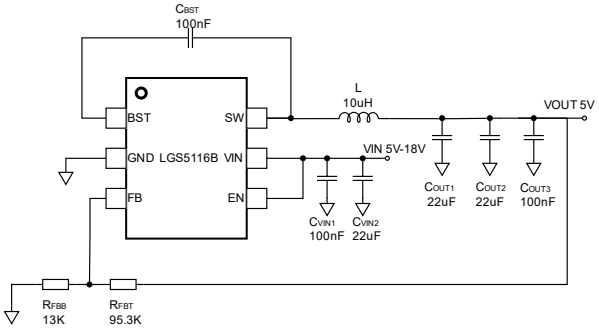


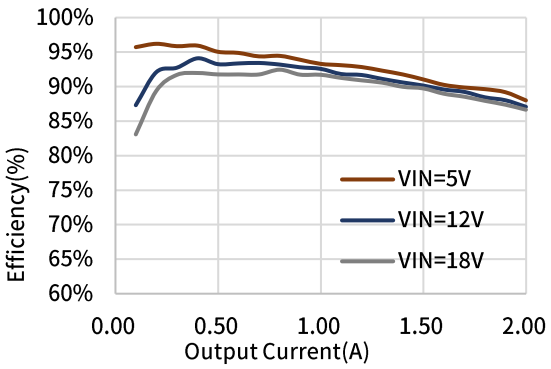
Figure 1 Typical Application Circuit

Description

LGS5116B is a synchronous buck converter with a wide input voltage range and high conversion efficiency. LGS5116B provides a load current capability of up to 2A and an adjustable output voltage over a wide range. The internally integrated peak current control mode allows external circuits to use small devices (including ceramic capacitors and small packaged inductors), while the low output voltage ripple characteristics make LGS5116B play an important role in high-precision and low-noise use. The internally integrated switch MOSFET, loop compensation, and soft start greatly reduce the number of external devices, enabling the design of small-sized solutions. The LGS5116B has extremely fast load transient response and high system conversion efficiency, making it an ideal choice for a variety of industrial and consumer applications.

Application

- 12V distributed power bus
- Industrial grade
  - ——Video surveillance and security system
  - ——Electrical appliances
- Consumer grade
  - ——Digital TV and LCD display
  - ——Digital set-top box
  - ——Router, modem



Efficiency (%) VOUT=3.3V

Typical application circuit

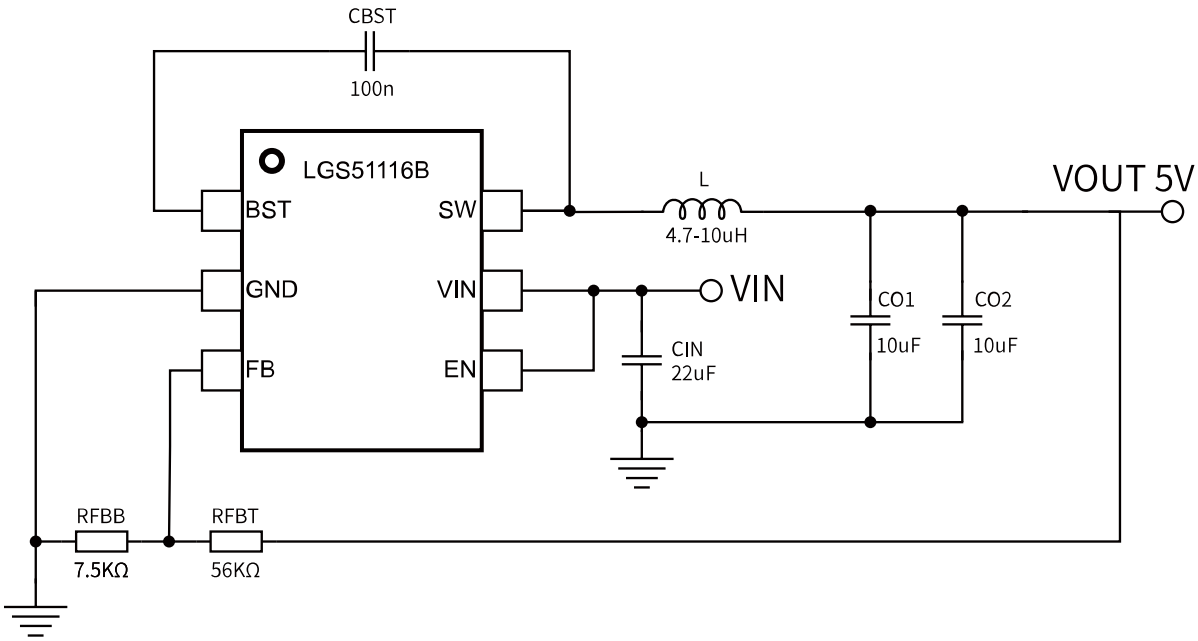


Figure 2 Typical Application Circuit of LGS5116B VO=5V

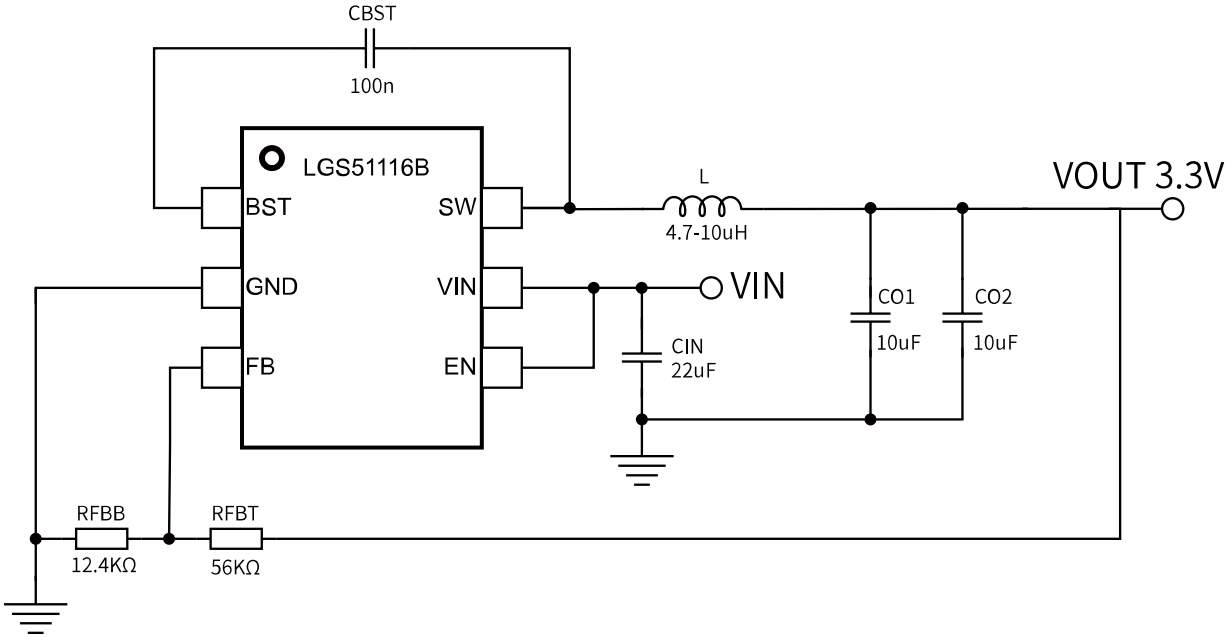


Figure 3 Typical application circuit of LGS5116B VO=3.3V

(1) It is recommended to use X7R or X5R ceramic capacitors as input capacitors and place them as close to the IC as possible. Please refer to the description of recommended input capacitors in the following text.

(2) Please choose ceramic capacitors with a withstand voltage higher than 16V for BST to SW, and place them as close as possible to the IC pins.

Packaging and Pin Arrangement

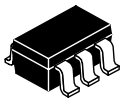


图 4 SOT23-6 Package

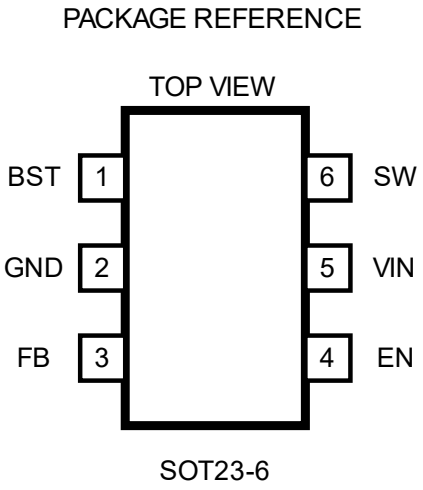


图 5 Package Reference Top View

Pin function

Pin Numbering	Pin Name	describe
1	BST	Bootstrap circuit pins. To increase the gate voltage of the high side MOSFET, a 0.1 μ F capacitor needs to be connected between this pin and the SW pin.
2	GND	Power ground pin.
3	FB	Feedback input pin. By dividing the voltage through an external resistor, the voltage fluctuation at the output terminal is fed back to the IC, and the output voltage value is set by the voltage division ratio of the resistor.
4	EN	Output enable pin. Enable high output; Set low to turn off the output.
5	VIN	Power input pin. Connect a bypass capacitor of 10 μ F or larger between this pin and the GND pin for filtering (1).
6	SW	Converter switch node. External connection power inductor.

(1) Pay attention to the filtering radius of the filtering capacitor. For convenience, try to place the capacitor as close to the chip as possible.

Absolute rated maximum value (1)

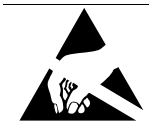
Temperature range: -40 ℃ -+125 ℃ (unless otherwise specified)

Parameter	MIN	MAX	Unit
VIN, EN, SW to GND voltage	- 0.3	25	V
BST to SW voltage	- 0.3	6	
FB to GND voltage	- 0.3	6	
Storage temperature Tstg	- 65	+ 150	℃
Junction Temperature TJ	- 40	+125	

(1) If the operating conditions of the device exceed the "absolute maximum value" mentioned above, it may cause permanent damage to the device. This is only a limit parameter, and it is not recommended for the device to operate at or beyond the limit value. Prolonged operation of the device under limit conditions may affect its reliability.

ESD level

			VALUE	UNIT
V_{ESD}	**Static discharge test**	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±1000	V



ESD (electrostatic discharge) sensitive devices.
Charged components and circuit boards may discharge without being noticed. Although this product has patented or proprietary protection circuits, the device may be damaged in the event of high-energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid device performance degradation or functional loss.

Recommended working conditions (1)

		MIN	MAX	Unit
Input Voltage	VIN to GND voltage	5	18	V
	EN to GND voltage	2	18	
Output voltage	V_{OUT}	0.6	12	
output current	I_{OUT}	0	2	A
Junction temperature	T_J	- 40	+ 125	℃

(1) The recommended working conditions indicate under what circumstances the chip can work normally, but do not represent specific parameter performance. Please refer to the technical specifications in the following text for details.

technical specifications

Unless otherwise specified, VIN=12V, VOUT=3.3V, TA=25 °C

parameter		Test conditions	MIN	TYP	MAX	单位
Input characteristics (VIN PIN)						
V_{IN_R}	Minimum input voltage (rising)			4.5	4.8	V
$HYS_{\_UVLO}$	Undervoltage locking hysteresis			0.35		V
V_{IN_MAX}	Maximum input voltage				18	V
I_{SD}	Shut Down Current	EN set low			15	μA
I_Q	static current	No Switch		400		μA
Enabling Characteristics (EN PIN)						
V_{EN_R}	EN rising threshold	T_J = 25°C		1.5		V
V_{EN_F}	EN decrease threshold			0.4		V
I_{EN}	EN leakage current	V_{EN}=2V			1	μA
Current characteristic (CURRENT LIMIT)						
I_{SC_HS}	High side MOSFET current limitation			3		A
MOSFET Characteristics						
R_{dson_HS}	On resistance of high side MOS transistor			160		mΩ
R_{dson_LS}	On resistance of low side MOS transistor			95		mΩ
Soft start process						
T_{SS}	The first SW pulse to $V_{OUT\ good}$ (1)	V_{IN} > 4.5V		0.5		ms
The first SW pulse to VOUT good						
V_{FB}	feedback voltage		0.588	0.6	0.612	V
I_{FB}	FB leakage current			0.1	1	μA
Switch characteristics						
FSW	**switching frequency**			500		KHz
System characteristics						
D_{MAX}	Maximum switch duty cycle			95		%
Thermal characteristics						
TSD	Hot shutdown (1)			150		°C
TSD_H	Delay of thermal shutdown (1)			40		°C
(1) Guaranteed by characterization or design, not production tested						

Application information: High efficiency synchronous buck switching regulator (Figure 1)

Unless otherwise specified, VIN=12V, VOUT=3.3V, TA=25 °C

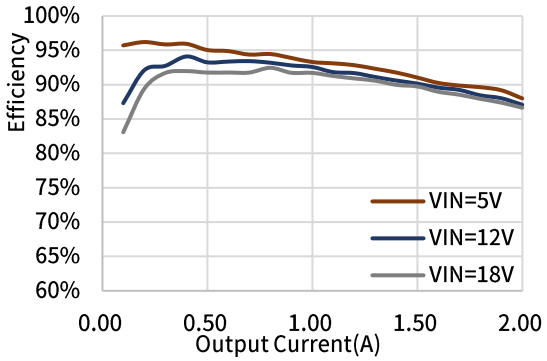


Figure 6-1 Efficiency 3.3V Output

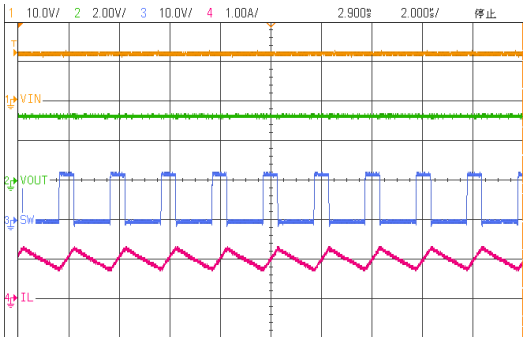


Figure 6-2 IO=1A Steady State CCM

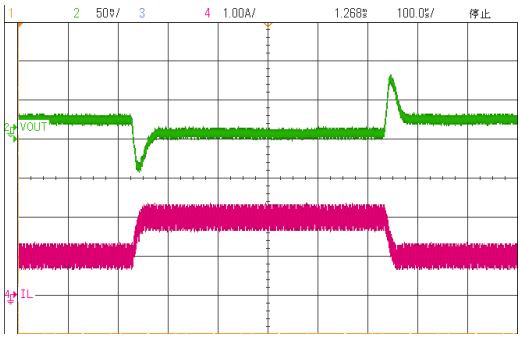


Figure 6-3 1-2A Load Transient

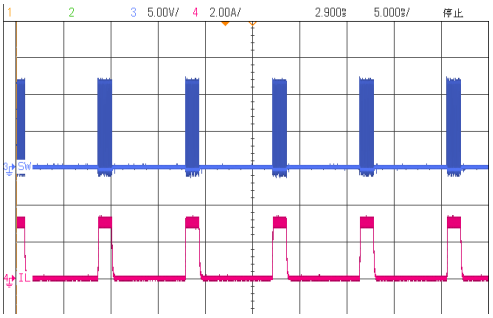


Figure 6-4 Current Limit

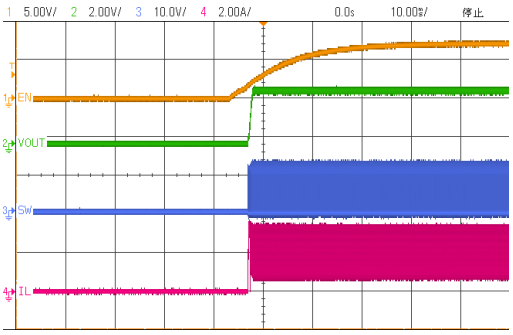


Figure 6-5 EN Power On

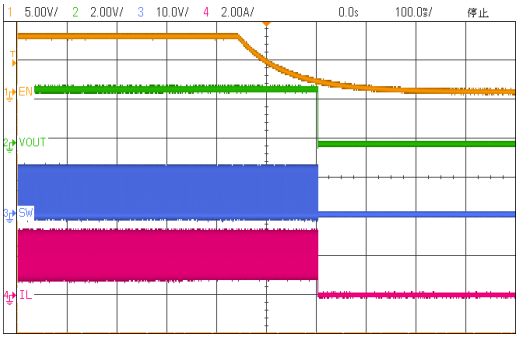


Figure 6-6 EN Power Off

Characteristic Description

Summary

LGS5116B is an internal switch type synchronous buck DC/DC regulator that integrates all controllers and protection circuits, greatly reducing system area. Equipped with SKIP control mode, it combines fast transient response with high efficiency. The LGS5116B external voltage divider network can set the output voltage to achieve wide output range changes to meet a wide range of usage needs.

Additional features include: soft start, hot shutdown, UVLO undervoltage lock, maximum duty cycle limit, and intelligent current limit shutdown timer. Simultaneously equipped with short-circuit protection function to prevent IC overheating in the event of output short circuit.

Power Save Mode

In addition to continuous conduction mode (CCM), LGS5116B also has a power-saving mode, which is achieved by pausing switch operations to reduce switch losses and maintain high efficiency of the converter under light load conditions. Skip comparator manages and switches working states by comparing I_{SKIP} and I_{REF}. When the current demand is lower than I_{SKIP}, the comparator controls to pause switching; When the current demand increases (V_{OUT} decreases), the comparator controls the activation current loop to enter continuous switching mode, causing VOUT to rise. At this time, I_{REF} will decrease. When I_{REF} is lower than I_{SKIP}, switching will be paused again. Due to the periodic sudden drops and recovery of the output voltage, the ripple of the output voltage in this mode is greater than that in CCM operating mode.

Soft Start

LGS5116B sets internal soft start. Soft start can prevent output voltage overshoot during the startup process. When the chip is started, the internal circuit of the IC generates a soft start voltage (V_{SS}), which starts to rise from 0V. When it is less than the internal reference (V_{REF}), V_{SS} replaces V_{REF} as the reference voltage for the error amplifier; When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference voltage.

Throughout the entire startup phase, the switch current limitation remains effective to avoid the occurrence of short circuits upon power up. When the output has a very large capacitance (such as 2200 μ F or even larger), the output voltage rise speed will be slower than V_{SS}, limited by the maximum switch current limit, and the time from startup to reaching the target voltage setting value will be longer than the soft start process.

EN - IC Enable

The voltage of the EN pin controls the startup and shutdown of LGS5116B. When the EN voltage is less than V_{EN_SUT}, the chip maintains a low-power standby state. When the voltage at the EN pin is greater than V_{EN_SUT}, the IC enters soft start mode. The high voltage resistance of the EN pin determines that it can be directly pulled up to the VIN voltage, which plays an important role in minimizing application solutions

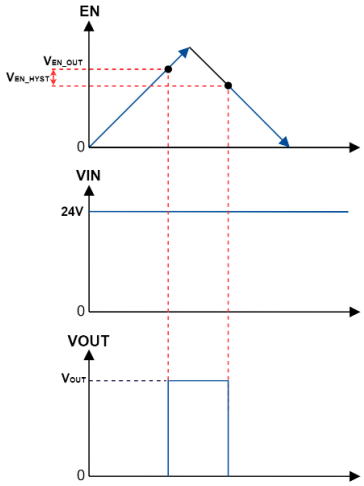


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Figure 7 EN Power on/Off Performance

Thermal Shutdown

When the junction temperature starts to rise above 150 °C, Thermal Shutdown will be activated and the system will forcibly shut down the regulator output. When the junction temperature drops below 130 ° C, LGS5116B will attempt a soft start again. The guaranteed operating junction temperature range of this device is -40 ° C to+125 ° C. High junction temperatures will reduce the working life, and when the junction temperature is above 125 ° C for a long time, the device life will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions, circuit board layout, rated package thermal resistance, and other environmental factors.

The junction temperature (T_J, unit: °C) is calculated based on the ambient temperature (T_A, unit: °C) and power consumption (P_D, unit: W), using the following formula:

$$T\_J = T\_A + (P\_D \times \theta\_JA)$$

Among them, θ_{JA} (unit: °C/W) is the thermal resistance of the package.

Maximum current limit

The LGS5116B DC-DC regulator output has a cycle by cycle overcurrent limiting function. When the SW current triggers the limit SW (Peak), BUCK output will enter a cycle by cycle current limiting state. $I_{LIMIT.SW\ (Peak)}$ is related to the inductance size and input voltage difference, and $I_{LIMIT.SW\ (Peak)}$ is only a reference minimum value. When there is a prolonged overcurrent or short circuit, it may trigger global OTP protection.

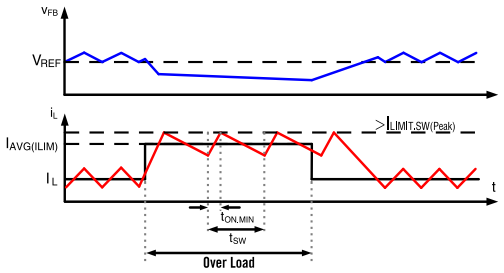


Figure 8 Current Limit

Input undervoltage protection (VULO)

In order to prevent misoperation of the chip under low voltage, an undervoltage locking circuit is integrated internally in LGS5116B. When the VIN voltage is below a certain value, the UVLO protection mechanism will be triggered to turn off the regulator output. When VIN is greater than UVLO rising, the chip will restart.

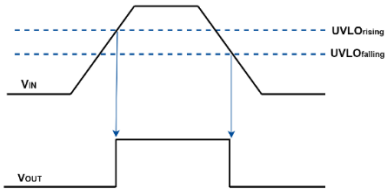


Figure 9 UVLO rise and fall threshold

Input overvoltage protection (OVP)

If the VIN voltage rises above the OVP voltage limit, the OVP circuit will prohibit the chip from switching. Once the

VIN drops below the OVP voltage, the soft start sequence will activate to complete the chip's restart operation.

Maximum duty cycle DMAX

When the input/output voltage difference is very low, BUCK switches to the maximum duty cycle operating state. At this time, the high-end N-channel MOSFET is in a normally open state, minimizing the turn off time. Under maximum duty cycle operating conditions, as the output voltage is the product of the input voltage value and the maximum duty cycle limit, the output voltage will drop sharply below the regulation range.

Application Information

Output voltage VOUT

The voltage regulation circuit of LGS5116B will adjust the FB voltage to be the same as the internal reference voltage, and the output voltage can be adjusted by changing the resistance ratio of R1 and R2. The resistive voltage divider is connected from the output node to ground and from the midpoint to the FB pin.

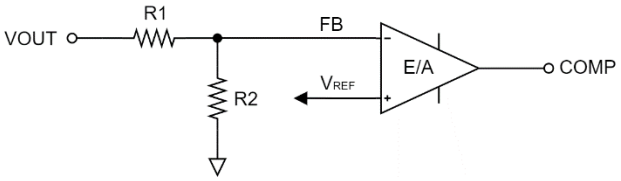


Figure 10 Setting output voltage

The resistance voltage divider network can be calculated according to the following formula:

$$R_2 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_1$$

A larger voltage divider resistor can reduce the current flowing through the voltage divider network and improve voltage conversion efficiency. However, a high resistance value makes the feedback loop more susceptible to noise interference. It is recommended to use voltage divider resistors with an accuracy of ± 1% or higher, and a temperature coefficient of 100ppm or lower.

If the FB pin is grounded or disconnected, the output voltage value will be driven to near the input voltage value. It should be noted that the load connected to the output at this time may be damaged. The feedback loop should be kept away from PCB noise interference, as shown in the PCB layout reference provided later.

Feedforward capacitor CFF

The feedforward capacitor C_{FF} can be connected across the resistance of V_{OUT-FB} to increase the phase margin of the loop and improve the transient response of the load.

The introduction of C_{FF} can form new zero points (Z_{FF}) and poles (P_{FF}) with the feedback resistor in the feedback loop. If the zero point is placed before the frequency at which the unity gain occurs, it can increase the frequency bandwidth, reduce the output ringing of the regulator, and stabilize it faster, thereby improving the transient response of the system.

The larger the selection value of C_{FF}, the greater the bandwidth it can provide. However, an excessively large C_{FF} can cause the loop gain bandwidth frequency to be too high, leading to loop instability. The general value of C_{FF} is between 22pF and 220pF.

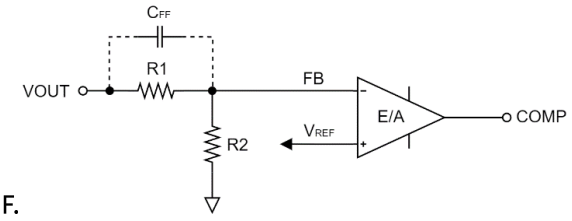


Figure 11 CFF pre compensation capacitor

CFF can be estimated according to the following formula:

$$C_{FF} = \frac{\sqrt{\frac{V_{FB}}{V_{OUT}}}}{2\pi \times R_1 \times f_c}$$

Bootstrap capacitor CBST

The high side switch driving circuit of LGS5116B buck driver requires a bias voltage higher than VDD to ensure that the high side MOS transistor is in the on state. The capacitance C_{BST} between BST and SW acts as a 'charge pump', raising the voltage at the BST end to SW+VDD (V_{BST-SW}=5V), The conducting diode for C_{BST} charging is integrated inside the LGS5116B chip to minimize the size of the usage scheme as much as possible. C_{BST} recommends using 0.1 μ F capacitors with a withstand voltage value higher than 16V.

Input capacitor CVIN

LGS5116B requires the use of decoupling capacitors to filter out noise interference at the input end. The typical recommended value for decoupling capacitors is 4.7 μ F, and the rated voltage must be greater than the maximum input voltage required by the IC, preferably twice the maximum input voltage (1). The increase of this capacitor can reduce input voltage ripple and maintain stable input voltage during load transients. Meanwhile, connecting a small 100nF ceramic capacitor in parallel with the filtering capacitor at the input end helps to filter out high-frequency noise. Small capacitors have a small filtering radius and should be placed as close as possible to the chip to ensure optimal filtering performance. In the testing process of LGS5116B, we selected 10 μ F 50V X7R and 100nF 50V X7R ceramic capacitors.

(1) The DC bias effect of ceramic capacitors causes a decrease in the effective value of the capacitor. Please refer to the DC bias characteristics of the selected capacitor as much as possible to choose the appropriate capacitor The packaging size, rated voltage, and dielectric material can all cause differences between the rated capacitance value and the effective capacitance value.

Output capacitor COUT

The range of output capacitor values allowed for LGS5116B is relatively wide. To ensure cost and small size, it is recommended to choose the appropriate output capacitor as much as possible. In practical applications, the output capacitance directly affects the voltage overshoot/undershoot and output voltage ripple during the transient response of the output current. When the load undergoes transient changes, the output capacitor needs to provide charge before the loop regulation is completed. The transient voltage change value Δ V_{OUT} can be calculated by the following formula:

$$\Delta VOUT = \Delta I_{OUT} * ESR$$

Where ΔV_{OUT} represents the jump value of the load current, and ESR is the equivalent series resistance value of the output capacitor.

The output voltage ripple consists of two parts: one is caused by the inductance current ripple flowing through the ESR of the output capacitor, and the other is caused by the inductance current ripple on the charging and discharging of the output capacitor.

$$\Delta V_{OUT-RIPPLE} = \frac{\Delta I_L}{8 * C_{OUT} * F_{SW}} + \Delta I_L * ESR$$

L represents inductor ripple current, and F_SW represents MOSFET switching frequency

In order to maintain a small output voltage overshoot or undershoot and reduce output ripple during transient changes, capacitors with large capacitance and small ESR are required, which also increases costs and volume. Choosing the appropriate output capacitor is crucial (1) and (2).

(1) Excessive output capacitance can also affect the normal startup and circuit stability of the chip.

(2) You can directly use the recommended X7R ceramic capacitor in typical applications, or use it as a reference standard for selecting output capacitance values.

Power inductor L

The selection of power inductors mainly considers the saturation current of the inductor, based on the expected ripple current ΔIL, which is the effective value of the AC current in the inductor that varies with the load current. Generally controlled between 20% -40% of the maximum load current $I_{OUT-MAX}$. The inductance value can be calculated using the following formula:

$$\Delta I_L = \frac{(V_{IN} - V_{VOUT}) * D}{L * F_{SW}}$$

D represents the duty cycle of the switch, which can be approximately calculated using $D=V_{\_OUT}/V_{\_IN}$. The unit of inductance value obtained is μ H.

The saturation current value of the inductor must be higher than the sum of the maximum load current and ripple current:

$$I_{L-MAX} \geq I_{OUT-MAX} + \frac{\Delta I_L}{2}$$

Generally speaking, choosing an inductor with a lower inductance value will result in a smaller DCR, which can handle faster transient responses, and the size of the proposed solution will be smaller. However, a too low inductance will generate greater inductance current ripple, resulting in larger output voltage ripple when using the same $C_{\_OUT}$.

After testing, the recommended inductance values for typical applications can serve as a reference for use.

Hot swappable security

Ceramic capacitors have the advantages of small size, good stability, and low impedance, making them an ideal choice for input bypass capacitors in LGS5116B circuits. However, if LGS5116B is plugged into a live power source, these capacitors may cause issues. A ceramic capacitor with low ESR characteristics forms an "underdamped slot circuit" with stray inductance in series with the power supply, The voltage at the VIN pin of LGS5116B may reach twice the nominal input voltage, which may exceed the rated value of LGS5116B and damage the parts. If the input power control is improper or the user needs to plug the LGS5116B into a power source, the design of the input network should prevent this overshoot.

Figure 12a shows the waveform generated when the LGS5116B circuit is connected to a 12V power supply via a 6-foot (2m) 24AWG twisted pair cable. The first figure shows the instantaneous response of a ceramic capacitor with a 22 μ F input. The input voltage is as high as 22V, and the peak input current is 13A.

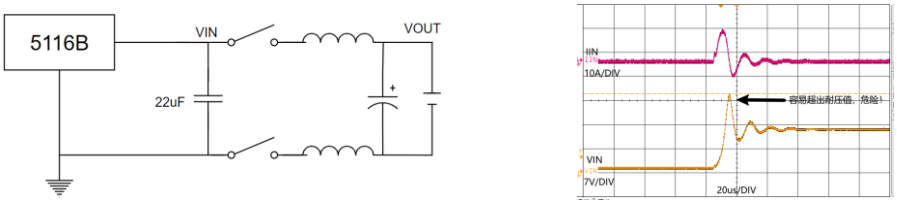


Figure 12 (a)

One way to improve and prevent the impact of this issue is to add another capacitor with a series resistor in the circuit. An aluminum electrolytic capacitor has been added in Figure 12b. The damping generated by the high equivalent series resistance of this capacitor can eliminate voltage overshoot. The additional capacitor improves the input ripple and can slightly increase the efficiency of the circuit. Another solution is shown in Figure 12c. A 1 Ω high-power resistor is connected in series with the input to eliminate voltage overshoot (which also reduces peak

input current). A 0.1 μ F capacitor improves high-frequency filtering. This solution is smaller and cheaper than electrolytic capacitors. For high input voltage, its impact on efficiency is minimal.

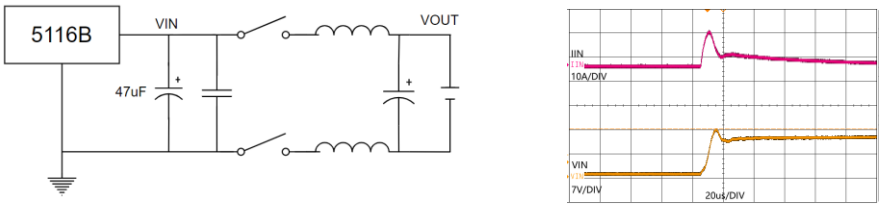


Figure 12 (b)

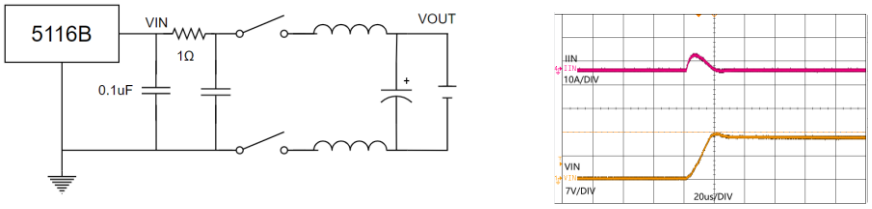


Figure 12(c)

Refer to PCB layout

Summary

The high integration of LGS5116B makes the PCB layout very concise and clear. Poor layout can affect the performance of LGS5116B, causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground jumping, and voltage loss, which in turn affects the stability of use. To optimize its electrical and thermal performance, please refer to the following rules to implement PCB layout and routing to ensure optimal performance:

- Place the high-frequency ceramic input capacitor CVIN as close as possible to the VIN and GND pins of LGS5116B to reduce high-frequency noise introduced to the output pins and minimize EMI radiation. In addition, keep the input and output capacitors connected to the large-area GND on the layer where they are located.
- It is best to use large-area copper coating for power circuits to make the input and output connection circuits as wide as possible, reduce losses during transmission, and maximize efficiency.
- To enhance heat dissipation and connectivity, the number of vias can be increased to achieve interconnection between the top layer and other power layers or layers. Please ensure that the PCB board has sufficient copper plated areas for heat dissipation, keeping the junction temperature below 125 °C.
- Consideration should be given to the ACR and DCR losses generated by inductance, which result in heat conduction to the chip. The inductor can be placed slightly further away or the heat island can be designed reasonably.
- The feedback resistors RFBT and RFBB should be located near the FB pin, and the feedforward capacitor CFF should be placed parallel to RFBT. The distance between the feedback loop and the FB and GND pins must be close, and the appropriate distance from VOUT can be relatively far. It is necessary to ensure that the feedback loop is away from any noise source (such as the SW node).

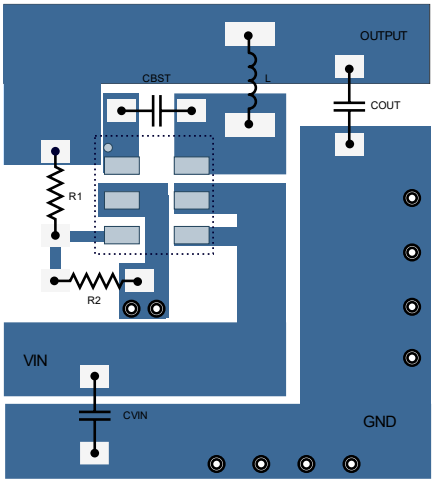
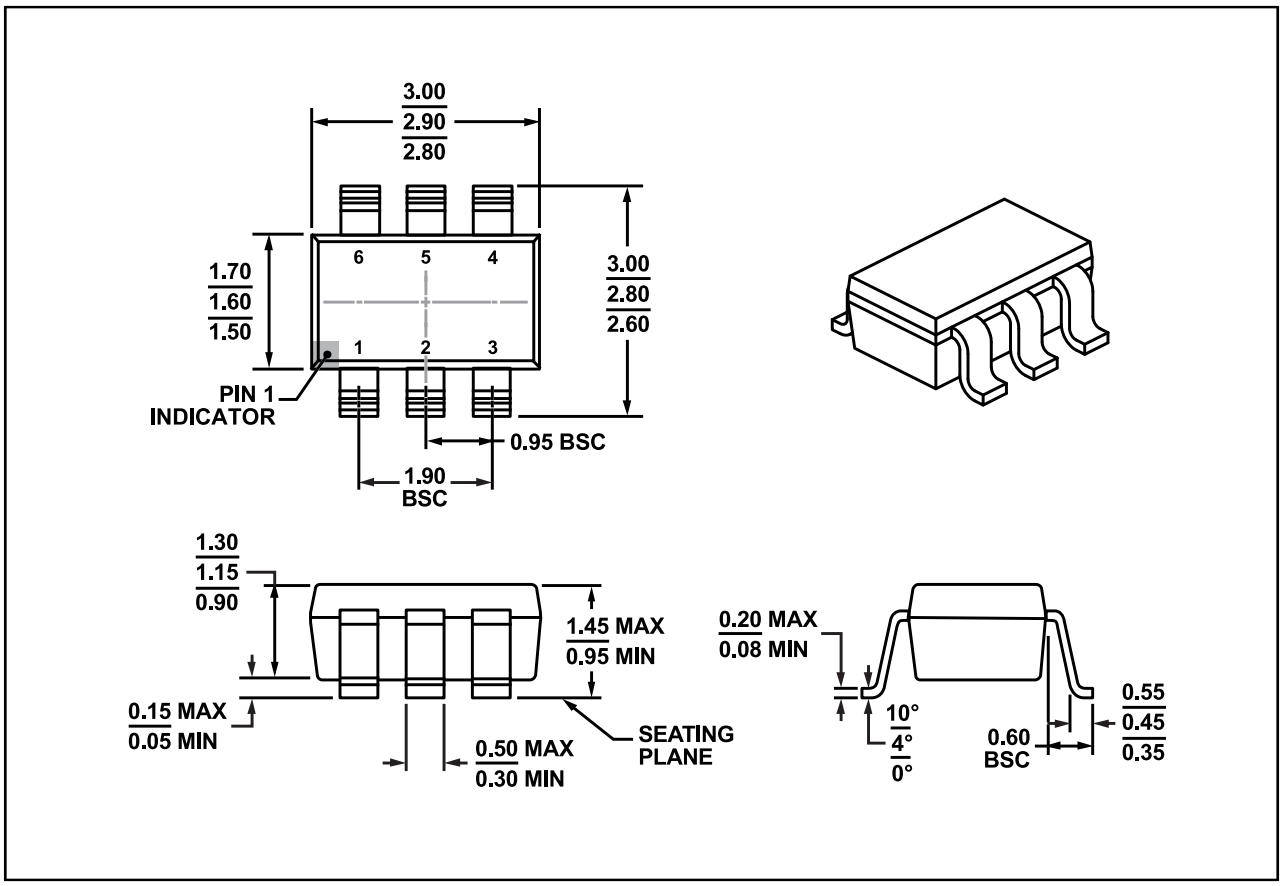


Figure 13: Reference PCB Layout

Package appearance description

1.45mm height 6-pin SOT-23 plastic encapsulated SOIC



NOTE:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only.

(2) This image is subject to change without prior notice.

(3) This size does not include mold burrs.

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