65V/600mA Asynchronous Step-Down Converter with Integrated LDO

Check for Samples: LGS51065

Features

NEW Special Industrial Power Application Design:

- Junction Temperature Range From -40°C to +125°C
- All ports have ± 2000V (HBM) ESD protection
- ESOP8 package with enhanced heat dissipation

NEW Built in 65V 600mA asynchronous step-down voltage regulator

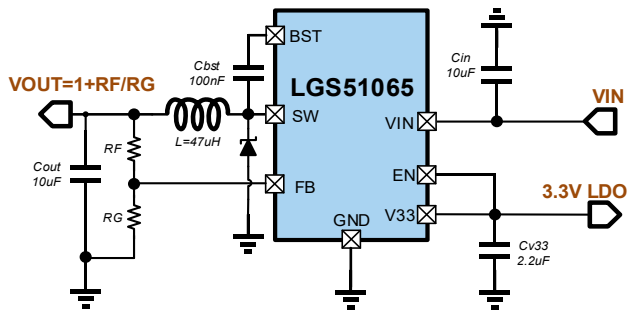
- Adaptive operation in constant voltage mode or LED driven constant current mode
- Peak efficiency up to 95%, light load efficiency up to 93%
- With soft start, thermal shutdown, input undervoltage locking, over-current protection and short-circuit protection.

NEW Built in 65V input wide range low I_Q 10mA LDO

- With over-current protection and thermal shutdown protection
- Accuracy: 2%
- Provide 3.3V fixed output

Applications

- Emergency evacuation lamp
- High voltage depressurization
- LED constant current drive
- Sensor network



Typical Application Topology

Description

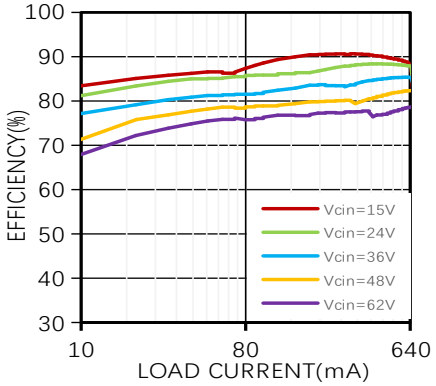
LGS51065 is internally integrated with high-voltage LDO and high-efficiency asynchronous step-down converter. Two outputs simultaneously support complete and reliable global thermal protection and short-circuit protection.

The LGS51065 step-down can realize the switching step-down of the maximum input 65V, and the output voltage can be set through the external voltage divider to achieve the maximum output current of 500mA. The LGS51065 can also provide a 3.3V LDO output with a maximum load of 10mA, which can be used as power supply for external control circuits. The LGS51,065 integrates an adaptive feedback loop design. It can work in voltage feedback mode and current feedback mode adaptively by detecting the ground impedance of the feedback pin. It can work in both constant voltage output mode and constant current output mode to drive LED lights.

Ordering Information

Part	Package	Top Mark
LGS51065	ESOP8	51065 YYWW(YW :Data Code)

Efficiency，Vout=5V，L=47uH



Revision History (†)

Rev. A V0.1 July.2022	Page
※ Initial version A. The relevant parameters in this manual only describe and acknowledge the relevant indicators of Version A	ALL
Rev. A V0.2 Aug.2022	**Page**
※ Revision A. Modify relevant parameters of version A; Optimize the chart section	ALL

† Note: Page numbers in previous editions may differ from current edition page numbers.

Absolute Maximum Ratings (†)

Table 3.1

Parameters	Range
Pin to GND voltage（VIN,SW）	-0.3~65V
Pin to GND voltage（3V3,EN,FB）	-0.3~6V
Pin to GND voltage（BST）	-0.3~SW+6V
Storage temperature（T_{stg}）	-65℃ to 150℃
Operating temperature	-40℃ to 125℃
ESD rating（HBM）	±2000V
ESD rating（CDM）	±1500V
ESD rating（MM）	±200V

†Note: If the operating conditions of the device exceed the above "absolute maximum", the device may be permanently damaged. This is only a limit parameter, and it is not recommended that the device operate at or above the limit value. The reliability of the device may be affected if it works under the limit conditions for a long time.

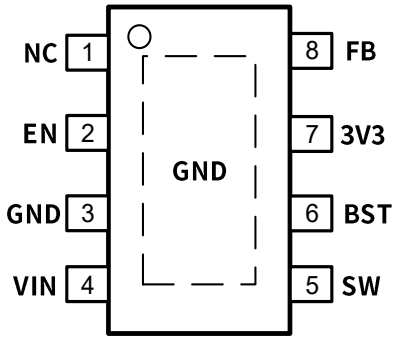
ESD 警告

ESD (electrostatic discharge) sensitive device.

Live devices and circuit boards may discharge without detection. Although this product has a patented or proprietary protective circuit, the device may be damaged when encountering high energy ESD. Therefore, appropriate ESD precautions should be taken to avoid device performance degradation or function loss.

Package and Pinout Diagram

Figure 3 Pin arrangement



ESOP8

Pin Function

Table 3.1 Pin Function Description

Pin number	Pin Name	Description
1	NC	Test pin, Floating.
2 (1)	EN	The BUCK output enable pin is set to enable the step-down output when it is high, and the step-down output is closed when it is empty or set to low.
2	GND	Chip system ground.
4	VIN	Input voltage stabilizing pin, external voltage stabilizing capacitor, it is not recommended to exceed 100uF.
5	SW	Internal power switch node. External connection power inductor, Schottky diode, and CBST capacitor.
6	BST	Power supply for the drive of the liftgate. High quality 100nF ceramic capacitors need to be connected between BST and SW.
7	3V3	LDO regulated output pin. Fixed output 3.3V, rated 10mA. At least 2.2uF external capacitance to ground.
8 (2)	FB	Step down feedback input pin, multi-mode adaptive. Constant voltage external resistance voltage division; Constant current external resistance samples LED current.

(1) The EN pin is 3.3V logic level high. Do not connect high voltage.

(2) If the FB impedance to ground is higher than 20K, it will be identified as a constant voltage mode. After the chip is powered on, it will detect once and latch the identification status.

Technical Specifications

Unless otherwise specified, The limit value is applicable to the working junction temperature (TJ) range from - 40 ℃ to+125 ℃. The minimum and maximum limits are specified by test, design, or statistical correlation. The typical value represents the most possible parameter specification when TJ=25 ℃, which is only for reference. All voltages are relative to GND.

Table 4.

Parameter		Test Conditions	MIN	TYPICAL	MAX	UNIT
BUCK Characteristic						
V_{IN}	Recommended input voltage range		12		65	V
V_{UVLO}	input undervoltage lock Rising edge			12	13	V
	Fall edge		10	10.5		V
I_Q (1)	Quiescent current	EN=0		65		μA
$I_{Q\text{-}BUCK}$	BUCK Module quiescent current	EN=1,V_{IN}=24V,V_{OUT}= 5V		125		μA
$R_{DS(ON)BUCK\_TOP}$	BUCK top tube R_{DSON}	T_J=25℃		600		mΩ
$F_{FB.CV}$	FB feedback voltage CV	Voltage stabilized output mode		1		V
$F_{FB.CC}$	FB feedback voltage CC	Constant current output mode		0.2		V
D_{MAX}	Maximum duty cycle		85			%
$I_{LIMT\_SW\ (Peak)}$	SW Current limit	VIN=48V		900		mA
$I_{FB.BIASA}$	FB bias current			10		nA
LDO Characteristic						
$V_{OUT.LDO}$	LDO Output voltage range		3.2	3.3	3.6	V
$I_{OUT.LDO}$	LDO Output current		10			mA
$I_{LIMIT.LDO}$	LDO Protective current limiting	Short to GND		15		mA
I/O standards						
V_{I/O_H}	Input I/O high logic threshold	Pin EN	1.4			V
V_{I/O_L}	Input I/O low logic threshold	Pin EN			0.6	V
Global thermal protection characteristics						
$T_{OTP\text{-}R}$	Over temperature protection	T_J Rising		150		℃
$T_{OTP\text{-}F}$	Release of over temperature protection	T_J Falling		130		℃

(1) This current is the total quiescent current when DCDC output is turned off.

Functional Block Diagram

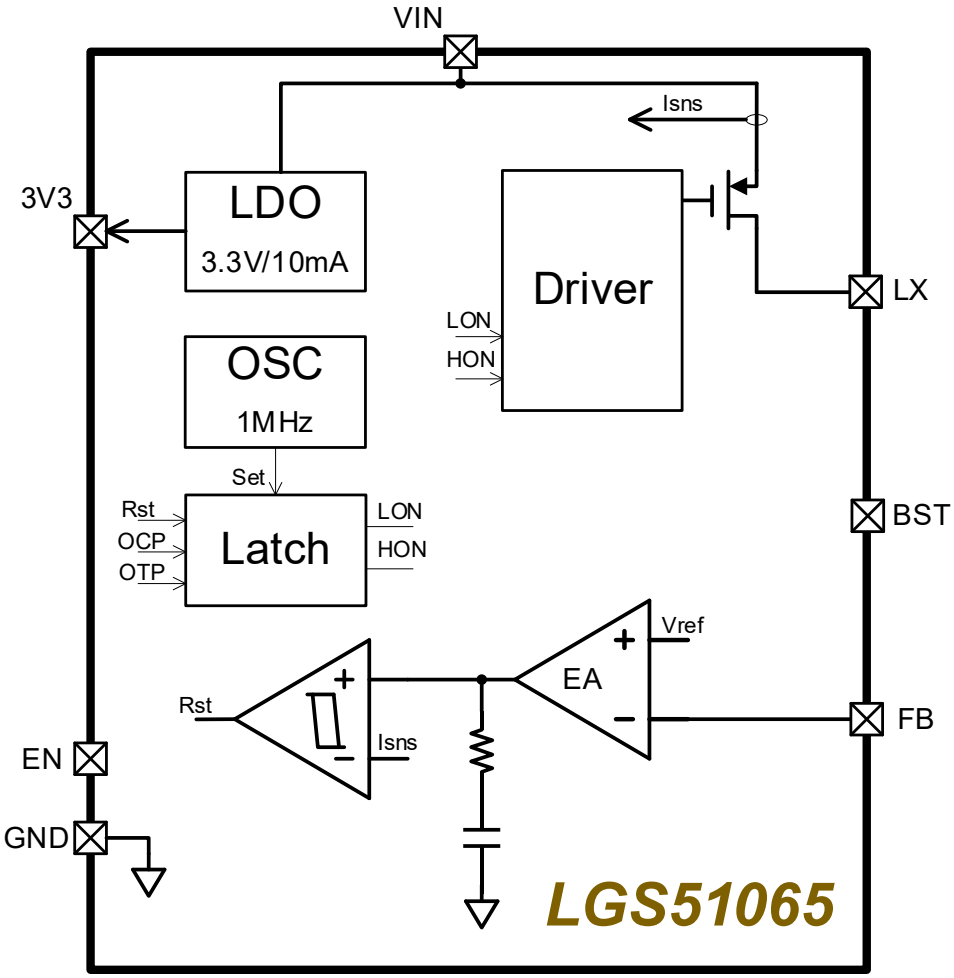


Figure 5 Internal Function Block Diagram

Application Information: Typical Application Circuit

LGS51065 is internally integrated with an adaptive feedback loop module, which detects the external impedance of FB at the initial stage of system power on. When the external impedance of FB is greater than 20KΩ, the system determines that the FB is in constant voltage mode, and the loop will adjust the FB voltage to 1V. The calculation formula of output voltage is

$$V_{OUT} = \frac{R_F + R_G}{R_G} (V)$$

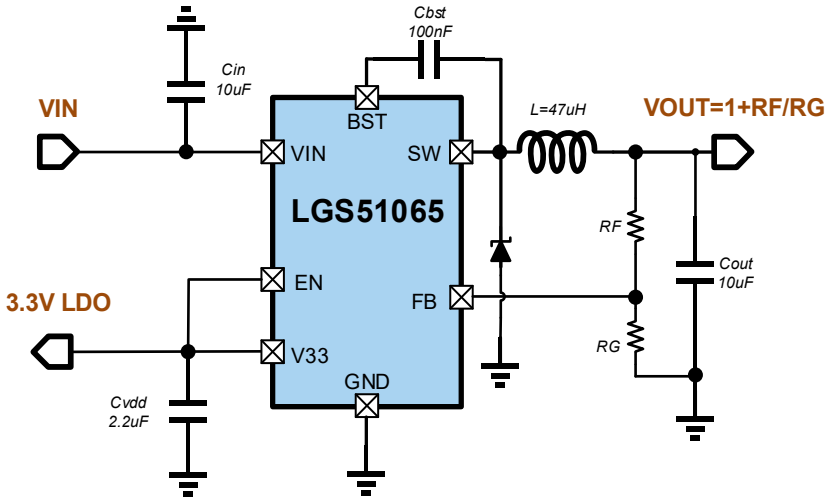


Figure 6. a Typical application of DC-DC module in step-down mode

When the external impedance of FB is less than 2K Ω, the system determines that the FB is in constant current mode, and the loop will adjust the FB voltage to 0.2V. The calculation formula of output current is:

$$VOUT = \frac{0.2\text{V}}{\text{Rsence}} (A)$$

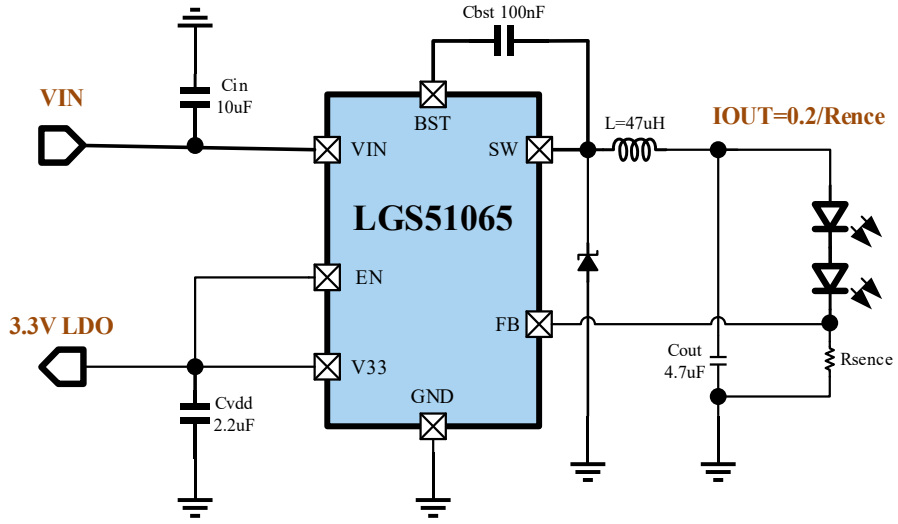


Figure 6. b Typical application of DC-DC module in constant current drive mode

Application Information: High Efficiency Asynchronous Step-Down Switching Regulator (Overview)

Summary

LGS51065 built-in asynchronous rectifier switch regulator. The external FB resistor can be configured to operate in the regulated output mode (CV) or constant current LED drive mode (CC).

Setting of CV and CC Modes

The LGS51065 can adaptively select voltage feedback or current feedback. If FB impedance to ground is higher than 20KΩ, it will be identified as constant voltage CV mode, and if FB impedance to ground is lower than 2K Ω, it will enter CC mode. After the chip is powered on, it will detect once and latch the identification status.

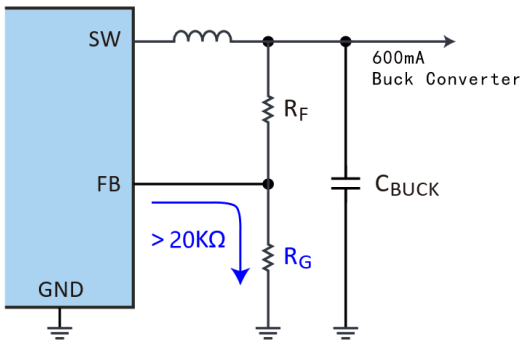


Figure 7.1 BUCK Setting in CV Mode

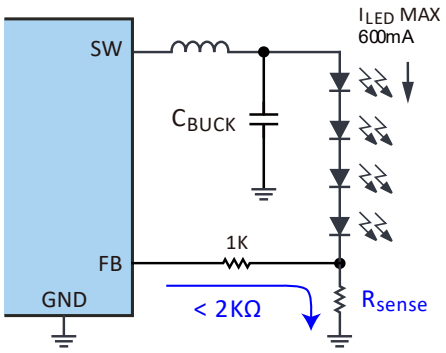


Figure 7.2 BUCK works in CC mode

Role of EN

Enable input pin of BUCK. Drive EN to the high-level state to open the BUCK converter; Turn off the converter by driving EN to low level. The typical value of the high level of EN control logic is 3.3V, the internal pull-down has been set, and the pin is suspended BUCK to output DISABLE.
This pin can be used for PWM digital dimming when BUCK is working in CC mode.
It is recommended that this pin be controlled by MCU, and it is not recommended that this pin be directly shorted to 3V3 to avoid the LDO output being closed due to excessive line loss and heavy load triggering UVLO when power is on.

Table 7. Pin EN working state

Pin	direction	Pin Status	function
EN (Pin1)	input	high	BUCK Output enable
		low	BUCK Output OFF

Maximum Duty Cycle of Skip Mode DMAX

When the output voltage drops to close to the input voltage, the BUCK switches to the maximum duty cycle working state. At this time, the N-channel MOSFET in the chip is in the open state, reducing the turn off time to the shortest. Under the maximum duty cycle operating condition, the output voltage drops below the regulation range suddenly because the output voltage is the product of the input voltage value and the maximum duty cycle limit value.

Enable failure conditions of BUCK

In addition to the EN pin status, it should also be noted that the following mechanisms can turn off the BUCK output:

1) LDO output over-current or short circuit, leading to system power good indication PG failure UVLO
2) Undervoltage protection triggered
3) OTP over temperature protection triggered

Application Information: High Efficiency Asynchronous Step-Down Switching Regulator (CV Mode)

Set Output Voltage (CV Mode)

LGS51065 works in constant voltage mode, and the output voltage can be adjusted externally through the resistance divider network. The recommended output voltage range is shown in the table below.

The voltage dividing network is composed of RG and RF. Please ensure that RG is greater than or equal to 20K. The converter regulates the output voltage by keeping the voltage on the FB pin equal to the internal reference voltage VREF.

Once RG is selected, RF value can be selected according to VFB.CV. Typical value of VFB.CV is 1V:

$$V_{OUT} = \frac{R_F + R_G}{R_G} \quad (V)$$

Table 8. Output Voltage Setting Quick Configuration

VOUT	RF	RG	*Set voltage* (1)	
2.5V	30K	20K	2.50V	0.00%
3.3V	47K	20K	3.35V	1.50%
4.2V	62K	20K	4.10V	2.38%
5.0V	82K	20K	5.10V	2.00%
9.0V	160K	20K	9.00V	0.00%

(1) Other voltage dividing resistor pairs and high-precision resistors can also be selected to achieve higher setting accuracy.

Over Current Protection and Short Circuit Protection (CV Mode)

BUCK operates in CV mode and has cycle by cycle overcurrent limit. When the SW current triggers I LIMIT.SW (Peak), the BUCK output will enter the cycle by cycle current limiting state.

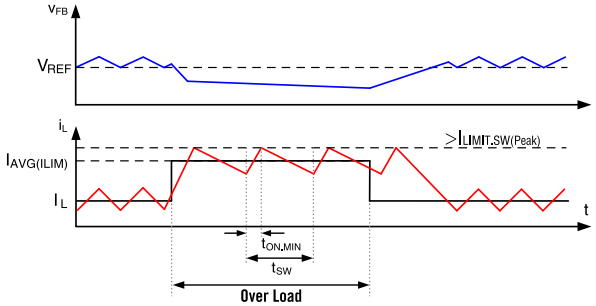


Figure 8.1 Description of overcurrent and short-circuit behavior in BUCK constant voltage mode

ILIMIT.SW (Peak) is related to the inductance size and input differential pressure. ILIMIT.SW (Peak) only

Is the reference minimum value. In case of long-time overcurrent or short circuit, global OTP protection may be triggered.

CFF Feedforward Compensation Capacitor

In some cases, feedforward capacitors can be used on RF to improve load transient response or loop phase margin.

This is especially true when using RF values>100 k Ω. Large RF value and parasitic capacitance at FB pin will reduce load transient response.

If the requirements for transient response of the load are high, a CFF can help mitigate the impact.

$$C_{FF} = \frac{V_{OUT}\sqrt{V_{OUT}} \times C_{OUT}}{120 \times R_F}$$

*If the CFF is less than 15pF, it is unnecessary to add it.

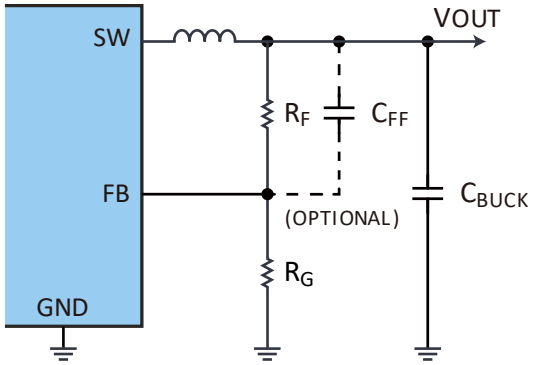


Figure 8.2 BUCK constant voltage mode and CFF pre compensation capacitor

CFF can be calculated according to the following formula:

Application Information: High Efficiency Asynchronous Step-Down Switching Regulator (CV Mode)

Inductance selection (CV mode)

The parameters for selecting inductance are inductance value and saturation current.

The inductor is based on the expected ripple current of the inductor, which is usually selected between 20% and 40% of the maximum output current value.

Experience shows that the optimal ripple current of the inductor is 30% of the maximum load current. Note that when selecting ripple current for applications where the maximum load is much smaller than the maximum available load of the device, use the maximum device current. The constant K is the percentage of inductance current ripple.

For most applications, the inductor value can be calculated from the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUT\,max}} \times \frac{V_{OUT}}{V_{IN}}$$

Higher inductance value can reduce ripple current, but increase conductance loss, magnetic core loss and current stress on inductor and switching device. This also requires a larger output capacitor to ensure the same output voltage ripple. The reasonable value is to ensure that the ripple current is 30% of the output DC. Since the ripple current will increase with the input voltage, the maximum input voltage also determines the inductance value accordingly. The DC resistance of inductance is an important parameter about efficiency.

When the LGS51065 operates in CV mode, the best selection range of inductance for most applications is 10

μH to 47μH。

The peak current of inductance can be calculated according to the following formula:

$$I_{L(peak)} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{2 f_{SW} \times L \times V_{IN(MAX)}}$$

Higher inductance value can reduce ripple current, but increase conductance loss, magnetic core loss and current stress on inductor and switching device. This also requires a larger output capacitor to ensure the same output voltage ripple. The reasonable value is to ensure that the ripple current is 30% of the output DC. Since the ripple current will increase with the input voltage, the maximum input voltage also determines the inductance value accordingly. The DC resistance of inductance is an important parameter about efficiency.

When the LGS51065 operates in CV mode, the best selection range of inductance for most applications is 10

μH to 47μ H。

The peak current of inductance can be calculated according to the following formula:

Selection of output capacitance (CV mode)

The output capacitance and its ESR value determine the output voltage ripple and load transient performance. Output capacitor banks are usually limited by load transient requirements and stability rather than output voltage ripple. The following formula can be used to estimate the lower limit of the total output capacitance and the upper limit of the capacitance ESR, which meet the specified load transient requirements:

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT} \times K} \times \left[\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times (1 + K) + \frac{K^2}{12} \times \left(2 - \frac{V_{OUT}}{V_{IN}}\right) \right]$$

$$ESR \leq \frac{(2 + K) \times \Delta V_{OUT}}{2 \times \Delta I_{OUT} \left[1 + K + \frac{K^2}{12} \times \left(1 + \frac{V_{IN}}{V_{IN} - V_{OUT}}\right) \right]}$$

ΔV_{OUT}= output voltage transient
ΔI_{OUT}= output current transient

Then the output capacitor and ESR can be adjusted to meet the requirements of load transient and output ripple.

In practical application, the output capacitance has the greatest influence on the transient response and the loop phase margin. Load transient testing and bode diagrams are the best way to validate any given design and must be completed before the application goes into production. In addition to the required output capacitance, at least one small ceramic capacitor is placed at the output end to help reduce high-frequency noise. Small ceramic capacitors in the range of 1nF to 100nF can be very helpful in reducing output spikes caused by parasitic inductors and circuit boards.

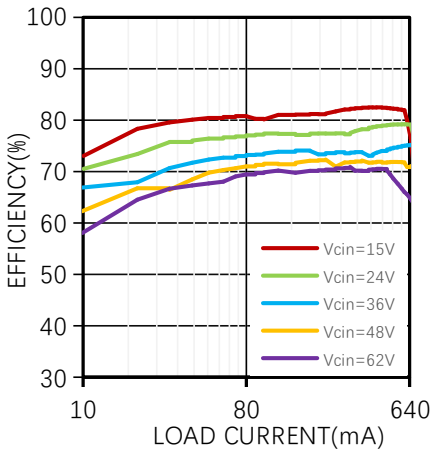
Ceramic capacitors using X5R or X7R dielectric to achieve low ESR characteristics.

When the LGS51065 works in CV mode, the 10uF ceramic capacitor can meet the requirements of most application scenarios.

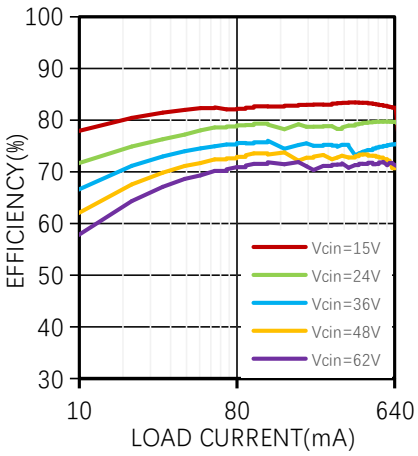
Application Information: High Efficiency Asynchronous Step-Down Switching Regulator: Diagram (CV Mode)

Unless otherwise specified, TA=25 ℃, all output voltages are based on RG=20K, and VCIN value is measured with DC input.

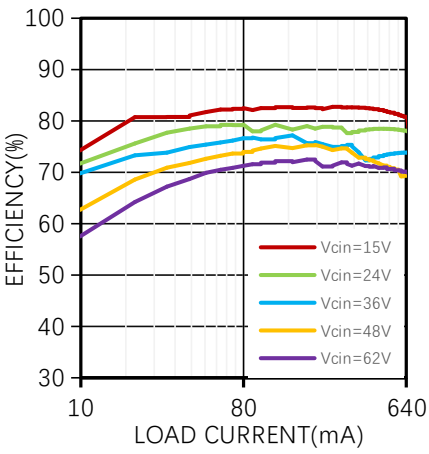
Efficiency, Vout=2.5V, L=10uH



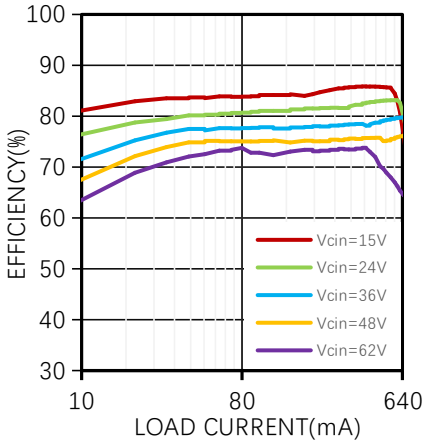
Efficiency, Vout=2.5V, L=22uH



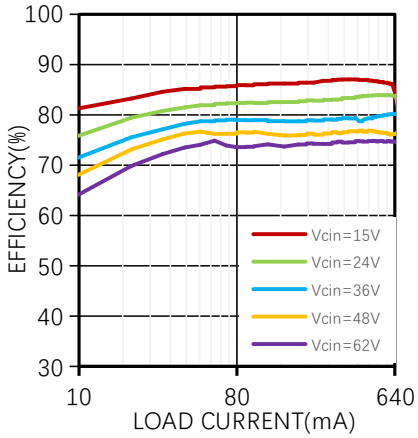
Efficiency, Vout=2.5V, L=47uH



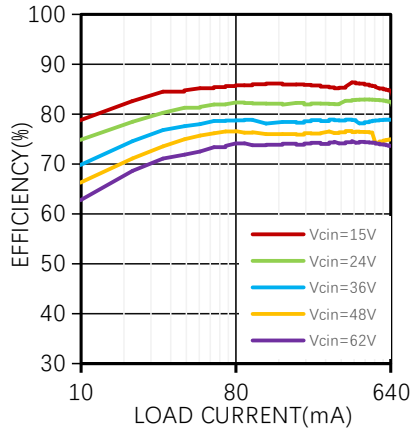
Efficiency, Vout=3.3V, L=10uH



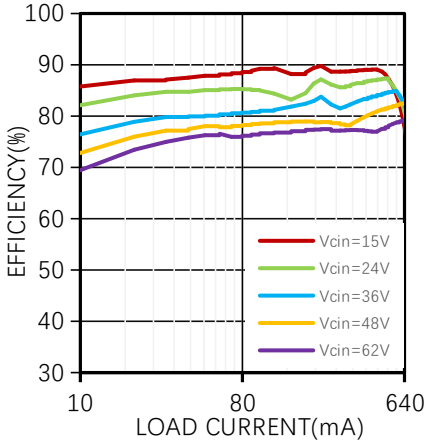
Efficiency, Vout=3.3V, L=22uH



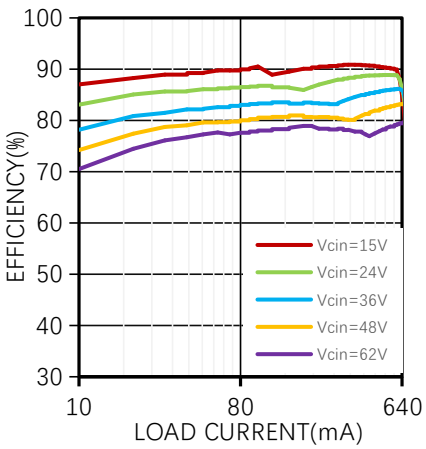
Efficiency, Vout=3.3V, L=47uH



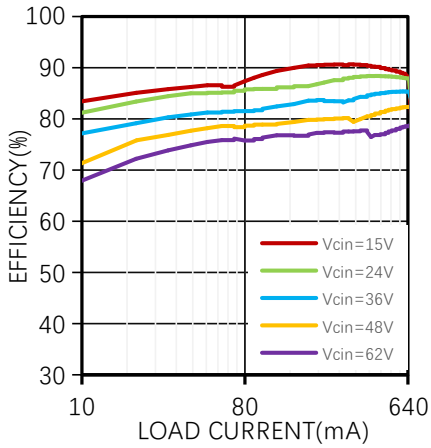
Efficiency, Vout=5V, L=10uH



Efficiency, Vout=5V, L=22uH



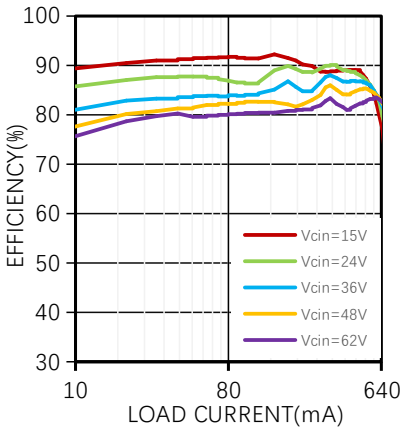
Efficiency, Vout=5V, L=47



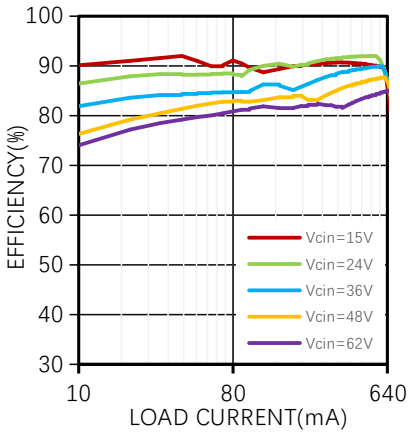
Application information: High efficiency asynchronous step-down switching regulator: diagram (CV mode)

Unless otherwise specified, TA=25 ℃, all output voltages are based on RG=20K, and VCIN value is measured with DC input.

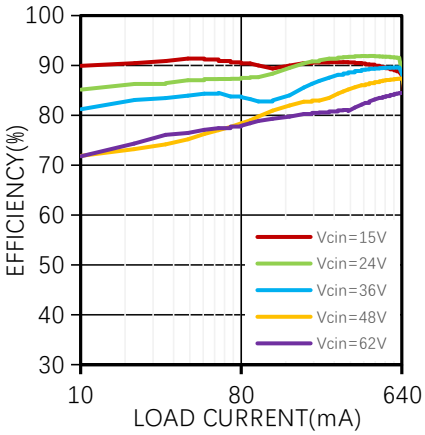
Efficiency，Vout=7.5V，L=10uH



Efficiency，Vout=7.5V，L=22uH

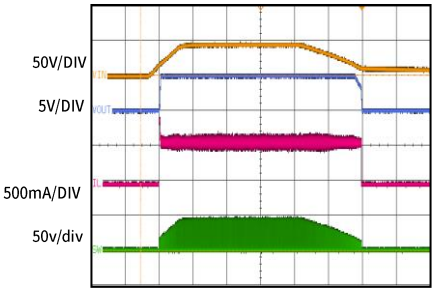


Efficiency，Vout=7.5V，L=47uH



Power Up and Power Down

EN=VIN

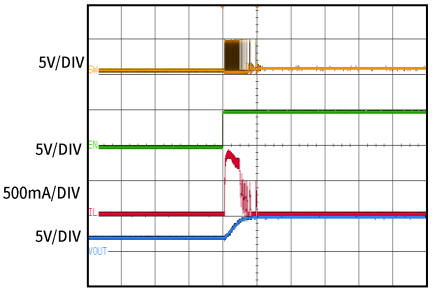


45VIN to 5VOUT, LOAD=600mA

L=47µH,COUT=10µF

Power Up and Power Down

NO LOAD

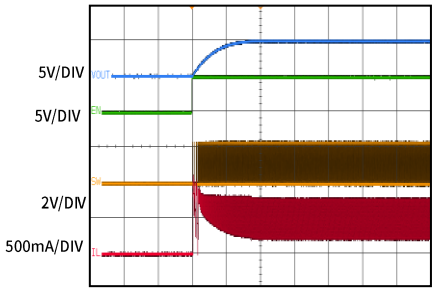


45VIN to 5VOUT, NO LOAD

L=47µH,COUT=10µF

Power Up and Power Down

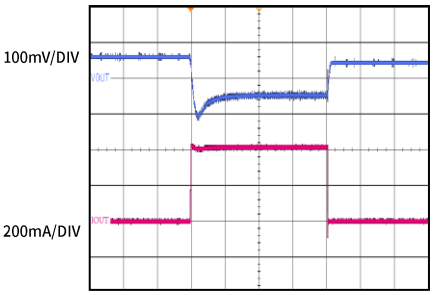
10R LOAD



45VIN to 5VOUT,LOAD=10Ω

L=47µH,COUT=10µF

Load Transient,VOUT=5V

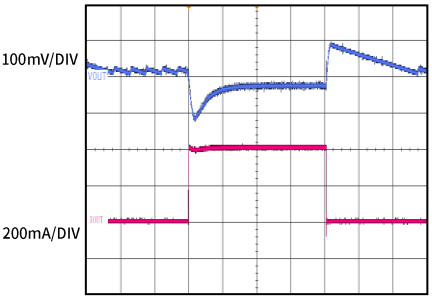


LOAD STEP=0mA TO 600mA

VIN=24V,Slew rate is 1.6A/µs

L=47µH,COUT=10µF,CFF=47pF

Load Transient,VOUT=5V

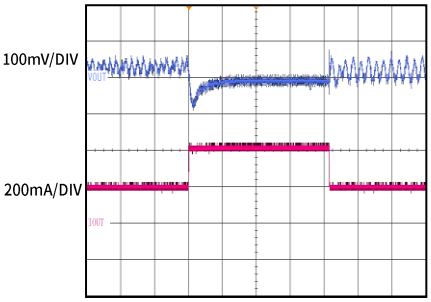


LOAD STEP=10mA TO 600mA

VIN=24V,Slew rate is 1.6A/µs

L=47µH,COUT=10µF,CFF=47pF

Load Transient,VOUT=5V



LOAD STEP=300mA TO 600mA

VIN=24V,Slew rate is 1.6A/µs

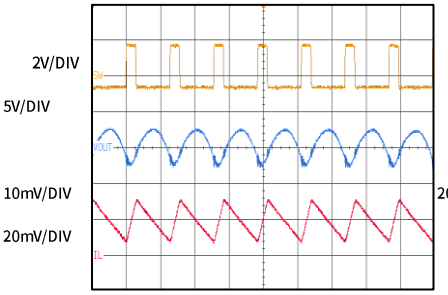
L=47µH,COUT=10µF,CFF=47pF

Application information: High efficiency asynchronous step-down switching regulator: diagram (CV mode)

Unless otherwise specified, TA=25 ℃, all output voltages are based on RG=20K, and VCIN value is measured with DC input.

Switching Waveforms

PWM Mode

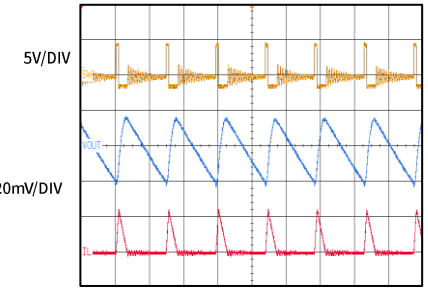


24VIN to 5VOUT, LOAD=500mA

L=47µH,COUT=10µF

Switching Waveforms

Burst Mode Operation

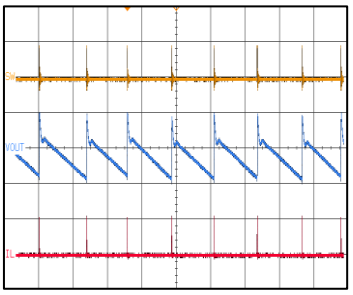


24VIN to 5VOUT, LOAD=60mA

L=47µH,COUT=10µF

Switching Waveforms

Pulse Skip Mode



24VIN to 5VOUT,LOAD=5mA

L=47µH,COUT=10µF

Application Information: High Efficiency Step-Down Switching Regulator (CC Mode)

Set output current (CC mode)

The output constant current value of LGS51065 working in constant current mode can be set through RSE, and the output current is determined by VFB CC and RSENCE decide.

The typical value of VFB.CC is 0.2V, which can be set according to the following formula:

$$I_{OUT} = \frac{0.2}{R_{Sence}}(A)$$

Table 13. Quick Configuration of Output Current Setting in CC Mode

R_{Sence}(Ω)	I_{OUT}(mA) (1)
2	100
1.33	125
1	200
0.8	250
0.68	294
0.56	357
0.47	425

Other high-precision resistors can also be selected to achieve higher setting accuracy.

Short Circuit of Lamp String (CC Mode)

LGS51065 works in constant current mode, and short circuit of lamp string will not cause damage. The output current can be calculated according to the following formula:

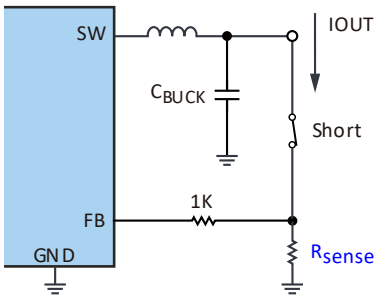


Figure 13.1 Schematic diagram of lamp bead short circuit in CC mode:

$$I_{OUT\ (LED-short)} = \frac{(V_{CIN} - 0.2) \times 16 \times 10^{-9}}{L} + I_{SET}$$

Although it will not cause damage, considering that it is of little significance to maintain this short circuit state, this anomaly can be obtained by monitoring the lamp bead anode through MCU ADC, and using EN to turn off the BUCK to reduce unnecessary heating and power consumption.

PWM Dimming Via EN (CC Mode)

LGS51065 can use the EN pin for PWM dimming. With PWM dimming, the output current of LED can vary from 0% to 100%.

The brightness of the LED is determined by the duty cycle of the PWM signal. For example, the duty cycle of PWM signal is 25%, and the average current of LED is 25% of (0.2/RSENSE). It is recommended to set the PWM dimming frequency above 100Hz to prevent people's eyes from seeing LED flicker. The advantage of PWM dimming over analog dimming is that it does not change the chromaticity of LED.

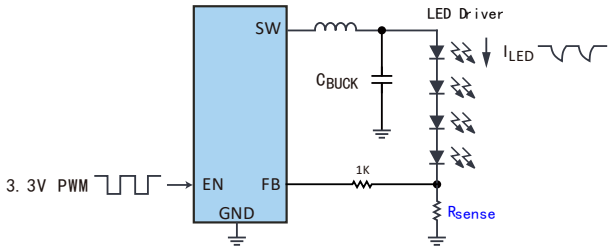


Figure 13.2 PWM Dimming via EN

Note that due to the fixed delay of soft start time and EN start, when the high pulse time of an EN is lower than 10us, the output may not respond. The minimum duty cycle of the PWM carrier frequency used can be evaluated accordingly.

Open Circuit of Lamp String (CC Mode)

When the LGS51065 works in the constant current mode, the VFB voltage will be close to 0 after the open circuit of the lamp string. At this time, the high side switch of the BUCK will be forced to open with the maximum PWM duty cycle DMAX, and the anode of the lamp string is approximately equal to the CIN voltage.

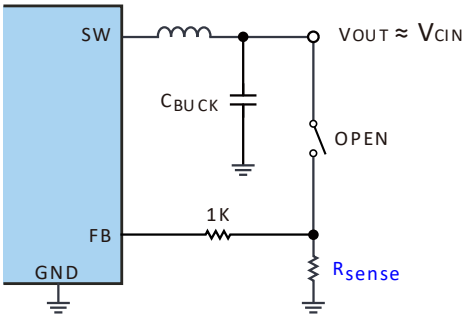


Figure 13.3 Schematic Diagram of CC Mode Lamp Bead Open Circuit

The chip can be identified under this working condition and enter the protection state, which will not cause damage. The withstand voltage selection of CBUCK capacitor under this working condition shall be considered.

Application Information: High Efficiency Step-Down Switching Regulator (CC Mode)

Inductance selection (CC mode)

The selection of inductance value needs to consider the working duty cycle and the on/off time of the power switch to ensure that the determined requirements are met within the full range of the working voltage and LED current.
The larger the inductance value, the smaller the change of LED output current in a wide input voltage range.
The recommended inductance parameter range of LGS51065 is 10uH - 47uH.
In order to obtain higher efficiency, it is recommended to choose inductance with smaller DC conduction impedance.
For most applications, the following equation can be used as a reference:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{Rsence} \times V_{IN} \times f_{SW}}$$

According to the selected inductance value, the user can calculate the actual inductance current ripple:

$$I_{L(ripple)} = \frac{V_{out} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}}$$

The saturation current of the inductor should be higher than the output peak current, and its nominal current value should be higher than the average output current.

The rms current and saturation current ratings of inductors must be greater than the ratings in the application. This ensures that the sensor does not overheat or saturate. Under power on, transient or fault conditions, the inductor current may exceed its normal operating current. Therefore, the most conservative method is to specify an inductor with a saturation current rating equal to or greater than the converter current limit.

The peak inductance current and root mean square current equations can refer to the following formulas:

$$I_{L(peak)} = I_{LED} + \frac{I_{L(ripple)}}{2}$$

$$I_{L(rms)} = \sqrt{I_{LED}^2 + \frac{I_{L(ripple)}^2}{12}}$$

Selection of output capacitance (CC)

The output capacitor can reduce the high-frequency ripple current passing through the LED string. Excessive ripple current in the LED string will increase the root mean square current in the LED string, so the LED temperature will also rise.

1) Calculate the total dynamic resistance (RLED) of the LED string using the LED manufacturer's data sheet

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#of\ LEDs$$

2) Calculate the impedance (ZOUT) required by the output capacitor and the acceptable LED peak to peak ripple current ILED (ripple). IL (ripple) is the peak to peak inductance ripple current previously calculated in inductance selection. The ripple current on the capacitor can be calculated by the following formula:

$$Z_{COUT} = \frac{R_{LED} \times \Delta I_{LED}}{I_{L(ripple)} - \Delta I_{LED}}$$

3) Calculate the required minimum effective output capacitance.

$$C_{OUT} = \frac{1}{2 \times \pi \times f_{SW} \times Z_{COUT}}$$

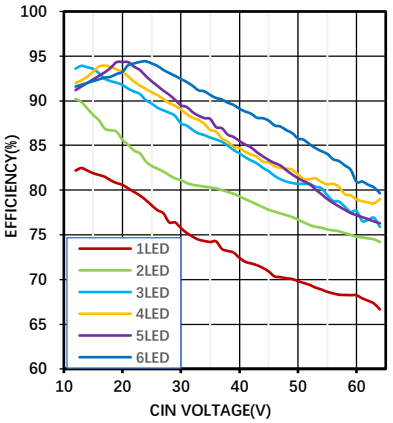
4) Increase the output capacitance appropriately according to the voltage derating effect in the capacitance manual

When the LGS51065 operates in CC mode, the 10uF capacitor can meet the requirements of most application scenarios.

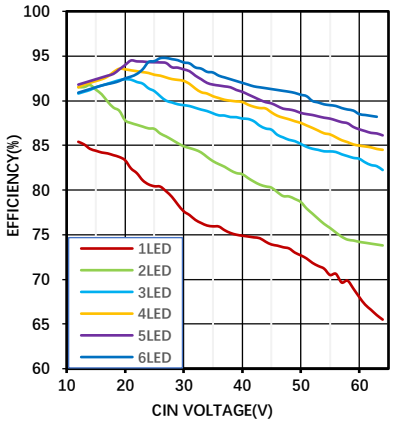
Application Information: High Efficiency Step-Down Switching Regulator: Diagram (CC Mode)

Unless otherwise specified, TA=25 ℃, VCIN value is measured with DC input.

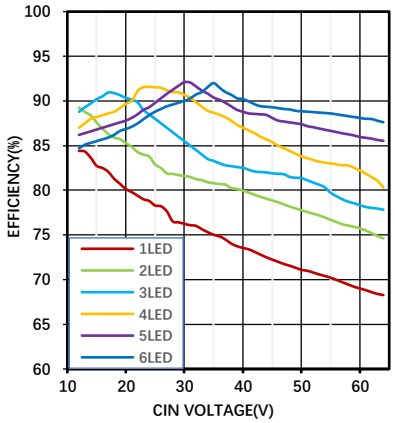
Efficiency, I_{SET}=100mA, L=10uH



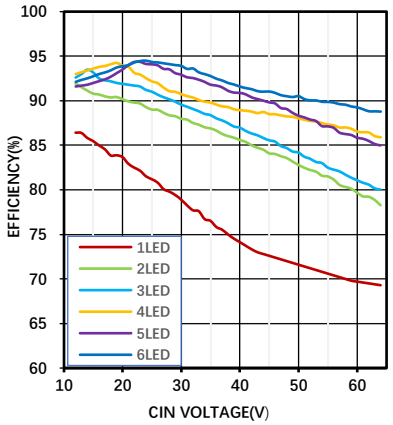
Efficiency, I_{SET}=100mA, L=22uH



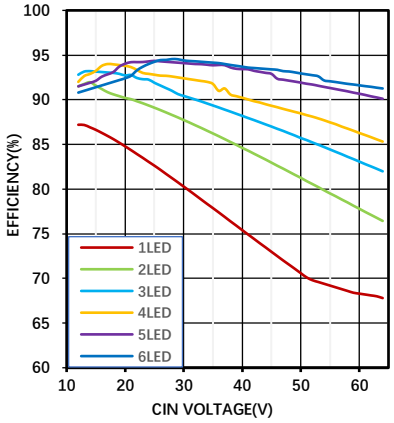
Efficiency, I_{SET21}=100mA, L=47uH



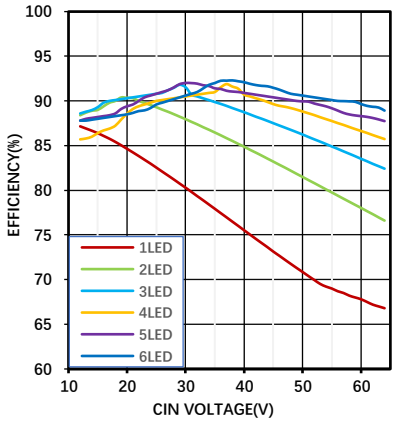
Efficiency, I_{SET}=300mA, L=10uH



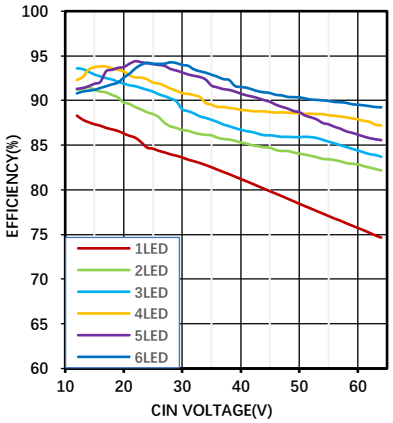
Efficiency, I_{SET}=300mA, L=22uH



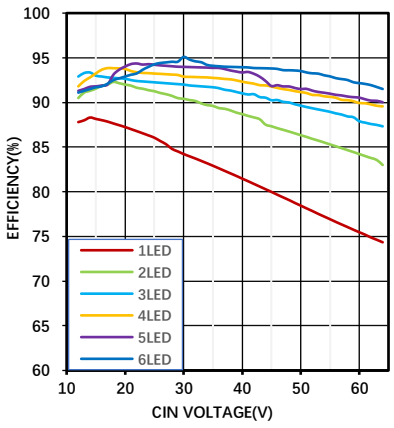
Efficiency, I_{SET}=300mA, L=47uH



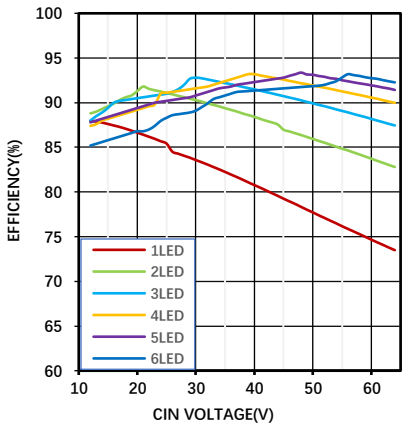
Efficiency, I_{SET}=600mA, L=10uH



Efficiency, I_{SET}=600mA, L=22uH



Efficiency, I_{SET}=600mA, L=47uH



Application Information: Wide Input Range 3.3V Constant Pressure LDO

Summary

The LGS51065 has a built-in high-voltage linear LDO, which can not only supply power to the device system core, but also output power externally.
The LDO outputs a constant voltage of 3.3V typical value, and the maximum current output capacity is 10mA
This LDO output can be used for MCU control power supply.

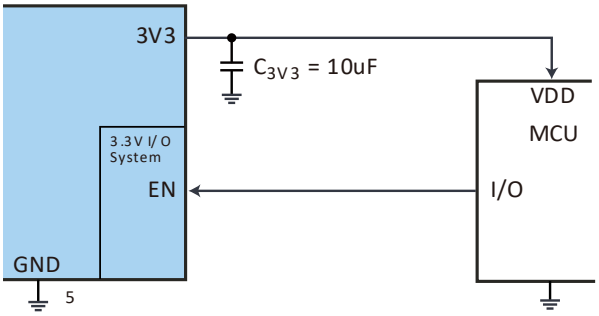


Figure 16.1 LDO output capacitor setting and low-voltage logic control IO

Note that even if the LDO function is idle, C3V3 cannot be omitted. The recommended value of C3V3 is 2.2uF.

Avoid high pressure in the output

The LDO output of the LGS51065 has only the current source capability, but no Sink capability. Therefore, high voltage should be avoided: for example, the high voltage output from BUCK is injected into LDO through a low resistance path. This may affect the LDO output accuracy, or even activate the LDO output ESD to cause damage. The ESD inside LDO will start to conduct when it exceeds 8V.

In some applications, 5V has to be used to supply power to MCU, or high voltage may be injected into the path of EN and 3V3 pins for other reasons. It is recommended to connect current limiting resistors in series to avoid affecting the accuracy of 3V3 and ensuring the long-term reliability of devices.

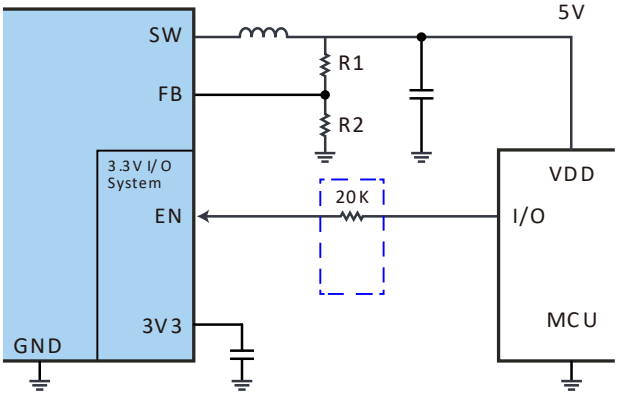


Figure 16.2 IO Processing Strategy for High Logic Level Voltage Input

LDO Output Short-Circuit Protection and Current Limiting

The LDO part of the device has complete over-current and short-circuit protection:
The output current limitation of LDO is designed to limit the output current in the following cases: the load impedance is abnormally low, including the case that the output may be directly short circuited to ground. See the "Chart" section for details.
It should be noted that continuous operation of LDO output under over-current and short-circuit conditions may trigger OTP protection.

3V3 and System Power Good (PG)

In addition to external output, LDO also supplies the internal system core of the device. A good power supply indication (3V3. PG) will be generated when the 3V3 is successfully established internally, and the BUCK function and communication module can only be opened.

Therefore, it should be noted that when LDO external load over-current or short circuit occurs, LDO output voltage will not be damaged after falling below 3V3.PG (Falling) threshold, but the system may enter the protection state. The BUCK and communication module will be turned off.

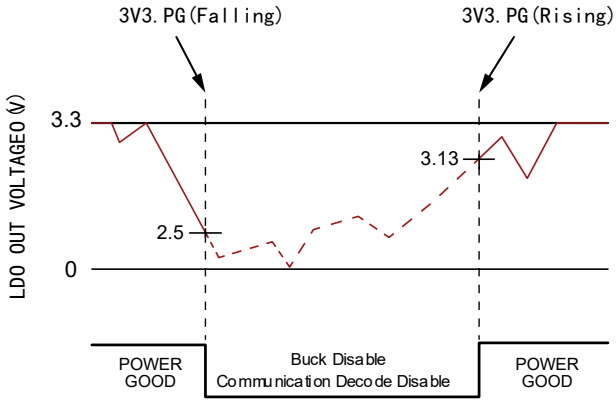


Figure 16.3 PG (Falling) and PG (Rising) Thresholds

Conditions that can cause LDO output to be Closed

1) LDO output is turned on by default, and the following two conditions can cause LDO output to turn off in the system:
2) UVLO undervoltage protection triggered
3) OTP over temperature protection triggered

Application Information: Reference Layout Example

Summary

The high integration of LGS51065 makes PCB layout very simple and easy. The poor layout will affect the performance of LGS51065, resulting in electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground jump and voltage loss, which will affect the voltage regulation and stability. In order to optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and routing to ensure optimal performance:

- The high-frequency ceramic input capacitor CIN. C must be placed as close as possible to the CIN (PIN5) and GND (PIN2) pins to minimize high-frequency noise.
- For the high current path, use a large copper clad area of PCB, including GND pin (PIN2). This helps minimize PCB conduction loss and thermal stress.
- In order to minimize the via conduction loss and reduce the thermal stress of the module, multiple via shall be used to realize the interconnection between the top layer and other power layers or strata.
- When BUCK is working in CC mode, attention should be paid to avoid high heat LED lamp set away from the chip or heat island design for thermal isolation.
- The loss of ACR and DCR caused by inductance and the heat conduction to the chip shall be considered. The inductor can be placed far away or the heat island can be reasonably designed as appropriate.
- FB pin impedance is high, and lead track should be as short as possible and far away from high noise SW node or shielded.

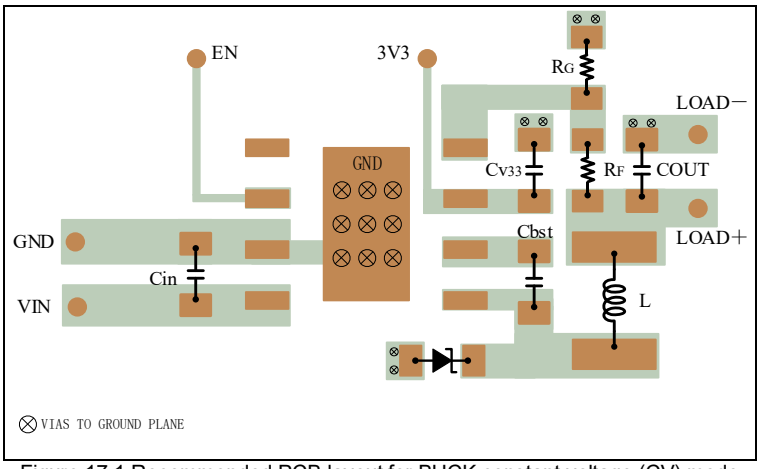


Figure 17.1 Recommended PCB layout for BUCK constant voltage (CV) mode

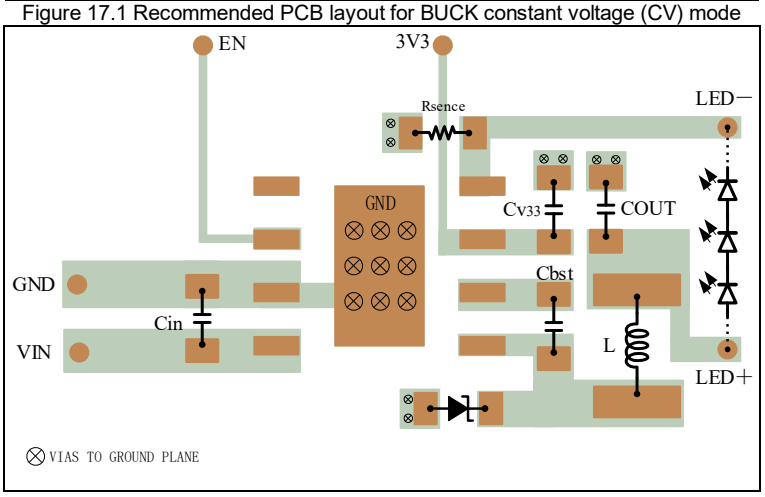
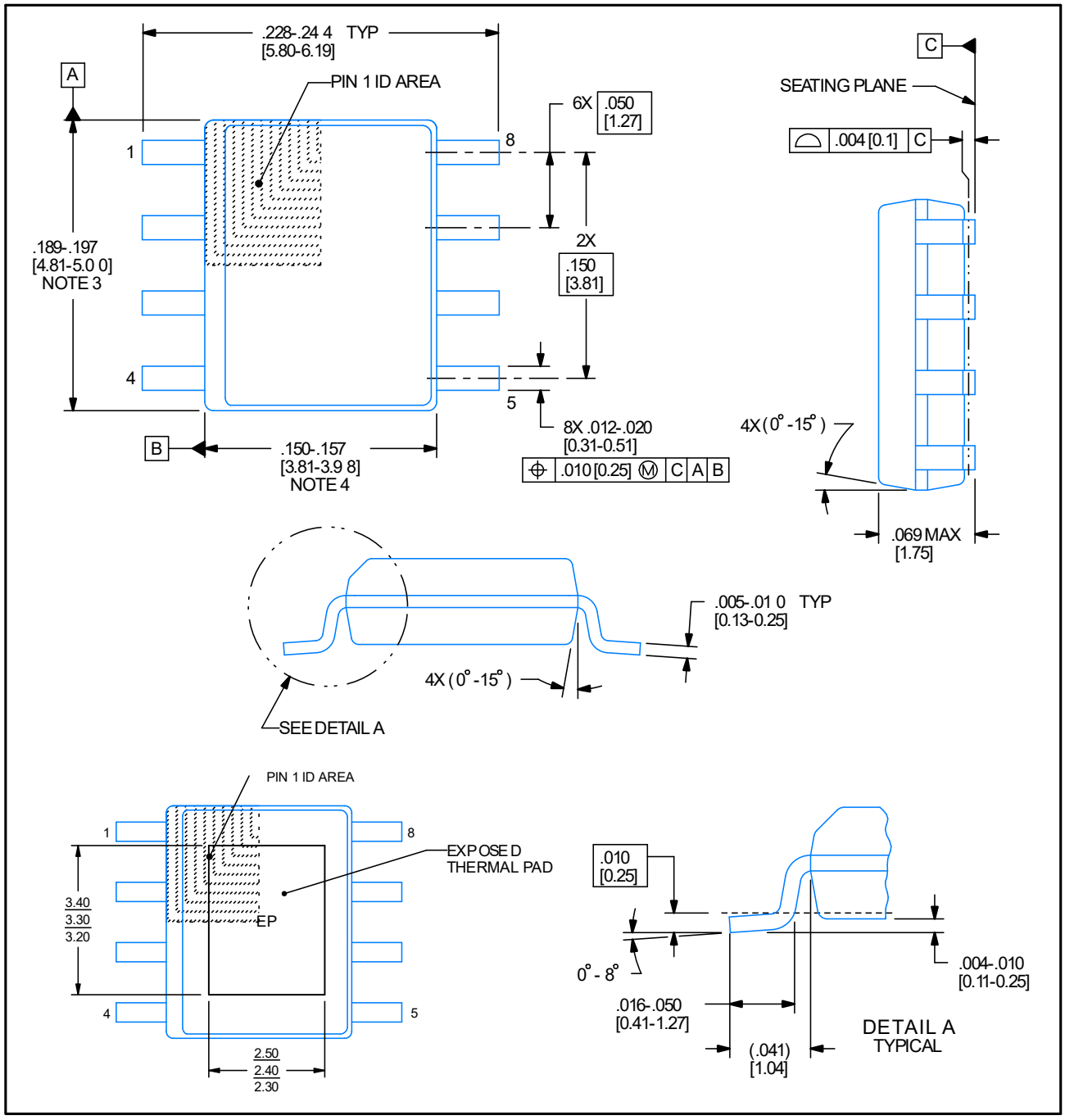


Figure 17.2 Recommended PCB layout for BUCK constant voltage (CC) mode

Footprint Description

8-pin plastic encapsulated SOIC with bottom EPAD



Note:

(1) All data units are in millimeters. Any dimensions in brackets are for reference only.

(2) This drawing is subject to change without notice.

(3) This dimension does not include molding burrs, projections, or nozzle burrs. The burr or protrusion on each side of the mold shall not exceed 0.15 mm.

(4) This dimension does not include the burr of the mold, and the burr or protrusion on each side of the mold does not exceed 0.25mm.

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