55V/1000mA 1.2MHz High Efficiency Asynchronous Buck Converter with Light Load SKIP Mode

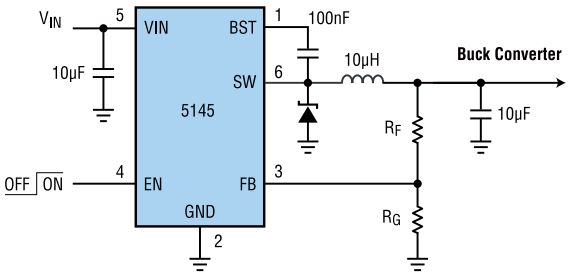
Check for Samples: LGS5145

Characterization

- Junction temperature range from -40°C to +125°C
- All ports are ESD protected to 3000V (HBM).
- Wide input voltage range: 4.5V-55V
- 600mΩ High Side Metal Oxide Semiconductor Field Effect Transistors
- At least 1000mA continuous current output capability
- Up to 90% efficiency
- SKIP mode provides very high light load efficiency
- 1.2MHz fixed operating frequency
- Internal compensation helps reduce solution size, cost and design complexity
- Supports capacitive start for large loads
- Cycle-by-cycle overcurrent protection
- Output short circuit protection
- thermal shutdown protection
- Available in ultra-small package SOT23-6 package

Appliance

- wattmeter
- Pre-stabilizer for linear regulators
- Distributed Power Systems
- WLED Driver
- Battery charging



Typical Application Topology

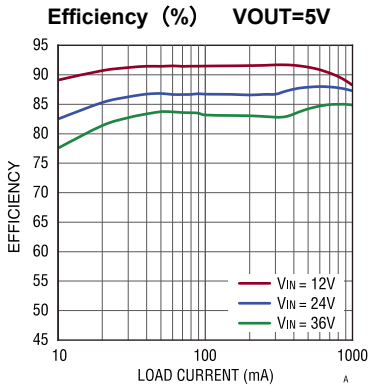
Descriptive

The LGS5145 is a step-down DC/DC regulator with internal switching, featuring SKIP control mode, which combines low quiescent current with high switching frequency to achieve high efficiency over a wide range of load currents. The SKIP mode uses a short “burst” cycle to switch the inductor current through the internal power MOSFETs, followed by a sleep cycle in which the power switch is turned off and the load current is supplied by the output capacitor. At light loads, the burst cycle is a fraction of the total cycle time, minimizing the average supply current and greatly improving efficiency at light loads.

The LGS5145 has a wide input voltage range of 4.5V-55V, minimizing the need for external surge suppression components.The LGS5145 features an integrated low resistance 0.6Ω high-side power MOSFET that provides at least 1A of output current capability with excellent load and line transient response.

The LGS5145 can be used in a variety of applications to efficiently regulate higher voltages.This regulator is well suited for the 42V automotive power bus range.Additional features include: soft-start, thermal shutdown, UVLO undervoltage lockout, gate driver undervoltage lockout, maximum duty cycle limit timer, and smart current limit shutdown timer. Wells also integrates output short-circuit protection, providing a Frequency FOLD-BACK mode at low FB voltages to avoid overheating in the event of a short-circuit.

The LGS5145 is available in a small 6-pin SOT23-6 package. Its 0.95mm pin pitch can be implemented for high voltage applications.



Absolute Maximum (†)

Table 2.1

parameters	realm
Pin to GND Voltage（VIN,SW,EN）	-0.3V~60V
Pin to GND Voltage（BST）	-0.3V~SW+6V
Pin to GND Voltage（FB）	-0.3~6V
Storage temperature	-65℃ to 150℃
operating temperature	-40℃ to 105℃
ESD Rating（HBM）	±3KV
ESD Rating（CDM）	±1KV
ESD Rating（MM）	±500V

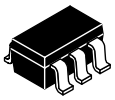
† NOTE: If the device is operated in conditions exceeding the "Absolute Maximums" listed above, permanent damage to the device may occur. This is a limiting parameter only and it is not recommended that the device be operated at or above these limits. Prolonged operation of the device under extreme conditions may affect its reliability.

ESD 警告

ESD (electrostatic discharge) sensitive devices。
Charged devices and circuit boards may discharge without being detected. Although this product has a patented or proprietary protection circuit, the device may be damaged when encountering high energy ESD. Therefore, appropriate ESD precautions should be taken to avoid degradation of device performance or loss of functionality.

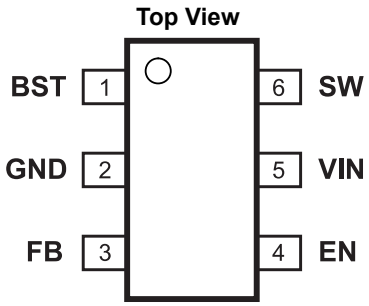
引脚排列

Figure 2 Pin Arrangement



SOT23-6 Package

6-LEAD PLASTIC SOT23



T_{MAX}=125°C,θ_{JA}=173°C/W

Package and Pin Arrangement

Table 2.2 Pin Function Descriptions

Pin Number	Pin Name	clarification
1	BST	Bootstrap gate driver power supply. A high quality 100nF ceramic capacitor needs to be connected between BST and SW to bias the internal high voltage side gate driver. Please note this capacitor withstanding voltage.
2	GND	ground pin
3	FB	Feedback Input Pin. Connected to an external resistor divider, this pin has an internal comparator voltage of 0.812V.
4 (1)	EN	Regulator output enable pin, set high to enable the output; null or low to turn off the regulator output.
5	VIN	Regulator power input. Use a 2.2μF or larger ceramic patch to bypass VIN to GND as close as possible.
6	SW	Internal power switching node. Externally connected power inductor, Schottky diode, and CBST capacitor.

（1）100nA weak pull-down is built-in, in order to get better anti-jamming ability, it is recommended to use pull-down resistor or use IO to set low, it is not recommended to leave it hanging. If you need to turn on the output automatically, you can connect this pin directly to VIN (PIN5).

Technical specifications

Limit values apply to the working junction temperature (TJ) range of -40°C to +125°C unless otherwise stated. Minimum and maximum limit values are specified by test, validation and statistical correlation. Typical values represent the most likely parameter specification at TJ = 25°C and are for reference only. All voltages are relative to GND.

Table 3.

parameters		test condition	minimum value	typical value	maximum values	unit
输入特性						
V_{IN}	Recommended Input Voltage Range		5		55	V
V_{UVLO}	Input undervoltage lockout	Rising		4.2		V
		Falling		3.5		V
I_Q	Static operating current	No load,VIN=12V, not switching		150		uA
I_S	Shutdown Current	EN=0,VIN=12V		4		uA
Switching Characteristics						
$R_{DS(ON)}$	BUCK upper tube RDSON	TJ= 25℃		600		mΩ
V_{FB}	FB Feedback Voltage		0.792	0.812	0.832	V
F_{SW}	switching frequency	PWM Operation	1	1.2	1.4	Mhz
F_{SW_FB}	Burp switching frequency	EN=1,FB=0.1V		300		Khz
D_{MAX}	Maximum Duty Cycle		90	94		%
$I_{LIMIT.SW(Peak)}$	SW Current Limit			1.2		A
$T_{D.EN}$	EN delay	EN=0 ⌐ EN=1		60		uS
$T_{ON.MIN}$	Minimum on-time			60		nA
t_{SS}	soft start time			2.4		mS
$I_{FB.BIAS}$	FB bias current			5		nA
$I_{SW.LKG}$	SW leakage current			1		uA
I/O Specifications						
V_{EN_H}	Input EN high logic threshold	4.5V≤VIN≤52V		1.4		V
V_{EN_L}	Input EN low logic threshold	4.5V≤VIN≤52V		1		V
I_{LKG-EN}	EN Input Current	4.5V≤VIN≤52V		1		uA
Global Thermal Protection Features						
T_{OTP-R}	overtemperature protection	TJ Rising		150		℃
T_{OTP-F}	Over-temperature protection release	TJ Falling		130		℃
thermal resistance						
θ_{JA}	Thermal resistivity from silicon core to surrounding air	0 LFPM Air Flow		173		℃/W
θ_{JB}	Thermal resistivity of silicon core to PCB board surface			33.2		℃/W
θ_{JCtop}	Coefficient of thermal resistance from silicon core to package upper surface			116		℃/W
Ψ_{JB}	Thermal resistivity of silicon core to PCB board surface			30		℃/W

Functional Block Diagram

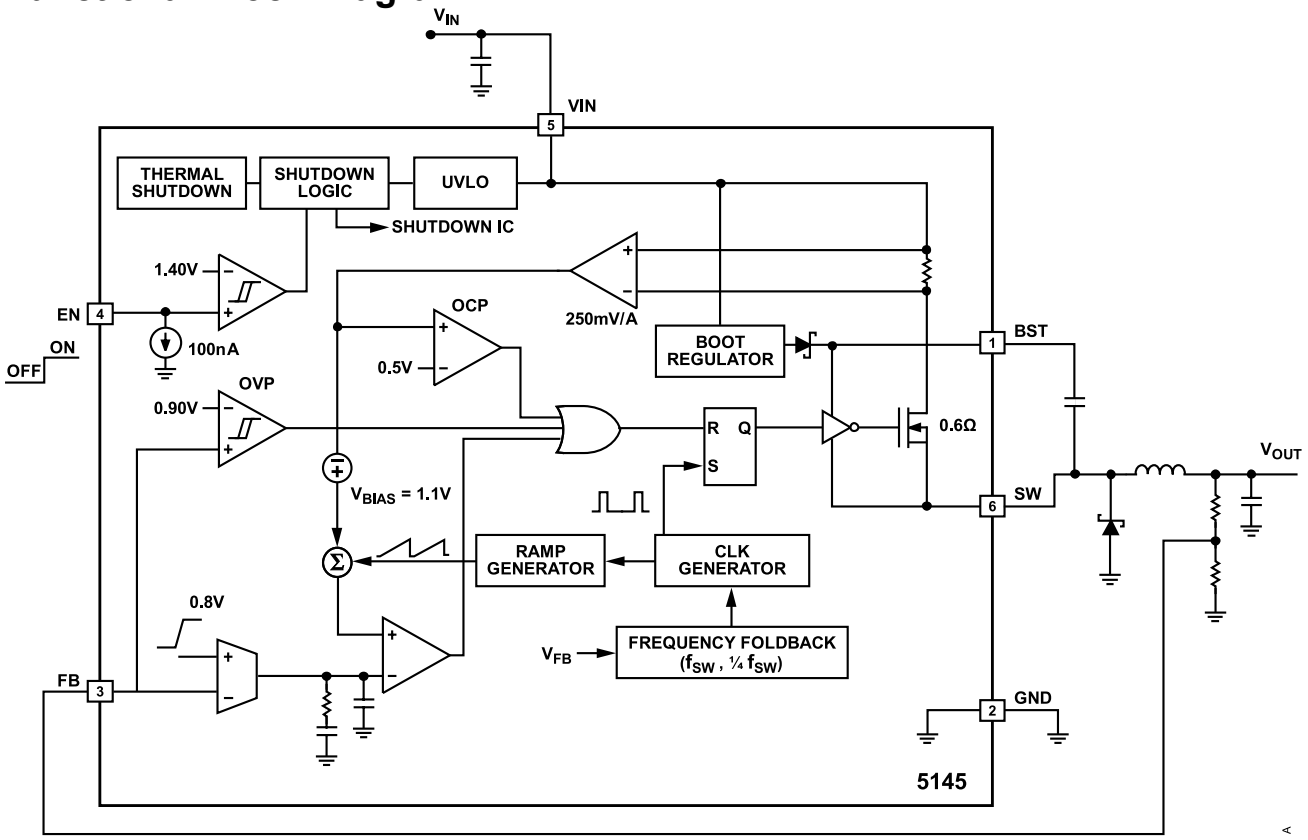


Figure 4 Internal Function Block Diagram

Application Information: Typical Application Circuits

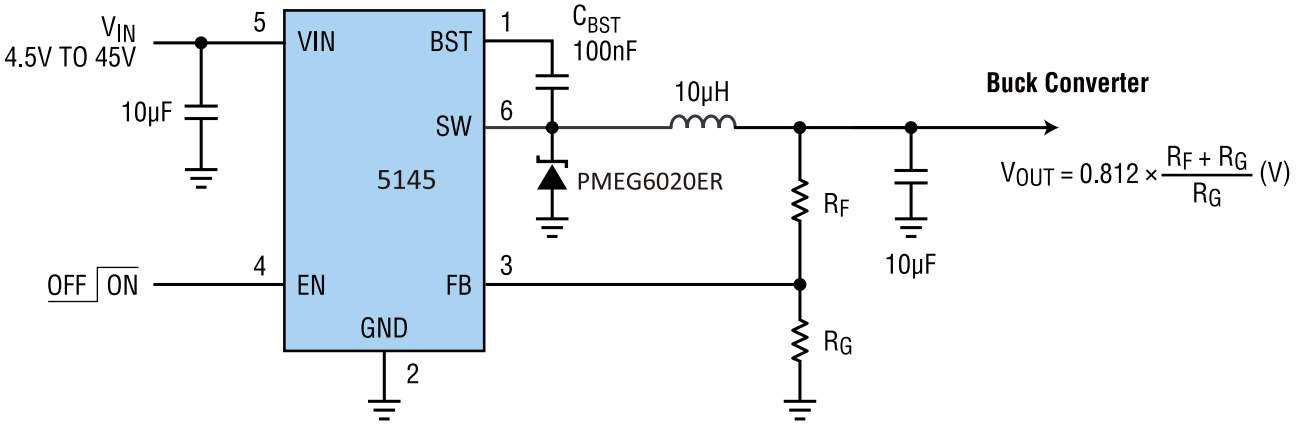


Figure 5.a Typical application topology for DC-DC buck mode

NOTE：

(1) Recommended input capacitors are 10uF X7R or X5R ceramic capacitors placed as close as possible to the power input pins 4 and 5.

(2) Select a ceramic capacitor with a withstand voltage of 16V or more for the CBST and place it as close as possible to pins 1 and 6.

Application Information: High Efficiency Step-Down Switching Regulators (Overview)

Summarize

The LGS5145 is an internal switching step-down DC/DC regulator with SKIP control mode that combines low quiescent current with high switching frequency for high efficiency over a wide range of load currents.
Additional features include: soft-start, thermal shutdown, UVLO undervoltage lockout, gate driver undervoltage lockout, maximum duty cycle limit timer, and intelligent current limit shutdown timer. Short-circuit protection provides a frequency FOLD-BACK at low FB voltage to avoid overheating in case of a short-circuit.

Setting Output Voltage

The LGS5145 output voltage is externally adjustable through a resistor divider network. Suggested output voltage resistor values are shown in the table below.

The voltage divider network consists of RG and RF, please ensure that RG is less than or equal to 30 K. The converter regulates the output voltage by keeping the voltage on the FB pin equal to the internal reference voltage VREF.

Once RG is selected the value of RF can be selected based on VFB, which is typically 0.812V:

$$V_{OUT} = 0.812 \times \frac{R_F + R_G}{R_G} \quad (V)$$

Table 6. Output Voltage Setting Quick Configuration

VOUT	RF	RG	设定误差（1）	
2.5V	6.8K	3.3K	2.49V	-0.88%
3.3V	13K	4.3K	3.27V	-1.33%
4.2V	16K	3.9K	4.14V	-1.67%
5.0V	82K	16K	4.97V	-0.63%
8.0V	160K	18K	8.03V	0.41%
12.0V	300K	22K	11.88V	-1.03%

（1）Other voltage divider pairs and high precision resistors are also available for higher setting accuracy.

SKIP Pulse Jump Mode

The LGS5145 has a built-in jump-pulse circuit; at light loads, this circuit is turned on; it switches only when necessary to keep the output voltage within the specified range. This reduces switching losses and allows the converter to maintain high efficiency under light load conditions.

In burst pulse mode, when the output voltage drops below the specified value, the LGS5145 enters PWM mode and stays in oscillator for several oscillator cycles to bring the output voltage up to the specified range. During the wait time between burst pulses, the power switch is disconnected and all load current is supplied by the output capacitor. The output voltage ripple in this mode is greater than that in the PWM mode of operation, since the output voltage dips and recovers at irregular intervals.

CFF Feedforward Compensation Capacitor

In some cases, such as high load transient response or high light load ripple requirements, feed forward capacitors can be connected in parallel to RF to improve the load transient response or to improve the phase margin of the loop.

CFF and RF form a high frequency “zero point”, so that the phase is ahead of the phase, thus increasing the phase margin. To reduce SKIP mode ripple and improve the transient response of the voltage loop.

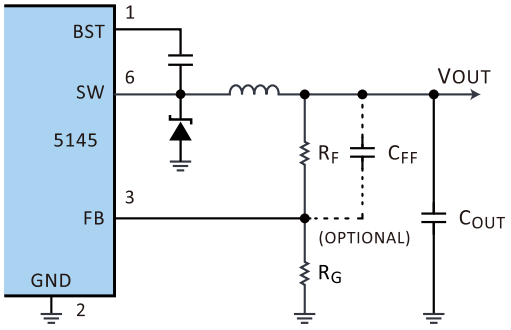


Figure 6.1 BUCK constant voltage mode with CFF front compensation capacitor

CFF can be calculated according to the following formula:

$$C_{FF} = \frac{1}{2\pi \times F_{SW} \times (R_F \,//\, R_G)}$$

Typically, 47pF is a good place to start.

Application Information: High Efficiency Step-Down Switching Regulators (Overview)

Role of EN

Enable input pin for BUCK. Driving EN to a high state turns on the converter of the BUCK; driving EN to a low state turns off the converter. This pin has two independent thresholds, the rising threshold is greater than 1.4V to enable the output, falling below 1V to turn off the regulator output, enter the low-power sleep mode. This pin has an internal weak pull-down.

The voltage withstand of this pin is the same as VIN (PIN4). The easiest way to realize the operation of the LGS5145 is to connect the EN pin to the VIN pin. This allows the device to self-start when VIN is in the operating range.

External logic signals can also be used to drive the EN input for system sequencing and protection. Due to the weak internal pull-down, an external pull-down resistor can be used if a reliable shutdown is required, and it is not recommended to leave this pin idle.

Table 7. pin EN operating state

pin	*orientations*	*Pin Status*	*functionality*
EN (Pin4)	Input	high	BUCK output enable
		low	BUCK output turned off

Enable failure conditions for BUCK

In addition to the EN pin status, it should also be noted that the following mechanisms can also turn off the BUCK output:

1) UVLO undervoltage protection triggered
2) OTP over temperature protection triggered

Input undervoltage protection (VULO)

An internal undervoltage locking circuit is included on the VIN pin of the device. When the VIN voltage drops below the threshold of UVLO, UVLO protection will be triggered to turn off the output of the voltage regulator. The rise threshold of this UVLO is about 4.4V. After the VIN reaches this voltage and the UVLO is removed, the controller will enter the soft start process.

Maximum Duty Cycle DMAX

When the input voltage drops close to the output voltage, the BUCK switches to the maximum duty cycle operating state. At this time, the low-end N-channel MOSFET is in the open state, reducing the turn off time to the shortest possible. Under maximum duty cycle operating conditions, as the output voltage is the product of the input voltage value and the maximum duty cycle limit, the output voltage drops sharply below the adjustment range.

Soft-Start

LGS5145 has an internal soft start of approximately 2.4ms. Soft start can prevent under damping and overshoot of the input power supply of the converter during the startup process. When the chip starts, the internal circuit generates a soft start voltage (SS). Rising at a fixed rate. During soft start, the output voltage will track the internal node voltage ramp proportionally.

When it is less than the internal reference (REF), SS covers REF, so the error amplifier uses SS as the reference. When SS exceeds REF, REF resumes control. Throughout the entire startup phase, the switch current limitation remains effective, which can reliably avoid situations where power is applied and a short circuit occurs.

When there is a very large capacitance in the output (such as 2200uf or even larger), the speed of output voltage rise will be slower than SS, limited by the maximum switch current limit, and the time to start to the target voltage setting value will be greater than the soft start time.

OTP

The thermal overload protection circuit limits the junction temperature to below 150 ℃ (typical value). Under extreme conditions (i.e. high ambient temperature and/or high power consumption), when the junction temperature begins to rise above 150 ℃, Over Temperature Protection (OTP) over temperature protection is activated, and the system will forcibly shut down the regulator output (if EN is enabled). When the junction temperature drops below 130 ° C, the OTP state will be unlocked, the voltage regulator output will be reopened, and the output current will return to normal operating values.

Thermal overload protection aims to protect devices from the effects of instantaneous accidental overload conditions.

The guaranteed operating junction temperature range of this device is -40 ° C to 105 ° C. High junction temperature will reduce the working life; When the junction temperature reaches 125 ° C for a long time, the lifespan of the device will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions and circuit board layout, rated packaging thermal resistance, and other environmental factors.

The junction temperature (TJ, unit: ℃) is calculated based on the ambient temperature (TA, unit: ℃) and power consumption (PD, unit: W). The calculation formula is as follows：

$$\boldsymbol{T_J = T_A + (P_D \times \theta_{JA})}$$

among θ JA (in ℃/W) is the thermal resistance of the package. The calculation method and thermal resistance model can be found in the "High Temperature Considerations" section for details.

Application information: High efficiency step-down switch voltage regulator (overview)

Output overload and short circuit protection

LGS5145 will allow short-circuit output. There are several characteristics used for protection in case of output short circuit and load overcurrent. The first method is that when FB is below the set value, the switching frequency will decrease to maintain inductor current control. Secondly, monitor the current of the upper tube switch, exceeding the safe level will end this cycle.

Output short-circuit protection and frequency folding

LGS5145 includes a Frequency Foldback mechanism,

To prevent excessive heat generation in the event of load current loss of control or output short circuit. When the voltage at the FB pin drops below a certain value, the switching frequency decreases, which causes the inductance current to decrease for a longer time, but increases the ripple current while adjusting the peak current. This leads to a decrease in the average output current and prevents the output current from losing control. The relationship between switch frequency and FB pin voltage is shown in Table 8.

Table 8. Correlation between Switching Frequency and FB Pin Voltage

FB pin voltage	switching frequency
VFB＞0.25V	f_{SW}
VFB≤0.25V	$1/4 f_{SW}$

After the short circuit (VFB ≤ 0.25V) is removed, the soft start starts to operate to adjust the output back to the set value during normal operation, which helps to limit surge current and prevent possible output voltage overshoot.

Switch current limiting protection

The output of the regulator has a periodic overcurrent limit. When SW current triggers L LIMITED SW (Peak), BUCK output will enter a cycle by cycle current limiting state.

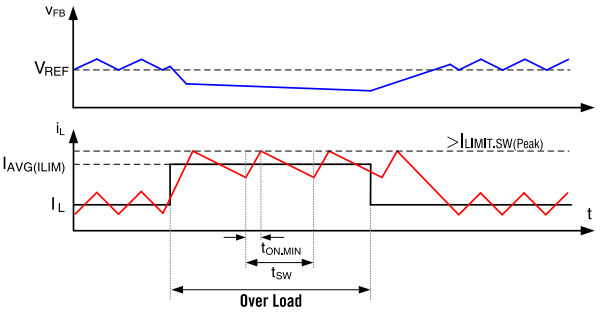


Figure 8.1 Description of BUCK output overcurrent behavior at Mtop

ILIMIT SW (Peak) is related to inductance size and input voltage difference, ILIMIT SW (Peak) is only the reference minimum value. When overcurrent or short circuit occurs for a long time, global OTP protection may be triggered.

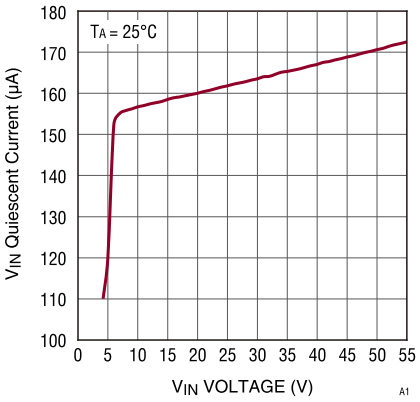
Selection of Bootstrap Capacitors

LGS5145 has an integrated boost voltage regulator that requires a small ceramic capacitor between the BST and SW pins to provide gate drive voltage for the high-voltage side MOSFET. When the high side MOSFE is turned off and the low side diode is conducting, the CBST capacitor is charged. The value of this ceramic capacitor should be 0.1 μ F, connected between the BST and SW pins for normal operation. It is recommended to use X7R or X5R level dielectric ceramic capacitors with a rated voltage of 10V or higher, as they have stable temperature and voltage characteristics. The rated voltage of capacitors should be 16V or higher.

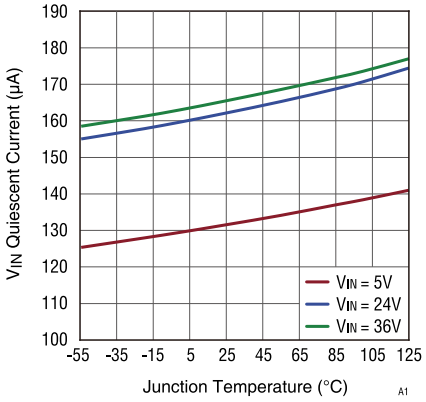
Application information: High efficiency step-down switch regulator (chart)1

Unless otherwise specified, T_A=25℃：

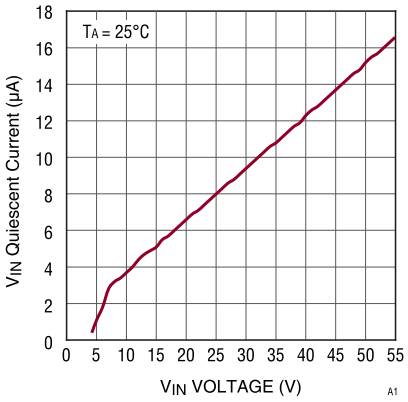
V_{IN} Quiescent Current vs V_{IN} Voltage, Not Switching



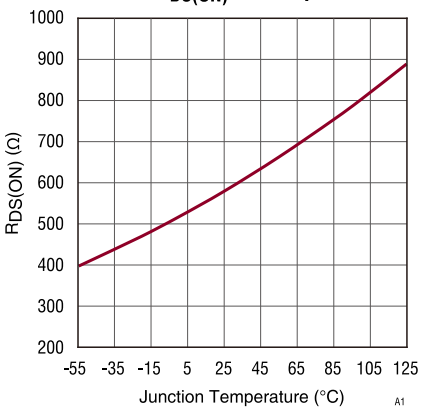
V_{IN} Quiescent Current vs Temperature, Not Switching



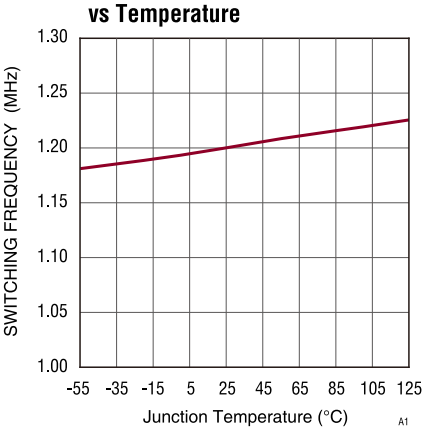
V_{IN} Shutdown Current vs V_{IN} Voltage(EN = 0V)



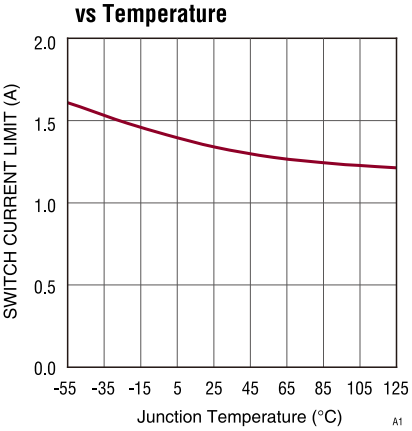
Switch $R_{DS(ON)}$ vs Temperature



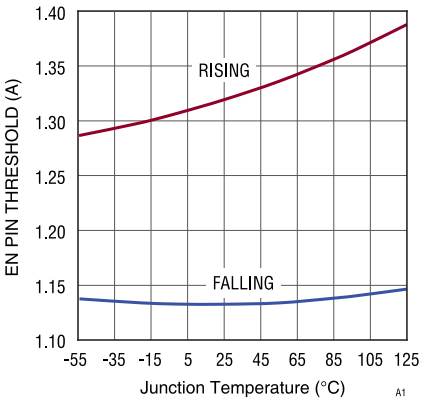
Oscillator Frequency vs Temperature



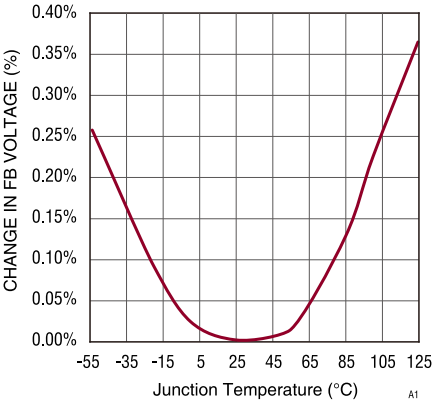
Switch Current Limit vs Temperature



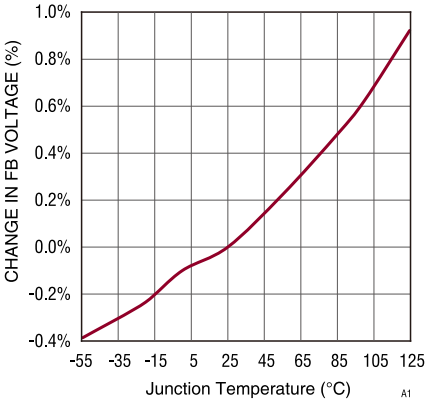
EN Pin Threshold vs Temperature



FB Voltage vs Temperature



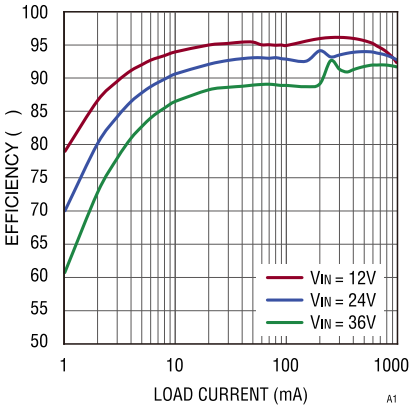
Burst Mode Operation, FB Voltage vs Temperature



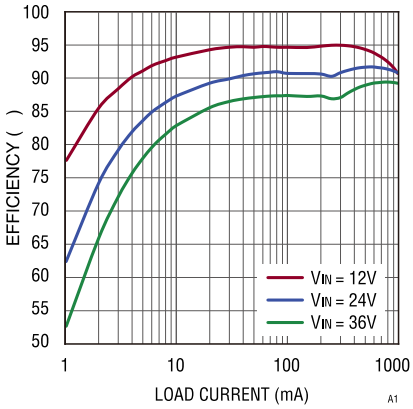
Application information: High efficiency step-down switch regulator (chart)) 2

Unless otherwise specified, T_A=25℃:

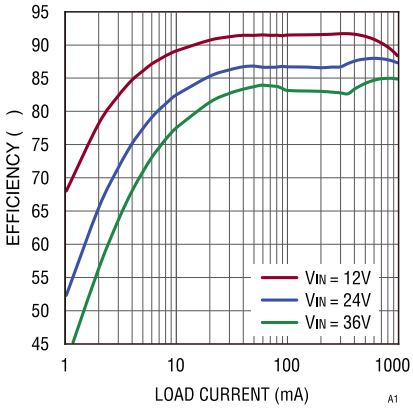
Efficiency, V_{OUT} = 12V



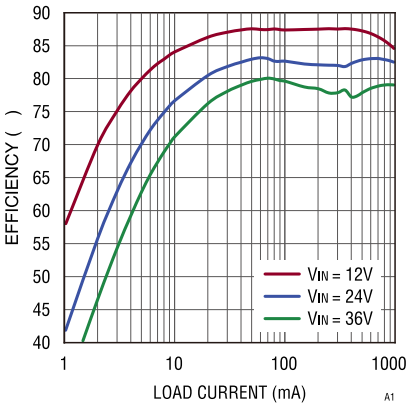
Efficiency, V_{OUT} = 8V



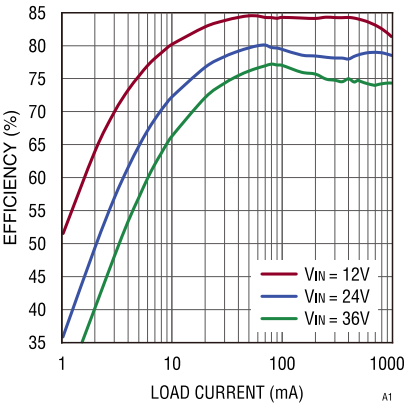
Efficiency, V_{OUT} = 5V



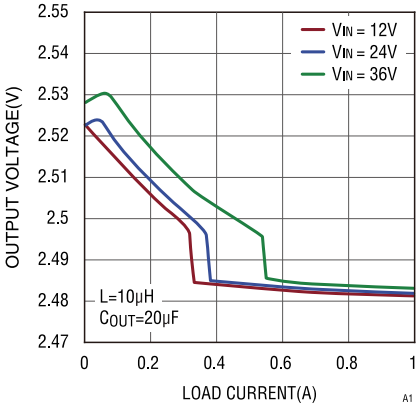
Efficiency, V_{OUT} = 3.3V



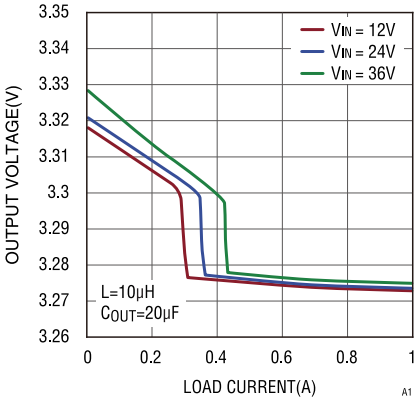
Efficiency, V_{OUT} = 2.5V



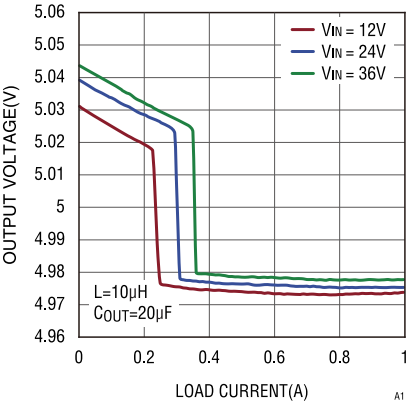
Load Regulation,V_{OUT} = 2.5V



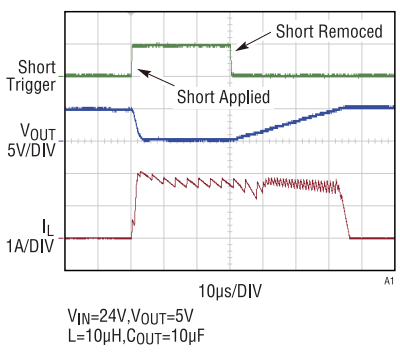
Load Regulation,V_{OUT} = 3.3V



Load Regulation,V_{OUT} = 5V



Short Circult and Recovery

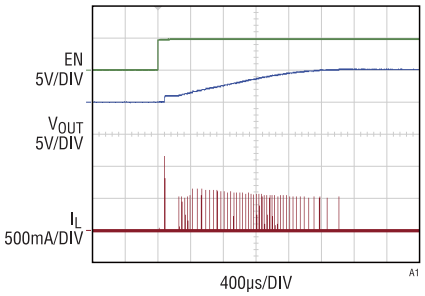


VIN=24V,VOUT=5V
L=10μH,COUT=10μF

Application information: High efficiency step-down switch regulator (chart)3

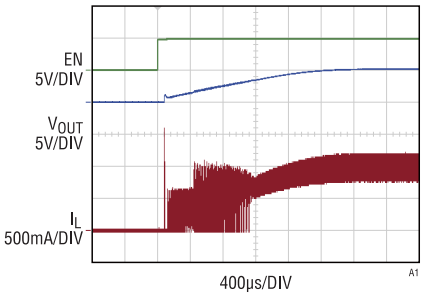
Unless otherwise specified, T_A=25℃:

Start-Up Waveforms NO LOAD



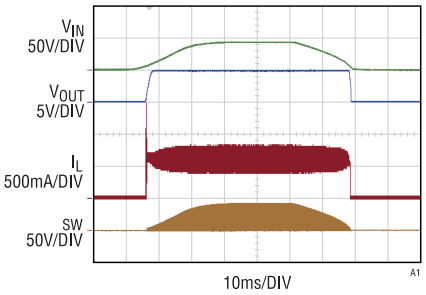
45V_{IN} to 5V_{OUT},NO LOAD
L=10uH,C_{OUT}=10uF

Start-Up Waveforms 5R LOAD



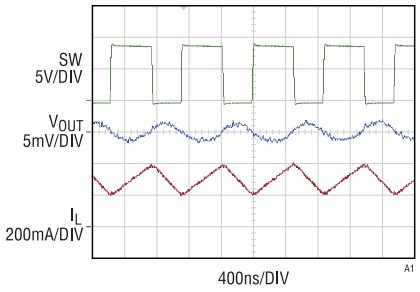
45V_{IN} to 5V_{OUT},LOAD = 5Ω
L=10uH,C_{OUT}=10uF

Power Up and Power Down EN = V_{IN}



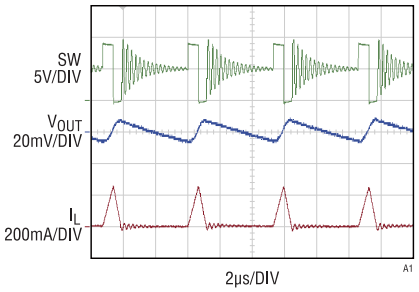
45V_{IN} to 5V_{OUT},LOAD = 600mA
L=10µH,C_{OUT}=10µF

Switching Waveforms, PWM Mode



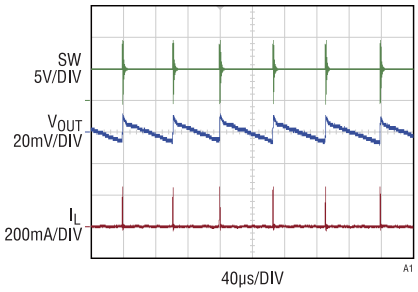
V_{IN}=9V,V_{OUT}=5V,LOAD=300mA
L=10µH,C_{OUT}=10µF

Switching Waveforms, Burst Mode Operation



V_{IN}=9V,V_{OUT}=5V,LOAD=28mA
L=10µH,C_{OUT}=10µF

Switching Waveforms, Pulse Skip Mode



V_{IN}=9V,V_{OUT}=5V,LOAD=2mA
L=10µH,C_{OUT}=10µF

Application information: Other considerations and design experience suggestions

Hot swapping security

Ceramic capacitors have advantages such as small size, good stability, and low impedance, making them an ideal choice for input bypass capacitors in LGS5145 circuits. However, if LGS5145 is plugged into a live power source, these capacitors may cause problems. A ceramic capacitor with low ESR characteristics and a stray inductor connected in series with the power supply form an underdamped slot circuit. The voltage at the VIN pin of LGS5145 may reach twice the nominal input voltage, exceed the rated value of LGS5145, and damage the parts. If the input power control is improper or the user needs to plug LGS5145 into the power supply, the design of the input network should prevent such overshoot.

Figure 20 shows the waveform generated when the LGS5145 circuit is connected to a 24V power supply through a 6-foot (2m) 24AW twisted pair. The first figure shows the instantaneous response of a ceramic capacitor with a 2.2 μ input terminal. The input voltage is as high as 35V, and the peak input current is 20A.

One way to improve and prevent the impact of this problem is to add another capacitor with a series resistor in the circuit. An aluminum electrolytic capacitor has been added in Figure 20b. The damping generated by the high equivalent series resistance of this capacitor can eliminate voltage overshoot. The additional capacitance improves the input ripple and can slightly increase the efficiency of the circuit, although it may be the largest component in the circuit.

Another solution is shown in Figure 20c. A 1 Ω resistor is connected in series with the input to eliminate voltage overshoot (which also reduces the peak input current). A 0.1 μ F capacitor improves high-frequency filtering. This solution is smaller and cheaper than electrolytic capacitors. For high input voltage, its impact on efficiency is minimal.

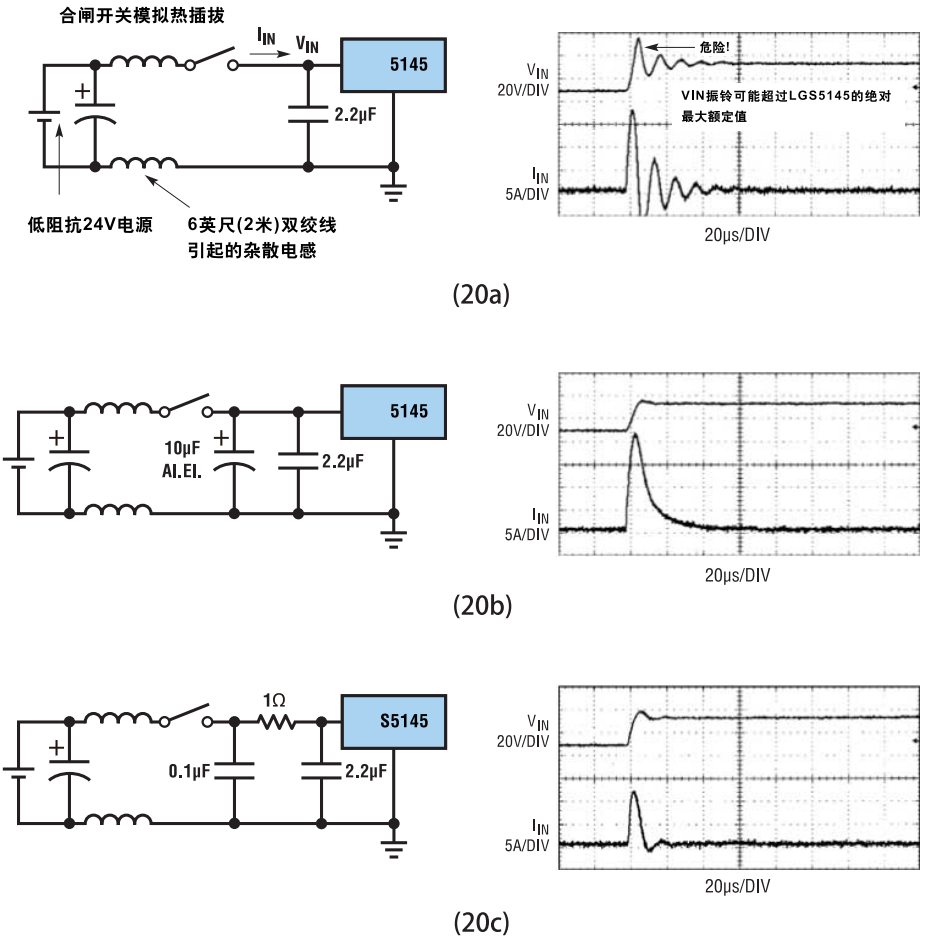


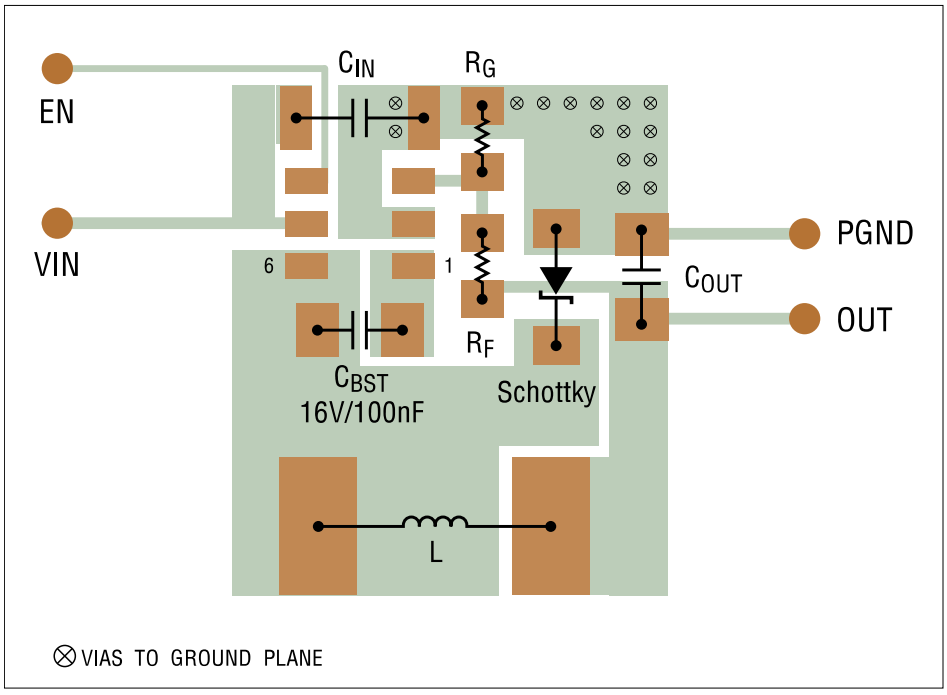
Figure 24 Carefully selected input network can prevent input voltage overshoot and ensure reliable operation of LGS5145 when connected to a live power source

Application Information: Reference Layout Example

Summary

The high integration of LGS5145 makes PCB board layout very simple and easy. Poor layout can affect the performance of LGS5145, causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground jumping, and voltage loss, thereby affecting voltage regulation and stability. To optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and wiring, ensuring optimal performance:

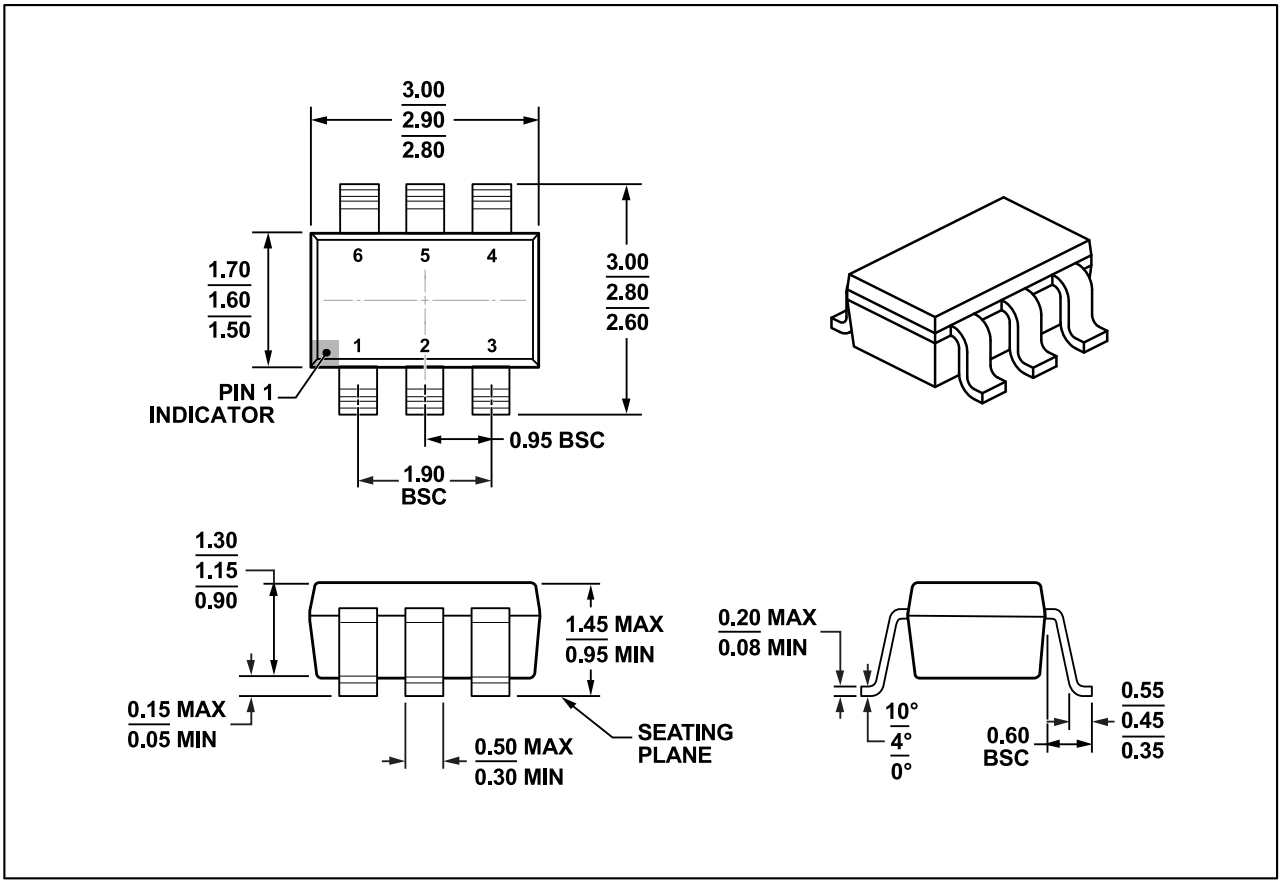
- The high-frequency ceramic input capacitor CIN must be placed as close as possible to the VIN (PIN5) and GND (PIN2) pins to minimize high-frequency noise
- For high current paths, a larger PCB copper-clad area should be used, including GND pins (PIN2). This helps to minimize PCB conduction loss and thermal stress to the maximum extent possible
- The conduction loss of the rectifier diode should be considered, and the thermal corona caused by it should be transmitted to the chip. The diode can be placed away from the chip, or the heat island can be designed reasonably
- To minimize through hole conduction loss and reduce module thermal stress, multiple through holes should be used to achieve interconnection between the top layer and other power layers or layers.
- The ACR and DCR losses generated by inductance should be considered, and the heat generated should be conducted to the chip. Inductors can be placed slightly further away or heat islands can be designed appropriately.
- The impedance of FB pins is high, and the lead trajectory should be as short as possible and kept away from high noise SW nodes or shielded



21.1 Figure 6a

Package Description

1.45mm height 6Pin SOT-23 Plastic sealing SOIC



notes：

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only. Dimensions and tolerances in accordance with ASME Y14.5M.

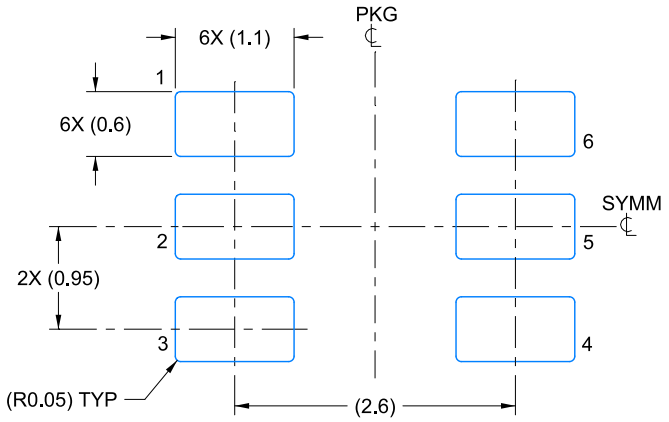
(2) This image is subject to change without prior notice

(3) This size does not include mold burrs, protrusions, or burrs on the nozzle. The burrs or protrusions on each side of the mold shall not exceed 0.15 millimeters.

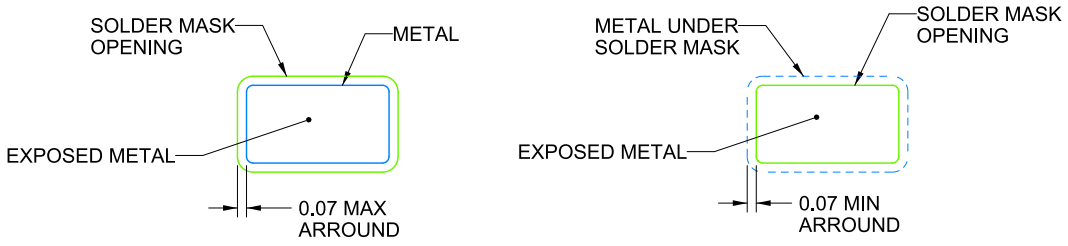
(4) This size does not include mold burrs, and the burrs or protrusions on each side of the mold do not exceed 0.25 millimeters.

Example of Layout of Device Packaging Pads

1.45mm height 6Pin SOT-23 Plastic sealed SOIC



器件封装焊盘布局举例
SCALE:15X



焊盘阻焊部详解
PADS 1-6

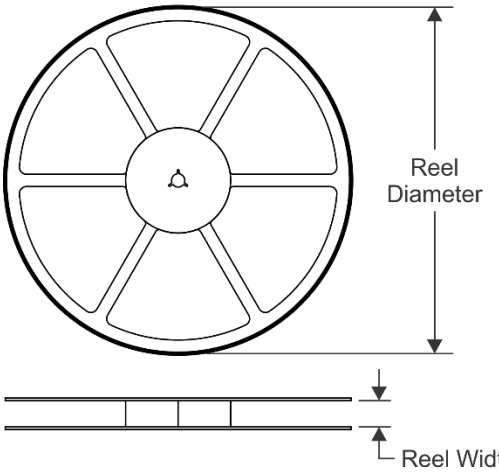
Note:

(1) Based on IPC-7351, relying on a proven mathematical algorithm that comprehensively considers manufacturing, assembly, and component tolerances, the solder pad graphics are accurately calculated.

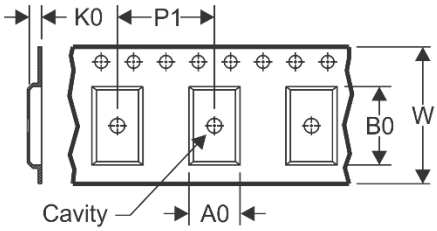
(2) The solder mask tolerances between and around signal pads may vary depending on the manufacturing of the circuit board.

TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

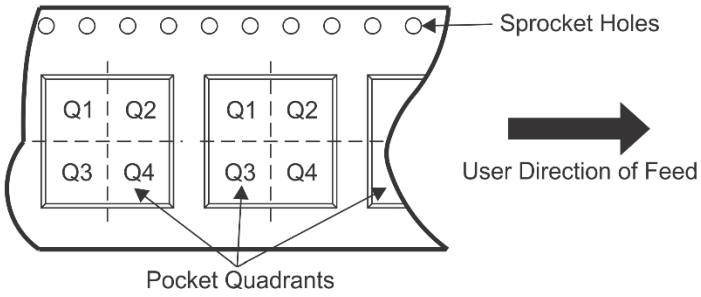


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LGS5145	SOT23-6	B6	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3