48V 600mA High-Efficiency Synchronous Buck Converter

Check for Samples: LGS5148

Features

- Wide input voltage range: 8V to 48V
- Adjustable output voltage range: 5V to 40V
- Junction temperature range: -40°C to +125°C
- Up to 97% peak efficiency
- 600mA load capability
- SKIP mode for ultra-high light-load efficiency
- Safe and reliable operation features:
  - (1) Integrated soft-start
  - (2) Integrated pre-start function
  - (3) Over-temperature and over-current protection
  - (4) Output short-circuit protection
- Internal compensation minimizes external components
- High efficiency and low power dissipation across full load range

Applications

- Pre-regulation for systems (tracking, telematics, network cameras)
- Battery backup power (electric meters, data concentrators)
- Thermoelectric device power (TEC, fiber modules)
- General-purpose voltage regulators and buck converters

Description

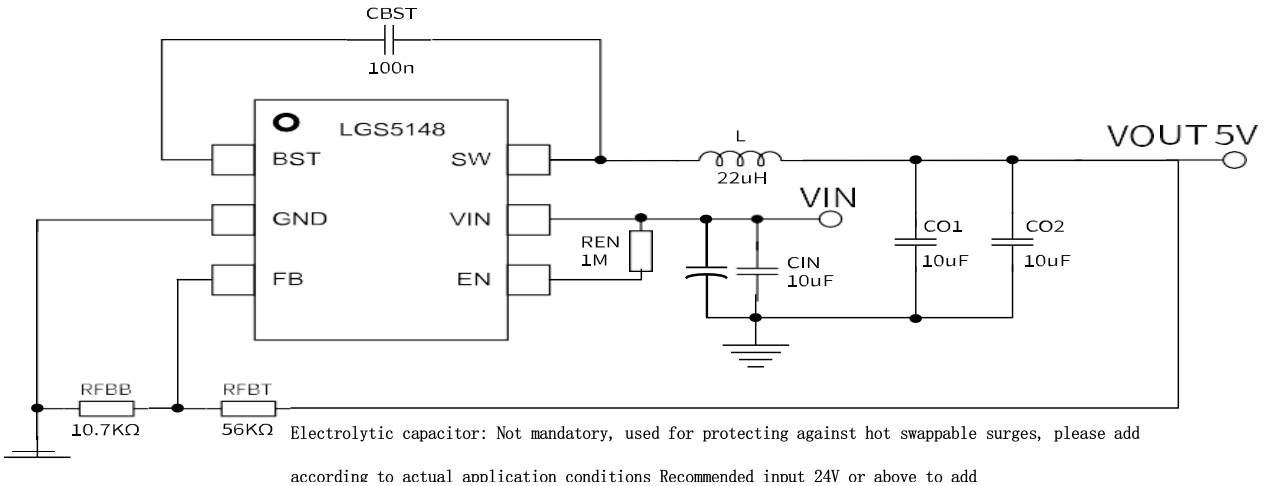
The LGS5148 is a synchronous buck DC-DC converter with a maximum input voltage of 48V and a load current of 0.6A, housed in a 3mm × 3mm SOT23-6 package. The output voltage is adjustable via external resistor dividers on the FB pin, supporting a range of 5V to 40V.

The LGS5148 features ultra-low quiescent current, enabling high efficiency under light loads, significantly reducing power consumption in battery-powered systems. Its wide input voltage range (8V–48V) minimizes the need for external surge suppression components, making it ideal for industrial and multi-cell battery applications.

Integrated power MOSFETs, peak current-mode control with internal compensation, and a maximum output current of 0.6A ensure excellent load and input transient response.

Ordering Information

Part Num	Package	Top Mark
LGS5148	SOT23-6	5148



Typical application circuit VO=5V

Absolute Maximum Ratings†

Table 3.1:

Parameter	Range
Pin-to-GND voltage (VIN, SW)	-0.3V~60V
BST-to-SW voltage	-0.3V~6V
PIN-to-GND voltage (FB, EN)	-0.3V~6V
Storage temperature	-65℃ to 150℃
Junction temperature	-40℃ to 125℃
ESD rating (HDM)	±2000V
ESD rating (CDM)	±1000V

† Note: Exceeding these limits may cause permanent damage. These are stress ratings only; prolonged operation under these conditions may affect reliability.

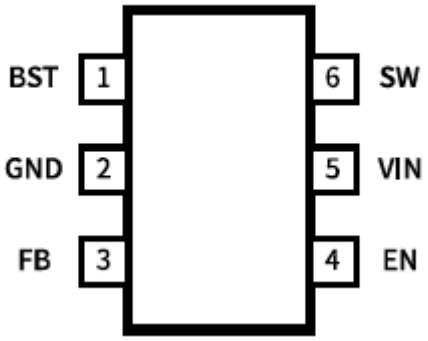
ESD Warning

ESD-Sensitive Device.

Charged devices and boards may discharge unnoticed. Despite built-in protection circuits, high-energy ESD events may damage the device. Proper ESD precautions must be taken to avoid degradation or failure.

Pin arrangement

Top View



SOT23-6

Packaging and Pin Arrangement

Table 3.2: Pin Descriptions

Pin number	Name	*Description*
1	BST	Internal power switch node. Connect to external inductor and Schottky diode.
2	GND	Power ground pin.
3	FB	Feedback input pin. Output voltage is set via an external resistor divider.
4	EN	Enable pin. Pull high to enable output; pull low to disable (1).
5	VIN	Input power pin. Connect a ≥4.7μF bypass capacitor to GND (2).
6	SW	Converter switch node. External connection power inductor.

Notes:

1. In typical applications, the EN pin is pulled up to VIN via a 1MΩ resistor.
2. Place the input capacitor close to the IC for optimal filtering.

Recommended Operating Conditions (1)

Parameter	Min	Max	Unit
VIN to GND voltage	8	48	V
EN to GND voltage	2	5	V
V_{OUT}	5	93%VIN	V
I_{OUT}	0	0.6	A
Junction temperature	-40	+125	°C

(1) For detailed performance specifications, refer to the Electrical Characteristics section

Electrical Characteristics

Unless otherwise specified, VIN=24V, VOUT=12V, TA=25 ℃; The maximum and minimum values are applicable for -40 ℃<TA=TJ<125 ℃.

Table 4: Electrical Specifications

Parameter		Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
VIN	Input voltage range		8		48	V
I_Q	IQ (quiescent)	No Switch		200		μA
I_S	ISD (shutdown)	EN=0,			1	μA
Enabling Characteristics (EN PIN)						
V_{EN_R}	*(rising threshold)*	TJ= 25℃		1.5	1.8	V
V_{EN_F}	*(falling threshold)*		0.6	1		V
I_{LKG_EN}	*EN input leakage current*			100		μA
Current Limit						
I_{SC_HS}	High side MOSFET current limitation		1	1.2	1.4	A
I_{ZC}	zero crossing detection	DCM mode, light load		90		mA
I_{SW}	Leakage current of SW				0.8	μA
MOSFET Characteristics						
Rdson_HS	On resistance of high side MOS transistor			450		mΩ
Rdson_LS	On resistance of low side MOS transistor			470		mΩ
Soft start process						
T_{SS}	The first SW pulse to VOUT GD (1)	V_{IN}> 4.5V		0.6		ms
Feedback loop						
I_{FB}	FB leakage current	V_{IN}=12V，FB=0.8V		100	120	nA
V_{FB}	feedback voltage		775	800	825	mV
Switching characteristic						
T_{ON_MIN}	Minimum conduction time of high side MOS (1)			100		ns
F_{SW}	switching frequency			900		Khz
System characteristics						
D_{MAX}	Maximum switch duty cycle			93		%
Thermal characteristics						
T_{SD}	Hot shutdown (1)			150		℃
T_{SD_H}	Delay of thermal shutdown			25		℃
Thermal resistance coefficient						
θ_{JA}	Thermal resistance coefficient from silicon core to surrounding air	0 LFPM Air Flow		173		℃/W
θ_{JB}	Thermal resistance coefficient from silicon core to PCB board surface			33.2		℃/W
θ_{JCtop}	Thermal resistance coefficient from silicon core to packaging surface			116		℃/W
Ψ_{JB}	Thermal resistance coefficient from silicon core to PCB board surface			30		℃/W
(1) Guaranteed by characterization or design, not production tested						

Application information: High efficiency synchronous buck switching regulator (Figure 1)

Unless otherwise specified, VIN=24V, VOUT=12V, TA=25 ℃

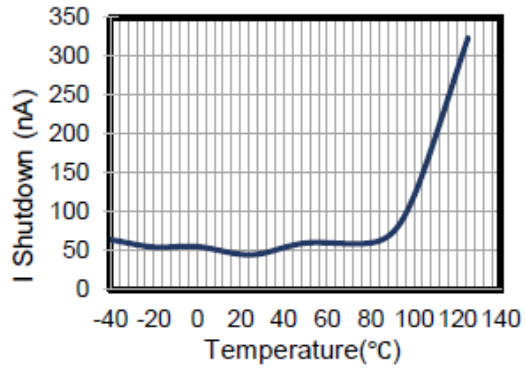


图 5.1-1 Shutdown Quiescent Current

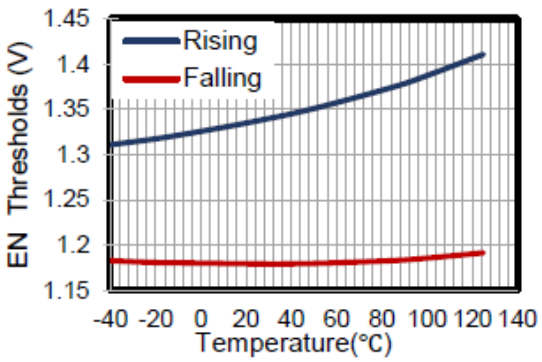


图 5.1-2 EN Threshold

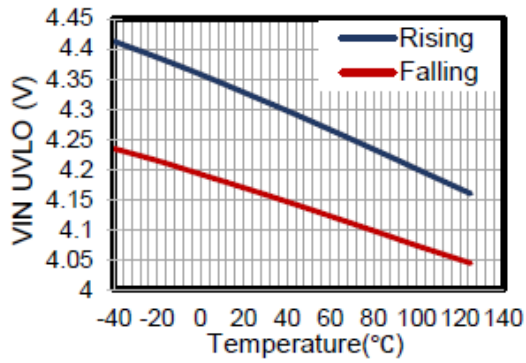


图 5.1-3 VIN UVLO

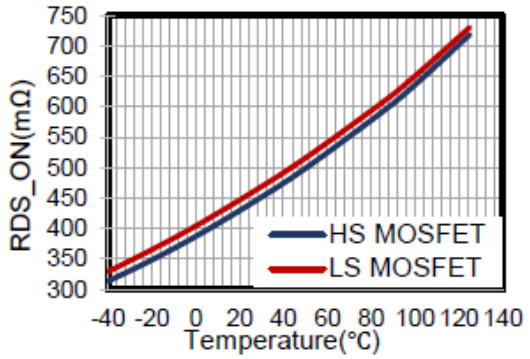


图 5.1-4 High-Side Low-Side RDS-ON

Application information: High efficiency synchronous buck switching regulator (Figure 2)

Unless otherwise specified, VIN=24V, VOUT=12V, TA=25 ℃

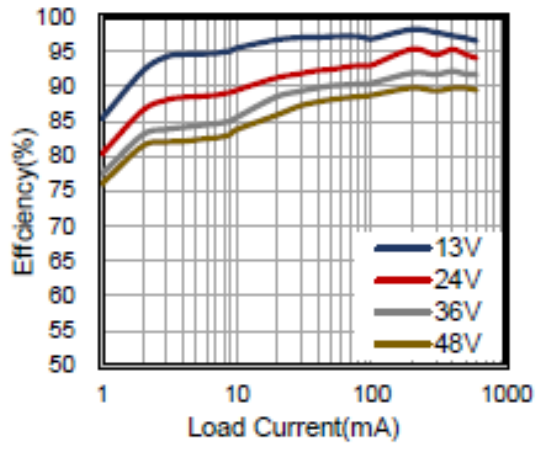


图 5.2-1 Efficiency 12V Output

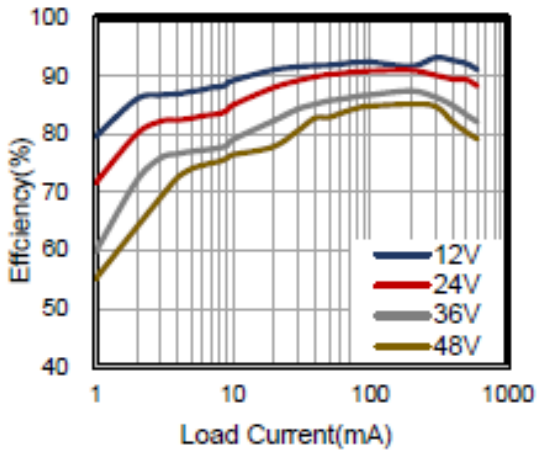


图 5.2-2 Efficiency 5V Output

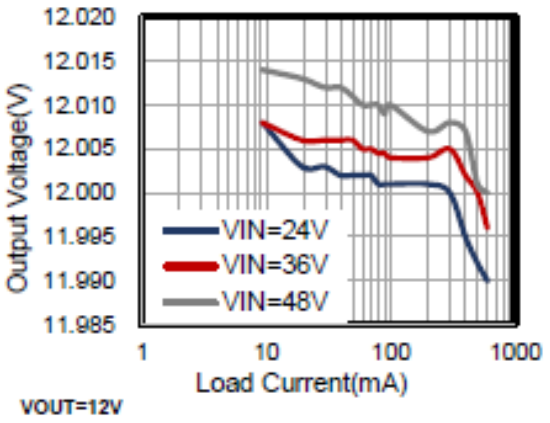


图 5.2-3 Line and Load Regulation

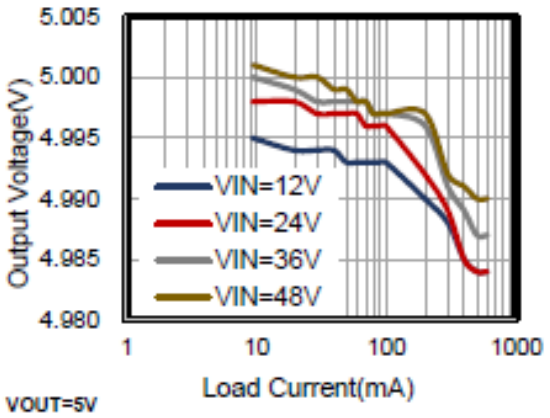
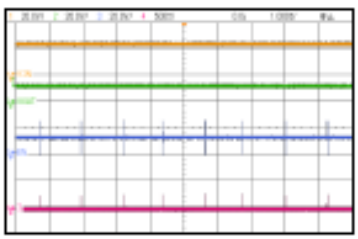
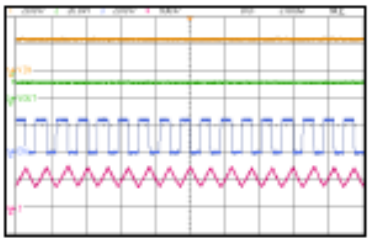


图 5.2-4 Line and Load Regulation



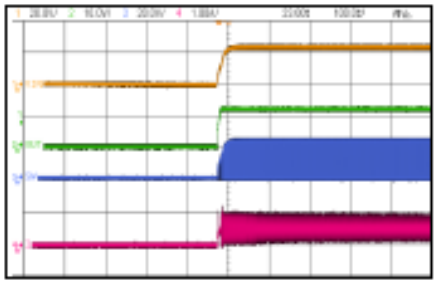
VIN=24V VOUT=12V LOAD=0Ω

图 5.2-5 Steady State Power Save Mode



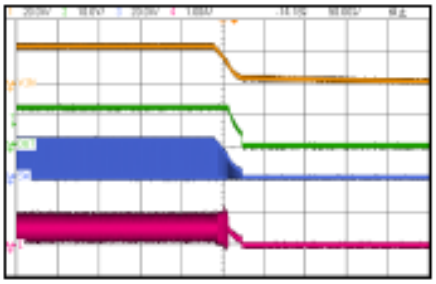
VIN=24V VOUT=12V LOAD=20Ω

图 5.2-6 Steady State CCM



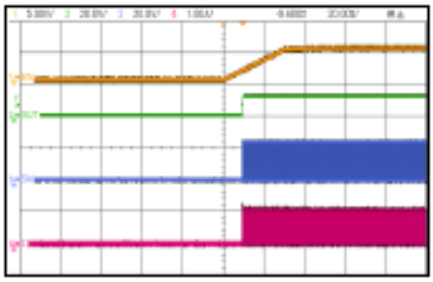
V_{IN}=24V V_{OUT}=12V LOAD=20Ω

图 5.2-7 12V Output VIN Power On



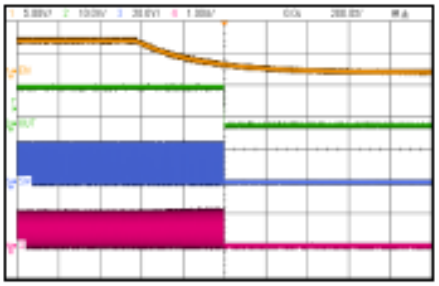
V_{IN}=24V V_{OUT}=12V LOAD=20Ω

图 5.2-8 12V Output VIN Power Off



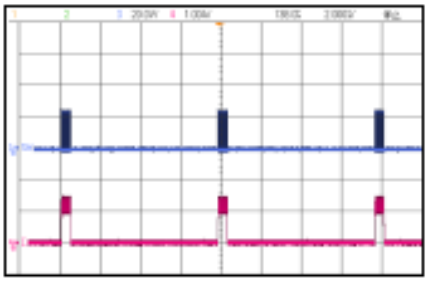
V_{IN}=24V V_{OUT}=12V LOAD=20Ω

图 5.2-9 12V Output EN Power On



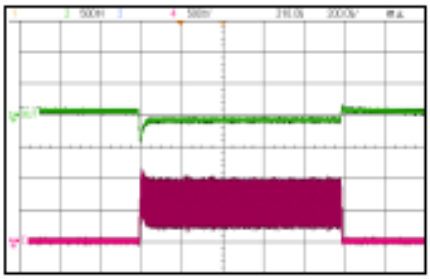
V_{IN}=24V V_{OUT}=12V LOAD=20Ω

图 5.2-10 12V Output EN Power Off



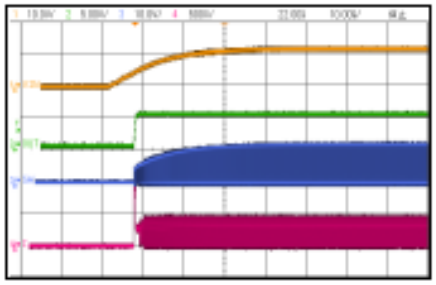
V_{IN}=24V V_{OUT}=12V LOAD=20Ω

图 5.2-11 Short-Circuit With Hiccup



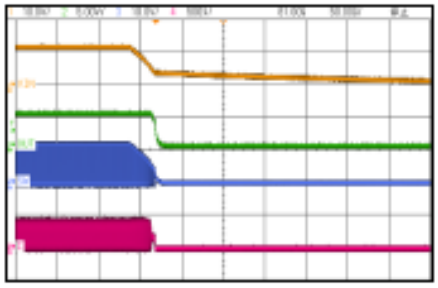
0A to 600mA，5A/μs

图 5.2-12 12V Output Load Transient



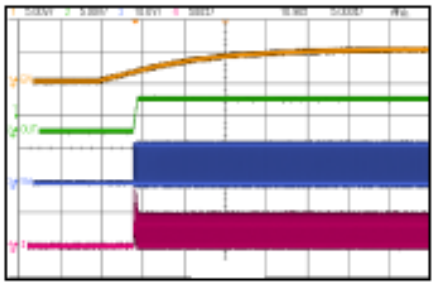
V_{IN}=12V V_{OUT}=5V LOAD=20Ω

图 5.2-13 5V Output VIN Power On



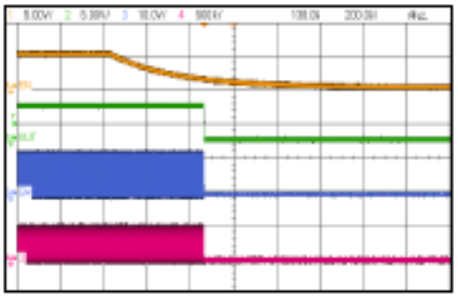
V_{IN}=12V V_{OUT}=5V LOAD=20Ω

图 5.2-14 5V Output VIN Power Off



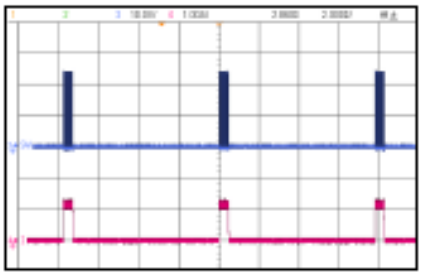
V_{IN}=12V V_{OUT}=5V LOAD=20Ω

图 5.2-15 5V Output EN Power On



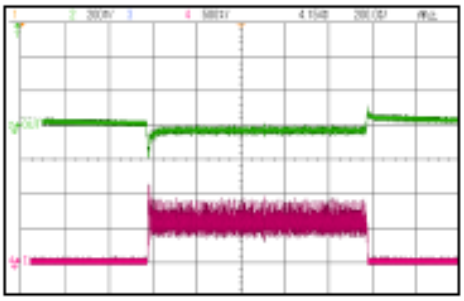
V_{IN}=12V V_{OUT}=5V LOAD=20Ω

图 5.2-16 5V Output EN Power Off



V_{IN}=12V V_{OUT}=5V LOAD=20Ω

图 5.2-17 Short-Circuit With Hiccup



0A to 600mA，5A/μs

图 5.2-12 5V Output Load Transient

Characteristic Description

Summary

LGS5148 is an internal switch type synchronous buck DC/DC regulator that integrates all controllers and protection circuits, greatly reducing system area. Equipped with SKIP control mode, it combines fast transient response with high efficiency. The LGS5148 external voltage divider network can set the output voltage to achieve a wide input and output range to meet a wide range of usage needs.
Additional features include: soft start, hot shutdown, maximum duty cycle limit, and intelligent current limit shutdown timer. Simultaneously equipped with short-circuit protection function to prevent IC overheating in the event of output short circuit.

Power Save Mode

In addition to continuous conduction mode (CCM), LGS5148 also has a power-saving mode, which is achieved by pausing switch operations to reduce switch losses and maintain high efficiency of the converter under light load conditions. Skip comparator manages and switches operating states by comparing ISKIP and I_{REF}, with current demand lower than
When I_{SKIP}, the comparator controls to pause switching; When the current demand increases (V_{OUT} decreases), the comparator controls the activation current loop to enter continuous switching mode, causing V_{OUT} to rise. At this time, I_{REF} will decrease. When I_{REF} is lower than I_{SKIP}, switching will be paused again. Due to the periodic sudden drops and recovery of the output voltage, the ripple of the output voltage in this mode is greater than that in CCM operating mode.

Soft-Start

LGS5148 sets internal soft start. Soft start can prevent output voltage overshoot during the startup process. When the chip is started, the internal circuit of the IC generates a soft start voltage (VSS), which starts to rise from 0V. When it is less than the internal reference (V_{REF}), V_{SS} replaces V_{REF} as the reference voltage for the error amplifier; When V_{SS} exceeds V_{REF}, error amplification occurs
The device uses V_{REF} as a reference voltage.
Throughout the entire startup phase, the switch current limitation remains effective to avoid the occurrence of short circuits upon power up. When the output has a very large capacitance (such as 2200 μ F or even larger), the output voltage rise speed will be slower than V_{SS}, limited by the maximum switch current limit, and the time from startup to reaching the target voltage setting value will be longer than the soft start process.

EN-IC Enable

The voltage of the EN pin controls the startup and shutdown of LGS5148. When the EN voltage is less than V_{EN_OUT}, the chip maintains a low-power standby state, and the input current at this time is 30 μ A（VIN=24V）， When the voltage at the EN pin is greater than VEN_SUT, the IC enters soft start mode. During the IC shutdown process, when the EN pin voltage drops to VEN-OUT - VEN-HYST, the LGS5148 regulator stops working and enters standby mode again.
If there are no special requirements, the EN pin can be connected to VIN through a 1M resistor. When VIN is powered on, the enable can be kept open at the same time (note: the withstand voltage value of the EN pin is 6V).

Thermal Shutdown

When the junction temperature starts to rise above 150 ℃, Thermal Shutdown will be activated and the system will forcibly shut down the regulator output. When the junction temperature drops below 125 ° C, LGS5148 will attempt a soft start again.
The guaranteed operating junction temperature range of this device is -40 ° C to+125 ° C. High junction temperatures will reduce the working life, and when the junction temperature is above 125 ° C for a long time, the device life will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions, circuit board layout, rated package thermal resistance, and other environmental factors.

The junction temperature (T_J, unit: ℃) is calculated based on the ambient temperature (T_A, unit: ℃) and power consumption (P_D, unit: W), using the following formula:

$$T_J = T_A + (P_D * \theta_{JA})$$

Among them, θ_{JA} (unit: ℃/W) is the thermal resistance of the package.

Frequency reversal protection

LGS5148 contains a fold back mode. When the switch duty cycle is very large and the minimum turn off time is not met, it will enter the fold back protection mode. At this time

The switching tube operates at 1/4 of F_{SW}, which significantly reduces the rise time of the inductor current and prolongs the discharge time of the inductor. LGS5148 integrates the Fold mode internally, which can effectively protect the chip from startup and short circuit, preventing output current overshoot. When the minimum duty cycle requirement is met, LGS5148 will exit the turnaround

Protection mode, perform a soft restart.

Maximum current limit

The voltage regulator output has a cycle by cycle overcurrent limiting function. When the SW current triggers the limit SW (Peak), BUCK output will enter a cycle by cycle current limiting state. ILIMIT.SW (Peak) and large inductance

The small and input pressure differences are related, and ILIMIT.SW (Peak) is only the reference minimum value. When there is a prolonged overcurrent or short circuit, OTP protection may be triggered.

Maximum duty cycle D_{MAX}

When the input/output voltage difference is very low, BUCK switches to the maximum duty cycle operating state. At this time, the high-end N-channel MOSFET is in a normally open state, minimizing the turn off time. Under maximum duty cycle operating conditions, as the output voltage is the product of the input voltage value and the maximum duty cycle limit, the output voltage will drop sharply below the regulation range.

Output voltage VOUT

The voltage regulation circuit of LGS5148 will adjust the FB voltage to be the same as the internal reference voltage, and the output voltage can be adjusted by changing the ratio of the two voltage divider resistors.

The output voltage can be calculated according to the following formula:

$$V_{OUT} = \frac{R_{FBT} + R_{FBB}}{R_{FBB}} * V_{FB}$$

Reference for output voltage configuration

VO(VΩ)	RFBT(KΩ)	RFBB(KΩ)
3.3	33	10.7
5	56	10.7
12	150	10.7

Note:

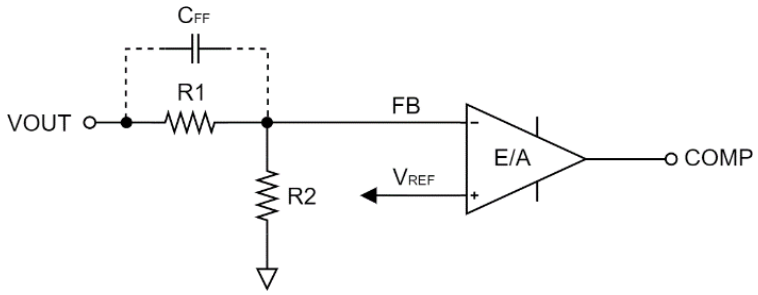
- A larger voltage divider resistor can reduce the current flowing through the voltage divider network and improve voltage conversion efficiency. However, a high resistance value makes the feedback loop more susceptible to noise interference. It is recommended to use voltage divider resistors with an accuracy of ± 1% or better, a temperature coefficient of 100ppm or lower, and a resistance limit of K level.
- If the FB pin is grounded or disconnected, the output voltage value will be driven to near the input voltage value. It should be noted that the load connected to the output at this time may be damaged.
- The feedback loop should be kept away from PCB noise interference, as shown in the PCB layout reference provided later.

Feedforward capacitor C_{FF}

In some cases, the feedforward capacitor C_{FF} can be connected across the resistance of V_{OUT}-FB to increase loop phase margin and improve load transient response.

The introduction of C_{FF} can form new zero points (Z_{FF}) and poles (P_{FF}) with the feedback resistor in the feedback loop. If the zero point is placed before the frequency at which the unity gain occurs, it can increase the frequency bandwidth, reduce the output ringing of the regulator, and stabilize it faster, thereby improving the transient response of the system.

The larger the selection value of C_{FF}, the greater the bandwidth it can provide. However, an excessively large C_{FF} can cause the loop gain bandwidth frequency to be too high, leading to loop instability. The general value of C_{FF} is between 22pF and 220pF.



CFF can be estimated according to the following formula:

$$C_{FF} = \frac{\sqrt{\frac{V_{FB}}{V_{OUT}}}}{2\Pi * R_1 * F_E}$$

Bootstrap capacitor C_{BST}

The high side switch driver circuit of LGS5148 buck driver requires a bias voltage higher than VDD to ensure that the high side MOS transistor is in the on state. The capacitance between BST and SW

CBST acts as a 'charge pump' to raise the voltage at the BST end to SW+VDD (V_{BST-SW}=5V), The conducting diode for CBST charging is integrated inside the LGS5148 chip to minimize the size of the usage scheme as much as possible. CBST recommends using 0.1 μ F capacitors with a withstand voltage value higher than 10-16V.

Input capacitor CVIN

LGS5148 requires the use of decoupling capacitors to filter out noise interference at the input end. The typical

recommended value for decoupling capacitors is 4.7 μ F, and the rated voltage must be greater than the maximum required by the IC

The input voltage should ideally be twice the maximum input voltage (1). The increase of this capacitor can reduce input voltage ripple and maintain stable input voltage during load transients.

Meanwhile, connecting a small 100nF ceramic capacitor in parallel with the filtering capacitor at the input end helps to filter out high-frequency noise. Small capacitors have a small filtering radius and should be placed as close as possible to the chip to ensure optimal filtering performance.

In the testing process of LGS5148, we selected ceramic capacitors with 4.7 μ F, 100V, X7R and 100nF, 100V, X7R.

(1) The DC bias effect of ceramic capacitors causes a decrease in the effective value of the capacitor. Please refer to the DC bias characteristics of the selected capacitor as much as possible to choose the appropriate capacitor The packaging size, rated voltage, and dielectric material can all cause differences between the rated capacitance value and the effective capacitance value.

Output capacitor COUT

LGS5148 allows for a wide range of output capacitor values. To ensure cost and small size, it is recommended to choose the appropriate output capacitor. In practical applications, losing

The output capacitance will directly affect the voltage overshoot undershoot and ripple of the output voltage during transient response of the output current. When the load undergoes transient changes, the output capacitor needs to provide charge before the loop regulation is completed. The transient voltage change value ΔV_{OUT} an be calculated by the following formula:

$$\Delta V_{OUT} = \Delta I_{OUT} * ESR$$

Among them, ΔI_{OUT} represents the jump value of the load current, and ESR is the equivalent series resistance value of the output capacitor.

The output voltage ripple consists of two parts: one is caused by the inductance current ripple flowing through the ESR of the output capacitor, and the other is caused by the inductance current ripple on the charging and discharging of the output capacitor.

$$\Delta V_{OUT-RIPPLE} = \frac{\Delta I_L}{8 * C_{OUT} * F_{SW}} + \Delta I_L * ESR$$

ΔIL represents the ripple current of the inductor, and F_{SW} represents the switching frequency of the MOSFET. In order to maintain a small output voltage overshoot or undershoot and reduce output ripple during transient changes, capacitors need to have a large capacitance and a small ESR, which will also increase costs and volume. Choosing the appropriate output capacitor is crucial (1) (2).

(1) Excessive output capacitance can also affect the normal startup and circuit stability of the chip.

(2) You can directly use the recommended 10 μ F, 100V, X7R ceramic capacitors for typical applications, or use them as a starting point for selecting output capacitance values.

Power inductor L

The selection of power inductors mainly considers the saturation current of the inductor, which should be based on the expected ripple current ΔIL, that is, the effective value of the AC current in the inductor that varies with the load current. Generally controlled between 20% -40% of the maximum load current $I_{OUT-MAX}$. The inductance value can be calculated using the following formula:

$$\blacktriangle I_L = \frac{(V_{IN} - V_{OUT}) * D}{F_{SW} * L}$$

D represents the duty cycle of the switch, which can be approximately calculated using $D = \frac{V_{OUT}}{V_{IN}}$

The unit of inductance obtained is μH.

The saturation current value of the inductor must be higher than the sum of the maximum load current and ripple current:

$$I_{L-MAX} \geq II_{OUT-MAX} + \blacktriangle I_L/2$$

Generally speaking, choosing an inductor with a lower inductance value will result in a smaller DCR, which can handle faster transient responses, and the size of the proposed solution will be smaller. However, a too low inductance will generate greater inductance current ripple, resulting in larger output voltage ripple when using the same C_{OUT}.

After testing, the recommended inductance values for typical applications can serve as a reference for use.

Hot swappable security

Ceramic capacitors have the advantages of small size, good stability, and low impedance, making them an ideal choice for input bypass capacitors in the LGS5148 circuit. But if LGS5148

Inserting a live power supply may cause the voltage at the VIN pin of LGS5148 to reach twice the nominal input voltage, potentially exceeding the rated value of LGS5148 and damaging parts. If the input power control is improper or the user needs to plug the LGS5148 into a power source, the design of the input network should prevent this overshoot.

Figure 8a shows the waveform generated when the LGS5148 circuit is connected to a 24V power supply via a 6-foot (2m) 24AWG twisted pair. The first figure shows the instantaneous response of a ceramic capacitor with a 10 μ F input. The input voltage is as high as 49V, and the peak input current is 36A.

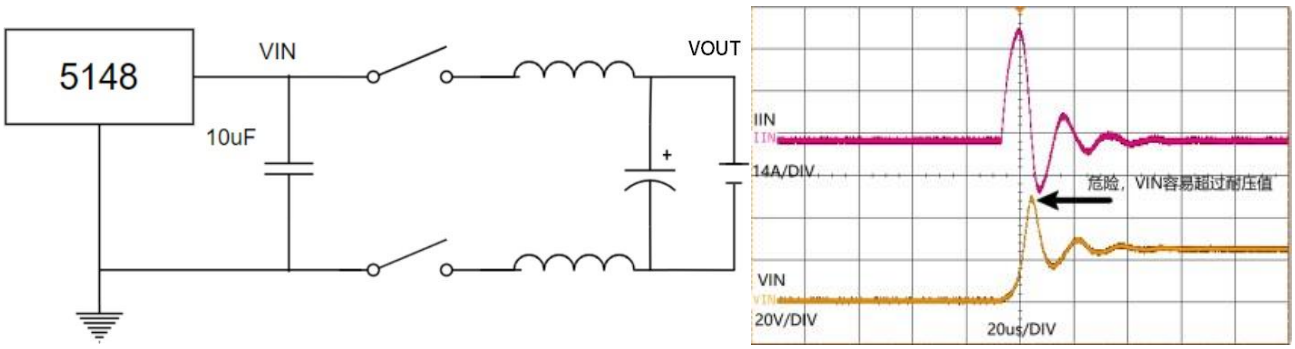


Figure 8 (a)

One way to improve and prevent the impact of this issue is to add another capacitor with a series resistor in the circuit. An aluminum electrolytic capacitor has been added in Figure 8b. this

The damping generated by the high equivalent series resistance of capacitors can eliminate voltage overshoot. The additional capacitor improves the input ripple and can slightly increase the efficiency of the circuit. Another solution is shown in Figure 8c. A 1.5 Ω resistor is connected in series with the input to eliminate voltage overshoot (which also reduces peak input current). A 0.1 μ F capacitor improves high-frequency filtering. This solution is smaller and cheaper than electrolytic capacitors. For high input voltage, its impact on efficiency is minimal.

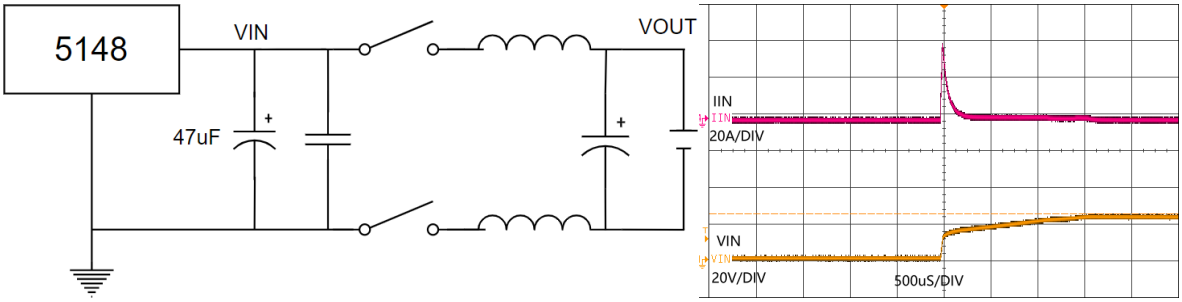


Figure 8 (B)

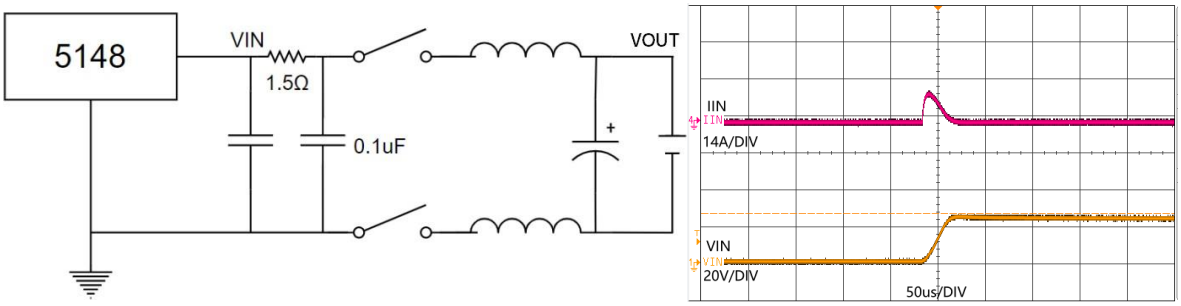


Figure 8 (C)

Refer to PCB layout

Summary

The high integration of LGS5148 makes the PCB layout very concise and clear. Poor layout can affect the performance of LGS5148, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) difference, ground jump, and voltage loss, which in turn affect the stability of use. To optimize its electrical and thermal performance, please refer to the following rules to implement PCB layout and routing to ensure optimal performance:

- Place the high-frequency ceramic input capacitor CVIN as close as possible to the VIN and GND pins of LGS5148 to reduce high-frequency noise introduced to the output pins and minimize EMI radiation. In addition, keep the input and output capacitors connected to the large-area GND on the layer where they are located.
- It is best to use large-area copper coating for power circuits to make the input and output connection circuits as wide as possible, reduce losses during transmission, and maximize efficiency.
- To enhance heat dissipation and connectivity, the number of vias can be increased to achieve interconnection between the top layer and other power layers or layers. Please ensure that the PCB board has sufficient copper plated areas for heat dissipation, keeping the junction temperature below 125 ℃.
- Consideration should be given to the ACR and DCR losses generated by inductance, which result in heat conduction to the chip. The inductor can be placed slightly further away or the heat island can be designed reasonably.
- The feedback resistors RFBT and RFBB should be located near the FB pin, and the feedforward capacitor CFF should be placed parallel to RFBT. The distance between the feedback loop and the FB and GND pins must be close, and the appropriate distance from VOUT can be relatively far. It is necessary to ensure that the feedback loop is away from any noise source (such as the SW node).

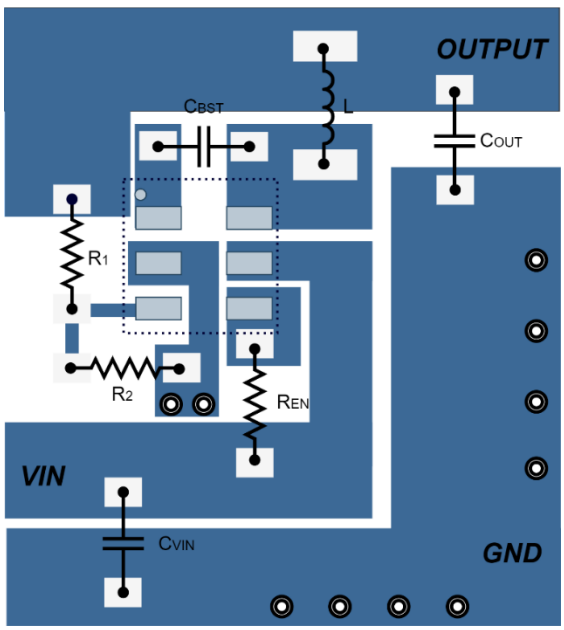
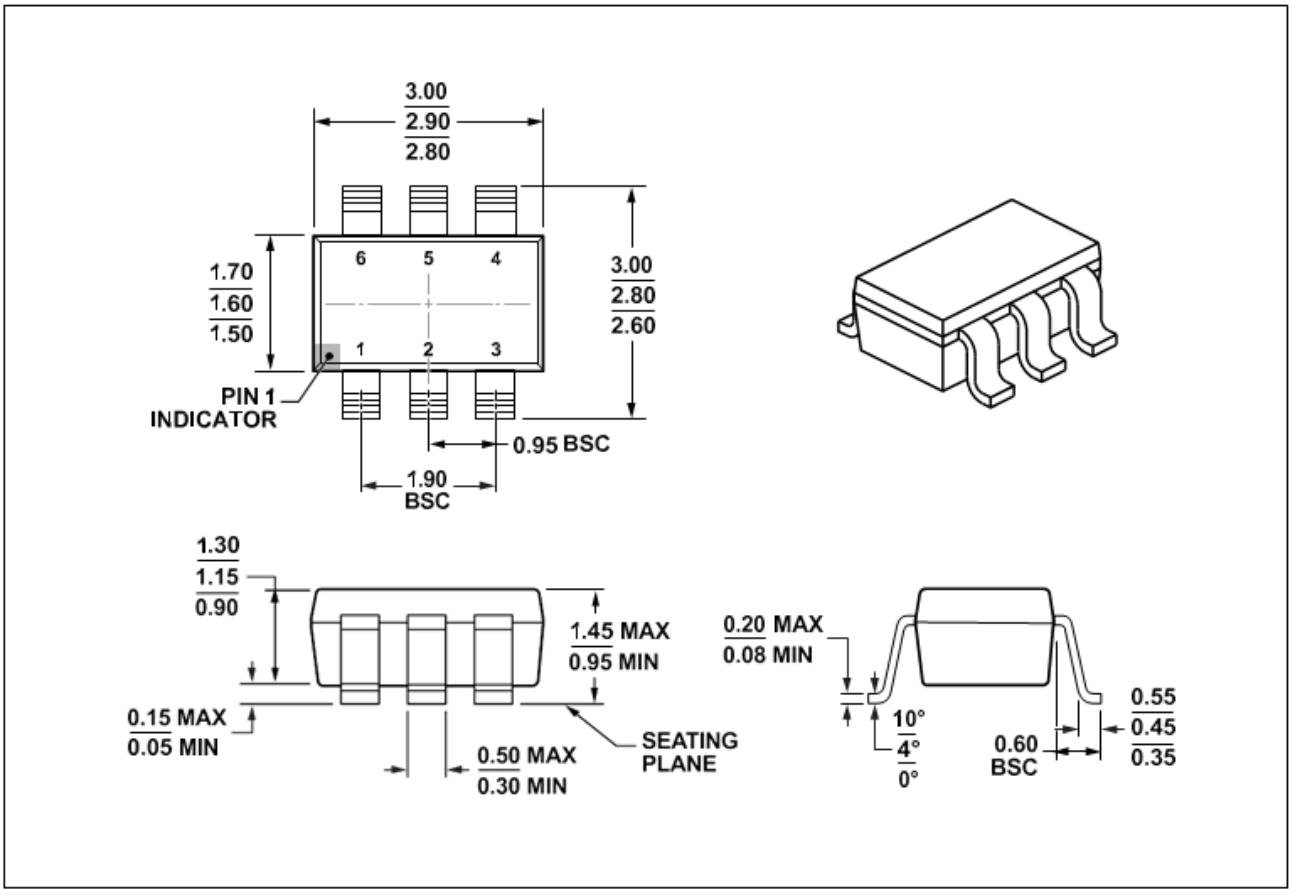


Figure 9: Reference PCB Layout

Example of Device Packaging Pad Layout

1.45mm height 6-pin SOT-23 plastic encapsulated SOIC



NOTE:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only.

(2) This image is subject to change without prior notice.

(3) This size does not include mold burrs.

Important Disclaimer and Disclaimer:

棱晶半导体
www.Legend-Si.com

Legend Si provides technical and reliable data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, security information, and other resources "as is" without warranty or any express or implied warranties, including but not limited to implied warranties of merchantability, suitability for a particular purpose, or non infringement of any third-party intellectual property rights.
The resources can be used by professional developers to design Legend Si products. You will be solely responsible for the following actions: (1) selecting the appropriate Legend Si product for your application; (2) Design, validate, and test your application; (3) Ensure that your application meets the appropriate standards and any other safety, security, or other requirements. The resources mentioned are subject to change without prior notice. Legend Si's authorization for your use of the aforementioned resources is limited to the development of applications related to Legend Si products. In addition, the said resources shall not be copied or displayed, and no other Legend Si or any third-party intellectual property licensing shall be provided. Legend Si shall not be liable for any claims, compensations, costs, losses, or liabilities arising from the use of the aforementioned resources, and you shall compensate for any damages caused to Legend Si and its representatives as a result.

All products provided by Legend Si are subject to Legend Si's sales terms and www.legendary Si The constraints of other applicable terms provided on Legend-si.com or accompanying Legend-Si products. The resources provided by Legend Si do not expand or otherwise alter the applicable warranty scope or warranty disclaimer issued by Legend Si for Legend Si products.

Mailing address: Room 1403, Building C, Tengfei Building, No. 88 Jiangmiao Road, Pukou District, Nanjing City, Jiangsu Province, China Phone: 025-58838327
Prism Semiconductor (Nanjing) Co., Ltd