# PCF8574 Remote 8-bit I/0 expander for I²C-bus with interrupt

## 1. General Description

### 1.1 Description

The PCF8574 provides general-purpose remote I/O expansion via the two-wire bidirectional I²C-bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 100kHz I²C-bus interface, three hardware address inputs and interrupt output operating between 2.5 V and 6 V. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. System master can read from the input port or write to the output port through a single register.

The active LOW open-drain interrupt output ( $\overline{\text{INT}}$ ) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state.It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I²C-bus.

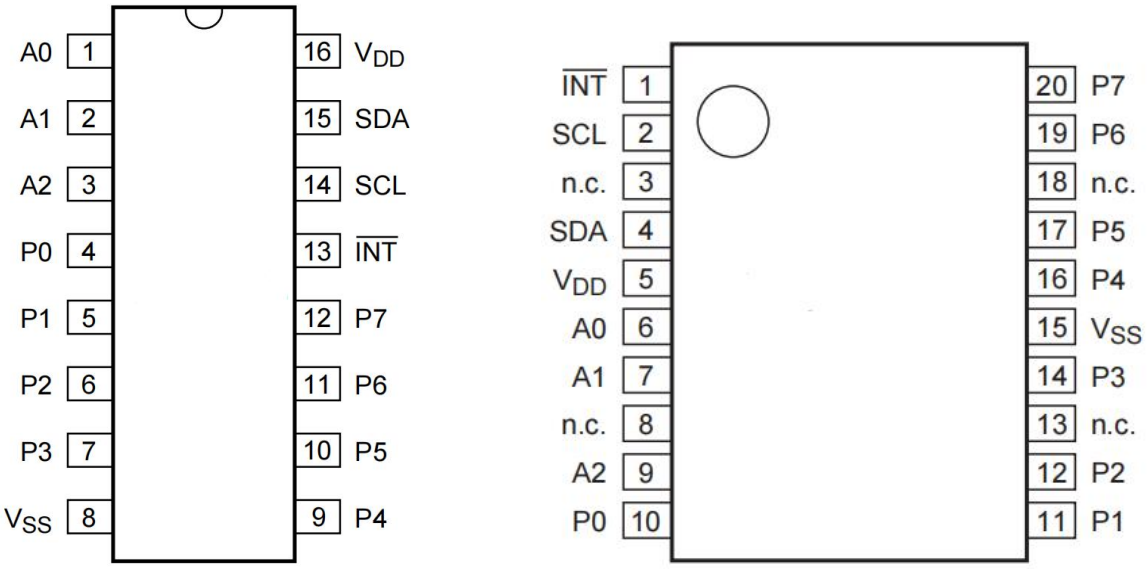
### 1.2 Features

- I²C-bus to parallel port expander
- 100kHz I²C-bus interface (Standard-mode I²C-bus)
- Operating supply voltage 2.5 V to 6 V
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs directly drive LEDs
- Active LOW open-drain interrupt output
- Eight programmable slave addresses using three address pins
- Low standby current (0 uA typical)

### 1.3 Ordering Information

| PART NUMBER | PACKAGE |
|---|---|
| PCF8574 | DIP |
| | SOP-W |
| | SSOP |
| | TSSOP |

# 2. Connection Diagrams and Pin Description




DIP16/SOP16-W Top View

SSOP20/TSSOP20 Top View

Figure 2.1 Top View

| PIN No. | | NAME | FUNCTION |
|---|---|---|---|
| DIP/SOP-W | SSOP/TSSOP | | |
| 1 | 6 | A0 | Address Input0 |
| 2 | 7 | A1 | Address Input1 |
| 3 | 9 | A2 | Address Input2 |
| 4 | 10 | P0 | Quasi-bidirectional I/O 0 |
| 5 | 11 | P1 | Quasi-bidirectional I/O 1 |
| 6 | 12 | P2 | Quasi-bidirectional I/O 2 |
| 7 | 14 | P3 | Quasi-bidirectional I/O 3 |
| 8 | 15 | VSS | Ground |
| 9 | 16 | P4 | Quasi-bidirectional I/O 4 |
| 10 | 17 | P5 | Quasi-bidirectional I/O 5 |
| 11 | 19 | P6 | Quasi-bidirectional I/O 6 |
| 12 | 20 | P7 | Quasi-bidirectional I/O 7 |
| 13 | 1 | $\overline{INT}$ | Interrupt Output (active LOw) |
| 14 | 2 | SCL | Serial Clock Line |
| 15 | 4 | SDA | Serial Data Line |
| 16 | 5 | VDD | Positive Supply Voltage |
| -- | 3,8,13,18 | NC | Not Connected |

# 3. System Diagram

## 3.1 Block Diagram

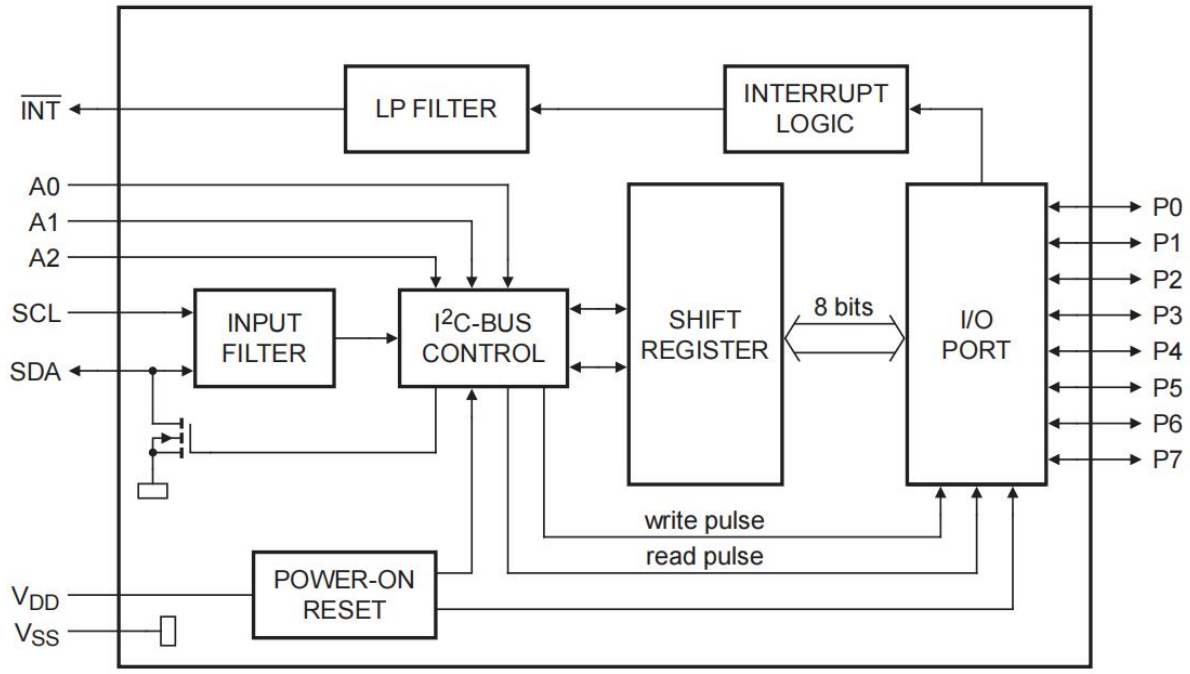



Figure 3.1：PCF8574 Block Diagram

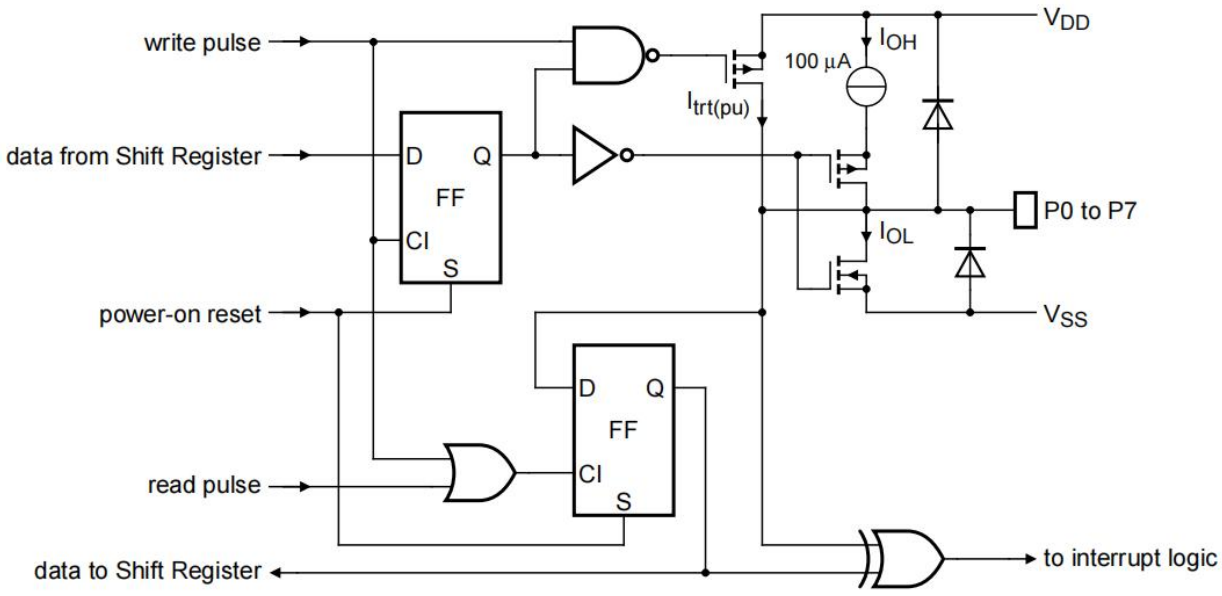



Figure 3.2：Simplified Schematic Diagram of P0 to P7

# 4. Specifications

## 4.1 Absolute Maximum Ratings

| Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|
| VDD | Supply Voltage | -0.5 | 6.5 | V |
| $V_I$ | DC Input Voltage | - 0.5 | VDD+0.5 | V |
| $V_O$ | DC Output Voltage | - 0.5 | VDD+0.5 | V |
| | Continuous current through VDD or VSS | | ±100 | mA |
| $T_J$ | Junction Temperature | | 150 | ℃ |
| $T_{OP}$ | Operating Temperature | -40 | 85 | ℃ |

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

## 4.2 Electrical Characteristics

($T_a$=25℃, voltages are referenced to VSS (ground=0V), unless otherwise specified)

| Symbol | Parameter | VDD | Test Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $V_{DD}$ | Supply Voltage | | | 2.5 | -- | 6 | V |
| $I_{DD}$ | Supply Current | 6 | Operating Mode; no load;<br>VI = VDD or VSS; $f_{SCL}$ = 100 kHz | -- | 0 | 100 | uA |
| $I_{STB}$ | Standby Current | 6 | Standby Mode: no load;<br>VI = VDD or VSS | -- | 0 | 10 | uA |
| $V_{POR}$ | Power-on Reset Voltage | 6 | no load; VI = VDD or VSS | -- | 1.3 | 2.4 | V |
| **Input SCL; input/output SDA** | | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | 2.5 - 6 | | 0.7VDD | -- | -- | V |
| $V_{IL}$ | Low-Level Input Voltage | 2.5 - 6 | | -- | -- | 0.3VDD | V |
| $I_{OL}$ | Low-Level Output Current | 2.5 - 6 | $V_{OL}$=0.4V | 3 | -- | -- | mA |
| $I_L$ | Leakage Current | 2.5 - 6 | VI = VDD or VSS | -5 | -- | 5 | uA |
| **I/0s; P0 - P7** | | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | 2.5 - 6 | | 0.7VDD | -- | -- | V |
| $V_{IL}$ | Low-Level Input Voltage | 2.5 - 6 | | -- | -- | 0.3VDD | V |
| $I_{IHL(max)}$ | Max allow Input Current through protection diode | 2.5 - 6 | VI≥VDD or VI≤VSS | -- | -- | ±400 | uA |
| $I_{OL}$ | Low-Level Output Current | 5 | $V_{OL}$=1V | 10 | -- | -- | mA |
| $I_{OH}$ | High-Level Output Current | 2.5 - 6 | $V_{OL}$=0.4V | 30 | -- | 300 | uA |
| $I_{trt(pu)}$ | Transient boosted pull-up Current | 2.5 | High during acknowledge ;<br>$V_{OH}$= VSS | -- | -1 | -- | mA |
| **Interrupt** $\overline{INT}$ | | | | | | | |
| $I_{OL}$ | Low-Level Output Current | 2.5 - 6 | $V_{OL}$=0.4V | 1.6 | -- | -- | mA |
| $I_L$ | Leakage Current | 2.5 - 6 | VI = VDD or VSS | -5 | -- | 5 | uA |

| Symbol | Parameter | VDD | Test Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| **Select inputs A0, A1, A2** | | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | 2.5 - 6 | | 0.7VDD | -- | -- | V |
| $V_{IL}$ | Low-Level Input Voltage | 2.5 - 6 | | -- | -- | 0.3VDD | V |
| $I_L$ | Leakage Current | 2.5 - 6 | VI = VDD or VSS | -5 | -- | 5 | uA |
| **I²C-bus timing** | | | | | | | |
| $f_{SCL}$ | SCL Clock Frequency | 2.5 - 6 | | -- | -- | 100 | kHZ |

# 5. Device Address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address format of the PCF8574 is shown in Figure 5.1. Slave address pins A2, A1 and A0 are held HIGH or LOW to choose one of eight slave addresses. To conserve power, no internal pull-up resistors are incorporated on A2, A1 or A0, so they must be externally held HIGH or LOW.The address pins (A2, A1, A0) can connect to VDD or VSS directly or through resistors.

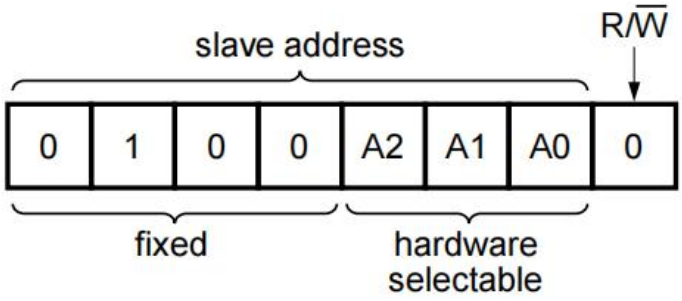



Figure 5.1：PCF8574 address format

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

# 6. I/O Programming

## 6.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O is an input or output port without using a direction control register.Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power on, all the ports are HIGH with a weak 100uA internal pull-up to VDD, but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

## 6.2 Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PCF8574 acknowledges and the master then sends the data byte for P7 to PO to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PCF8574. If a LOW is written, the strong pull-down turns on and

stays on. If a HIGH is written, the strong pull-up turns on for 1/2 of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.

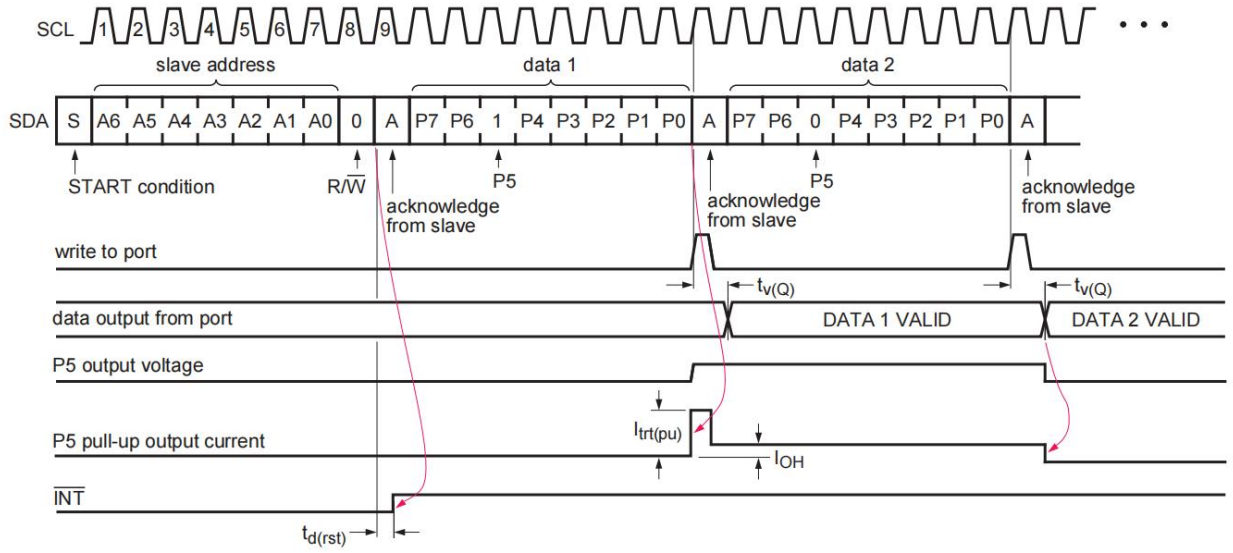



Figure 6.1：Write mode (output)

## 6.3 Reading from a port (input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset. To enter the Read mode the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the pin.

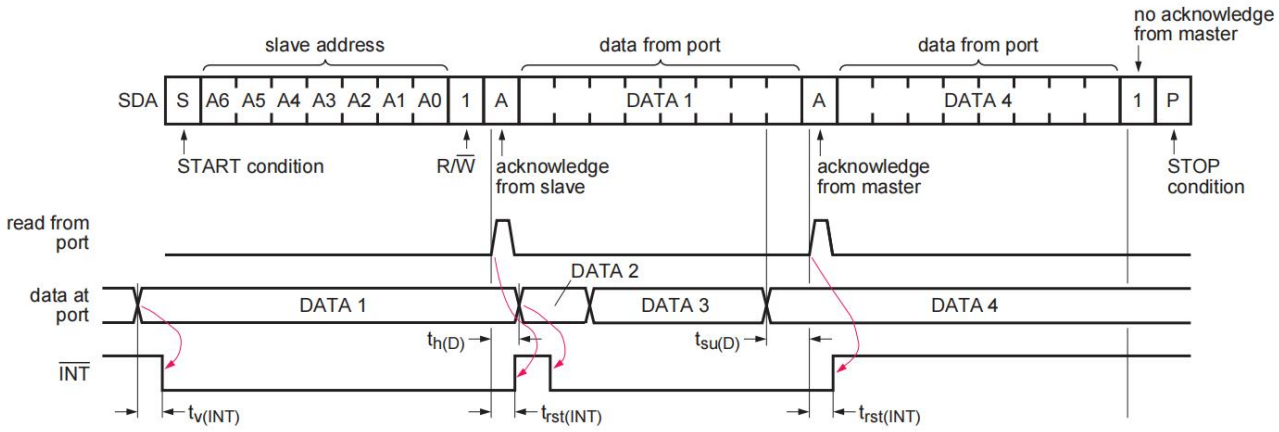



Figure 6.2：Read mode (input)

A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

## 6.4 Interrupt output ($\overline{\text{INT}}$)

The PCF8574 provides an open-drain output ( $\overline{\text{INT}}$ ) which can be fed to a corresponding input of the microcontroller. As soon as a port input is changed, the $\overline{\text{INT}}$ will be active (LOW) and notify the microcontroller. An interrupt is generated at any rising or falling edge of the port inputs. After time tv(Q), the signal $\overline{\text{INT}}$ is valid.

The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master.

In the Write mode, the interrupt may be reset (HIGH) on the rising edge of the acknowledge bit of the address byte and also on the rising edge of the write to port pulse.The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see Figure 6.1).

The interrupt is reset (HIGH) in the Read mode on the rising edge of the read from port pulse (see Figure 6.2).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an $\overline{\text{INT}}$.

At power-on reset all ports are in input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

# 7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-wire communication between different ICs or modules. The two wires are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

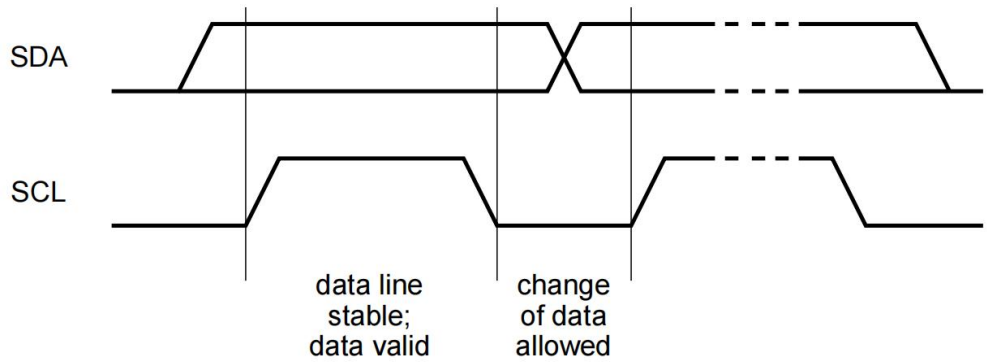



Figure 7.1：Bit transfer

## 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition(P).

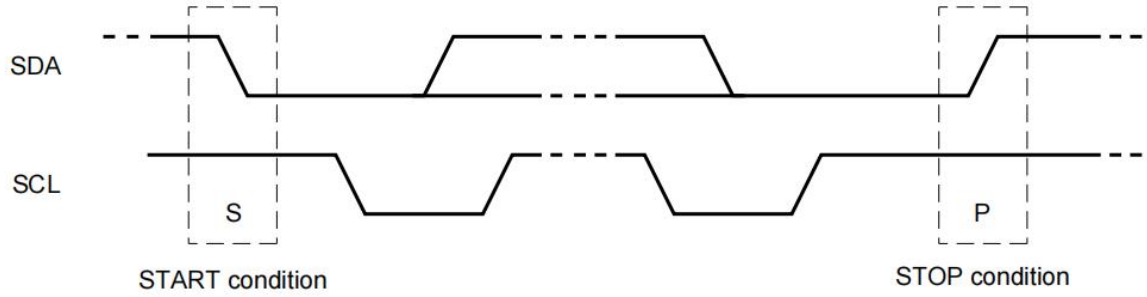



Figure 7.2：Definition of START and STOP conditions

## 7.3 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

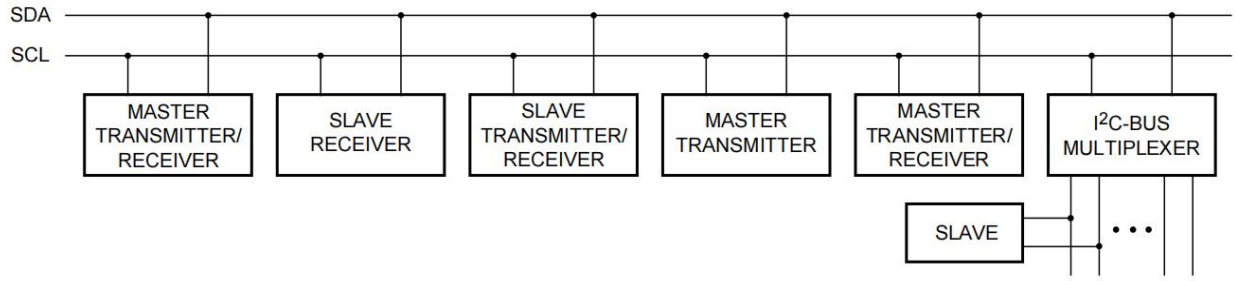



Figure 7.3：System configuration

## 7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is an active LOW level (generated by the receiving device) that indicates to the transmitter that the data transfer was successful.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that wants to issue an acknowledge bit has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge bit related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

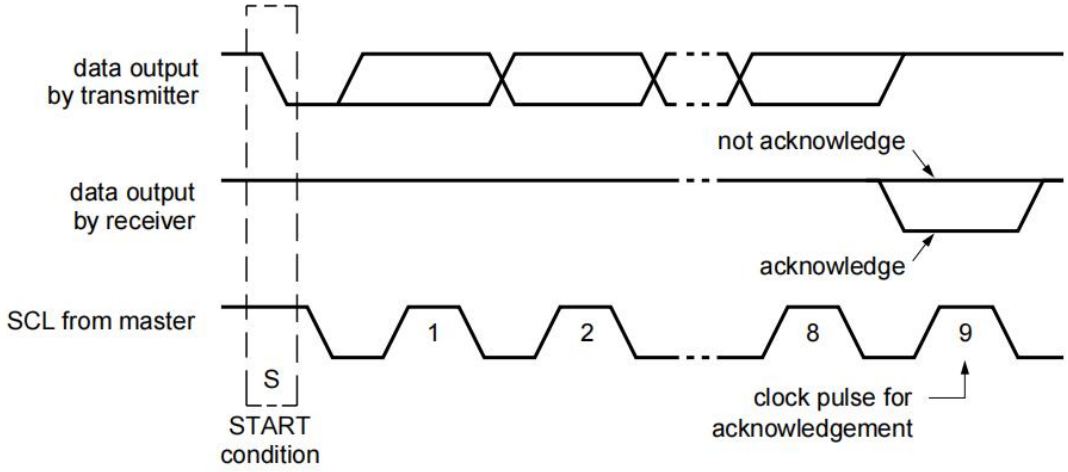



Figure 7.4：Acknowledgement on the I²C-bus

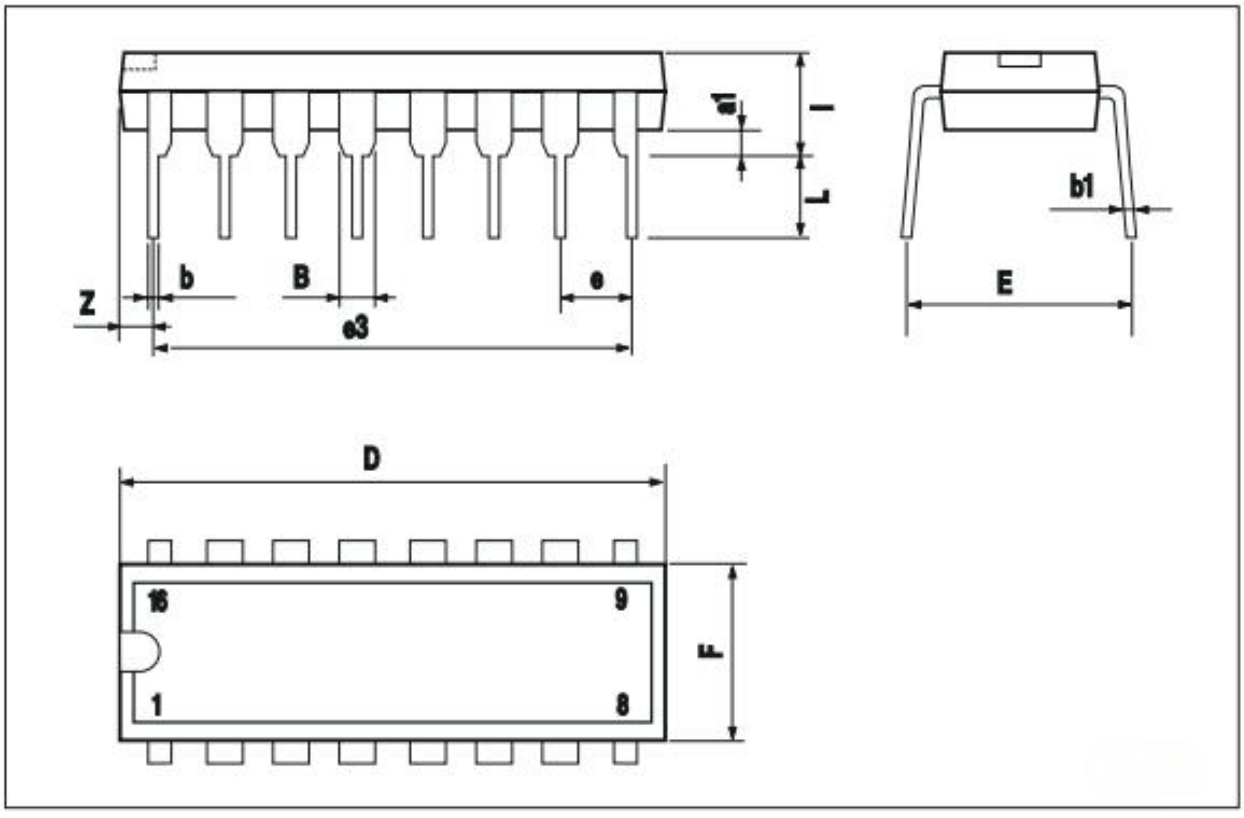
# 8. Ordering Information

| Orderable Device | Package Type | Pins | Packing | Package Qty |
|---|---|---|---|---|
| PCF8574ND16ATBE | DIP | 16 | Tube | 25 |
| PCF8574WS16ARAE | SOP - W | 16 | Tape & Reel | 1500 |
| PCF8574SS20ARBQ | SSOP | 20 | Tape & Reel | 2000 |
| PCF8574TS20ARCQ | SSOP | 20 | Tape & Reel | 3000 |

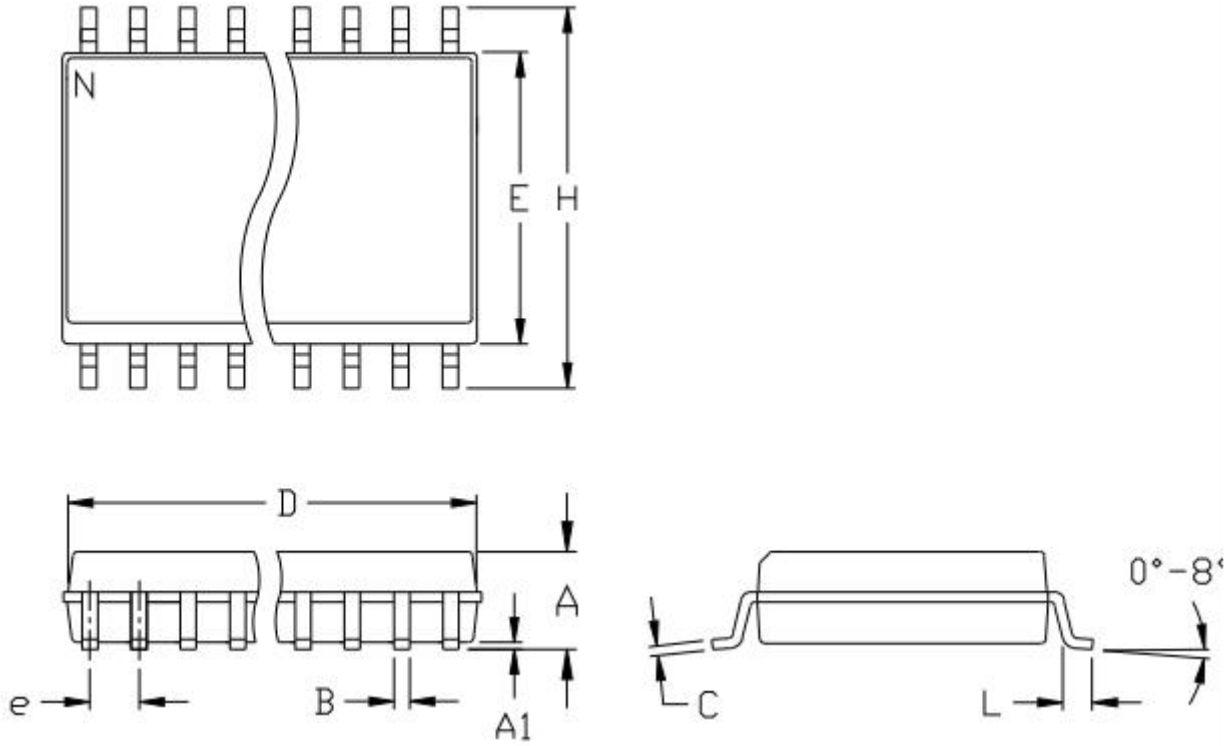
# 9. Package Information

## 9.1 DIP16

| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |



## 9.2 SOP16-W

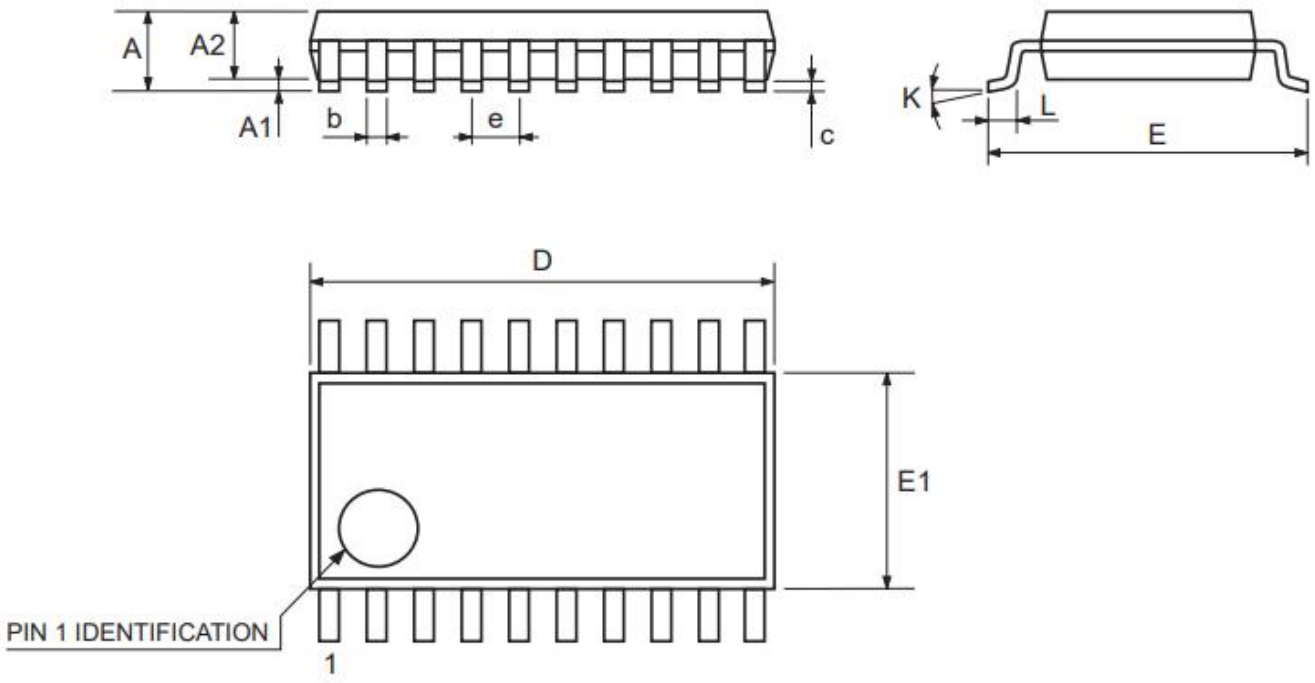



| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| e | 0.050 | | 1.27 | |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| h | 0.010 | 0.030 | 0.25 | 0.75 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS013 |
| D | 0.398 | 0.413 | 10.10 | 10.50 | 16 | AA |
| D | 0.447 | 0.463 | 11.35 | 11.75 | 18 | AB |
| D | 0.496 | 0.512 | 12.60 | 13.00 | 20 | AC |
| D | 0.598 | 0.614 | 15.20 | 15.60 | 24 | AD |
| D | 0.697 | 0.713 | 17.70 | 18.10 | 28 | AE |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

## 9.3 SSOP20




| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2 | | | 0.079 |
| A1 | 0.05 | | | 0.002 | | |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | | 0.38 | 0.009 | | 0.015 |
| c | 0.09 | | 0.25 | 0.004 | | 0.010 |
| D | 6.9 | 7.2 | 7.5 | 0.272 | 0.283 | 0.295 |
| E | 7.4 | 7.8 | 8.2 | 0.291 | 0.307 | 0.323 |
| E1 | 5 | 5.3 | 5.6 | 0.197 | 0.209 | 0.220 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | 4° | 8° | 0° | 4° | 8° |
| L | 0.55 | 0.75 | 0.95 | 0.022 | 0.030 | 0.037 |

## 9.4 TSSOP20

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 6.4 | 6.5 | 6.6 | 0.252 | 0.256 | 0.260 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |