8 BIT PISO SHIFT REGISTER

Features

- Low power dissipation: I_{CC} = 8μA (MAX.) at T_A = 25°C
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4mA (MIN.)
- Balanced propagation delays: $T_{PLH} \cong T_{PHL}$
- Wide operating voltage range: V_{CC}(OPR.) = 2V TO 6V

DIP-16

SOP-16

TSSOP-16

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC165DN	DIP-16	74HC165D	TUBE	1000pcs/box
74HC165DM/TR	SOP-16	74HC165D	REEL	2500pcs/reel
74HC165DMT/TR	TSSOP-16	HC165D	REEL	2500pcs/reel

Description

The 74HC165D is a high-speed CMOS 8 BIT PISO SHIFT REGISTER fabricated with silicon gate CMOS technology.

This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data enters when the shift/ $\overline{load}$ input is low. The parallel data can change while shift/ $\overline{load}$ is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/$\overline{load}$ must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

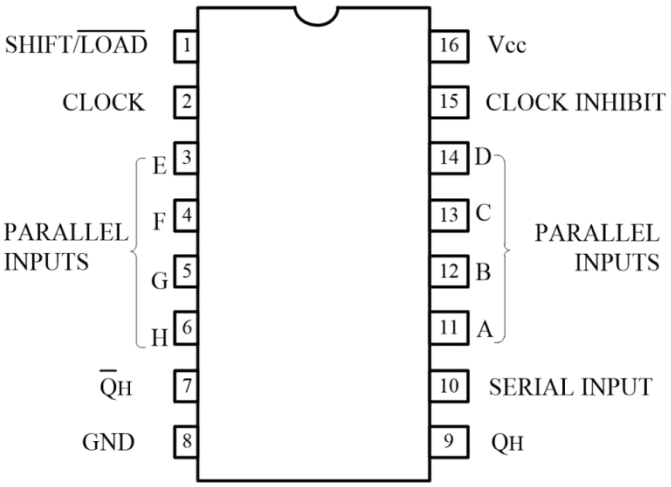
To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Applications

- Industrial
- Computer
- Consumer

Pin information



DIP-16/SOP-16/TSSOP-16

Pin description

Pin No	Symbol	Name and function
1	SHIFT/ $\overline{\text{LOAD}}$	Data Inputs
7	$\overline{\text{Q}}$H	Complementary Output
9	QH	Serial Output
2	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	SI	Serial Data Inputs
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	Clock Inhibit
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Functional description

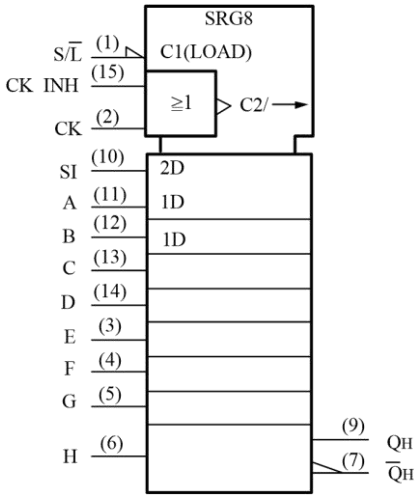
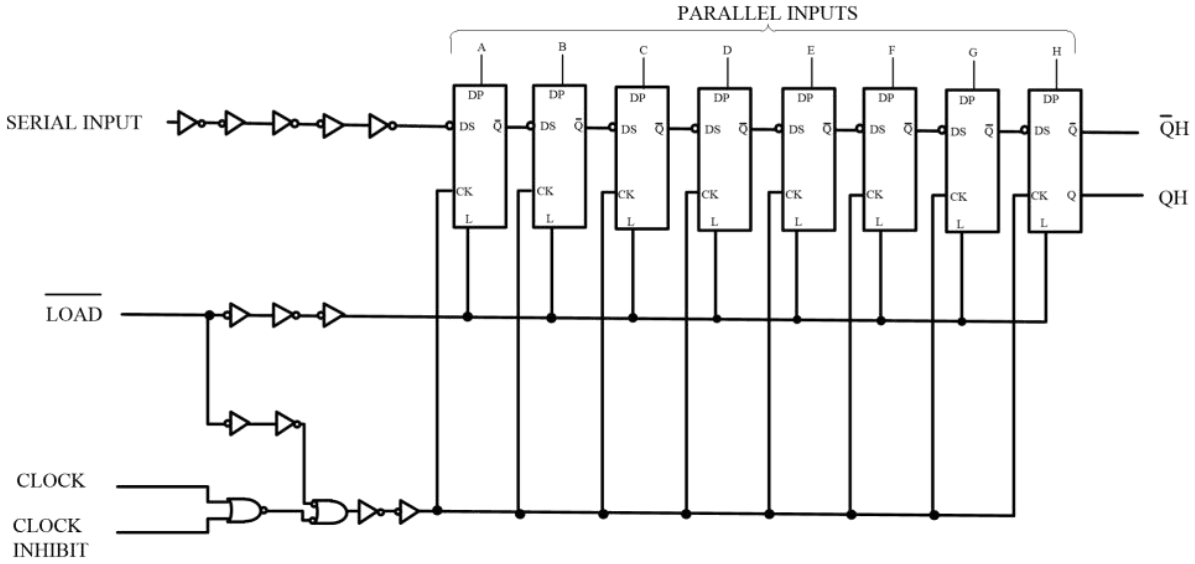


Figure 1. IEC logic symbols



This logic diagram has not been used to estimate propagation delays

Figure 2. Logic diagram

Truth table

INPUTS					INTERNAL OUTPUTS		OUTPUTS	
$\overline{\text{SHIFT/LOAD}}$	CLOCK INH	CLOCK	SI	A……H	QA	QB	QH	$\overline{Q}H$
L	X	X	X	a……h	a	b	h	$\overline{h}$
H	L	⎍	H	X	H	QAn	QGn	$\overline{Q}$Gn
H	L	⎍	L	X	L	QAn	QGn	$\overline{Q}$Gn
H	⎍	L	H	X	H	QAn	QGn	$\overline{Q}$Gn
H	⎍	L	L	X	L	QAn	QGn	$\overline{Q}$Gn
H	X	H	X	X	NO CHANGE			
H	H	X	X	X	NO CHANGE			

a……h: The level of steady input voltage at inputs a through respectively

QAn - QGn : The level of QA - QG, respectively. before the most-recent transition of the clock

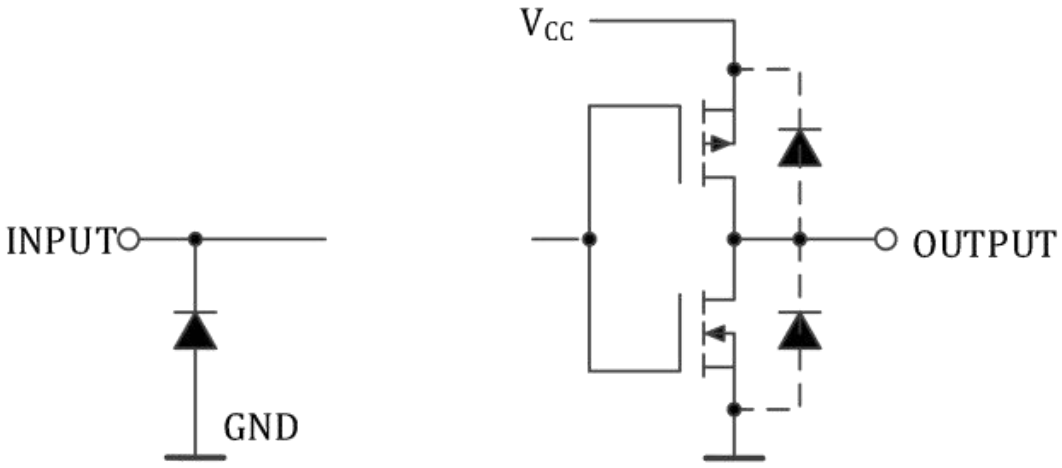


Figure 3. Input and output equivalent circuit

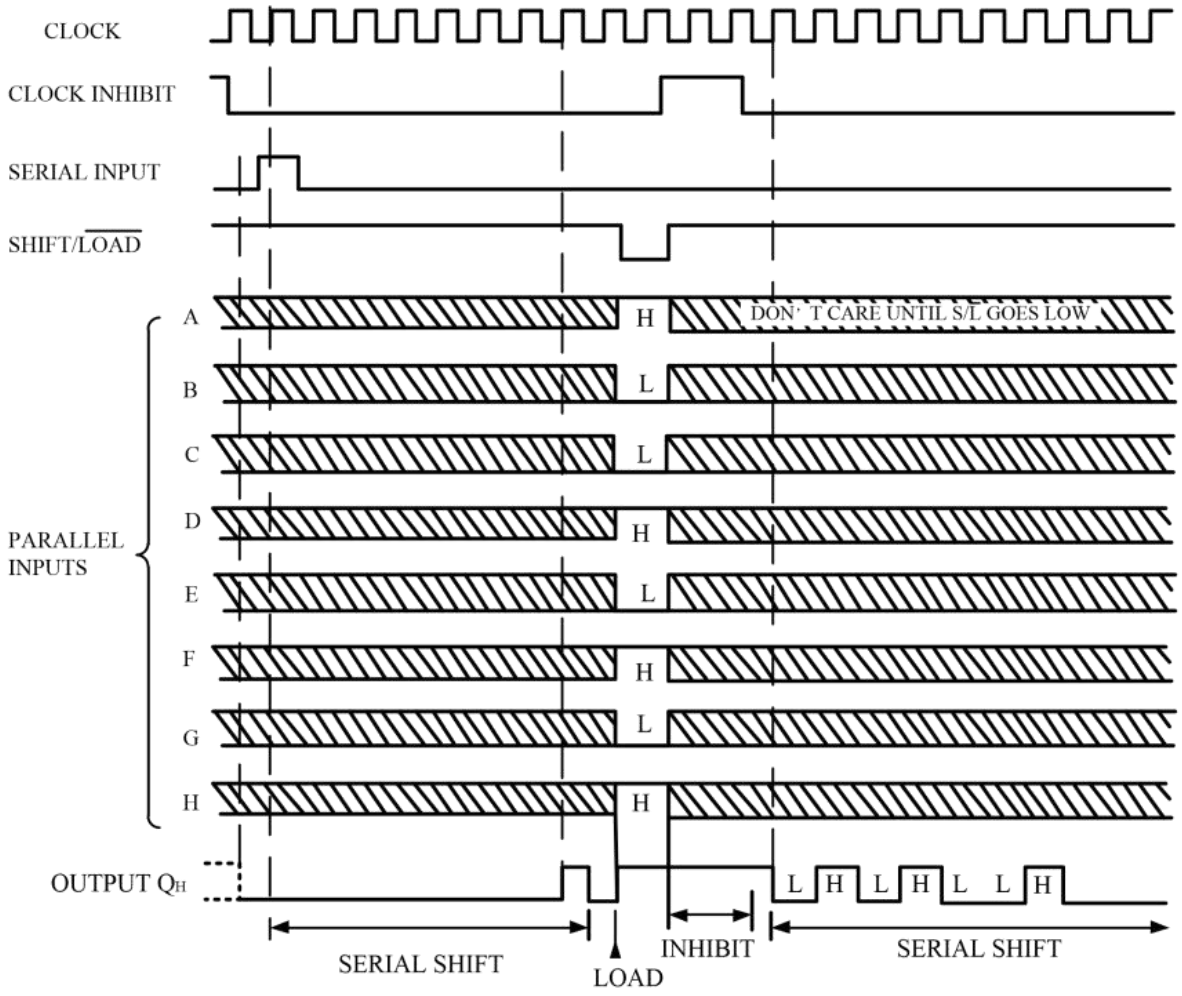


Figure 4. Timing chart

Electrical characteristics

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC}or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	260	°C

Note:Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C

DC specifications

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		T_A = 25 °C		-40 to 85°C		
				Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5		1.5		V
		4.5		3.15		3.15		
		6.0		4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V
		4.5			1.35		1.35	
		6.0			1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20uA	1.9		1.9		V
		4.5	I_O=-20uA	4.4		4.4		
		6.0	I_O=-20uA	5.9		5.9		
		4.5	I_O=-4.0 mA	3.98		3.7		
		6.0	I_O=-5.2 mA	5.48		5.2		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 uA		0.1		0.1	V
		4.5	I_O=20 uA		0.1		0.1	
		6.0	I_O=20 uA		0.1		0.1	
		4.5	I_O=4.0 mA		0.26		0.4	
		6.0	I_O=5.2mA		0.26		0.4	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND		±0.1		±1	uA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		8		160	uA

AC electrical characteristics

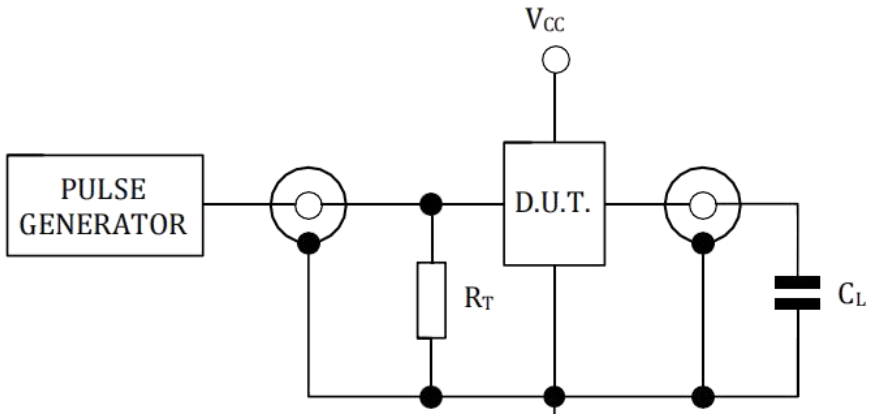
(CL = 50pF, Input tr = tf = 6ns)

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		T_A= 25°C		-40 to 85°C		
				Min	Max	Min	Max	
$t_{TLH}t_{THL}$	Output Transition Time	2.0			75		110	ns
		4.5			15		22	
		6.0			13		19	
$t_{PLH}t_{PHL}$	Propagation Delay Time(CLOCK – QH, $\overline{QH}$)	2.0			150		225	ns
		4.5			30		45	
		6.0			26		38	
$t_{PLH}t_{PHL}$	Propagation Delay Time (SHIFT/ $\overline{LOAD}$ – QH, $\overline{QH}$)	2.0			150		225	ns
		4.5			30		45	
		6.0			26		38	
$t_{PLH}t_{PHL}$	Propagation Delay Time (H– QH, $\overline{QH}$)	2.0			150		225	ns
		4.5			30		45	
		6.0			26		38	
f_{MAX}	Maximum Clock Frequency	2.0		6		4.2		MHz
		4.5		31		21		
		6.0		36		25		

Capacitive characteristics

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		T_A = 25°C		-40 to 85°C		
				Min	Max	Min.	Max.	
C_{IN}	Input Capacitance	5.0			10		10	pF

Test circuit



R_T=Z_{OUT} of pulse generator (typically 50 Ω).

C_L = 50 pF or equivalent (includes jig and probe capacitance)

Figure 5. Test circuit

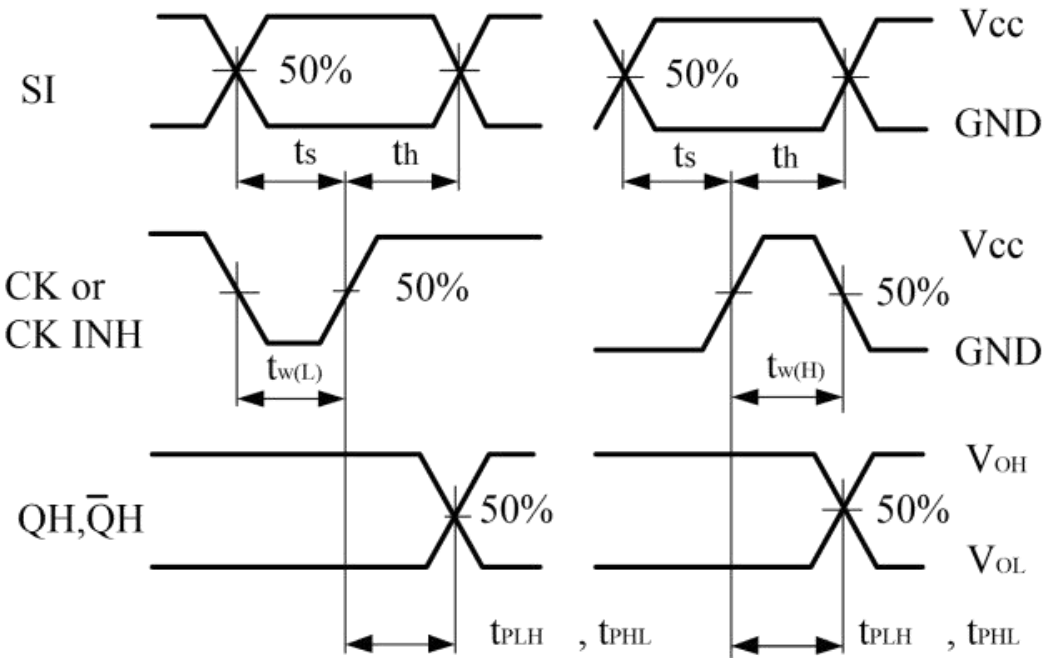


Figure 6. Waveform 1: serial mode propagation delay (f=1MHz; 50% duty cycle)

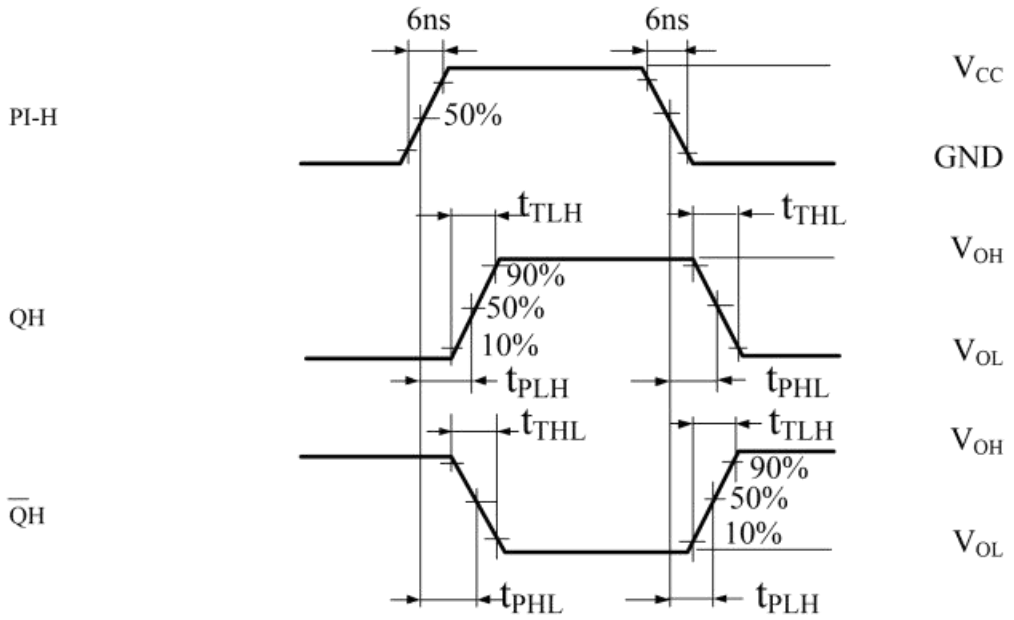


Figure 7. Waveform 2:parallel mode propagation delay (f=1MHz; 50% duty cycle)

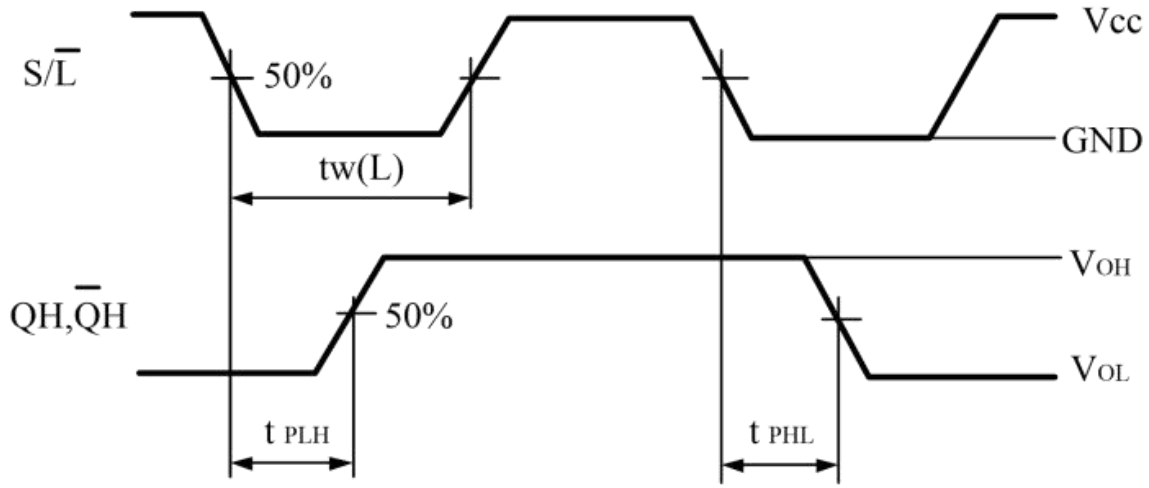


Figure 8. Waveform 3:minimum pulse width(S/ L), propagation delay times (f= 1MHz; 50% duty cycle)

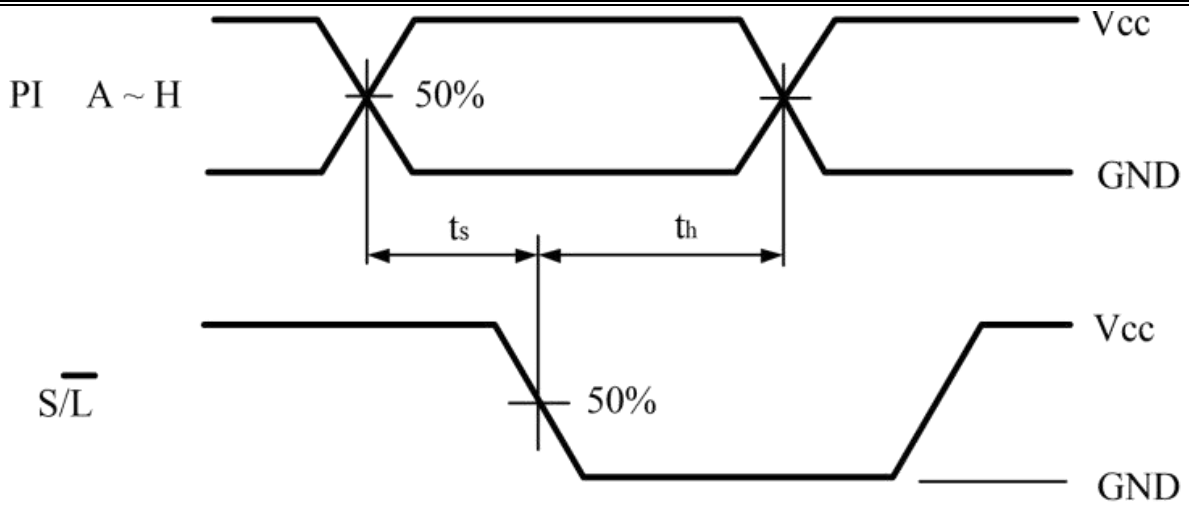


Figure 9. Waveform 4:setup and hold time (PI to S/ L̄) (f= 1MHz; 50% duty cycle)

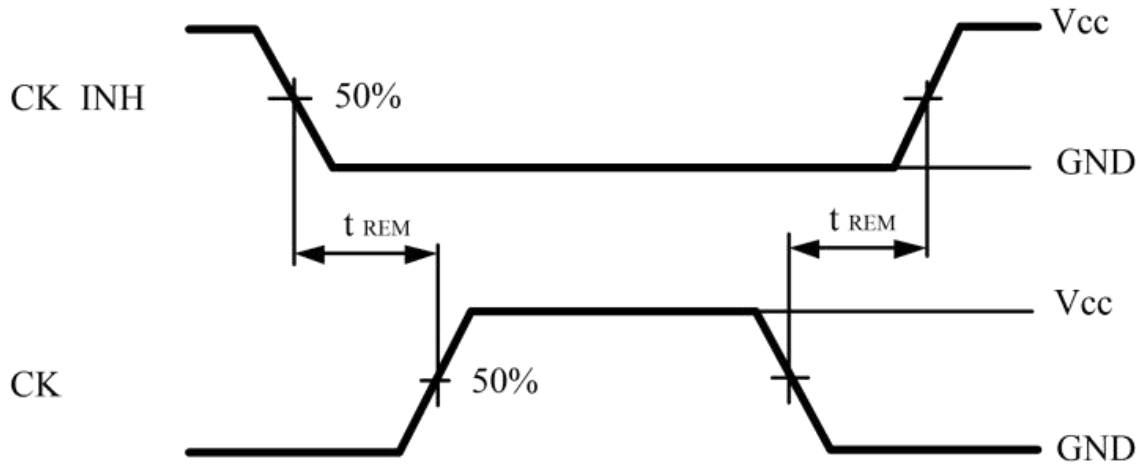
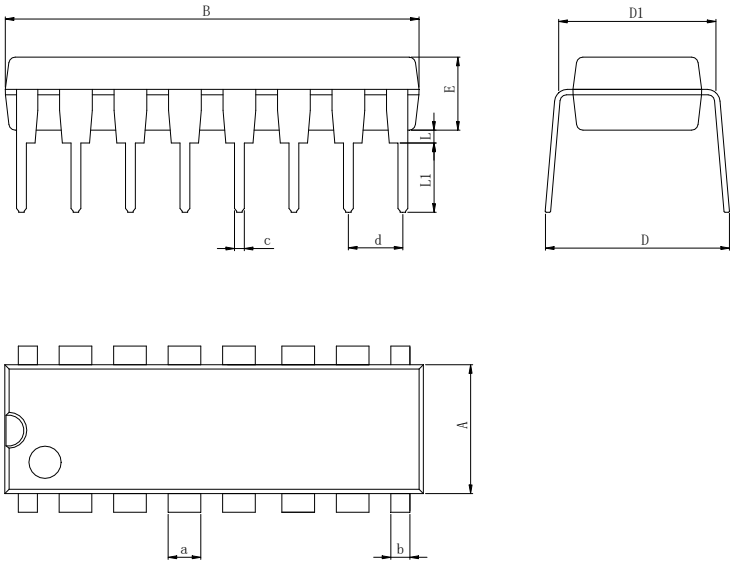


Figure 10. Waveform 5: minimum removal time (CK INH to CK) (f= 1MHz; 50% duty cycle)

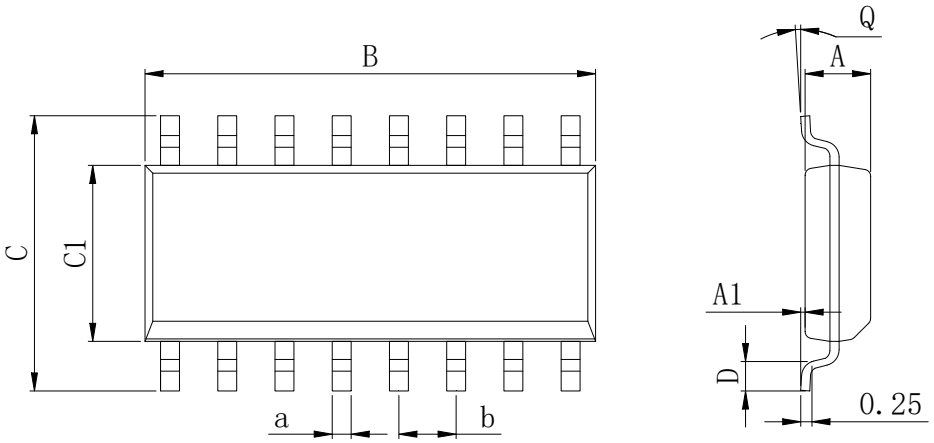
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

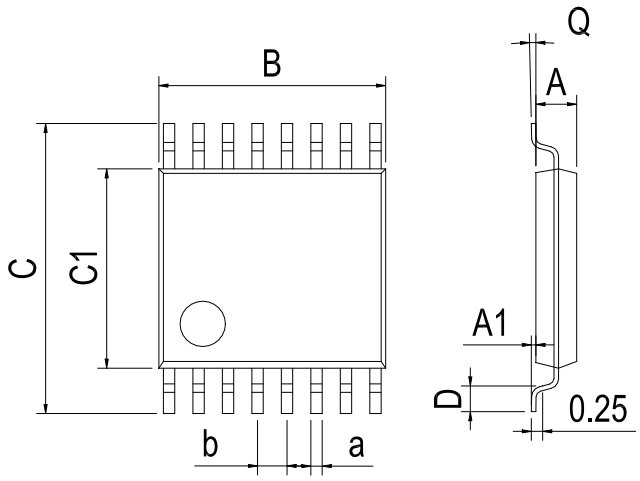
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2020-5	New	1-12
V1.1	2025-4	Document Reformatting	1-15

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