XPD1024 Datasheet

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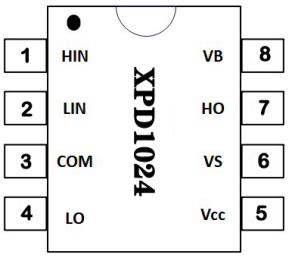
1. Pin Configurations and Functions

Symbol	Pin#	Description
HIN	1	Logic input for high side gate driver output (HO), in phase
LIN	2	Logic input for low side gate driver output (LO), in phase
COM	3	Low-side gate drive return
LO	4	Low side gate drive output
VCC	5	Low side and logic fixed supply
VS	6	High side floating supply return
HO	7	High side gate drive output
VB	8	High side floating supply



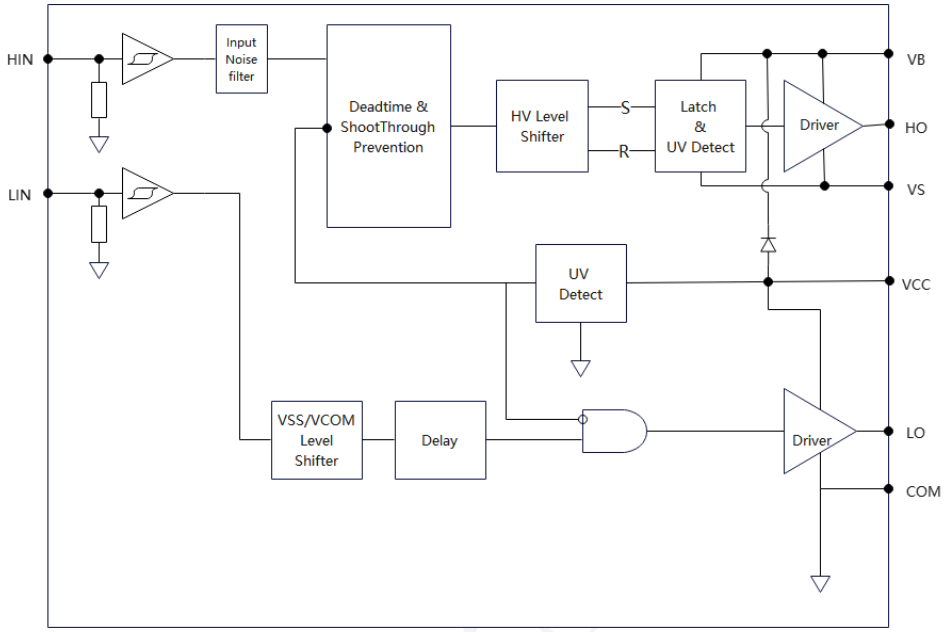
XPD1024-SOP8

2. Ordering Information

Base Part Number	Package Type	Ordering Part Number
XPD1024	SOP8	XPD1024IQ08E

3. Block Diagram

3.1 XPD1024 Block Diagram



4. EC Table

4.1 Absolute Parameters

Symbol	Definition	Min.	Max.	Units
VB	High-side floating well supply voltage	-0.5	650	V
VS	High-side floating well supply return voltage Note 1	VB – 25	VB + 0.5	
VBS	High-side floating supply voltage (VB vs. VS) (internally clamped)	-0.5	25	
VHO	Floating gate drive output voltage	VS – 0.5	VB + 0.5	
VCC	Low side supply voltage (VCC vs. VSS) (internally clamped)	-0.5	25	
VLO	Low-side output voltage	–0.5	VCC + 0.5	
VIN	Logic input voltage (HIN, LIN)	COM - 0.5	VCC + 0.5	
dVS/dt	Allowable VS offset supply transient relative to COM	—	50	V/nS
PD	Package power dissipation @ TA ≤25°C	—	1.6	W
Rth_{JA}	Thermal resistance, junction to ambient	—	78	°C/W

Ψ_{Jtop}	Characterization parameter junction to package top Note		4	
T_J	Junction temperature	-40	150	℃
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Note : Obtained in the simulation according to JEDEC-standard and Ta = 50 °C, PD= 1W, PCB: JEDEC 2s2p (JESD 51-5)

4.2 Typical Parameters

Symbol	Definition	Min	Max	Units
V_B	Bootstrap voltage Note 1	V_S + 13	V_S + 20	V
V_{BS}	High-side floating well supply voltage	13	20	
V_S	High-side floating well supply offset voltage Note 1	-8	600	
V_{St}	Transient High-side floating well supply offer voltage (<700ns) Note 2	-100	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
VLO	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN, LIN, RFE, ITRIP)	COM	V_{CC}	
t_{IN}	Minimal pulse width for ON or OFF	0.3	—	μs
T_A	Ambient temperature	-40	125	℃

Note 1: In case VCC > VB there is an additional power dissipation in the internal bootstrap diode between pins VCC and VB in case of activated bootstrap diode.

Note 2: Consistent power dissipation of all outputs. All parameters inside operating range.

4.3 Static Parameters

V_{BIAS} (V_{CC}, V_{BS}) = 15V, @T_A = +25°C, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.5	0.9	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8	V_{CCUV+}	V_{CC} supply undervoltage positive going threshold
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0	V_{CCUV-}	V_{CC} supply undervoltage negative going threshold

V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.5	0.9	—	V_{CCUVHY}	V_{CC} supply undervoltage hysteresis
I_{LK}	High-side floating well offset supply leakage	—	0.5	20	uA	V_B = 600 V V_S = 600 V
I_{QCC}	Quiescent V_{CC} supply current	—	700	1000		V_{IN} = 0V or 3.3V
I_{QBS}	Quiescent V_{BS} supply current	—	100	180		
V_{OH}	High level output voltage drop, V_{cc}- V_{LO} , V_B- V_{HO}	—	0.32	0.7	V	I_O = 100 mA
V_{OL}	Low level output voltage drop, V_O	—	0.18	0.4		
I_o+mean	Mean output current from 4.5 V to 7.5 V	1.4	2	—	A	C_L = 56 nF
I_o+1	Peak output current turn-on	—	2.3	—		R_L = 0 Ω PW ≤ 10 μs
Io-mean	Mean output current from 7.5 V to 4.5 V	2.8	4	—		C_L = 56 nF
Io-1	Peak output current turn-off	—	4.6	—		R_L = 0 Ω PW ≤ 10 μs
V_{IH}	Logic “1” input voltage (HIN, LIN)	2.0	2.3	2.6	V	
V_{IL}	Logic “0” input voltage (HIN, LIN)	1.0	1.3	1.6		
I_{IN+}	Input bias current (Output = High)	15	35	60	μA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (Output = Low)	—	0	—		V_{IN} = 0 V

4.4 Dynamic Parameters

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay		220	360	500	ns	V_{IN} = 0 V or 3.3 V V_S = 0 V or 600 V
t_{OFF}	Turn-off propagation delay		200	330	470		
t_R	Turn-on rise time		—	22	40		V_{IN} = 0 or 3.3 V C_L = 1nF
t_F	Turn-off fall time		—	16	30		
t_{FILIN}	Input filter time at LIN/HIN for turn-on and -off		100	150	—		V_{IN} = 0 & 3.3 V
$t_{UVLOFIL}$	UVLO Noise filter		1	1.5	—		

M_T	Delay matching time (HS & LS turn-on/off)		—	10	60	ns	external dead time > 500ns
PM	Output pulse width matching		—	20	80		P_{WIN} > 1 μs

5. Functions and Applications

5.1 IN/OUT Timing

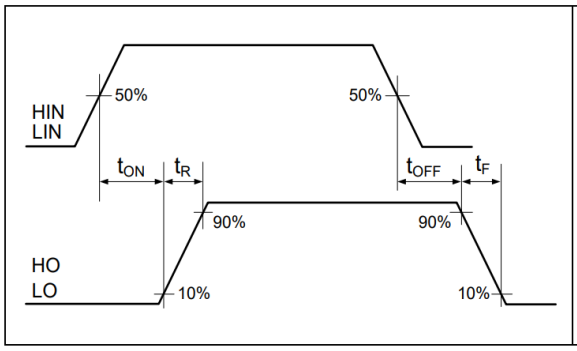


Figure 1 Switching timing diagram

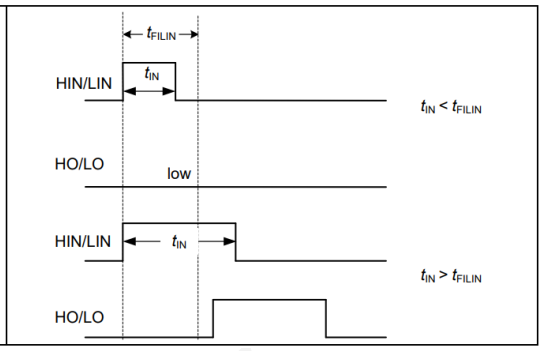


Figure 2 Input Filter

5.2 Deadtime Protection

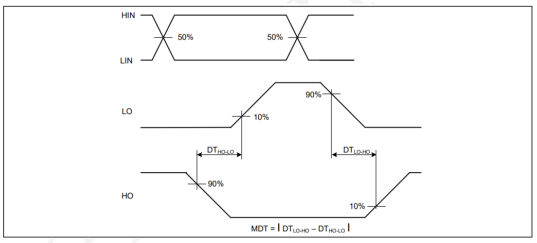


Figure 4 Deadtime matching waveform definition

This XPD1024 features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than internal deadtime; external deadtimes larger than internal deadtime are not modified by the gate driver. Figure 4 illustrates the deadtime period and the relationship between the output gate signals. The deadtime circuitry of XPD1024 is matched with respect to the high- and low-side outputs. Figure 4 defines the two deadtime parameters (i.e., DTLO-HO and DTHO-LO); the deadtime matching parameter (MDT) associated with the XPD1024 specifies the maximum difference between DTLO-HO and DTHO-LO.

5.3 Propagation Delay Match

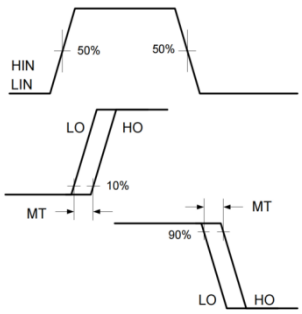


Figure 5 Delay matching waveform definition

The XPD1024 is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (M_T). The propagation turn-on delay (t_{ON}) of the XPD1024 is matched to the propagation turn-on delay (t_{OFF}).

5.4 VIH/VIL

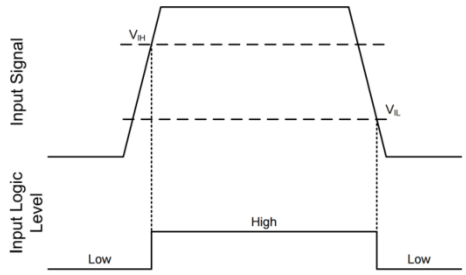


Figure 6 HIN & LIN input thresholds

The input pins are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With typical high threshold (VIH) of 2.0 V and typical low threshold (VIL) of 0.9 V, along with very little temperature variation as summarized in Figure 6 the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 1.1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. XPD1024 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The XPD1024 features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved by using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The XPD1024 has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

5.5 UVLO Protection

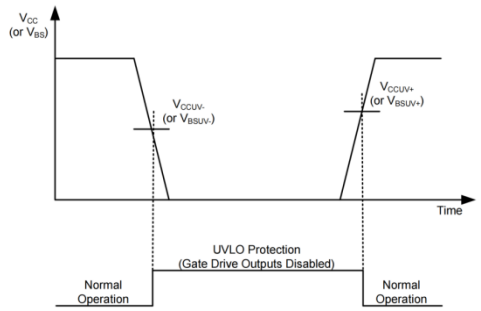


Figure 7 UVLO protection

This IC provides undervoltage lockout protection on both the VCC (logic and low-side circuitry) power supply and the VBS (high-side circuitry) power supply. Figure 7 is used to illustrate this concept; VCC (or VBS) is plotted over time and as the waveform crosses the UVLO threshold (VCCUV+/- or VBSUV+/-) the undervoltage protection is enabled or disabled. Upon power-up, should the VCC voltage fail to reach the VCCUV+ threshold, the IC won't turn-on. Additionally, if the VCC voltage decreases below the VCCUV- threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs. Upon power-up, should the VBS voltage fail to reach the VBSUV+ threshold, the IC won't turn-on. Additionally, if the VBS voltage decreases below the VBSUV- threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC. The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

5.6 Negative Voltage Transient Tolerance of VS pin

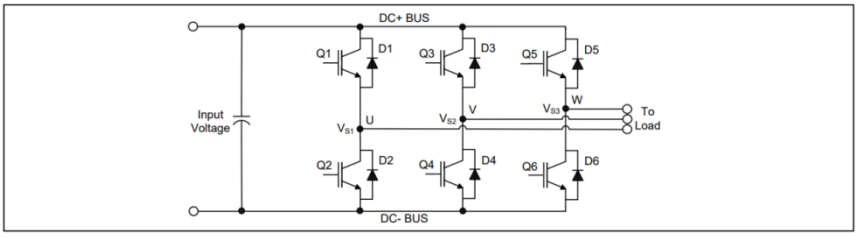


Figure 8 Three phase inverter

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 8 here we define the power switches and diodes of the inverter. If the high-side switch (e.g., the IGBT Q1 in Figure 9) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node VS1, swings from the positive DC bus voltage to the negative DC bus voltage.

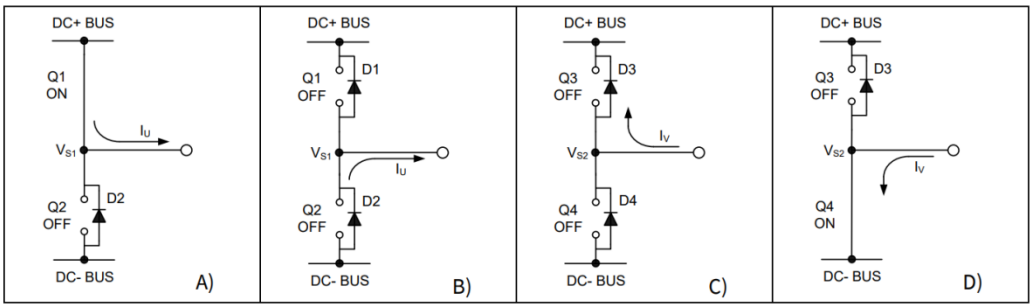


Figure 9 A.Q1conducting B. D2 conducting C. D3 conducting D. Q4 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figure 9 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, VS2, swings from the positive DC bus voltage to the negative DC bus voltage. However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative VS transient”.

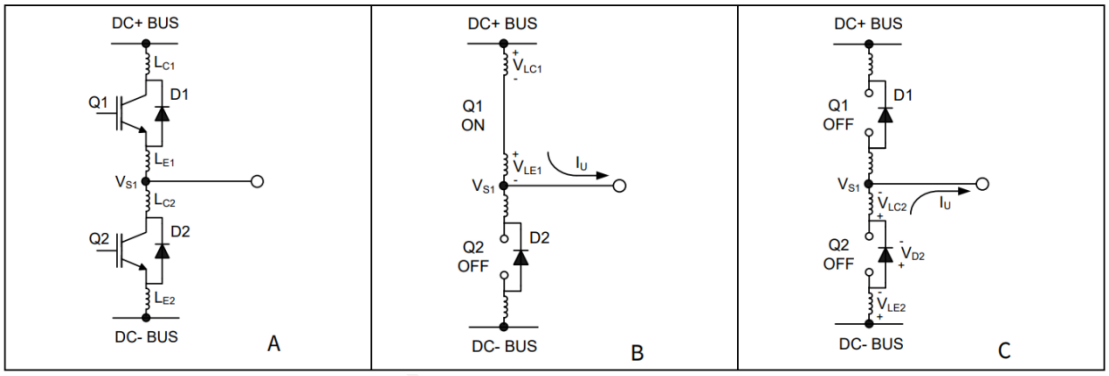


Figure 10 Figure A shows the Parasitic Elements. Figure B shows the generation of VS positive. Figure C shows the generation of VS negative

The circuit shown in Figure 10-A depicts one leg of the three phases inverter; Figure 10-B and Figure 10-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in LC and LE for each IGBT. When the high-side switch is on, VS1 is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to VS1 (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between VS1 and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the VS pin).

5.7 NTSOA – Negative Transient Safe Operating Area

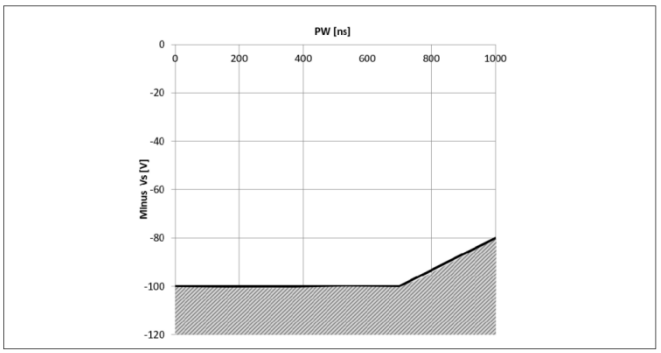


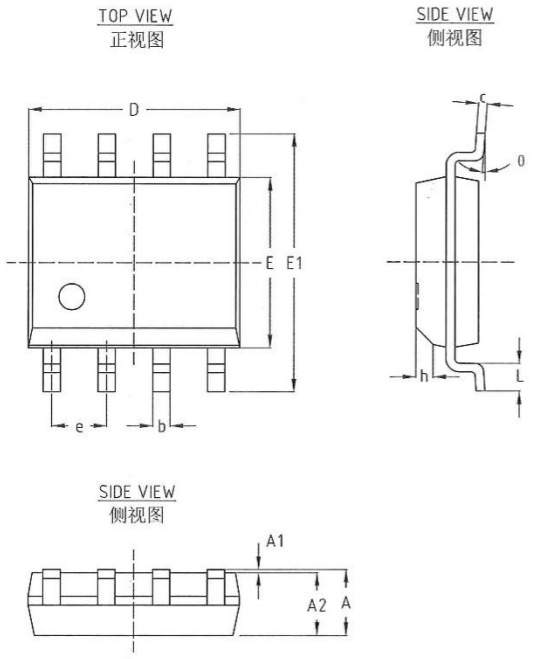
Figure 11 Negative VS transient SOA for XPD10XX

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation. Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the XPD1024's robustness can be seen in Figure 11, where the XPD1024's Safe Operating Area is shown at VBS=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

Even though the XPD1024 has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

Package Description

5.8 SOP8



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.04	–	0.12
A2	1.35	1.45	1.55
b	0.35	–	0.50
c	0.19	–	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.50	–	0.80
θ	0°	–	8°

6. Revision History

Rev.	History	Time
0.1	1. Initial	2025.3
0.2	2. Modified some parameters value according to design simulation resilts.	2025.6
0.3	3. Corrected some labeling mistakes	2025.6