MSKSEMI 美森科













ESD

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TSS

MOV

GDT

PLED

MSADP7118AUJZ-x.x

Product specification





GENERAL DESCRIPTION

The MSADP7118AUJZ-x.x series are a group of low-dropout (LDO) voltage regulators offering the benefits of wide input voltage range, low dropout voltage, low power consumption, and miniaturized packaging.

Quiescent current of only 1.5µA makes these devices ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life.

The MSADP7118AUJZ-x.x series of linear regulators are stable with the ceramic output capacitor over its wide input range from 2V to 24V and the entire range of output load current (0mA to 300mA).

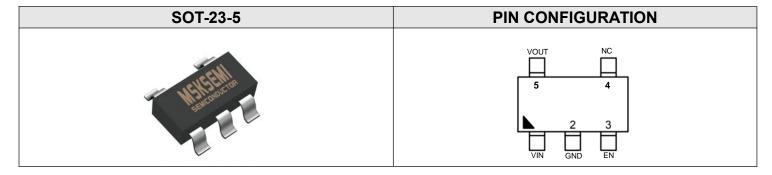
FEATURES

- 1.5µA Ground Current at no Load
- ±2% Output Accuracy
- 300mA Output Current
- Wide Operating Input Voltage Range: 2V to 24V
- Dropout Voltage: 0.35V at 100mA / Vout 5V
- Support Fixed Output Voltage 1.8V, 2.5V, 3.3V, 5V
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-23-5 Packages Available

APPLICATIONS

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems
- Industrial Controls
- Weighting Scales
- Meters
- Home Automation

Reference News



Description of Functional Pins

| Pin No SOT-23-5 | Pin Name | Pin Function | |
|--------------------|----------|--------------------------|--|
| 2 | GND | Ground | |
| 5 | VOUT | Output of the Regulator | |
| 1 | VIN | Input of Supply Voltage. | |
| 4 | NC | No Internal Connection. | |
| 3 | EN | Enable Control Input. | |



MARKING

| MSADP7118AUJZ-1.8 | MSADP7118AUJZ-2.5 | MSADP7118AUJZ-3.3 | MSADP7118AUJZ-5.0 | |
|-------------------|-------------------|-------------------|-------------------|--|
| LPA#MS | LPB#MS | LPC#MS ● | LPD#MS | |
| ● | ● | | ● | |

ORDER INFORMATION

| P/N | Output Voltage | PKG | QTY | |
|-------------------|-------------------|----------|------|--|
| MSADP7118AUJZ-1.8 | 1.8V | SOT-23-5 | | |
| MSADP7118AUJZ-2.5 | 2.5V | | 3000 | |
| MSADP7118AUJZ-3.3 | 3.3V | | | |
| MSADP7118AUJZ-5.0 | 5.5V | | | |

Typical Application Circuits

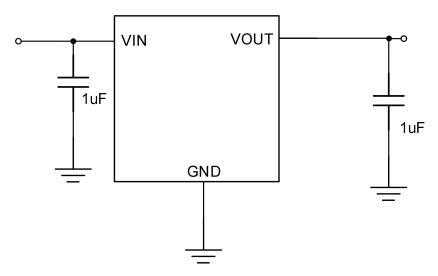
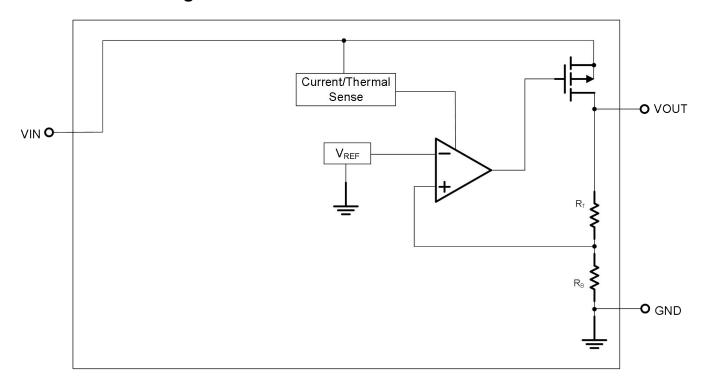


Figure 1: Application circuit of Fixed V_{OUT} LDO



Function Block Diagram





MSADP7118AUJZ-x.x

| Absolute Maximum Ratings (Note 1) | |
|---------------------------------------|-----------------|
| VIN to GND | 0.3V to 28V |
| VOUT to GND | |
| 1.8V,2.5V,3.3V,5.0V | 0.3V to 6.0V |
| VOUT to VIN | 28V to 0.3V |
| Package Thermal Resistance (Note 2) | |
| SOT-23-5, θ JA | 200 °C /W |
| Lead Temperature (Soldering, 10 sec.) | 260 °C |
| Junction Temperature | |
| Storage Temperature Range | 40 °C to 150 °C |
| ESD Susceptibility | |
| HBM | 2KV |
| MM | 200V |
| | |
| | |
| Recommended Operating Conditions | |
| Input Voltage VIN | 2.0V to 24V |
| Junction Temperature Range | |
| | |



Electrical Characteristics

(V_{IN} =15V, V_{EN} =5V, T_A =25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Тур | Max | Unit |
|--|------------------------|---|-----|------|-----|------|
| Supply Voltage | V _{IN} | | 2 | | 24 | V |
| DC Output Voltage Accuracy | | I _{LOAD} =0.1mA | -2 | | 2 | % |
| Dropout Voltage (I _{LOAD} =100mA) | V _{DROP} | V _{OUT} ≥ 5V | | 0.35 | | |
| | V _{DROP_3.3V} | V _{OUT} = 3.3V | | 0.42 | | V |
| | V _{DROP_1.8V} | V _{OUT} = 1.8V | | 0.5 | | |
| Ground Current (I _{LOAD} = 0mA) | ΙQ | V _{OUT} = 5V | | 2.2 | | μA |
| Line Regulation | ΔLINE | $I_{LOAD} = 1 \text{mA},$ $5 \le V_{IN} \le 30 \text{V}$ | | 0.3 | | % |
| Load Regulation | ΔLOAD | 1mA≤ I _{LOAD} ≤ 0.2A | | 0.1 | | % |
| Output Current Limit | I _{LIM} | V _{OUT} =0 | | 300 | 500 | mA |
| Power Supply Rejection Ratio | PSRR | V _{OUT} =5V, I _{LOAD} =1mA, V _{IN} = 12V, f = 100Hz | | 70 | | dB |
| Thermal Shutdown Temperature | T _{SD} | ILOAD =10mA | | 160 | | °C |
| Thermal Shutdown Hysteresis | ΔT _{SD} | ILUAD - IUIIA | | 15 | | °C |

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.



Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of MSAD P7118AUJZ-x.x series must be properly selected f or stability and performance. Use a $1\mu F$ or larger input capacitor and place it close to the IC's VIN and GN D pins. Any output capacitor meeting the minimum 1m Ω ESR (Equivalent Series Resistance) and effective c apacitance between $1\mu F$ and $22\mu F$ requirement may be used. Place the output capacitor close to the IC's V OUT and GND pins.Increasing capacitance and de creasing ESR can improve the circuit's PSRR and lin e transient response.

Current Limit

The MSADP7118AUJZ-x.x series contain the curren t limiter of output power transistor, which monitors a nd controls the transistor, limiting the output cur rent to 500mA(typical).

The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The MSADP7118AUJZ-x.x series use a PMOS pass transistor to achieve low dropout. When (VIN – VOUT) is less than the dropout voltage (VDROP the PMOS pass device is in the linear region of operation and the input- to-output resistance is the RDS(ON) of the PMOS pass element. VDROP scales approximately with the output current because the PMOS device behaves as aresistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (VIN – VOUT) approaches dropout condition.

OTP (Over Temperature Protection)

The over temperature protection function of MSAD P7118AUJZ-x.x series will turn off the PMOSFET w hen the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by appro ximately 15°C, the regulator will automatically resume operation.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

The max PD (Max)= $(125^{\circ}C - 25^{\circ}C) / (200^{\circ}C/W) = 0.5W$ for SOT-23-3 / SOT-23-5 packages.

The max PD (Max)= $(125^{\circ}C - 25^{\circ}C) / (120^{\circ}C/W) = 0.83W$ for SOT-89-3 package

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

PD = (VIN - VOUT) × IOUT

Layout Consideration

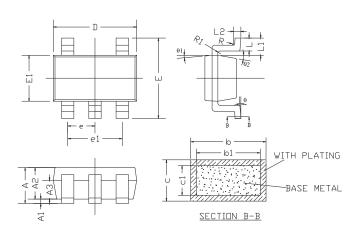
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the MSADP7118AUJZ-x.x ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.



Package Outline

Package SOT-23-5

Package dimension (mm):



Devices per reel

| Symbol | MIN | NORM | MAX | |
|------------|----------|----------|-------|--|
| А | - | - | 1.25 | |
| A1 | 0.00 | - | 0.15 | |
| A2 | 1.00 | 1.10 | 1.20 | |
| A3 | 0.60 | 0.65 | 0.70 | |
| b | 0.36 | - | 0.50 | |
| b1 | 0.36 | 0.38 | 0.45 | |
| С | 0.14 | - | 0.20 | |
| c1 | 0.14 | 0.15 | 0.16 | |
| D | 2.826 | 2.926 | 3.026 | |
| Е | 2.60 | 2.80 | 3.00 | |
| E1 | 1.526 | 1.626 | 1.726 | |
| е | 0.90 | 0.95 | 1.00 | |
| e1 | 1.80 | 1.90 | 2.00 | |
| L | 0.35 | 0.45 | 0.60 | |
| L1 | | 0.59 REF | | |
| L2 | 0.25 BSC | | | |
| R | 0.05 | - | - | |
| R1 | 0.05 | - | 0.20 | |
| Θ | 0° | - | 8° | |
| Θ1 | 3° | 5° | 7° | |
| Θ 2 | 6° | - | 14° | |



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