MSKSEMI 美森科
SEMICONDUCTOR

ESD TVS TSS MOV GDT PLED

MSIR2113STR

Product specification

产品概述

MSIR2113STR 是一款高压、高速的功率 MOSFET 和 IGBT 驱动器，它提供独立的高边、低边输出驱动信号。采用专有的高压集成电路和锁存免疫 CMOS 技术，提供可靠的单芯片驱动方案。逻辑输入电平与标准 CMOS 或 LSTTL 输出兼容，最低支持 3.3V 逻辑。输出驱动器具有高脉冲电流缓冲级，以减小驱动器交叉导通。延时匹配功能方便应用于高频设备。浮动通道可用于驱动高边配置的 N 型沟道功率 MOSFET 或 IGBT，工作电压可以达到 600V。

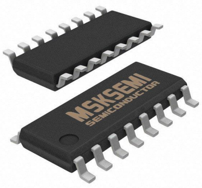
主要特点

- 为自举供电设计的浮动通道
- 工作电压最高达到 600V
- 允许瞬态负电压，不受 dV/dt 影响
- 驱动电源范围从 10V 到 20V
- 高低边欠压锁定
- 3.3V、5V 和 15V 逻辑兼容
- 逻辑地和功率地能承受±5V 偏置
- 防止交叉导通逻辑
- 带有下拉电阻的施密特触发器
- 逐周期边缘触发的关闭逻辑
- 两通道间的传递延时匹配
- 输入输出同相
- 典型驱动电流：2.0A/2.0A
- 典型开启/关闭延时：140ns/140ns
- 符合 RoHS
- SOP-16 封装

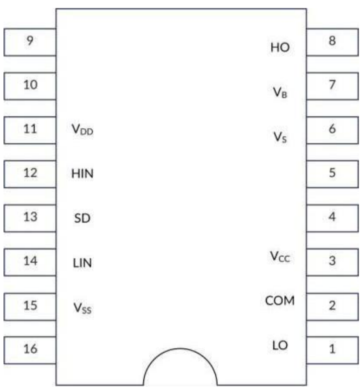
典型应用

- 充电器、电源适配器等
- 通用逆变器
- 电机驱动

封装信息

SOP-16	管体标记
	MSKSEMI R2113S MS**

引脚排列



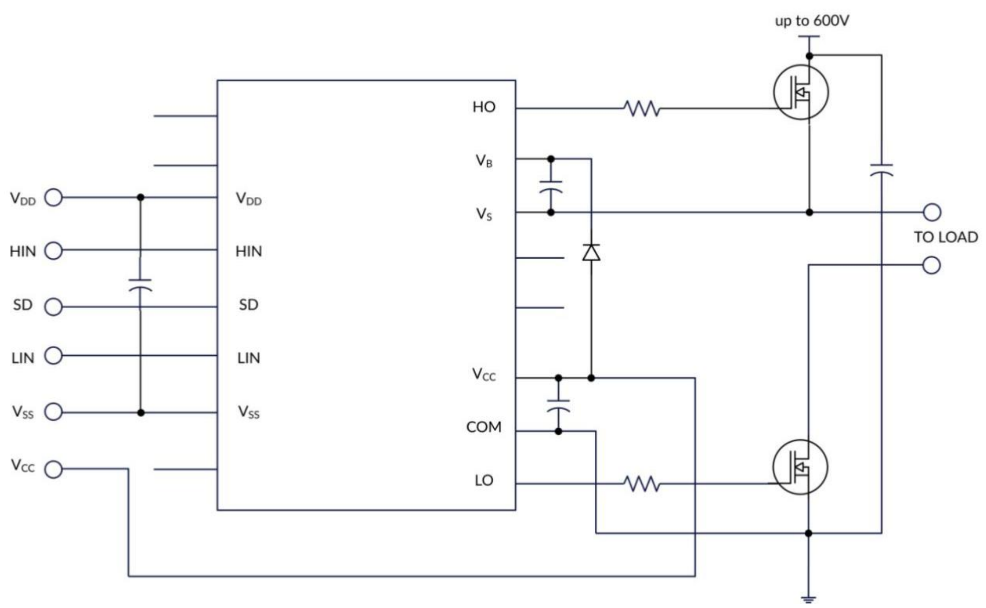
引出端功能

序号	符号	功能描述
1	LO	低端驱动输出
2	COM	低端公共端
3	V_{CC}	低端电源
4	NC	
5	NC	
6	V_S	高端悬浮输出端
7	V_B	高端自举电源
8	HO	高端驱动输出
9	NC	
10	NC	
11	V_{DD}	逻辑电源
12	HIN	高端驱动逻辑输入
13	SD	驱动关闭控制
14	LIN	低端驱动逻辑输入
15	V_{SS}	逻辑地
16	NC	

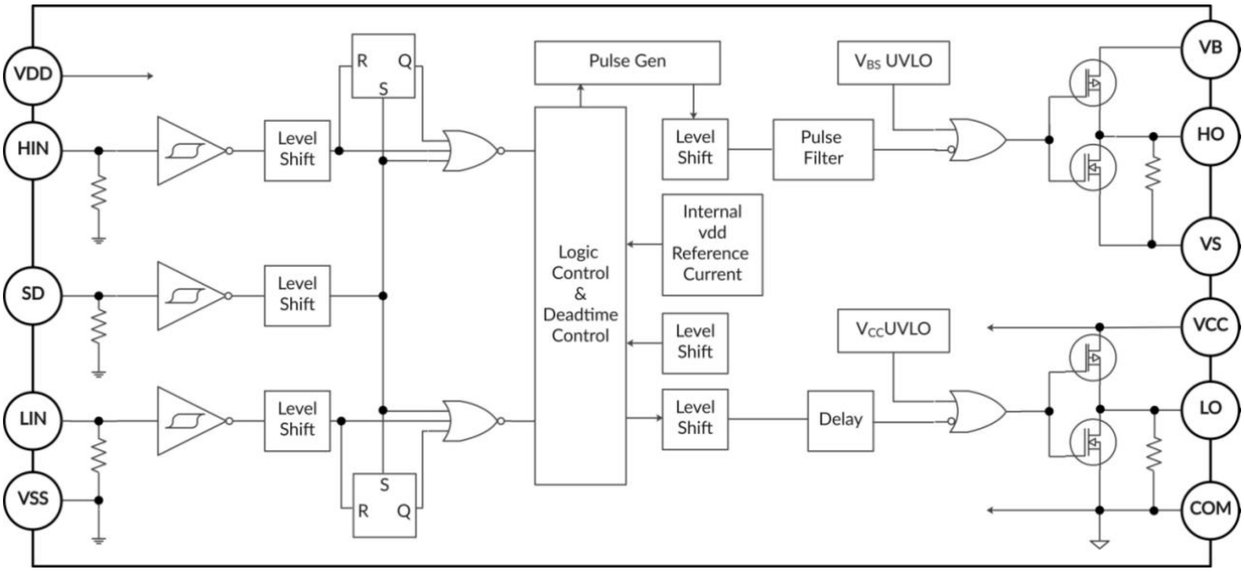
订货信息

型号	封装形式	QTY
MSIR2113STR	SOP-16	1500PCS

典型应用



电路方框图


VDD
HIN
SD
LIN
VSS
Level Shift
Level Shift
Level Shift
R Q S
S R Q
Pulse Gen
Logic Control & Deadtime Control
Level Shift
Internal vdd Reference Current
Level Shift
Level Shift
Pulse Filter
Delay
VBS UVLO
VCCUVLO
VB
HO
VS
VCC
LO
COM

最大额定值

无特别说明情况下，COM 为参考地，T_A=25℃

项目	符号	最小值	最大值	单位
高端自举电源电压	V_B	-0.3	625	V
高端悬浮输出端电压	V_S	V_B-25	V_B+0.3	V
高端驱动输出电压	V_{HO}	V_S-0.3	V_B+0.3	V
低端电源电压	V_{CC}	-0.3	25	V
逻辑电源电压	V_{DD}	-0.3	V_{SS}+20	V
逻辑地	V_{SS}	V_{CC}-20	V_{CC}+0.3	V
低端驱动输出电压	V_{LO}	-0.3	V_{CC}+0.3	V
逻辑输入电压（HIN，LIN&SD）	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
V_S允许的电压变化斜率	dVs/dt	-	50	V/ns
最大功耗@T_A≤+25℃	P_D	-	1.25	W
PN 结到环境的热阻	θ_{JA}	-	100	℃/W
结温	T_J	-	150	℃
储存温度	T_S	-55	150	℃
焊接温度(焊接，10 秒)	T_L	-	300	℃

注：超最大额定值应用可能会对器件造成永久性损伤。

推荐工作条件

参数说明	符号	最小值	最大值	单位
高端自举电源电压	V_B	V_S+10	V_S+20	V
高端悬浮输出端电压	V_S		600	V
高端驱动输出电压	V_{HO}	V_S	V_B	V
低端电源电压	V_{CC}	10	20	V
逻辑电源电压	V_{DD}	V_{SS}+3	V_{SS}+20	V
逻辑地	V_{SS}	-5	5	V
低端驱动输出电压	V_{LO}	0	V_{CC}	V
逻辑输入电压（HIN，LIN&SD）	V_{IN}	V_{SS}	V_{DD}	V
环境温度	T_A	-40	125	℃

注：输入/输出时序如图 1 所示。VS 和 VSS 偏移值在所有电源偏置在 15 V 的情况下测试。

电气参数

无特别说明情况下，V_{BIAS}（V_{CC}，V_{BS}，V_{DD}）=15 V，T_A=25° C。

参数说明	符号	测试条件	最小值	典型值	最大值	单位
V_{BS}静态电流 1	I_{QBS1}	V_{IN}=0V		35	60	uA
V_{CC}静态电流 1	I_{QCC1}			130	250	uA
V_{DD}静态电流 1	I_{QDD1}			0.1	1	uA
V_{BS}静态电流 2	I_{QBS2}	V_{IN}=V_{DD}		370	600	uA
V_{CC}静态电流 2	I_{QCC2}			450	800	uA
V_{DD}静态电流 2	I_{QDD2}			0.1	1	uA
偏置电源漏电流	I_{LK}	V_B=V_S=600V			50	uA
逻辑“1”输入偏置电流	I_{IN+}	V_{IN}=15V		25	50	uA
逻辑“0”输入偏置电流	I_{IN-}	V_{IN}=0V		0	5	uA
逻辑“1”输入电平	V_{IH}	V_{DD}=15V	10.0		—	V
逻辑“0”输入电平	V_{IL}		—		5.0	V
高电平输出电压，V_{BIAS}-V_O	V_{OH}	I_O=2mA	—		0.2	V
低电平输出电压，V_O	V_{OL}		—		0.15	V
高端欠压保护正阈值	V_{BSUV+}		7.5	8.6	9.7	V
高端欠压保护负阈值	V_{BSUV-}		7.0	7.9	9.2	V
低端欠压保护正阈值	V_{CCUV+}		7.5	8.6	9.7	V
低端欠压保护负阈值	V_{CCUV-}		7.0	7.9	9.2	V
输出高短路电流	I_{O+}	V_O=0V, VIN=Logic “1”, PW≤10us	—	2.0	—	A
输出低短路电流	I_{O-}	V_O=15V, VIN=Logic “0”, PW≤10us	—	2.0	—	A
开启传递延时	t_{on}	C_L=1000 pF, V_S=0V	—	140	200	ns
关闭传递延时	t_{off}	C_L=1000 pF, V_S=0V	—	140	200	ns
SD 关闭延时	t_{sd}	C_L=1000 pF, V_S=0V	—	130	180	ns
开启上升延时	t_r	C_L=1000 pF	—	10	35	ns
关闭下降延时	t_f	C_L=1000 pF	—	10	35	ns
延时匹配	MT		—	—	10	ns

特性曲线

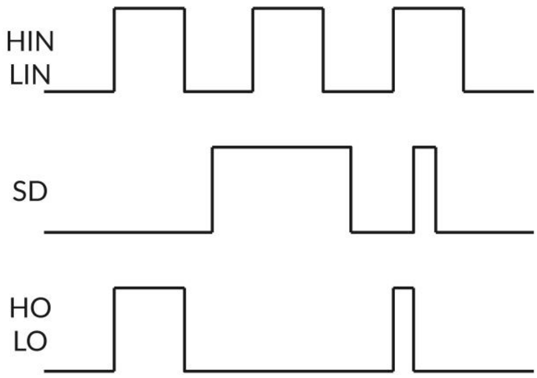


图 1. 输入/输出时序图

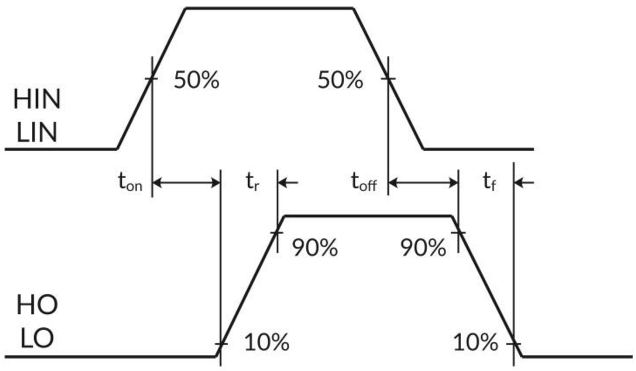


图 2. 信号传递时序图

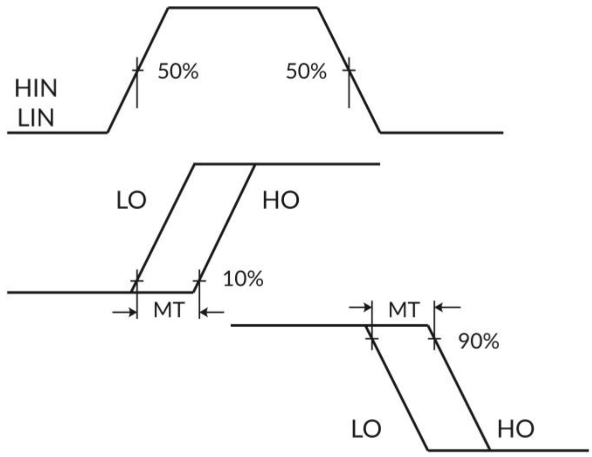


图 3.延迟匹配波形图

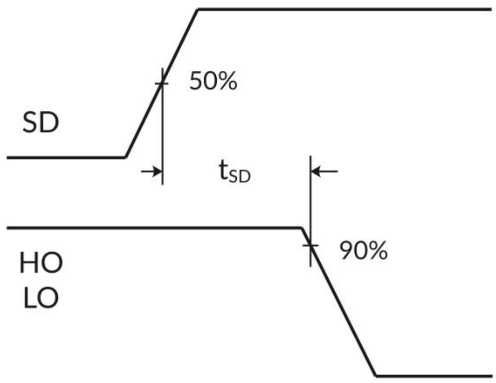


图 4. SD 关闭延时波形图

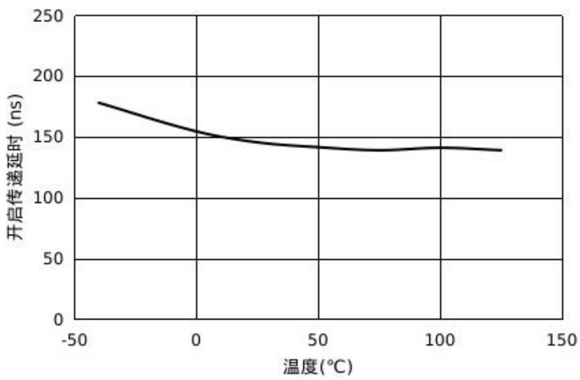


图 5.开启传递延时 vs. 温度

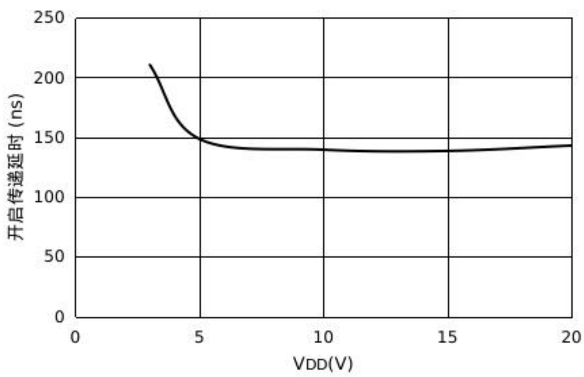


图 6.开启传递延时 vs. V_{DD}

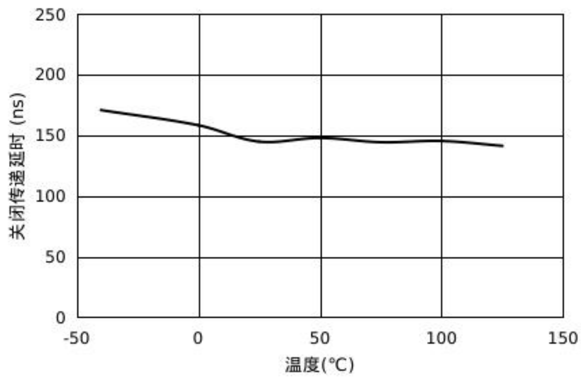


图 7.关闭传递延时 vs. 温度

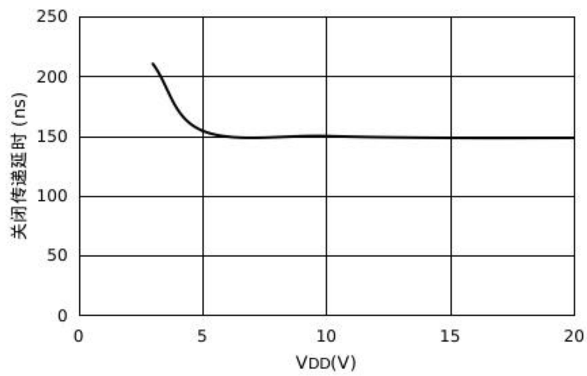


图 8.关闭传递延时 vs. V_{DD}

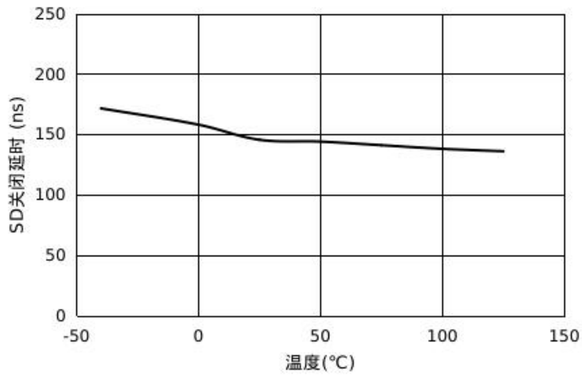


图 9.SD 关闭延时 vs. 温度

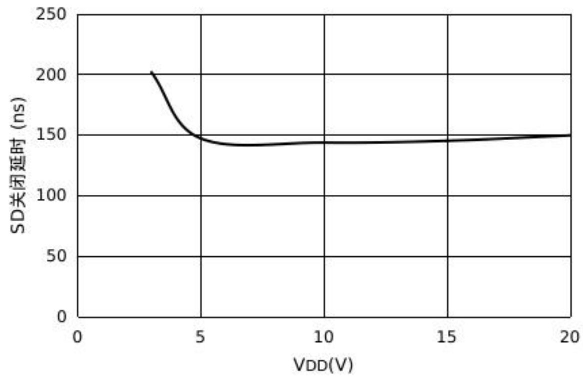


图 10.SD 关闭延时 vs. V_{DD}

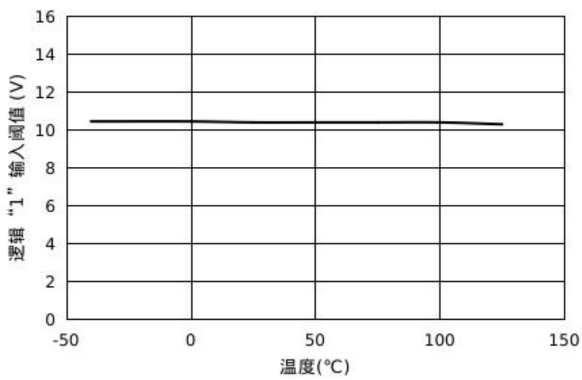


图 11.逻辑“1”输入阈值 vs. 温度

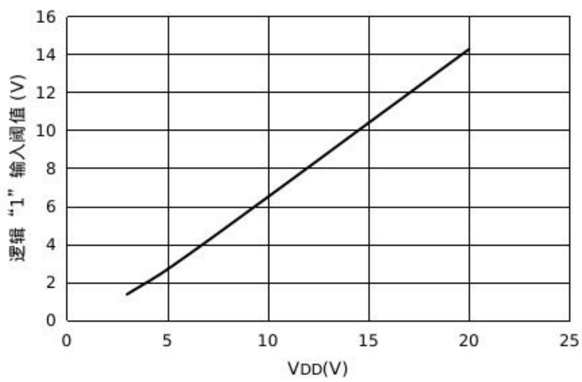


图 12.逻辑“1”输入阈值 vs. V_{DD}

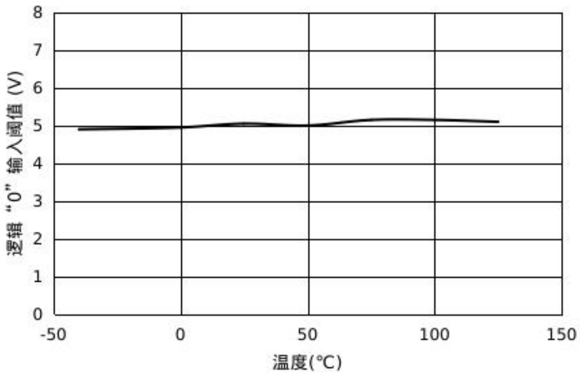


图 13. 逻辑“0”输入阈值 vs. 温度

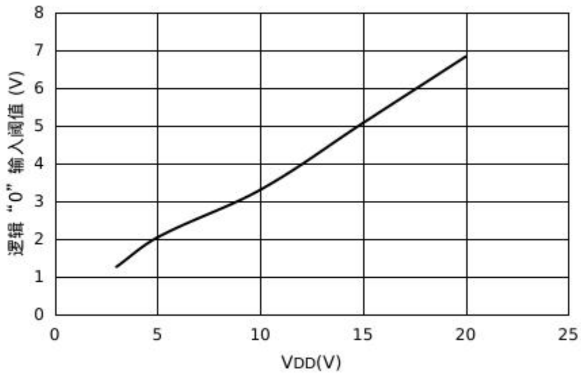


图 14.逻辑“0”输入阈值 vs. V_{DD}

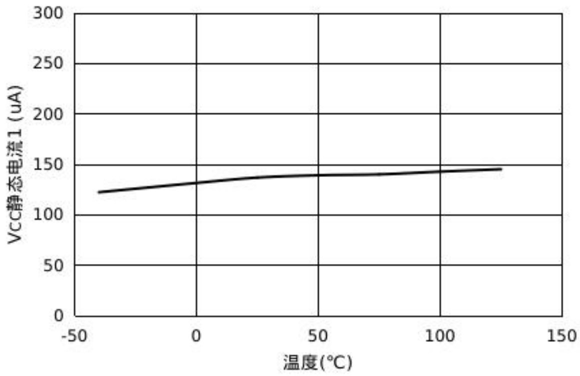


图 15. V_{CC}静态电流 1 vs. 温度

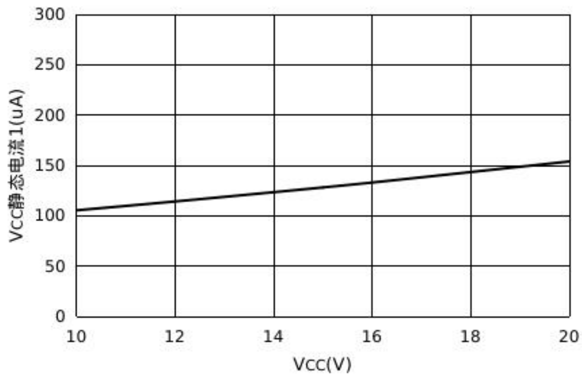


图 16.V_{CC}静态电流 1 vs. V_{CC}

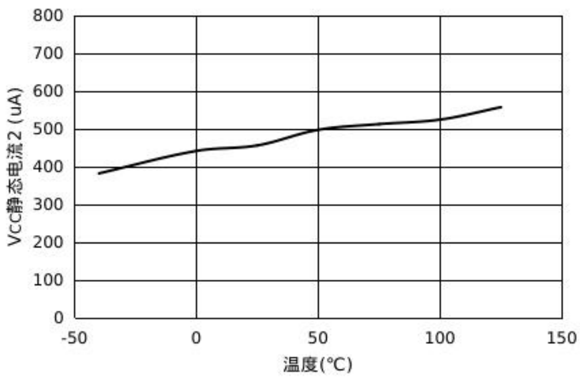


图 17. V_{CC}静态电流 2 vs. 温度

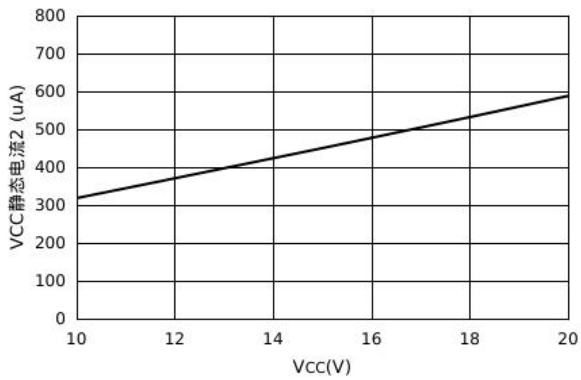


图 18.V_{CC}静态电流 2 vs. V_{CC}

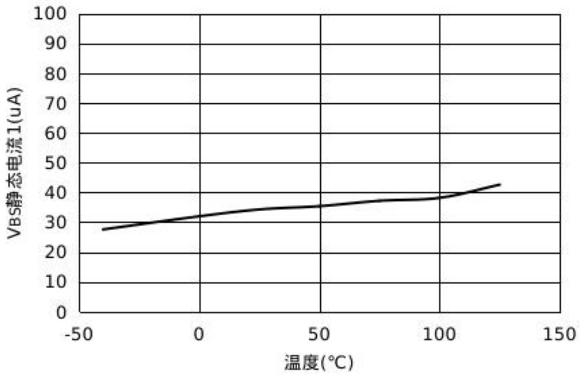


图 19. V_{BS}静态电流 1 vs. 温度

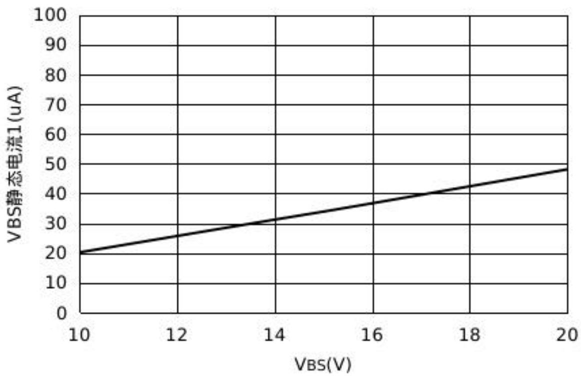


图 20. V_{BS}静态电流 1 vs. V_{BS}

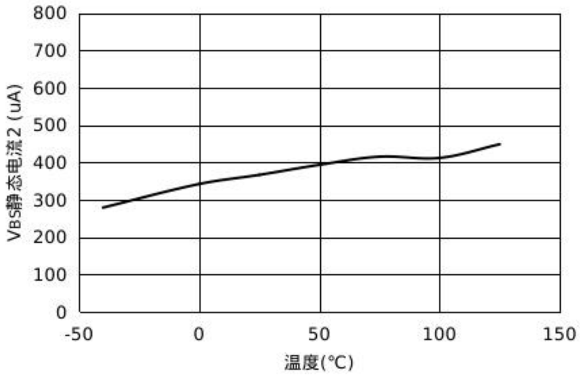


图 21. V_{BS}静态电流 2 vs. 温度

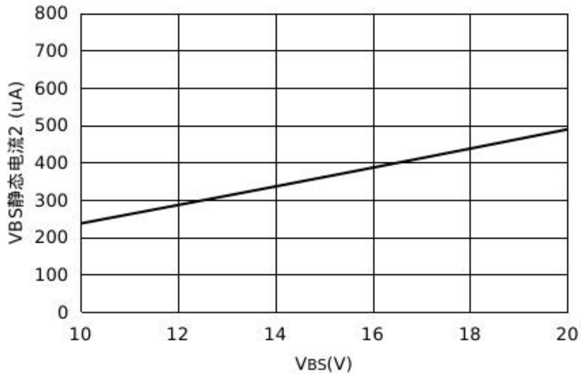


图 22. V_{BS}静态电流 2 vs. V_{BS}

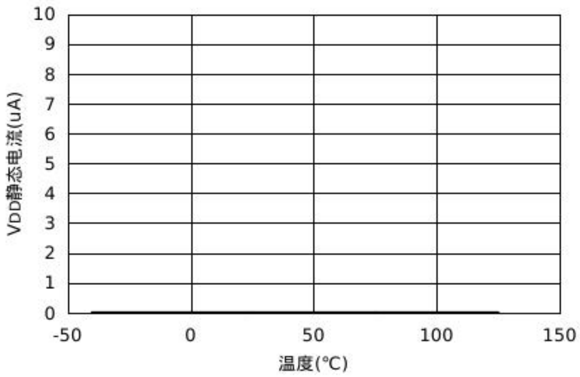


图 23. V_{DD}静态电流 vs. 温度

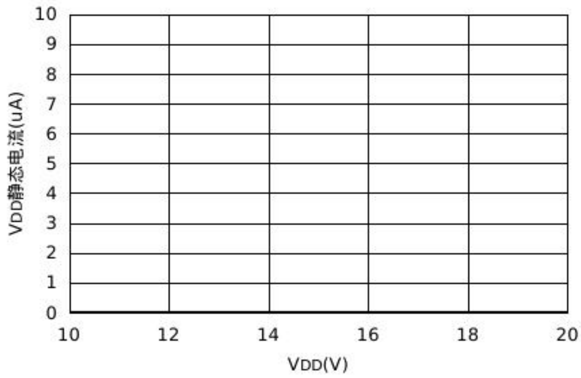


图 24. V_{DD}静态电流 vs. V_{DD}

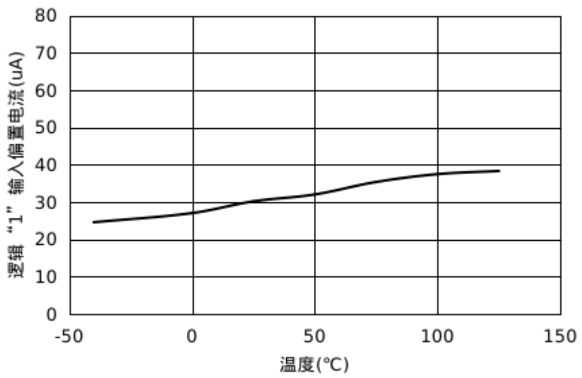


图 25. 逻辑“1”输入偏置电流 vs. 温度

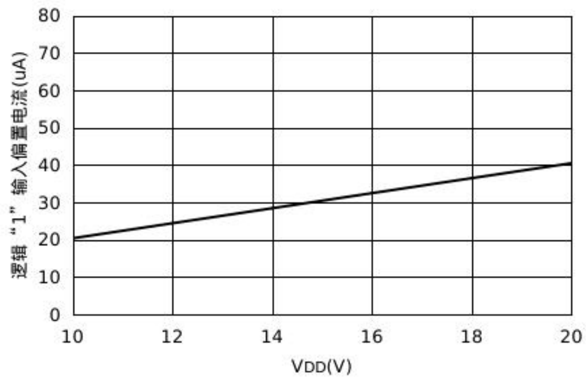


图 26. 逻辑“1”输入偏置电流 vs. V_{DD}

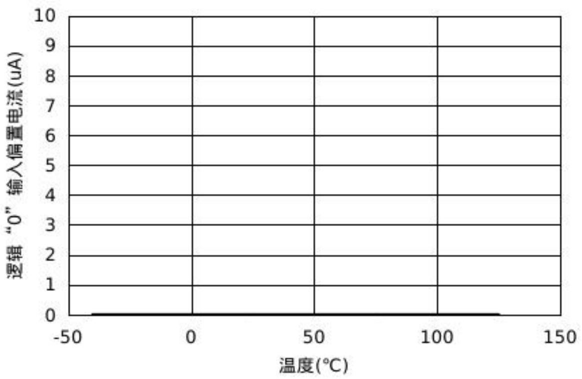


图 27. 逻辑“0”输入偏置电流 vs. 温度

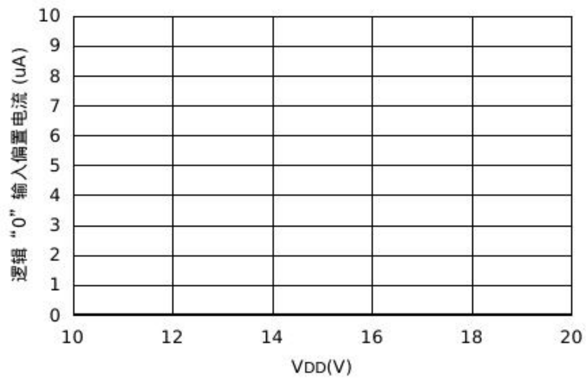


图 28. 逻辑“0”输入偏置电流 vs. V_{DD}

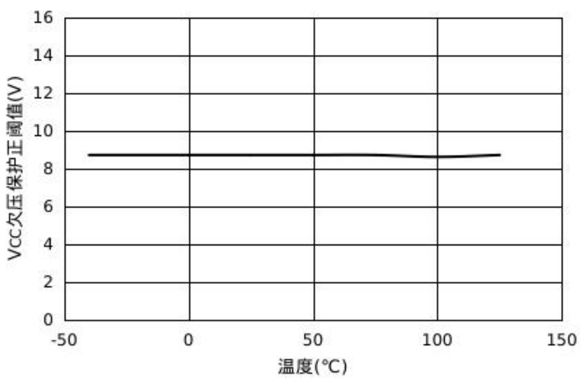


图 29. V_{CC}欠压保护正阈值 vs. 温度

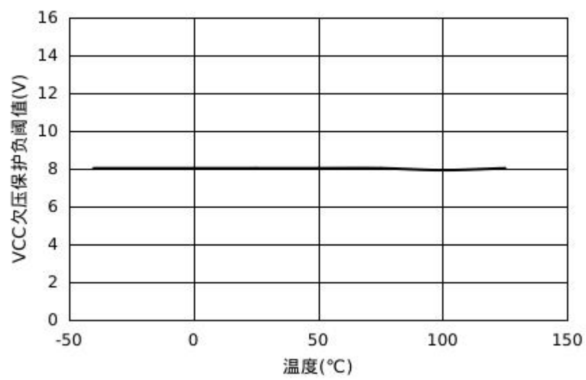


图 30. V_{CC}欠压保护负阈值 vs. 温度

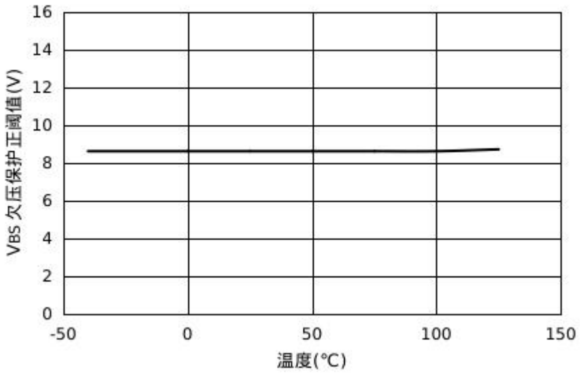


图 31. V_{BS}欠压保护正阈值 vs. 温度

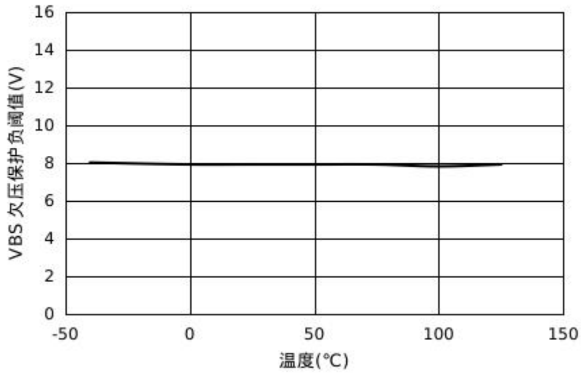
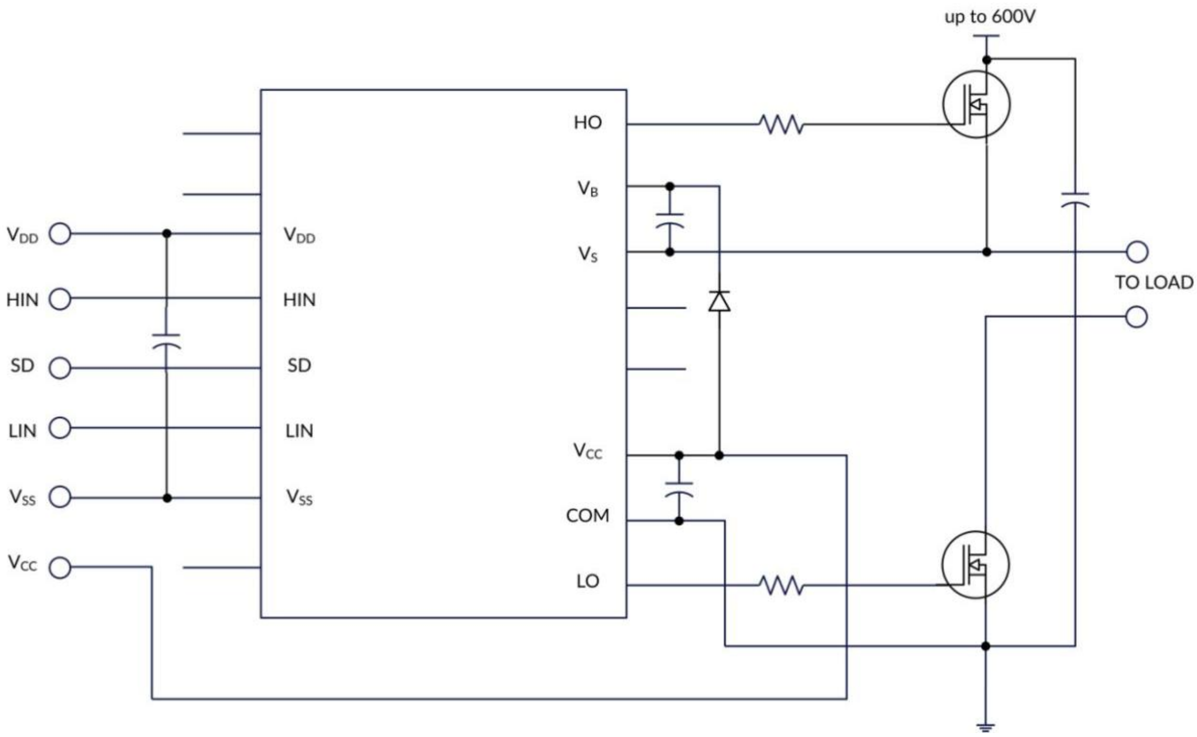


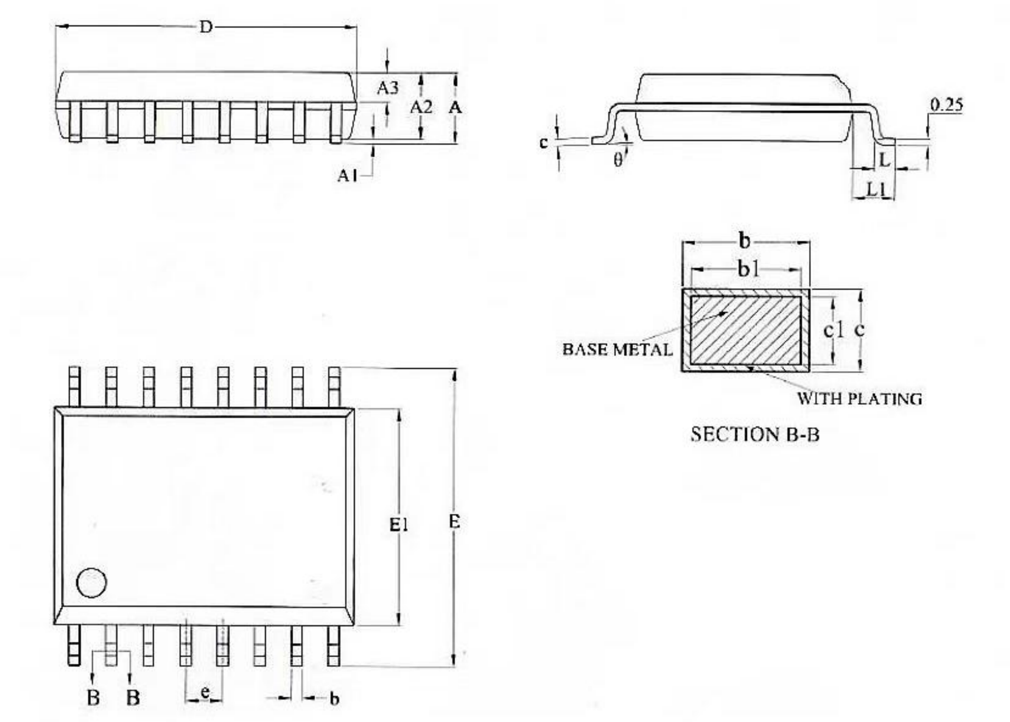
图 32. V_{BS}欠压保护负阈值 vs. 温度

应用电路



封装外形图和尺寸

SOP-16



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.270(BSC)		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specificationsof any andall MSKSEMI Semiconductor products described orcontained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer'sproducts orequipment.

■ MSKSEMI Semiconductor. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with someprobability. It is possiblethat these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits anderror prevention circuitsfor safedesign, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from theauthorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringementsof intellectual property rights or other rightsof third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. Whendesigning equipment, referto the "Delivery Specification" for the MSKSEMI Semiconductor productthat you intend to use.