H4423P

30V P-CHANNEL MOSFET

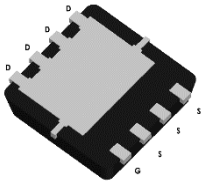
Product Summary

VDS	RDS(ON) max	ID max
−30V	<7.4mΩ @ VGS = -10V	-34A
	<10.6mΩ @ VGS = -4.5V	

Description and Applications

- Trench Power MOSFET technology
- Low RDSON
- RoHS and Halogen-Free Complaint
- Notebook AC-in Load Switch
- Battery Protection Charge/Discharge
- 100% UIS Tested
- 100% Rg Tested

View and Internal Schematic Diagram



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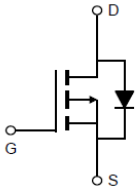


Internal Schematic

Maximum Ratings (@TA = +25°C unless otherwise specified.)

Parameters		Symbol	Max	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current G	T_C= +25°C T_C = +100°C	I_D	-34 -32	A
Pulsed Drain Current C		I_{DM}	200	A
Avalanche Current C		I_{AS}	-41	A
Avalanche Energy C	L=0.1mH	E_{AS}	84	mJ
Power Dissipation B	T_C = +25°C T_C= +100°C	P_D	30 12	W
Operating and Storage Temperature Range		T_J, T_G	-55 to+150	°C

Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	20	25	°C/W
Maximum Junction-to-Ambient A D	Steady-State		45	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.5	4.2	°C/W

Electrical Characteristics (@TA = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=VGS I_D=-250μA	-1.1	-1.58	-2.1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-20A		6	7.4	mΩ
		T_J=125℃		9.1	11.3	
		V_{GS}=-4.5V, I_D=-16A		8.6	10.6	mΩ
g_{FS}	Forward Trans conductance	V_{DS}=-5V, I_D=-20A		70		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-34	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		3406		pF
C_{oss}	Output Capacitance			369		pF
C_{rss}	Reverse Transfer Capacitance			306		pF
R_g	Gate resistance	f=1MHz	1	4.6	9	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-20A		69.8		nC
Q_{gs}	Gate Source Charge			13.6		nC
Q_{gd}	Gate Drain Charge			14		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-15V, R_L=0.75Ω, R_{GEN}=3Ω		11.3		ns
t_r	Turn-On Rise Time			71.3		ns
$t_{D(off)}$	Turn-Off Delay Time			95		ns
t_f	Turn-Off Fall Time			82		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=100A/μs		15.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=100A/μs		1.6		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with TA=25℃

G. The maximum current rating is package limited

TYPICAL ELECTRICAL AND THERMAL CHARACTERIS

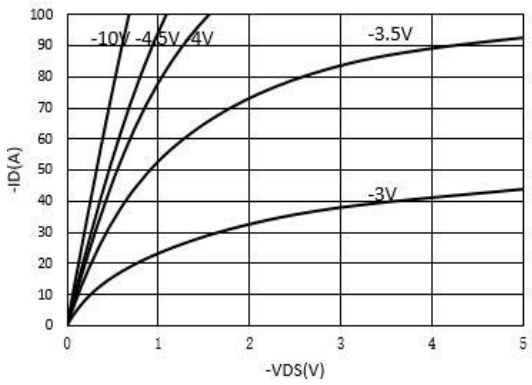


Figure 1：On-Region Characteristics (Note E)

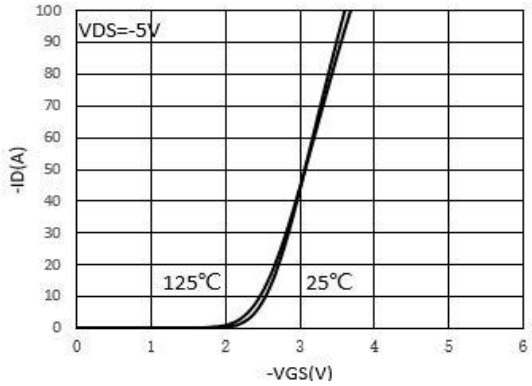


Figure 2 Transfer Characteristics (Note E)

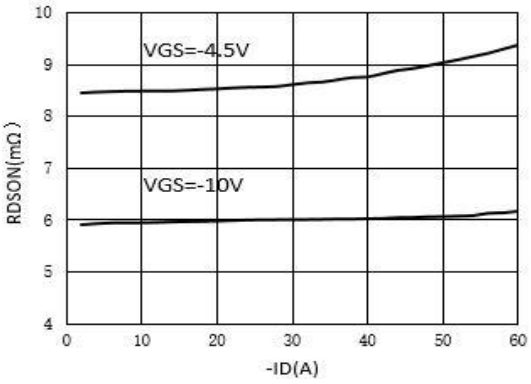


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

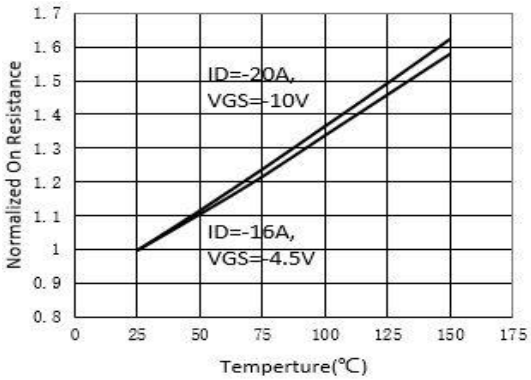


Figure 4: On-Resistance vs. Junction Temperature (Note E)

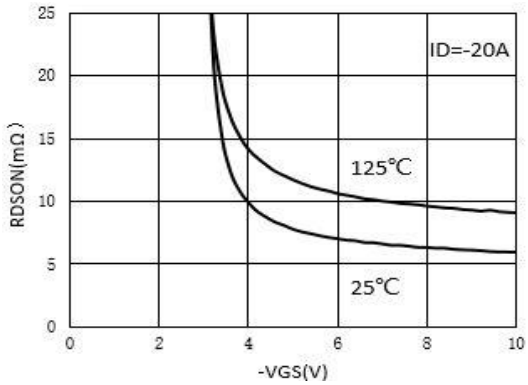


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

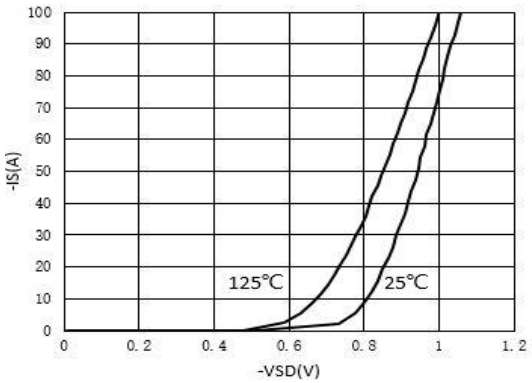


Figure 6: Body-Diode Characteristics (Note E)

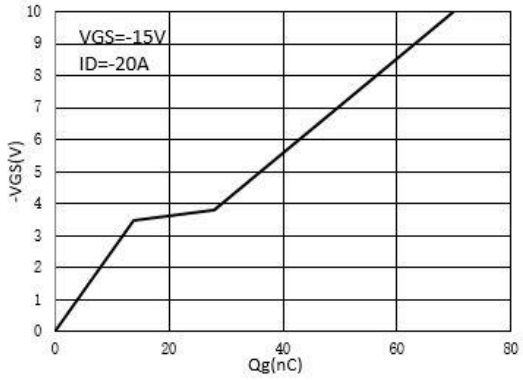


Figure 7: Gate-Charge Characteristics

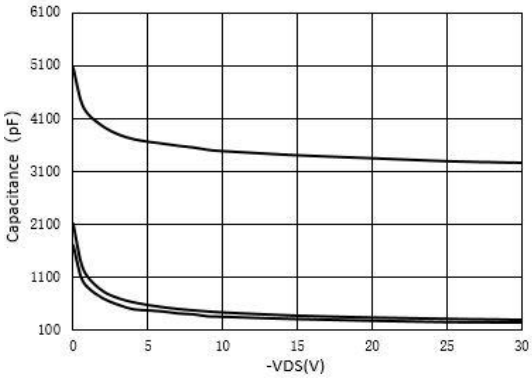


Figure 8: Capacitance Characteristics

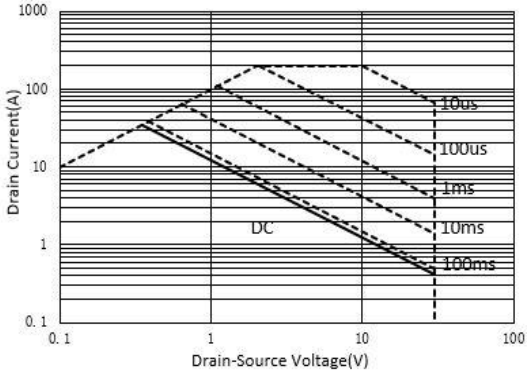


Figure 9: Maximum Forward Biased Safe Operating Area

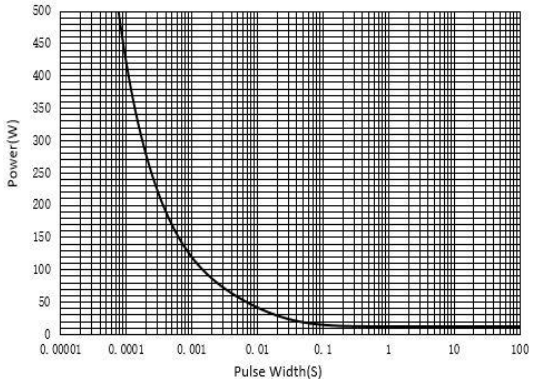


Figure 10: Single Pulse Power Rating Junction-to-Case

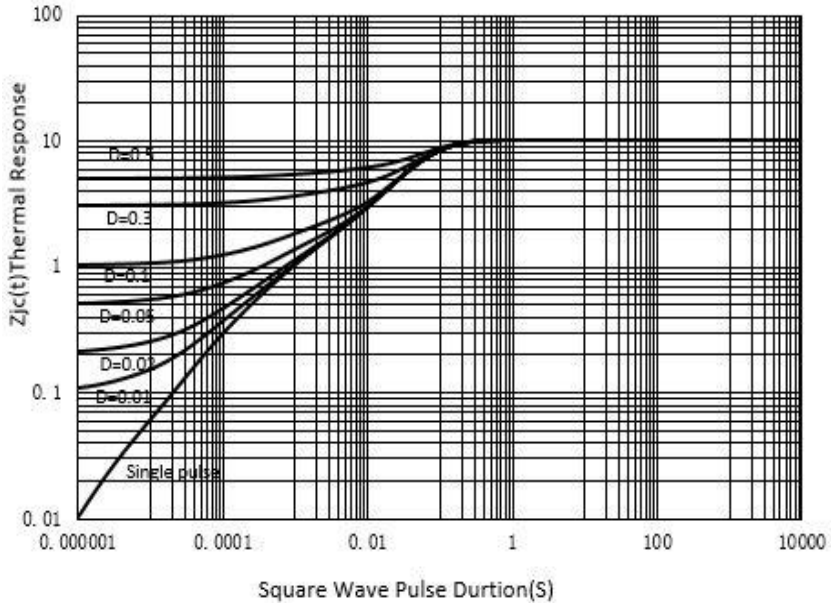
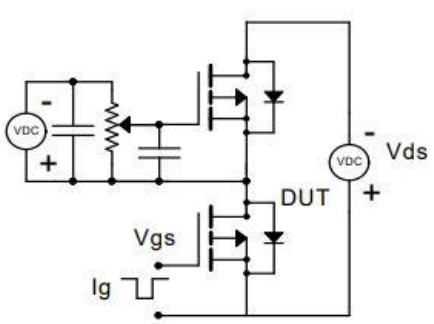
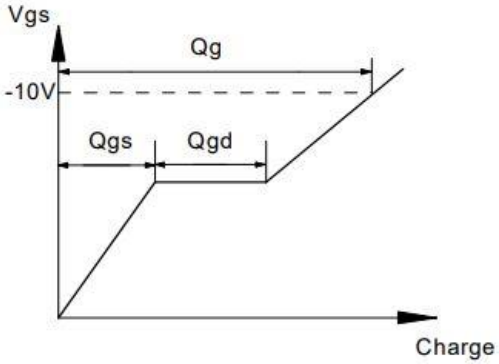


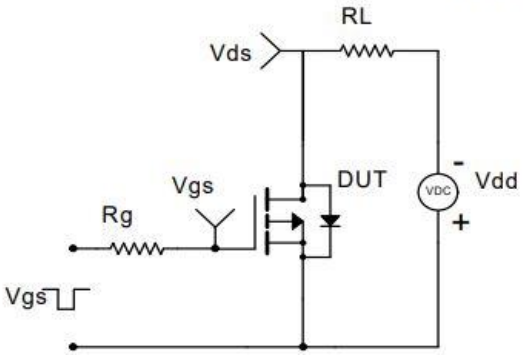
Figure 11: Normalized Maximum Transient Thermal Impedance

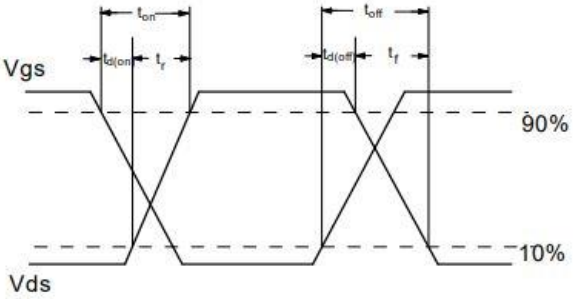
Gate Charge Test Circuit & Waveform



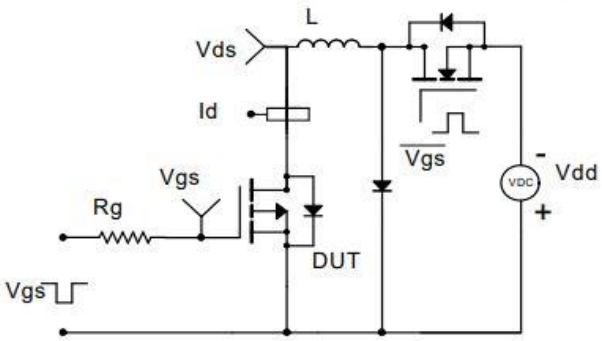


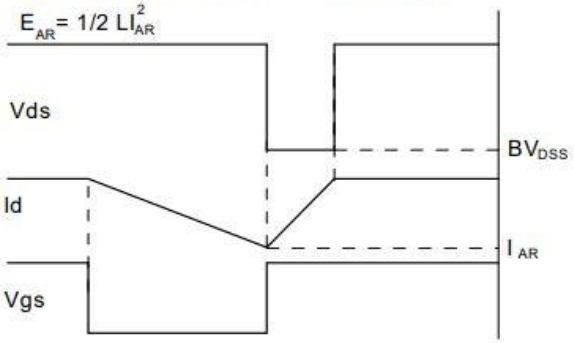
Resistive Switching Test Circuit & Waveforms



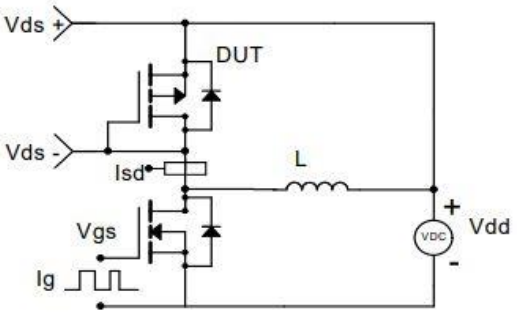


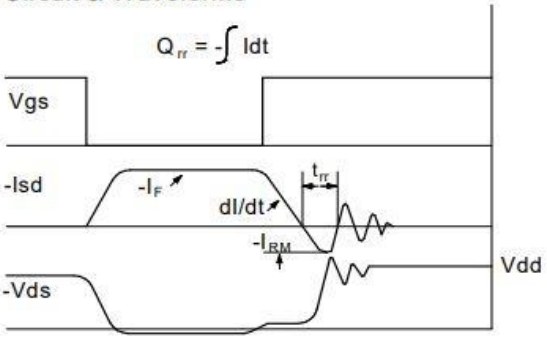
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



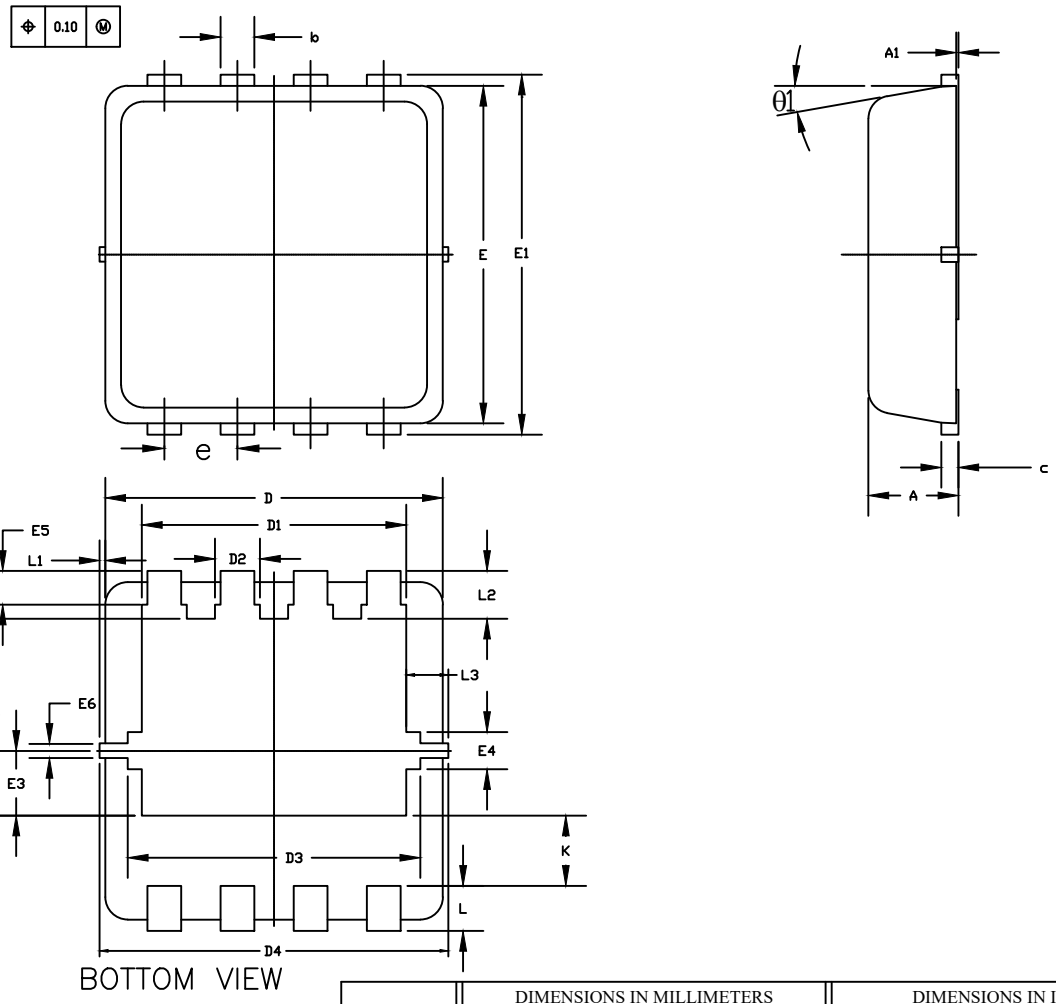


Diode Recovery Test Circuit & Waveforms

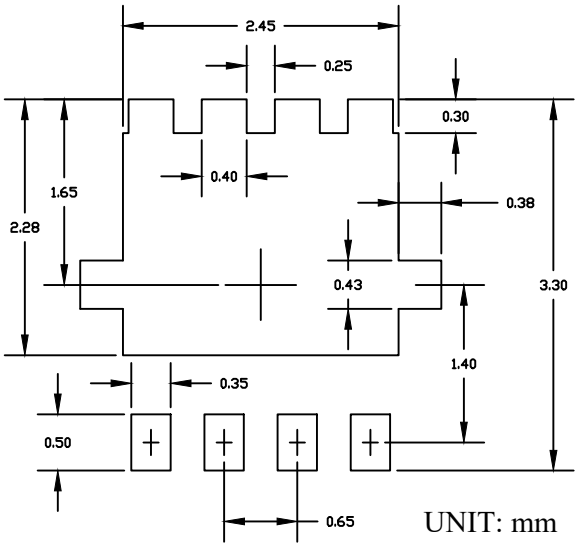




DFN3x3EP PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0. 70	0. 80	0. 90	0. 028	0. 031	0. 035
A1	0. 00	0.025	0. 05	0. 000	0.001	0. 002
b	0. 24	0. 30	0. 35	0. 009	0. 012	0. 014
c	0. 10	0. 15	0. 25	0. 004	0. 006	0. 010
D	2. 90	3. 00	3. 10	0. 114	0. 118	0. 122
D1	2. 25	2. 35	2. 45	0. 089	0. 093	0. 097
D2	0. 30	0. 40	0. 50	0. 012	0. 016	0. 020
D3	2. 50	2. 60	2. 70	0. 098	0. 102	0. 106
D4	3. 00	3. 10	3. 20	0. 118	0. 122	0. 126
E	2. 90	3. 00	3. 10	0. 114	0. 118	0. 122
E1	3. 10	3. 20	3. 30	0. 122	0. 126	0. 130
E2	1. 65	1. 75	1. 85	0. 065	0. 069	0. 073
E3	0. 48	0. 58	0. 68	0. 019	0. 023	0. 027
E4	0. 23	0. 33	0. 43	0. 009	0. 013	0. 017
E5	0. 20	0. 30	0. 40	0. 008	0. 012	0. 016
E6	0. 075	0. 125	0. 175	0. 003	0. 005	0. 007
e	0. 60	0. 65	0. 70	0. 024	0. 026	0. 028
K	0. 52	0. 62	0. 72	0. 020	0. 024	0. 028
L	0. 30	0. 40	0. 50	0. 012	0. 016	0. 020
L1	0	0. 05	0. 10	0	0. 002	0. 004
L2	0. 33	0. 43	0. 53	0. 013	0. 017	0. 021
L3	0. 275	0. 375	0. 475	0. 011	0. 015	0. 019
θ1	0°	10°	12°	0°	10°	12°

NOTE
1. PACKAGE DIMENSION IS EXCLUSIVE OF MOLD GATE BURR
2. PACKAGE DIMENSION IS EXCLUSIVE OF MOLD FLASH AND CUTTING BURR
3. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.