

BMB65N100UC1

Super Junction Power MOSFET

650 V, 35 A, 100 mΩ



Description

BMB65N100UC1 is power MOSFET using bestirpower's advanced super junction technology that can realize very low on resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

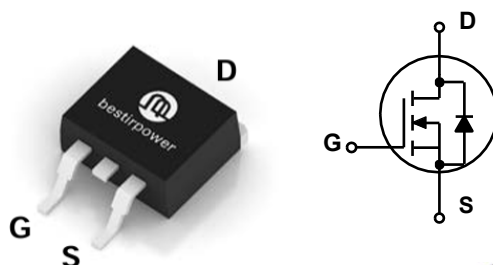
Applications

- AC/DC power supply.
- PC power.
- Telecom/Sever.
- Solar inverter.

Features

$BV_{DSS} @ T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,type}$
700 V	35 A	100 mΩ	66 nC

- Ultra-fast body diode.
- Extremely low losses due to very low FOM $R_{dson} \cdot Q_g$ and E_{oss} .
- Very high commutation ruggedness.



Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value max	Unit
V_{DSS}	Drain to Source Voltage(1)		650	V
V_{GSS}	Gate to Source Voltage		± 30	V
I_D	Drain Current(2)	$V_{GS} = 10 \text{ V}, (T_C = 25^\circ\text{C})$	35	A
		$V_{GS} = 10 \text{ V}, (T_C = 100^\circ\text{C})$	22	
I_{DM}	Drain Current	Pulsed	105	A
E_{AS}	Single Pulsed Avalanche Energy(3)		750	mJ
dv/dt	MOSFET dv/dt ruggedness		50	V/ns
	Peak Diode Recovery dv/dt		50	
P_D	Power Dissipation	$(T_C = 25^\circ\text{C})$	278	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	$^\circ\text{C}$
I_S	Continuous diode forward current		35	A
$I_{S \text{ Pulse}}$	Diode pulse current(2)		105	A

1) Limited by T_J max. Maximum duty cycle $D=0.75$.

2) Pulse width t_p limited by T_J max.

3) $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62	
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	260	$^\circ\text{C}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	3.0	4.0	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}, T_J = 25^\circ\text{C}$	-	82	100	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 250\text{ KHz}$	-	2990	-	pF
C_{oss}	Output Capacitance		-	141	-	pF
C_{rss}	Reverse transfer capacitance		-	5.8	-	pF
$C_{o(tr)}$	Time Related Output Capacitance ²⁾	$V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$	-	452	-	pF
$C_{o(er)}$	Energy Related Output Capacitance ¹⁾		-	88	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DD} = 400\text{ V}, I_D = 18\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$	-	66	-	nC
Q_{gs}	Gate to Source Charge		-	20	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	25	-	nC
$V_{plateau}$	Gate plateau voltage		-	6.1	-	V
R_G	Gate Resistance	$f = 1\text{ MHz open drain}$	-	2.7	-	Ω
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 18\text{ A}, V_{GS} = 10\text{ V},$	-	21	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	76	-	ns
t_f	Turn-Off Fall Time		-	8	-	ns

Source-Drain Diode Characteristics

V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_F = 18\text{ A}, T_J = 25^\circ\text{C}$	-	0.88	-	V
t_{rr}	Reverse Recovery Time	$V_R = 400\text{ V}, I_F = 18\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	140	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.15	-	μC
I_{mm}	Peak reverse recovery current		-	15	-	A

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Typical Performance Characteristics

Figure 1. Power dissipation

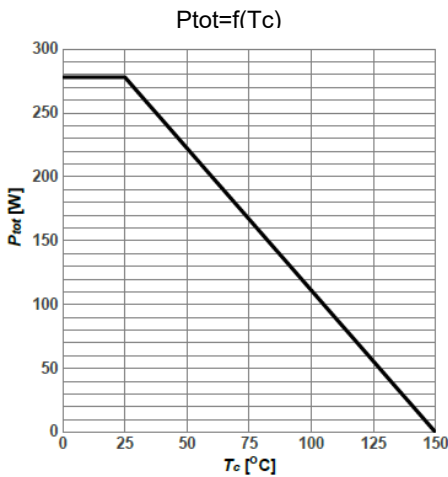


Figure 2: Max. transient thermal impedance

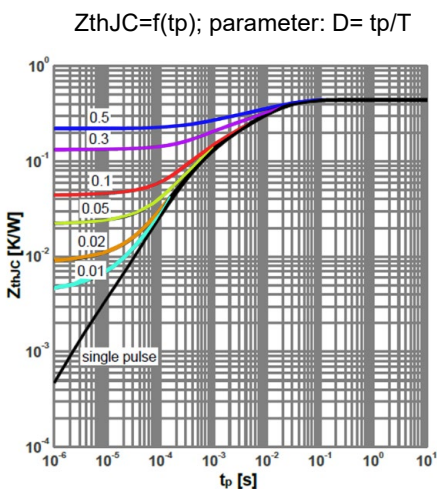


Figure 3: Safe operating area

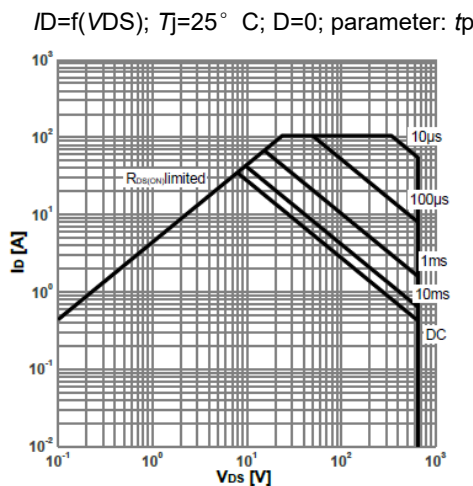


Figure 4: Typ. output characteristics

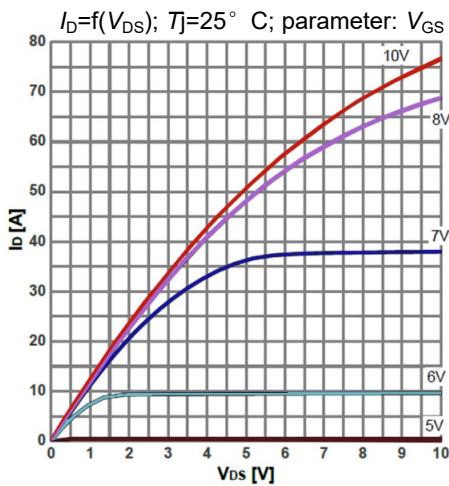


Figure 5: Typ. output characteristics

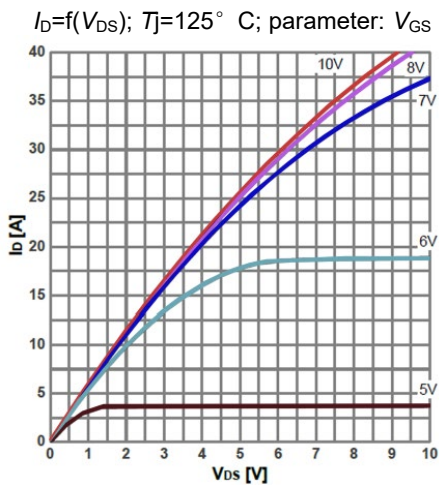
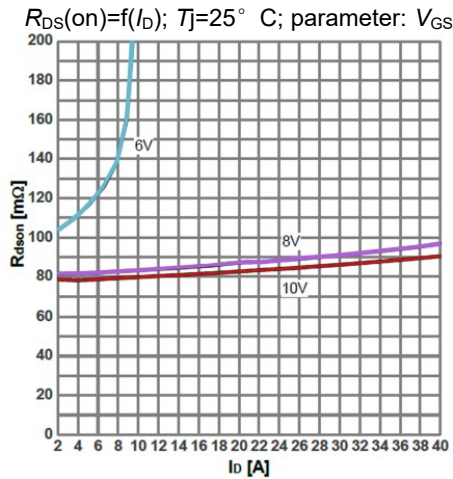


Figure 6: Typ. drain-source on-state resistance



Typical Performance Characteristics

Figure 7: Drain-source on-state resistance

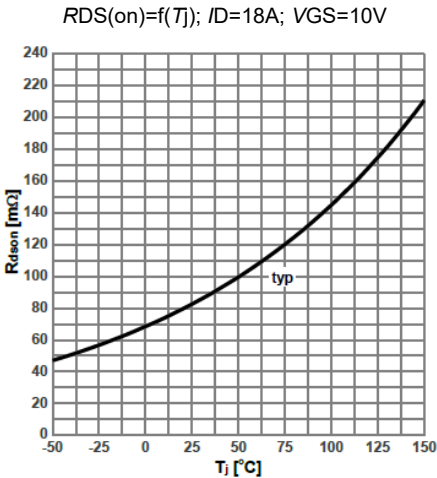


Figure 8: Typ. transfer characteristics

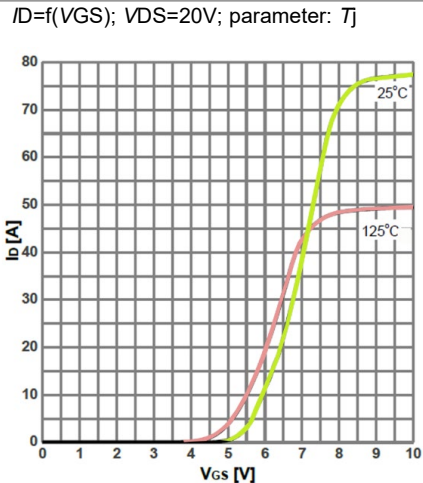


Figure 9: Typ. gate charge

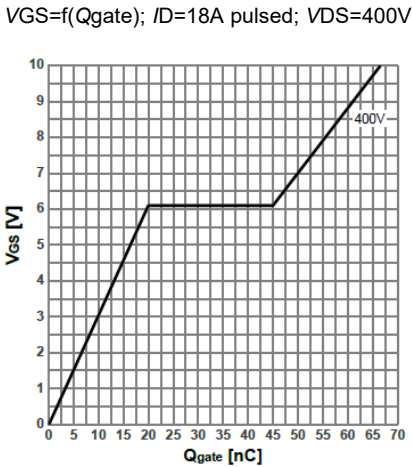


Figure 10: Forward characteristics of reverse diode

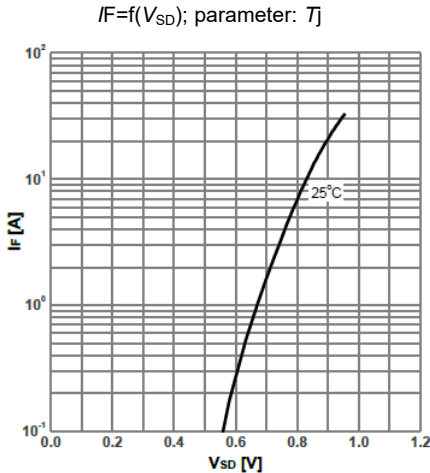


Figure 11: Drain-source breakdown voltage

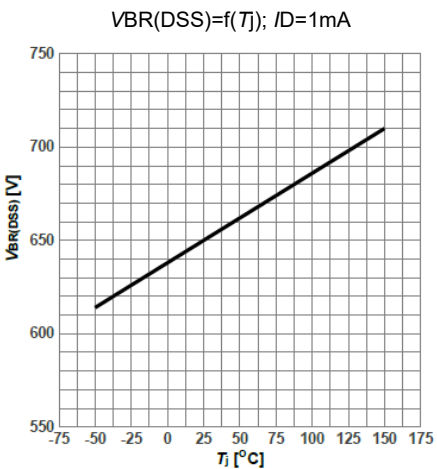
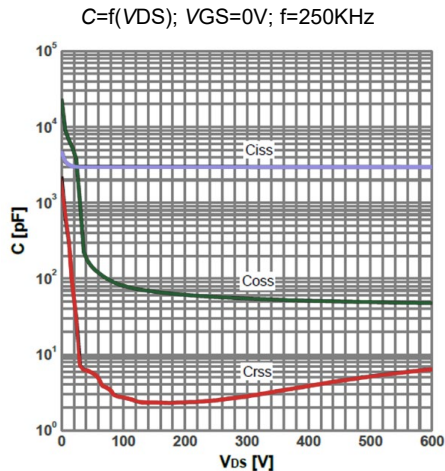


Figure 12: Typ. capacitances



Typical Performance Characteristics

Figure 13: Typ. Coss stored energy

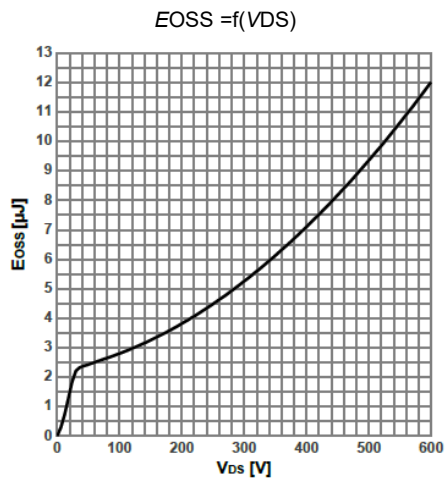
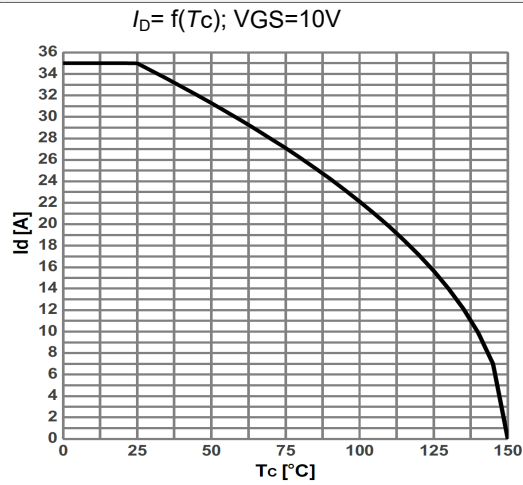


Figure 14: Max. Drain Current



Test Circuits

Figure 15. Diode Characteristics

Test circuit for diode characteristics and Diode recovery waveform

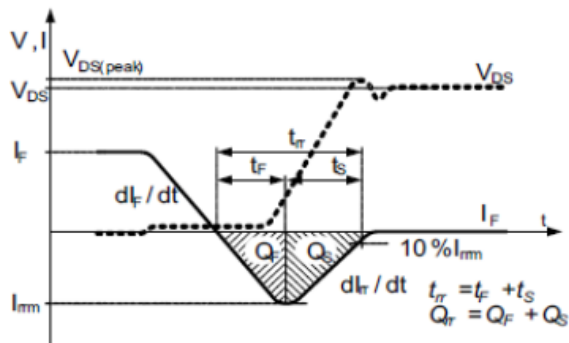
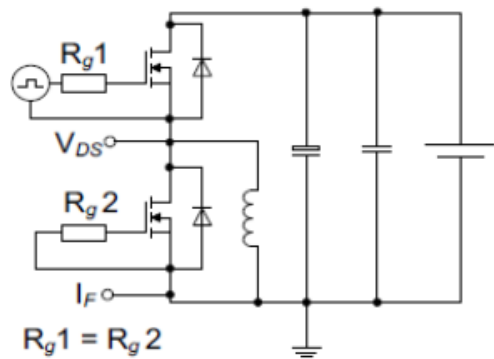


Figure 16. Switching Times

Switching times test circuit for inductive load and Switching times waveform

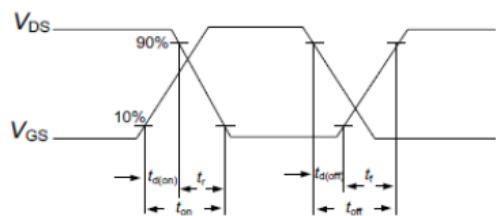
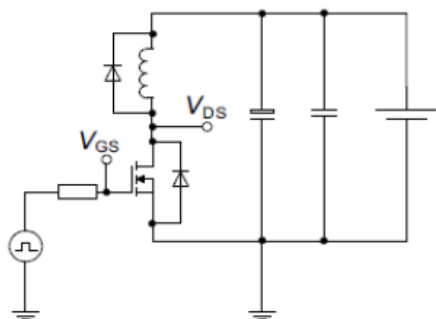
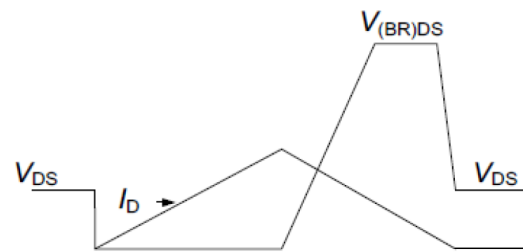
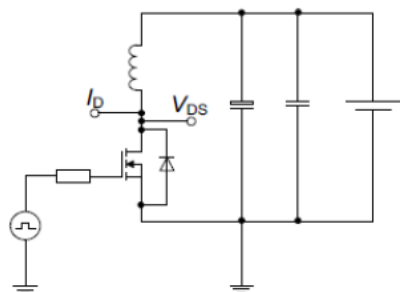


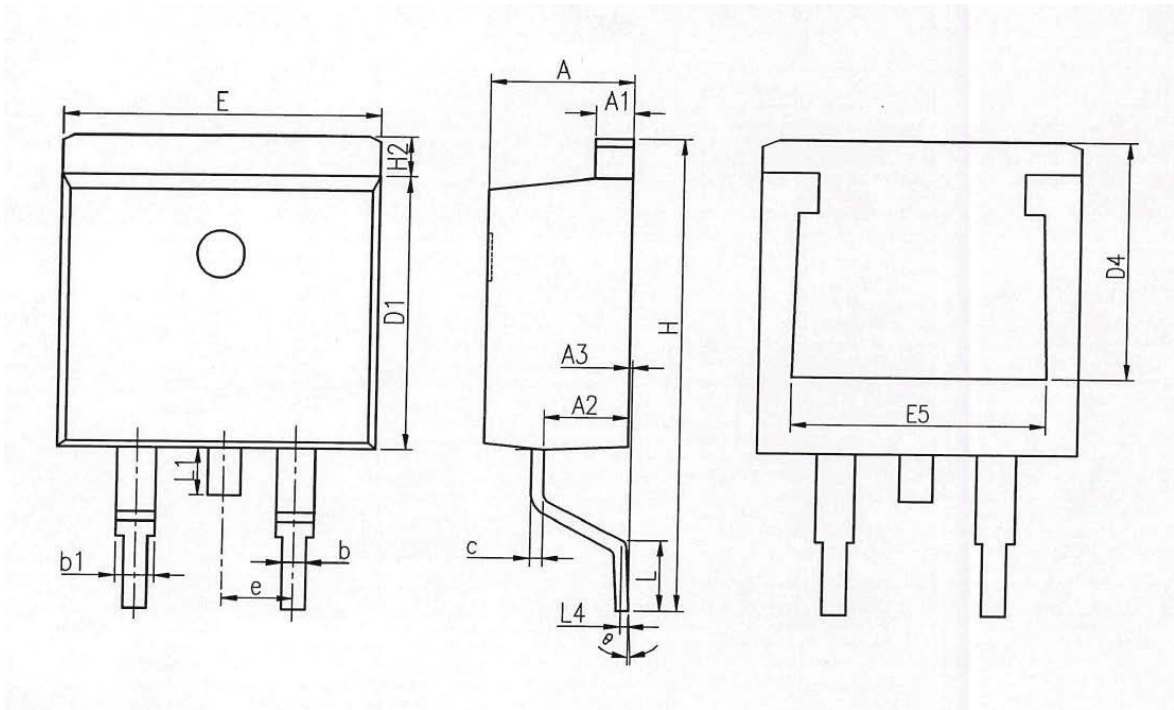
Figure 17 Unclamped Inductive Load

Unclamped inductive load test circuit and Unclamped inductive waveform



Package Outlines

D²PAK



COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
A3	0.00	0.13	0.25
b	0.70	0.81	0.96
b1	1.17	1.27	1.47
c	0.30	0.38	0.53
D1	8.50	8.70	8.90
D4	6.60	-	-
E	9.86	10.16	10.36
E5	7.06	-	-
e	2.54 BSC		
H	14.70	15.10	15.50
H2	1.07	1.27	1.47
L	2.00	2.30	2.60
L1	1.40	1.55	1.70
L4	0.25 BSC		
θ	0°	5°	9°

* Dimensions in millimeters

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
BMB65N100UC1	BMB65N100UC1	TO-263(D ² PAK)	Tape & Reel	800 units

Disclaimer

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