

MDDG04R01L

40V N-Channel Enhancement Mode MOSFET

1. Description

This N-Channel MV MOSFET is produced using MDD Semiconductor's advanced Power Trench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

2. Features

- Max $R_{DS(on)}$ = 0.85 m Ω at V_{GS} = 10 V, I_D = 75 A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIS Tested
- 100% dVDS Tested

3. Application

- PWM Application
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter
- Battery management System

4. Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

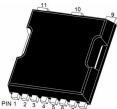
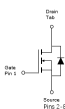
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	320	A
Pulsed Drain Current (Note 2)	I_{DM}	1280	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	576	mJ
Thermal Resistance (min. footprint)	$R_{\theta JA}$	91	$^{\circ}\text{C}/\text{W}$
Power Dissipation	P_D	125	W
Junction Temperature	T_J	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	$-55 \sim +150$	$^{\circ}\text{C}$

Note: 1) Calculated continuous current based on maximum allowable junction temperature.

2) Repetitive rating, pulse width limited by max. junction temperature.

3) E_{AS} condition : $T_J=25^{\circ}\text{C}$, $V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=48\text{A}$.

5. Pinning information

Pin	Symbol	Description	Simplified outline	Equivalent Circuit	Marking	Package
1	G	Gate			MDD G04R01L	TOLL
9-11	D	Drain				
2-8	S	Source				

6. $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Condition	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		$V_{GS}=0V, I_D=250\mu A$	40	—	—	V
I _{SS}	Gate-Source Leakage Current	Forward	$V_{GS}=20V$	—	—	100	nA
		Reverse	$V_{GS}=-20V$	—	—	-100	nA
I _{DSS}	Drain-Source Leakage Current		$V_{DS}=40V, V_{GS}=0V$	—	—	1	μA
$V_{GS(TH)}$	Gate Threshold Voltage		$V_{DS}=V_{GS}, I_D=250\mu A$	1.1	1.65	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance		$V_{GS}=10V, I_D=75A$	—	0.6	0.85	m Ω
			$V_{GS}=4.5V, I_D=30A$	—	0.92	1.2	m Ω

7. Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C _{iss}	Input Capacitance	$V_{GS}=0V$	—	7300	—	pF
C _{oss}	Output Capacitance	$V_{DS}=20V$	—	3550	—	pF
C _{rss}	Reverse Transfer Capacitance	$f=1MHz$	—	145	—	pF
Q _g	Total Gate Charge	$V_{GS}=10V$	—	130	—	nC
Q _{gs}	Gate Source Charge	$V_{DS}=32V$	—	43	—	nC
Q _{gd}	Gate Drain Charge	$I_D=150A$	—	29	—	nC

8. Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t _{d(on)}	Turn on Delay Time	$V_{GS}=10V$ $V_{DD}=20V$ $I_D=100A$ $R_G=5\Omega$	—	19	—	ns
t _r	Turn on Rise Time		—	26	—	ns
t _{d(off)}	Turn Off Delay Time		—	85	—	ns
t _f	Turn Off Fall Time		—	45	—	ns

9. Source Drain Diode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{SD}	Drain-Source Diode Forward Voltage	$I_S=75A, V_{GS}=0V$	—	0.8	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	$I_F=10A$	—	141	—	ns
Q _{rr}	Body Diode Reverse Recovery Charge	$di/dt=100A/\mu s$	—	333	—	nC

10. Test Circuits And Waveforms

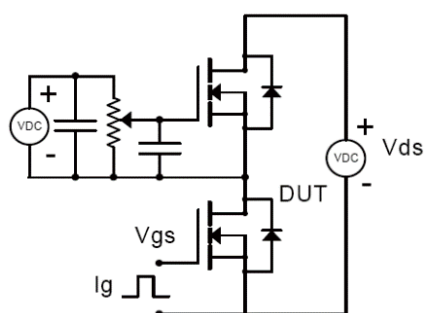


Figure 1. Gate charge test circuit & waveform

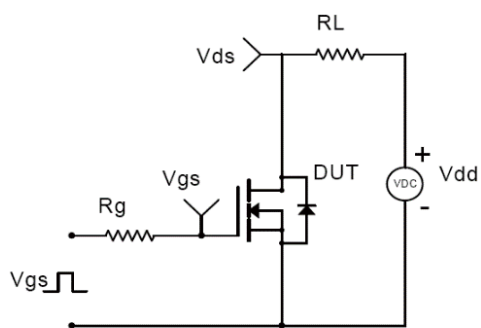
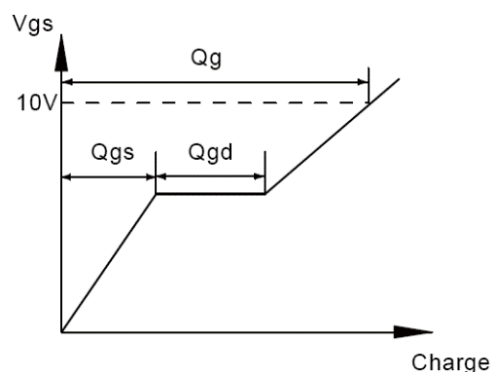


Figure 2. Switching time test circuit & waveforms

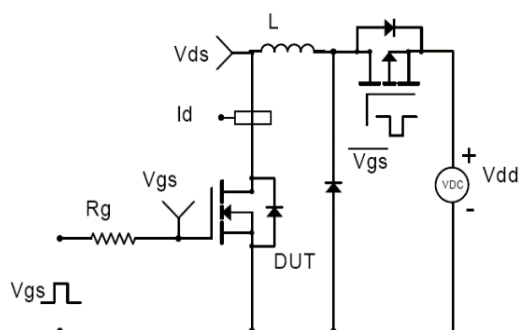
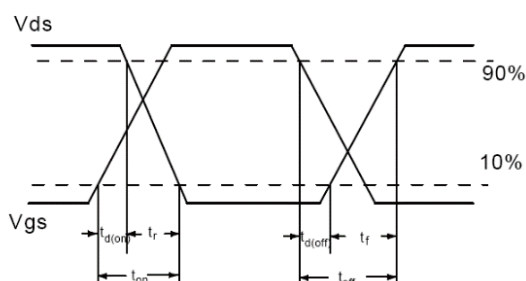


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

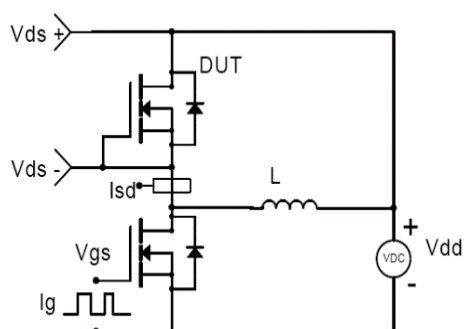
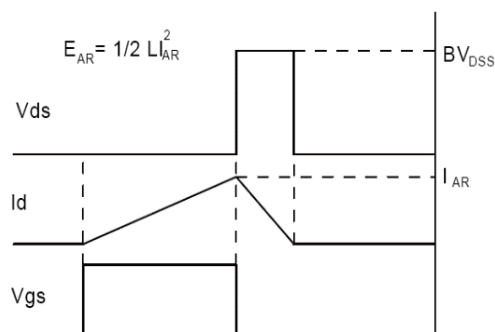
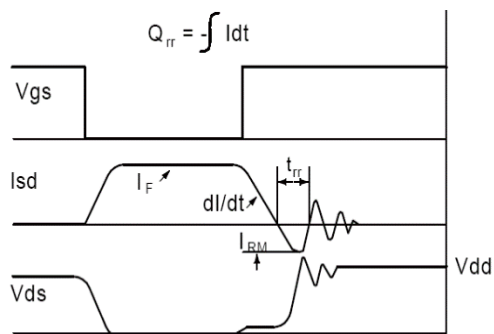


Figure 4. Diode reverse recovery test circuit & waveforms



II. Electrical Characteristics Diagrams

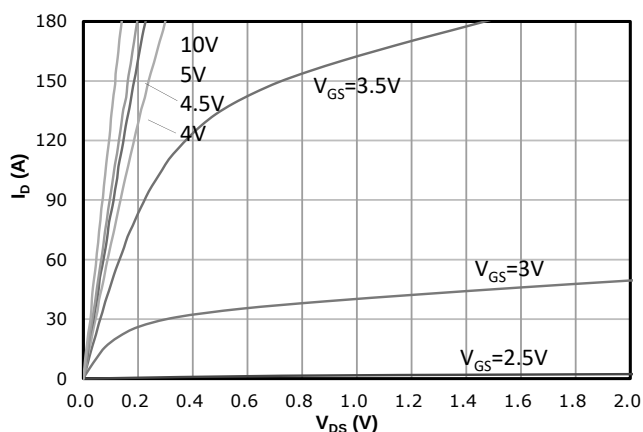


Figure 1. Typ. output characteristics

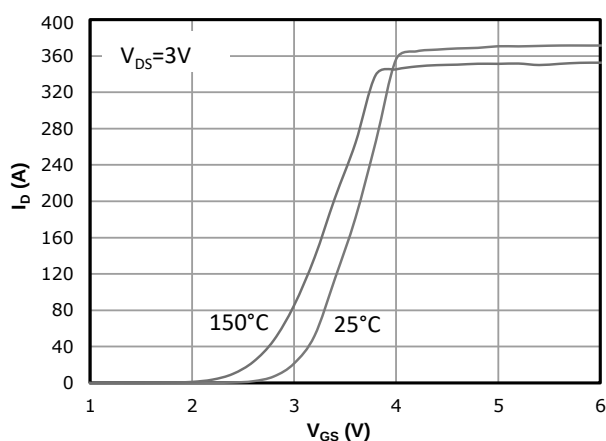


Figure 2. Typ. transfer characteristics

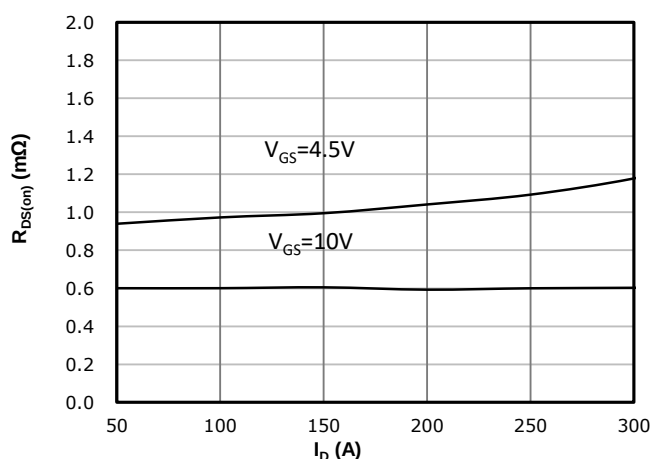


Figure 3. On-Resistance vs. Drain Current

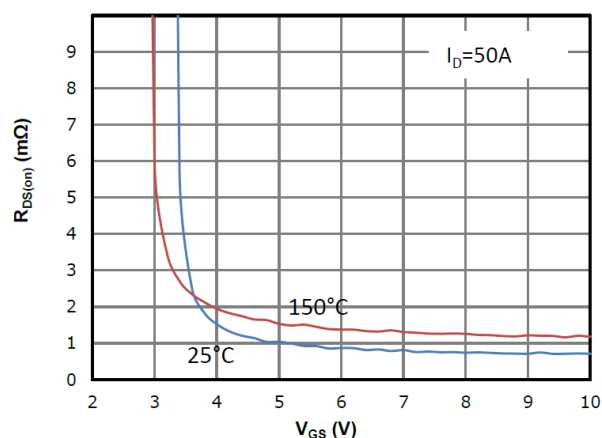


Figure 4. On-Resistance vs. Gate Voltage

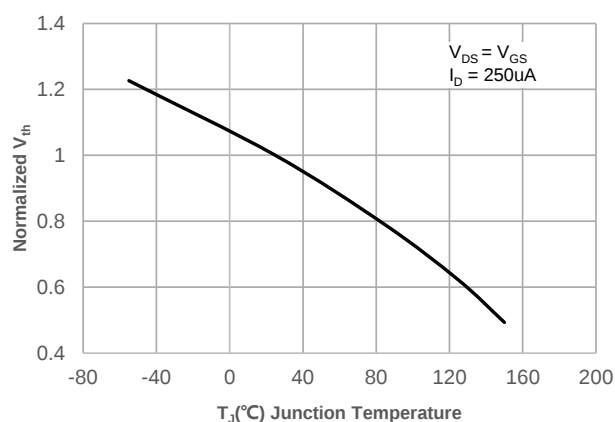


Figure 5. Normalized Threshold Voltage vs. Junction Temperature

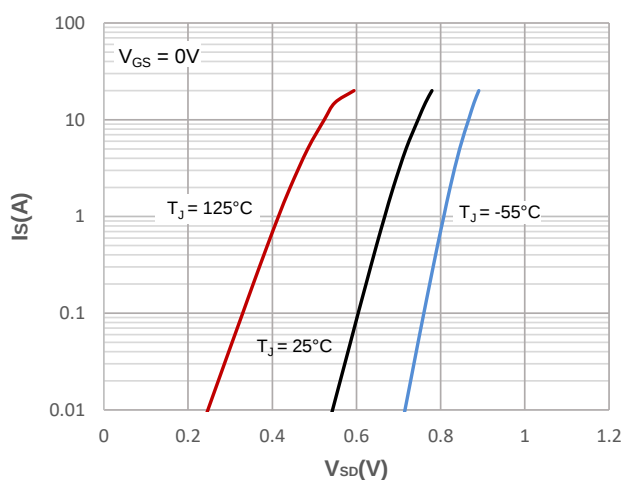
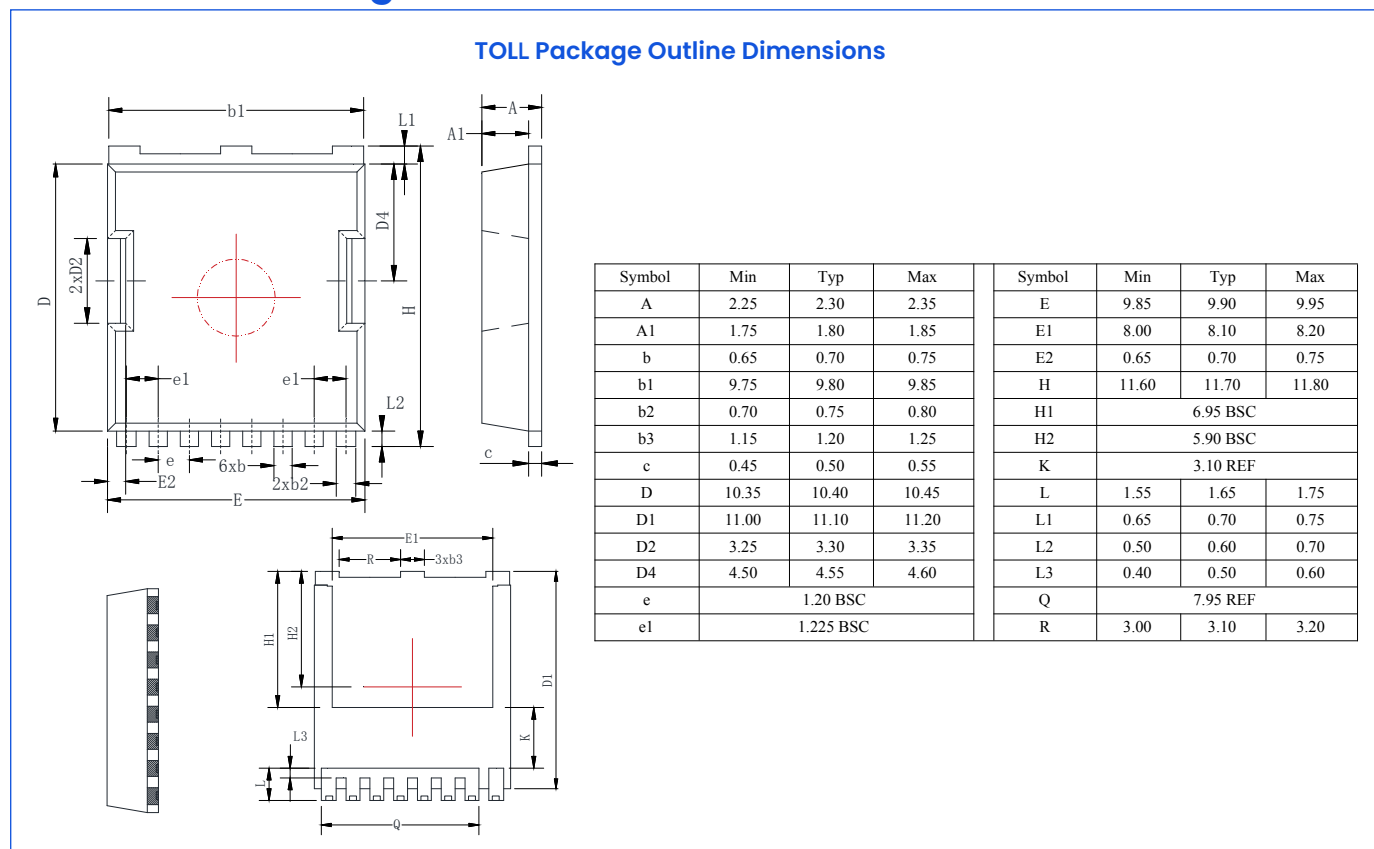


Figure 6. Forward characteristic of body diode

12. Outline Drawing



13. Important Notice and Disclaimer

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