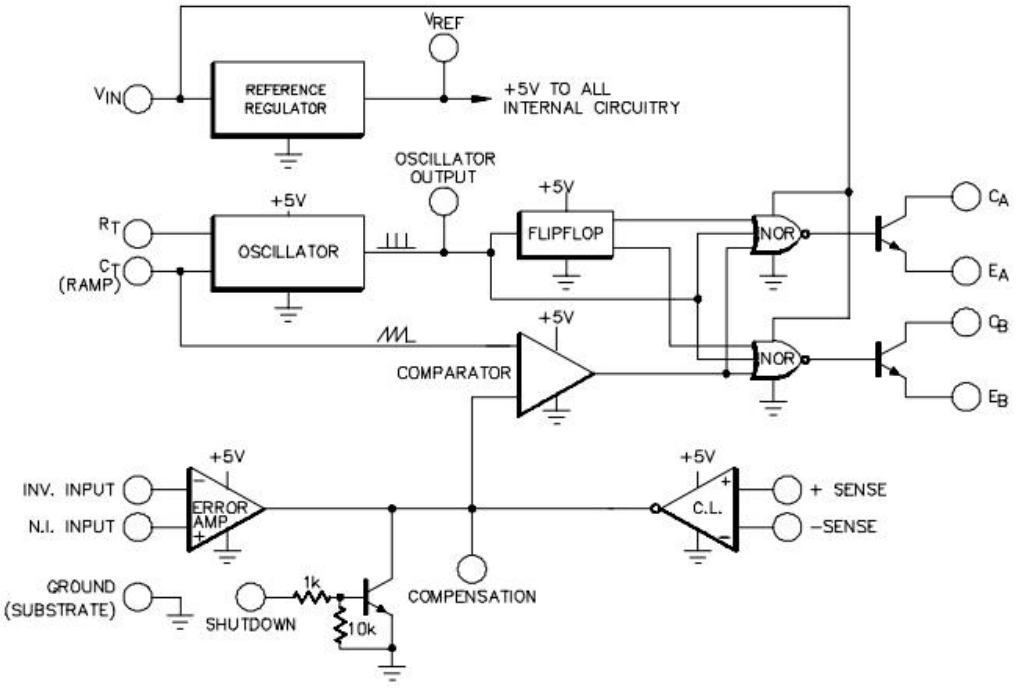
1. DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformer-less voltage doublers, and polarity converters, as well as other power applications.

2. FEATURES

- 8V to 40V operation
- 5V reference
- Reference line and load regulation of 0.4%
- 100 Hz to 300 kHz oscillator range
- Excellent external sync capability
- Dual 50 mA output transistors
- Current limit circuitry
- Complete PwM power control circuitry
- Single-ended or push-pull outputs
- Total supply current less than 10 mA



3. ABSOLUTE MAXIMUM RATINGS

Table 1-1. Absolute Maximum Ratings[1]

Parameter	Value	Units
Input voltage (+V_{IN})	42	V
Collector voltage	40	V
Logic inputs	–0.3 to 5.5	V
Current limit sense inputs	–0.3 to 0.3	V
Output current (each transistor)	100	mA
Reference load current	50	mA
Oscillator charging current	5	mA
Operating Junction Temperature		
Hermetic (J, L packages)	150	°C
Plastic (N, D packages)	150	°C
Storage temperature range	-65 to 150	°C
Lead temperature (soldering, 10 seconds)[2]	300	°C

Notes:
1. Values beyond which damage may occur
2. Pb-free/RoHS peak package solder reflow temp. (40 sec. max. exposure) 260 °C (+0, –5)

4. THERMAL DATA

Table 2-1. Thermal Data [(1-2)]

Parameter	Value	Units
J Package		
Thermal resistance-junction to case, θ_{JC}	30	°C/W
Thermal resistance-junction to ambient, θ_{JA}	80	°C/W
N Package		
Thermal resistance-junction to case, θ_{JC}	40	°C/W
Thermal resistance-junction to ambient, θ_{JA}	65	°C/W
DW Package		
Thermal resistance-junction to case, θ_{JC}	50	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W
L Package		
Thermal resistance-junction to case, θ_{JC}	35	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W

Notes:
1. Junction temperature calculation: TJ = TA + (PD × θJA)
2. The above numbers for θJC are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θJA numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

5. RECOMMENDED OPERATING CONDITIONS

Table 3-1. Recommended Operating Conditions[1]

Parameter	Value	Units
Input voltage (+Vin)	8 to 40	V
Collector voltage	0 to 40	V
Error amp common mode range	1.8 to 3.4	V
Current limit sense common mode range	-0.3 to 0.3	V
Output current (each transistor)	0 to 50	mA
Reference load current	0 to 20	mA
Oscillator charging current	30 µAto 2 mA	µA, mA
Oscillator frequency range	100 Hz to 300 kHz	Hz, kHz
Oscillator timing resistor (Rt)	1.8 to 100	kΩ
Oscillator timing capacitor (Ct)	1 nF to 1.0 µF	nf, µF
Operating Ambient Temperature Range		
XLSG3524	–25 to 85	°C

Note:

1. Range over which the device is functional and parameter limits are guaranteed.

6. Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for XLSG3524 with 0 °C ≤ T_A ≤ 70 °C, and +V_{IN} = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Table 4-1. Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Units
Reference Section[1]					
Output voltage	T_J = 25°C	4.60	5.00	5.40	V
Line regulation	V_{IN} = 8V to 40V	—	—	30	mv
Load regulation	I_L =0 to 20 mA	—	—	50	mv
Temperature stability[2]	Over operating temperature range	—	—	50	mv
Output voltage range[2]	Over line, load and temperature	4.60	—	5.40	V
Short circuit current	V_{REF}=OV	25	50	150	mA
Oscillator Section[3]					
Initial accuracy	T_J=25 °C	36	44	44	kHz
	Min ≤ TJ ≤ Max	34	—	46	kHz
Voltage stability	V_{IN} = 8V to 40V	—	0.1	1	%
Maximum frequency	RT = 2 kΩ, CT = 1 nF	200	400	—	kHz
Sawtooth peak voltage	V_{IN} = 40V	3	—	3.8	V
Sawtooth valley voltage	V_{IN} = 8V	0.6	1	1.2	V
Clock amplitude	—	3.2	—	—	V
Clock pulse width	—	0.3	—	1.5	µs
Error Amplifier Section[4]					
Input offset voltage	R_S ≤ 2 kΩ	—	2	10	mv
Input bias current	—	—	1	10	µA
Input offset current	—	—	—	2	µA
DC open loop gain	R_L ≥ 10 MΩ, T_J = 25 °C	60	—	—	dB
Output low level	$V_{PIN\ 1}$ – $V_{PIN\ 2}$ ≥ 150 mV	—	0.2	0.5	V
Output high level	$V_{PIN\ 2}$ – $V_{PIN\ 1}$ ≥150 mV	3.8	4.2	—	V
Common mode rejection	V_{CM} = 1.8V to 3.4V	—	—	—	dB
Supply voltage rejection	V_{IN} = 8V to 40V	—	—	—	dB
Gain-bandwidth product[2]	T_J = 25 °C	1	2	—	MHz
P.W.M. Comparator[3]					
Minimum duty cycle	V_{COMP} = 0.5V	—	—	0	%
Maximum duty cycle	V_{COMP} = 3.6V	45	49	—	%
Current Limit Amplifier Section[5]					
Sense voltage	T_J = 25 °C	180	200	220	mV
Input bias current	—	—	—	200	µA
Shutdown Section					
Threshold voltage	T_J = 25 °C	0.5	0.8	1.2	V
	Min ≤ T_J ≤ Max	0.2	—	1.8	V

Parameter	Test Conditions	Min	Typ	Max	Units
Output Section (Each Transistor)					
Collector leakage current	V_{CE} = 40V	—	—	50	µA
Collector saturation voltage	I_C = 50 mA	—	—	2	V
Emitter output voltage	I_E = 50 mA	17	—	—	V
Collector voltage rise time	R_C = 2 kΩ	—	—	0.4	µs
Collector voltage fall time	R_C = 2 kΩ	—	—	0.2	µs
Power Consumption					
Standby current	V_{IN} = 40V	—	7	10	mA

Notes:

1. I_L = 0 mA
2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. F_{OSC} = 40 kHz (R_T = 2.9 kΩ, C_T = 0.01 µF)
4. V_{CM} = 2.5V
5. V_{CM} = 0V

7. APPLICATION NOTES

7.1. Oscillator

The oscillator in the XLSG3524 uses an external resistor RT to establish a constant charging current into an external capacitor CT. While this uses more current than a series-connected RC, it provides a linear ramp voltage at CT which is used as a time-dependent reference for the PWM comparator. The charging current is equal to 3.6V/RT, and should be restricted to between 30 µA and 2 mA. The equivalent range for RT is 100k to 1.8k.

The range of values for CT also has limits, as the discharge time of CT determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead-time relationship is shown in Figure 5-1. A pulse width below 0.35 microseconds may cause failure of the internal flip-flop to toggle. This restricts the minimum value of CT to 1000 pF. (Note: Although the oscillator output is a convenient oscilloscope sync input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly.) Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of CT fall between 1000 pF and 0.1 µF, although successful 120 Hz oscillators have been implemented with values up to 5 µF and a series surge limit resistor of 100 ohms.

The oscillator frequency is approximately 1/RT×CT; where R is in ohms, C is in microfarads, and the frequency is in Megahertz. For greater accuracy, the chart in Figure 5-2 may be used for a wide range of operating frequencies. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip-flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is 1/2 the oscillator frequency.

If it is desired to synchronize the XLSG3524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with RT and CT values that cause it to free-run at 90% of the external sync frequency. A sync pulse with a maximum logic 0 of +0.3 volts and a minimum logic 1 of +2.4 volts applied to Pin 3 will lock the oscillator to the external source. The minimum sync pulse-width should be 200 nanoseconds, and the maximum is determined by the required dead-time. The clock pin should never be driven more negative than –0.3 volts, nor more positive than +5.0 volts. The nominal resistance to ground is 3.2k at the clock pin, ±25% over temperature.

If two or more XLSG3524 must be synchronized together, program one controller unit with RT and CT for the desired frequency. Leave the RT pins on the target open, connect the CT pins to the CT of the controller, and connect the clock pins to the clock pin of the controller. Since CT is a high-impedance node, this sync technique works best when all devices are close together.

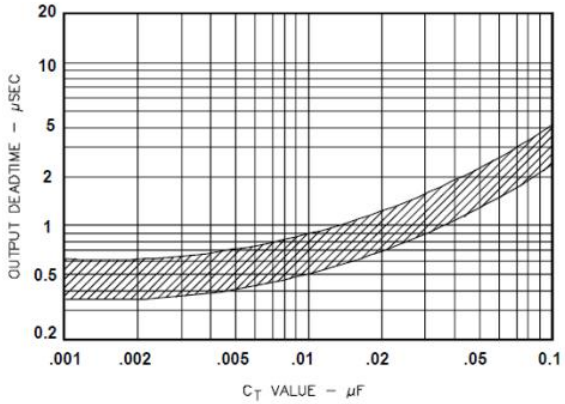


Figure 5-1. Output Stage Dead-time V_S. Ct

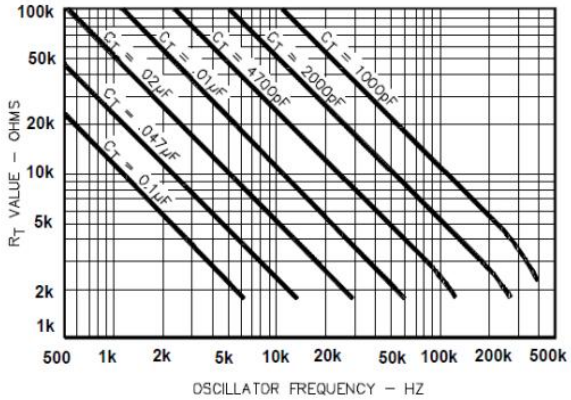


Figure 5-2. Oscillator Frequency Vs. RT and CT

7.2. Current Limiting

The current limiting circuitry of the XLSG3524 is shown in Figure 5-3. By matching the base-emitter voltages of Q1 and Q2 and assuming a negligible voltage drop across R1:

C.L. Threshold = $V_{BE}(Q1) + I_1 \times R_2 - V_{BE}(Q2) = I_1 \times R_2 \sim 200$ mV.

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use because of its simplicity.

The most important of these is the limited common-mode voltage range: ±0.3 volts around ground. This requires sensing in the ground or return line of the power supply. Also precautions should be taken to not turn on the parasitic substrate diode of the integrated circuit, even under transient conditions. A Schottky clamp diode at Pin 5 may be required in some configurations to achieve this.

A second factor to consider is that the response time is relatively slow. The current limit amplifier is internally compensated by R_1, C_1, and Q1, resulting in a roll-off pole at approximately 300 Hz. A third factor to consider is the bias current of the C.L. sense pins. A constant current of approximately 150 μA flows out of Pin 4, and a variable current with a range of 0-150 μA flows out of Pin 5. As a result, the equivalent source impedance seen by the current sense pins should be less than 50 ohms to keep the threshold error less than 5%.

Since the gain of this circuit is relatively low (42 dB), there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle (+2 volts at the error amplifier output) with the error amplifier signaling maximum duty cycle.

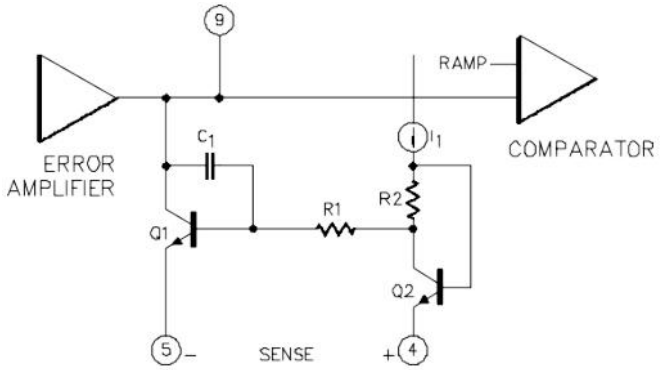
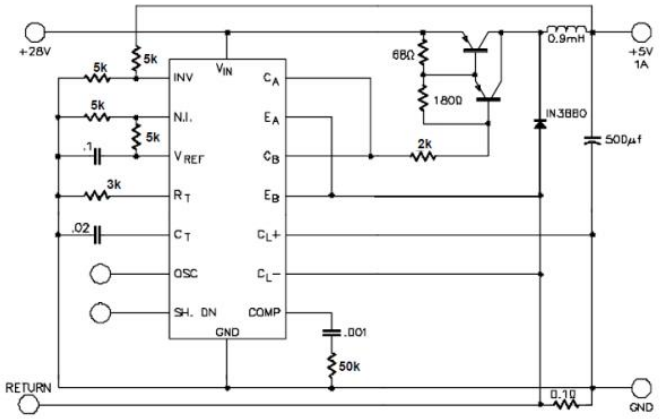
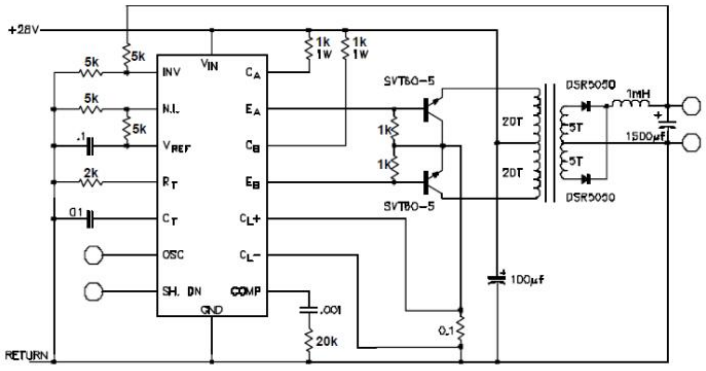


Figure 5-3. Current Limiting Circuitry of the XLSG3524



In this conventional single-ended regulator circuit, the two outputs of the XLSG3524 are connected in parallel for effective 0-90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability



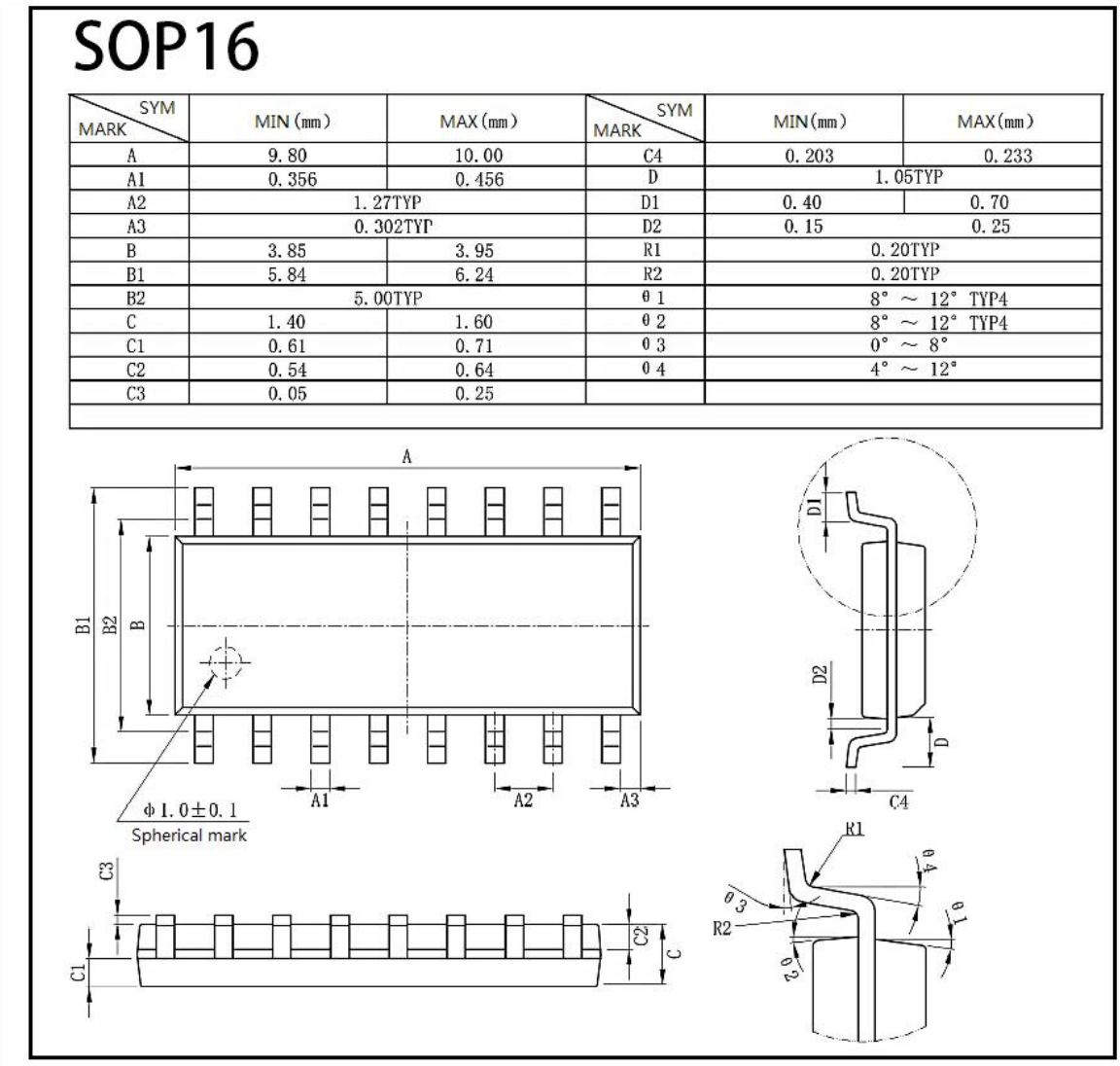
Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the XLSG3524 internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

8. ORDERING INFORMATION

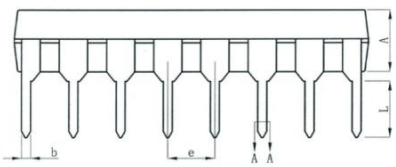
Ordering Information

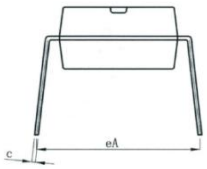
Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLSG3524N	XL3524N	DIP16	19.05*6.35	-25 to +85	MSL3	Tube 25	1000
XLSG3524DR	XL3524D	SOP16	10.00*3.95	-25 to +85	MSL3	T&R	2500

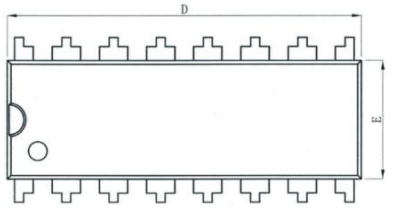
9. DIMENSIONAL DRAWINGS

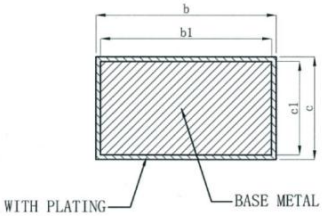


DIP16









symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---