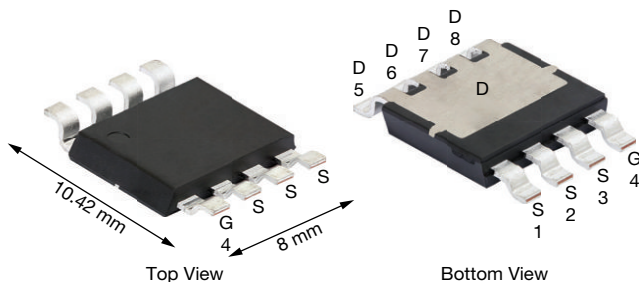


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

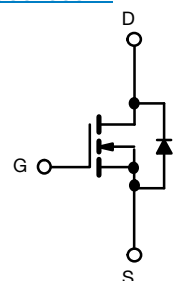
PowerPAK® 8 x 8LR


FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.00065
I_D (A) ^e	413
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ140ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ^e	I_D	413	A
		238	
Continuous source current (diode conduction) ^e	I_S	194	
Pulsed drain current ^{a, e}	I_{DM}	1653	
Single pulse avalanche current	I_{AS}	84	mJ
Single pulse avalanche energy		352	
Maximum power dissipation ^e	P_D	214	W
		71	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	44	°C/W
Junction-to-case (drain) ^d	R_{thJC}	0.7	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

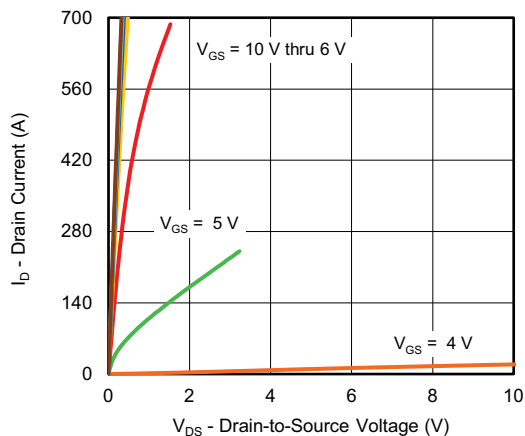
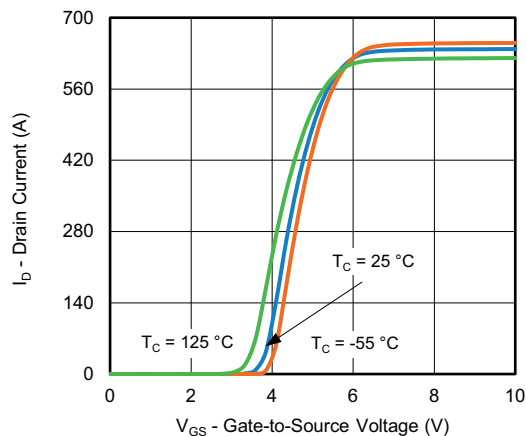
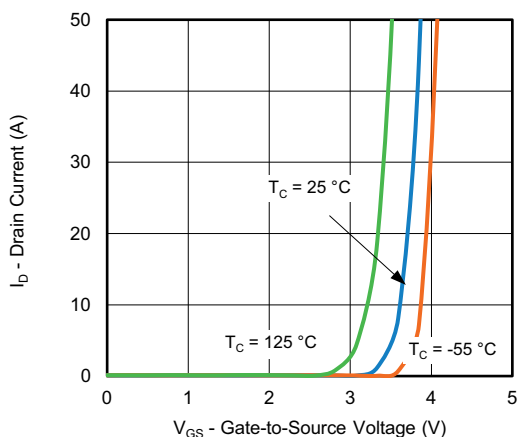
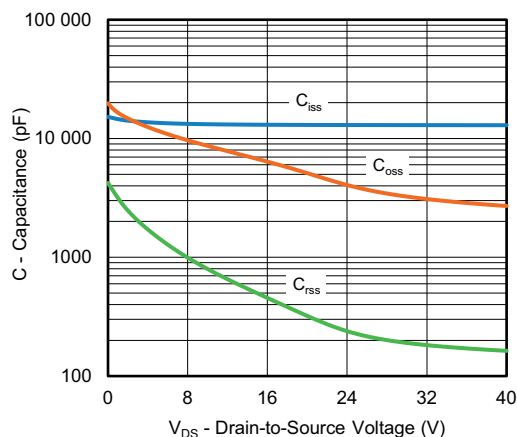
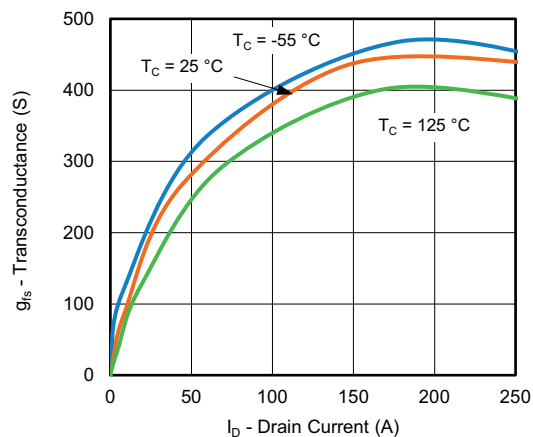
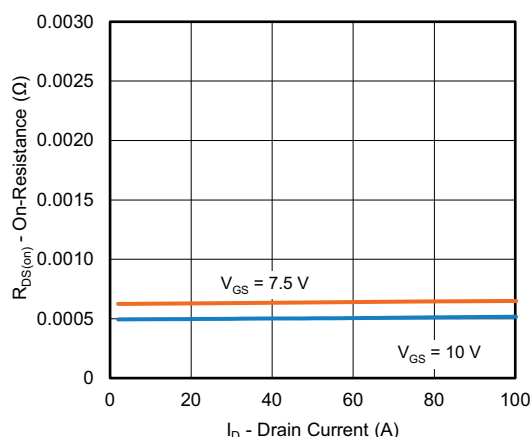


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.3	2.7	3.3	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	100	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.00057	0.00065	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0012	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0015	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 80 A		-	160	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	13 160	18 424	pF
Output capacitance	C _{oss}			-	3768	5276	
Reverse transfer capacitance	C _{rss}			-	226	317	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 40 A	-	192	288	nC
Gate-source charge ^c	Q _{gs}			-	58	-	
Gate-drain charge ^c	Q _{gd}			-	39	-	
Gate resistance	R _g	f = 1 MHz		1.7	1.6	2.7	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 0.5 Ω I _D ≅ 40 A, V _{GEN} = 10 V, R _g = 1 Ω		-	24	36	ns
Rise time ^c	t _r			-	27	41	
Turn-off delay time ^c	t _{d(off)}			-	60	90	
Fall time ^c	t _f			-	26	39	
Source-Drain Diode Ratings and Characteristics ^b							
Reverse recovery time	t _{rr}	V _{DD} = 32 V, I _{FM} = 20 A, di/dt = 100 A/μs		-	88	176	ns
Reverse recovery charge	Q _{rr}			-	184	368	nC
Reverse recovery current	I _{RM}			-	-3.7	-	A
Pulsed current ^a	I _{SM}			-	-	776	A
Forward voltage	V _{SD}	I _F = 50 A, V _{GS} = 0		-	0.8	1.1	V

Notes

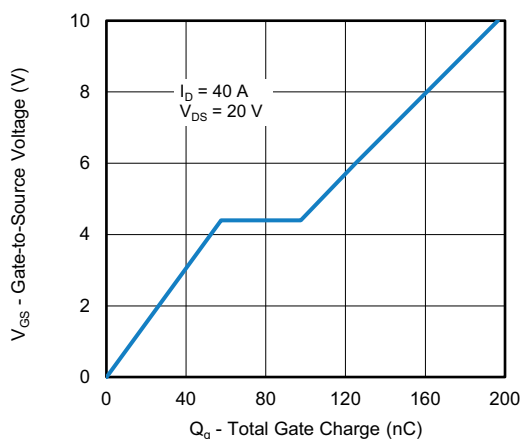
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

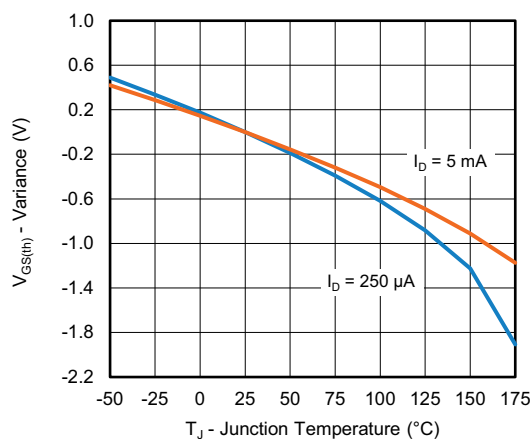
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Capacitance

Transconductance

On-Resistance vs. Drain Current



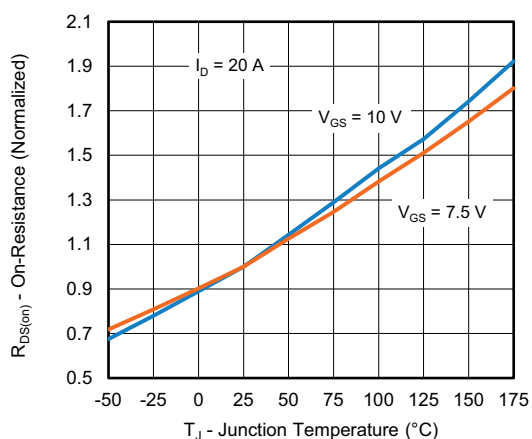
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



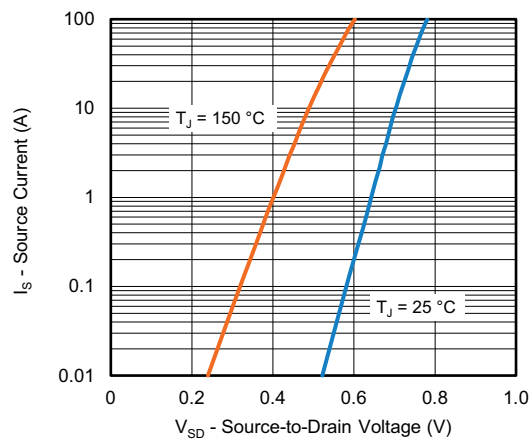
Gate Charge



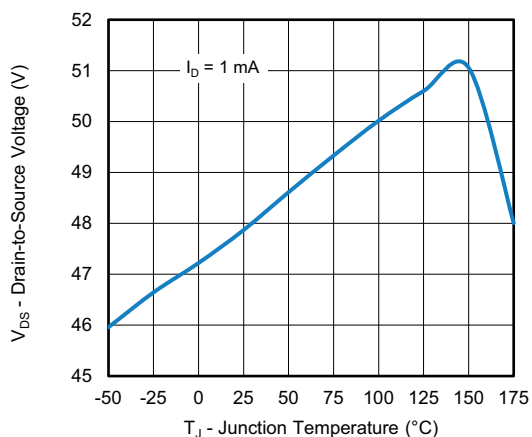
Threshold Voltage



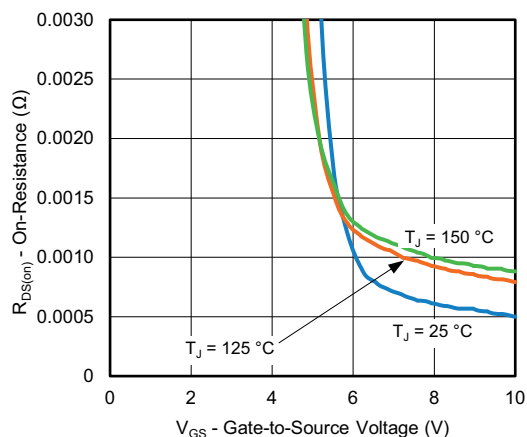
On-Resistance vs. Junction Temperature



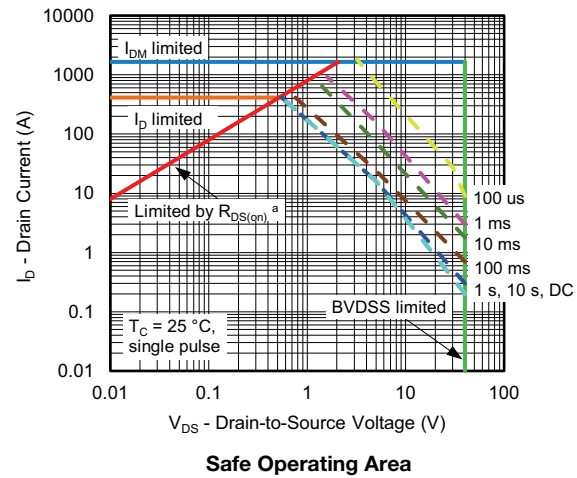
Source Drain Diode Forward Voltage



Drain Source Breakdown vs. Junction Temperature



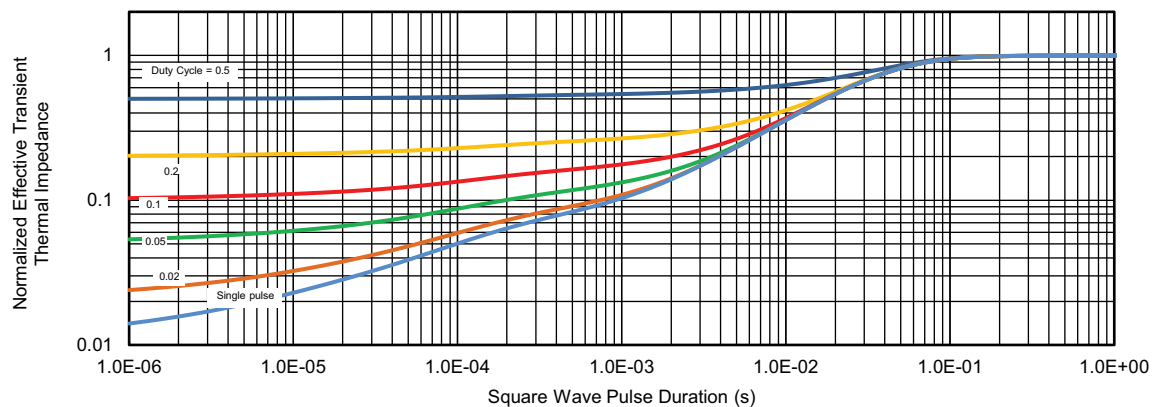
On-Resistance vs. Gate-to-Source Voltage


Note

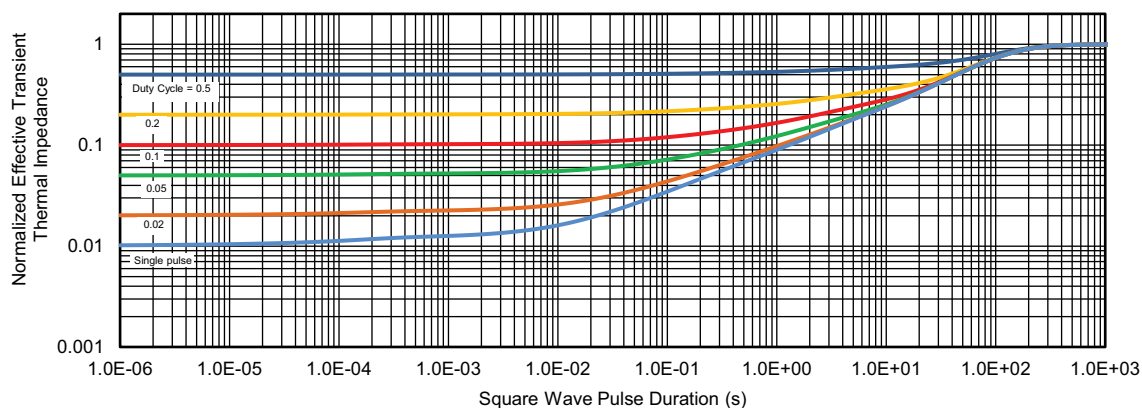
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



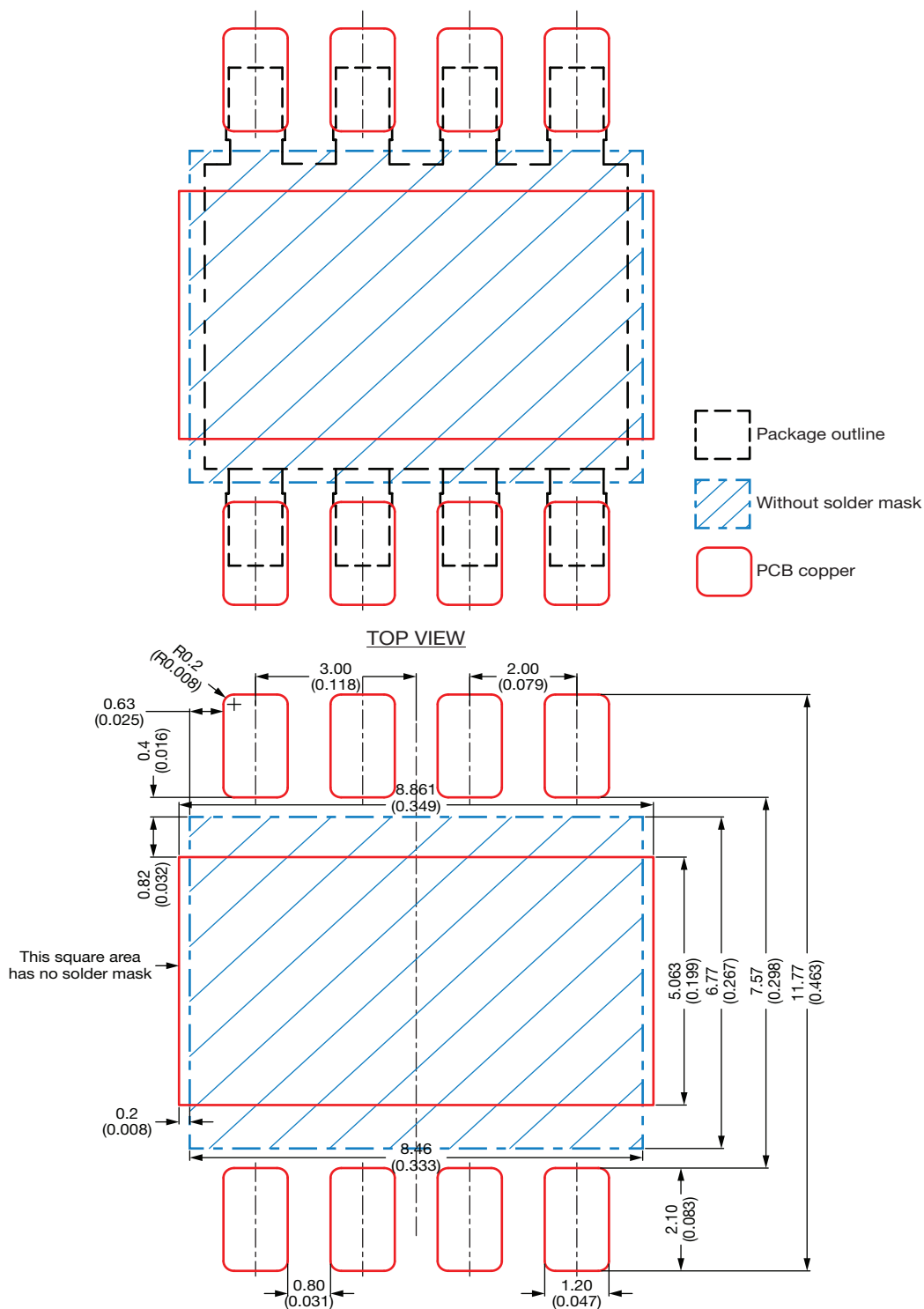
Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023

DWG: 3002



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