MAE0621A-Q3C, MAE0621A-Q3I Gigabit Ethernet Transceiver Datasheet

Version 1.1

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Document History

Version	Effect Date	Description of Version
1.0	2022/10	Initial Official Release
1.1	2024/8	1. Update DVDD10/AVDD10 recommended operating voltage in Table 10-2; 2. Update Vih/Vil in Table 10-3 Crystal Requirements and Table 10-4 Oscillator/External Clock Requirements; 3. Update Table 10-5 DC Characteristics.

Table of Contents

Table of Figures

Table of Tables

1 Overviews

The MAE0621A-Q3C/MAE0621A-Q3I (hereinafter referred to as MAE0621A) is a single-chip Gigabit Ethernet Transceiver, which is compliant with IEEE 802.3 10BASE-T, IEEE 802.3u 100BASE-TX and IEEE 802.3ab 1000BASE-T. It provides RGMII MAC interface and implements the physical layer functions to transmit and receive data on existing CAT.5 unshielded twisted pair cable.

The MAE0621A uses advanced mix-signal processing to achieve the functions of digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders and decoders, echo and crosstalk cancelers to provide robust and reliable high-speed data transmission.

2 Features

- 1000BASE-T IEEE 802.3ab Compliant
- 100BASE-TX IEEE 802.3u Compliant
- 10BASE-T IEEE 802.3 Compliant
- RGMII MAC interface
- Configurable RGMII I/O voltage (3.3V, 2.5V, 1.8V, 1.5V)
- Advanced baseline wander correction
- Auto-negotiation and parallel detection
- MDI/MDIX crossover detection and auto-correction
- Automatic polarity correction
- 25MHz clock source oscillator or crystal as clock source input
- 25MHz or 125MHz clock generator
- Support interrupt function
- Wake-on-LAN (WoL)
- PHYRSTB core power turn-off
- Link down power saving
- Integrated switching voltage regulator and LDO
- Support operating with single 3.3V supply
- Configurable network status indicator
- Commercial or industrial grade device
- 40-pin QFN package

3 System Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Switch
- Industrial Network and Factory Automation
- IP Network Camera
- Intelligent Building

In addition, the MAE0621A can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection.

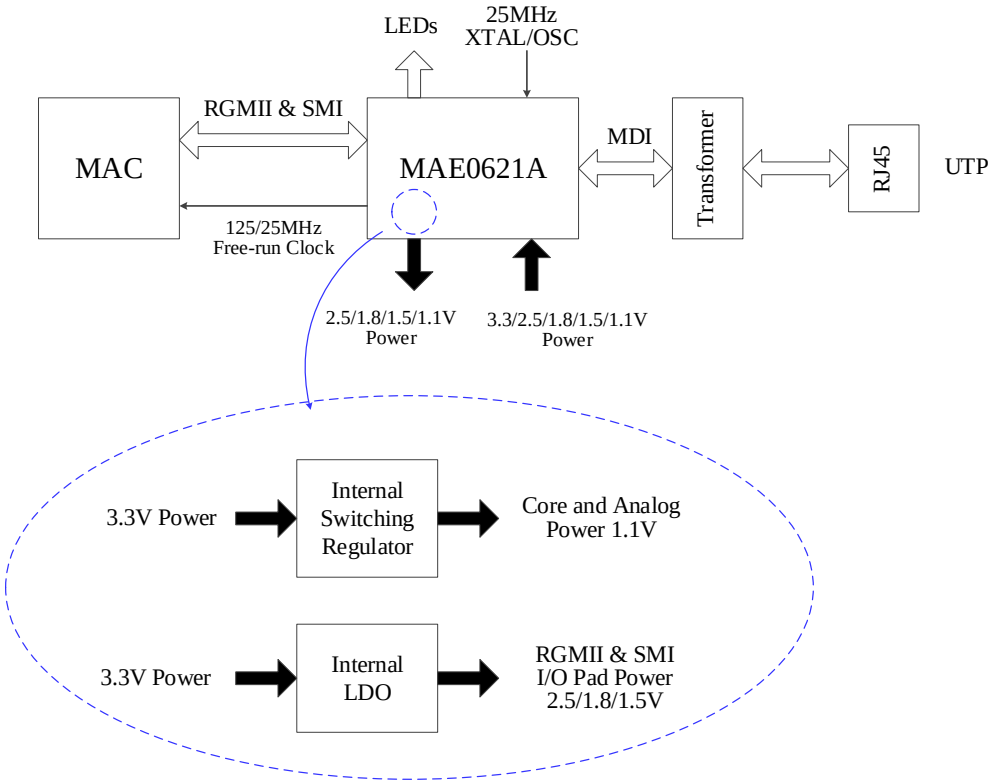


Figure 3-1 Application Diagram

4 Block Diagram

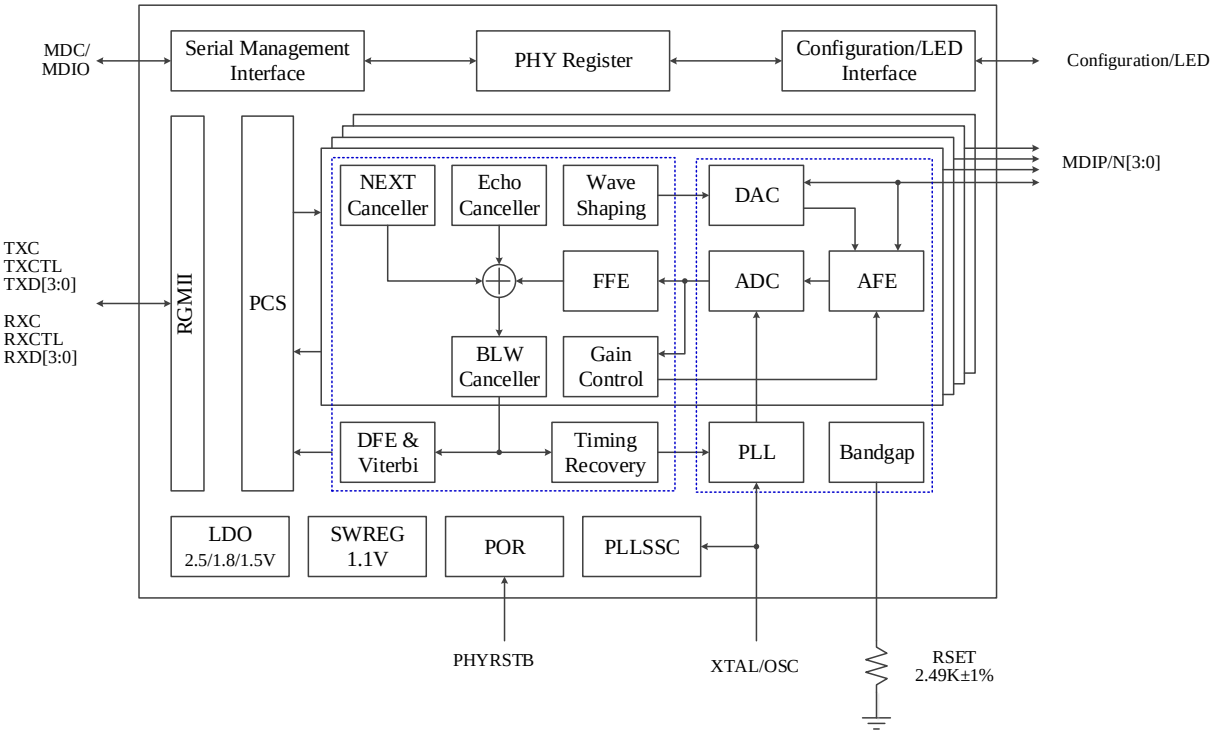


Figure 4-1 Block Diagram

5 Pin Assignments

5.1 Pin Assignments

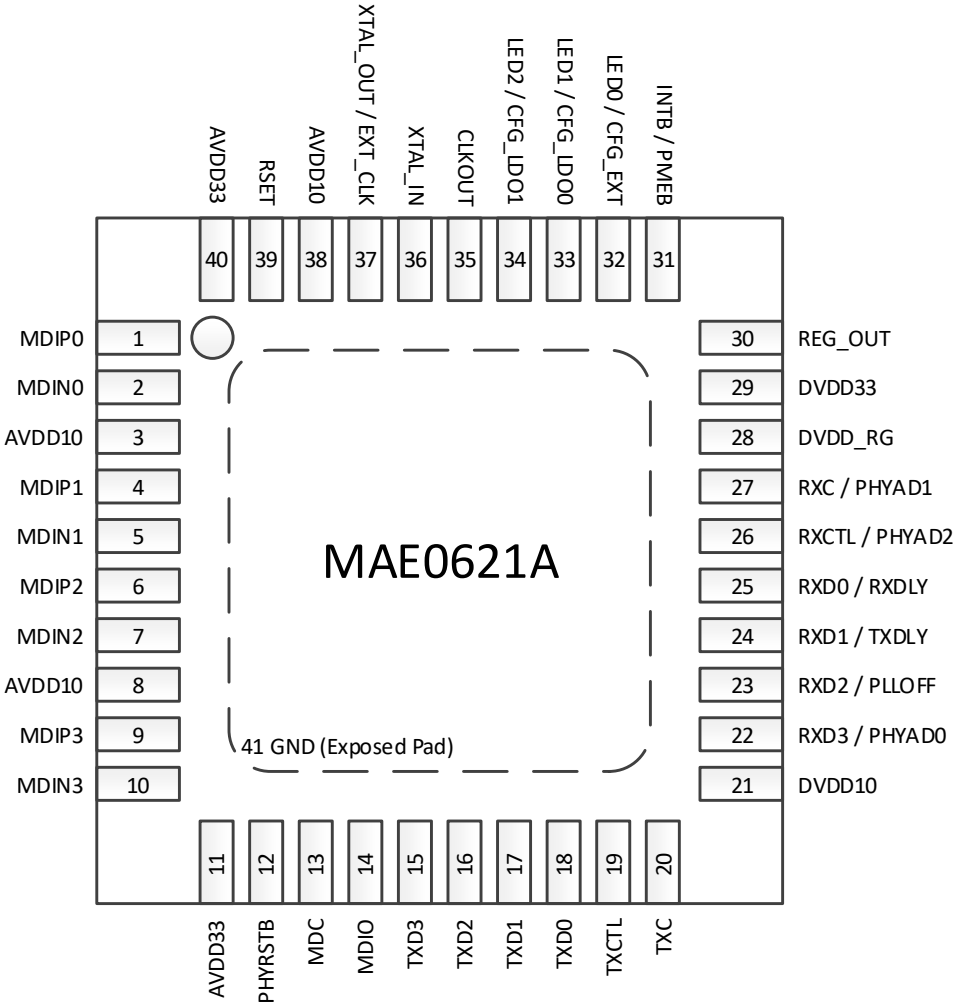


Figure 5-1 Pin Assignments (40-Pin QFN)

5.2 Pin List Table

Table 5-1 Pin List

Pin No.	Pin Name	Pin No.	Pin Name
1	MDIP0	21	DVDD10
2	MDIN0	22	RXD3/PHYAD0
3	AVDD10	23	RXD2/PLLOFF
4	MDIP1	24	RXD1/TXDLY
5	MDIN1	25	RXD0/RXDLY
6	MDIP2	26	RXCTL/PHYAD2

Pin No.	Pin Name	Pin No.	Pin Name
7	MDIN2	27	RXC/PHYAD1
8	AVDD10	28	DVDD_RG
9	MDIP3	29	DVDD33
10	MDIN3	30	REG_OUT
11	AVDD33	31	INTB/PMEB
12	PHYRSTB	32	LED0/CFG_EXT
13	MDC	33	LED1/CFG_LDO0
14	MDIO	34	LED2/CFG_LDO1
15	TXD3	35	CLKOUT
16	TXD2	36	XTAL_IN
17	TXD1	37	XTAL_OUT/EXT_CLK
18	TXD0	38	AVDD10
19	TXCTL	39	RSET
20	TXC	40	AVDD33
		41	GND

6 Signal Description

6.1 Pin Type Definition

The functionalities of the pins are defined below:

Table 6-1 Pin Type Definition

Pin Type	Definition
I	Input
LI	Latched Input During Power up or Reset
O	Output
OD	Open Drain
IO	Bi-directional Input and Output
PU	Internal Pull Up During Power On Reset
PD	Internal Pull Down During Power On Reset
P	Power
G	Ground

6.2 Media Dependent Interface (MDI)

Table 6-2 MDI

Pin Name	Pin No.	Type	Description
MDIP0	1	IO	Media Dependent Interface [0]. In 1000BASE-T MDI mode, MDI[0]+/- correspond to BI_DA+/-. In crossover mode, MDI[0]+/- correspond to BI_DB+/-. In 100BASE-TX and 10BASE-T MDI modes, MDI[0]+/- are used for the transmitting pair. In crossover mode, MDI[0]+/- are used for the receiving pair.
MDIN0	2	IO	
MDIP1	4	IO	Media Dependent Interface [1]. In 1000BASE-T MDI mode, MDI[1]+/- correspond to BI_DB+/-. In crossover mode, MDI[1]+/- correspond to BI_DA+/-. In 100BASE-TX and 10BASE-T MDI modes, MDI[1]+/- are used for the receiving pair. In crossover mode, MDI[1]+/- are used for the transmitting pair.
MDIN1	5	IO	
MDIP2	6	IO	Media Dependent Interface [2]. In 1000BASE-T MDI mode, MDI[2]+/- correspond to BI_DC+/-. In crossover mode, MDI[2]+/- correspond to BI_DD+/-. In 100BASE-TX and 10BASE-T MDI modes, MDI[2]+/- are not used.
MDIN2	7	IO	
MDIP3	9	IO	Media Dependent Interface [3]. In 1000BASE-T MDI mode, MDI[3]+/- correspond to BI_DD+/-. In crossover mode, MDI[3]+/- correspond to BI_DC+/-.

Pin Name	Pin No.	Type	Description
MDIN3	10	IO	In 100BASE-TX and 10BASE-T MDI modes, MDI[3]+/- are not used.

6.3 Clock Interface

Table 6-3 Clock Interface

Pin Name	Pin No.	Type	Description
XTAL_IN	36	I	25MHz Crystal Input. It should be connected to GND if an external 25MHz oscillator drives XTAL_OUT/EXT_CLK.
XTAL_OUT/EXT_CLK	37	O	25MHz Crystal Output. If a 25MHz oscillator is used, connect XTAL_OUT/EXT_CLK to the oscillator's output.
CLKOUT	35	O	125/25MHz Reference Clock Output. Continuous 25/125MHz output generated from internal PLL.

Note: The external 25MHz clock shall be 3.3V domain. Please refer to section 10.3 for more information.

6.4 Reduced Gigabit Media Independent Interface (RGMII)

Table 6-4 RGMII Interface

Pin Name	Pin No.	Type	Description
TXC	20	I	RGMII Transmit Clock. It provides the 125MHz, 25MHz or 2.5MHz reference clock depending on the speed.
TXCTL	19	I	RGMII Transmit Control from the MAC.
TXD0	18	I	RGMII Transmit Data. In RGMII mode, TXD[3:0] run at double data rate with bits[3:0] presented on the rising edge of TXC, bits[7:4] presented on the falling edge of TXC.
TXD1	17	I	
TXD2	16	I	
TXD3	15	I	
RXC	27	O/LI/PD	RGMII Receive Clock. 2.5/25/125MHz Output. It is recovered from the received the data stream and is used to synchronize the receive data outputs: 125MHz in 1000Mbps RGMII mode; 25MHz in 100Mbps mode; 2.5MHz in 10Mbps mode.
RXCTL	26	O/LI/PD	RGMII Receive Control to the MAC.
RXD0	25	O/LI/PU	RGMII Receive Data. In RGMII mode, RXD[3:0] run at double data rate with bit [3:0] on the rising-edge of RXC, bit [7:4] on the falling-edge of RXC.
RXD1	24	O/LI/PD	
RXD2	23	O/LI/PD	
RXD3	22	O/LI/PU	

6.5 Serial Management Interface (SMI)

Table 6-5 SMI

Pin Name	Pin No.	Type	Description
MDC	13	I	Serial Management Clock. The MDC clock must be provided to allow MII management functions.
MDIO	14	IO/PU	Serial Management Data I/O. The serial input/output bit is used to read from and write to the MII registers. Pull up 3.3/2.5/1.8/1.5V for 3.3/2.5/1.8/1.5V I/O respectively.

6.6 Interrupt Interface

Table 6-6 Interrupt Interface

Pin Name	Pin No.	Type	Description
INTB/PMEB	31	O/OD	Interrupt/Power Management Event. Keep this pin floating if either of the functions is not used. 1. Interrupt Active low. Set low if the specified events happened. 2. Power Management Event. Active low. Set low if received a magic packet or wake-up frame, or wake-up event. Note 1: The behavior of this pin is level-triggered. Note 2: See section 7.12 for more details.

6.7 Reset Interface

Table 6-7 Reset Interface

Pin Name	Pin No.	Type	Description
PHYRSTB	12	I/PU	Hardware Reset. The active low PHYRSTB initializes or re-initializes the PHY. All internal registers will reinitialize to default value upon assertion of PHYRSTB. See section 7.8 for more details.

6.8 Hardware Configuration Interface

Table 6-8 Hardware Configuration Interface

Pin Name	Pin No.	Type	Description
PHYAD0	22	O/LI/PU	PHYAD[2:0]. Sampled on reset. The PHY address selects MII management PHY address.
PHYAD1	27	O/LI/PD	
PHYAD2	26	O/LI/PD	
PLLOFF	23	O/LI/PD	ALDPS Mode PLL Off Configuration. Pull up to stop PLL when entering ALDPS mode.
TXDLY	24	O/LI/PD	RGMII Transmit Clock Timing Control. Pull up to add 2ns delay to TXC for TXD latching.

Pin Name	Pin No.	Type	Description
RXDLY	25	O/LI/PU	RGMII Receive Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching.
CFG_EXT	32	O/LI/PD	RGMII and SMI I/O Pad Power Source Mode Configuration. When pulling down CFG_EXT, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved; 2'b01: 2.5V from internal LDO; 2'b10: 1.8V from internal LDO; 2'b11: 1.5V from internal LDO. When pulling up CFG_EXT, CFG_LDO[1:0] represent the input voltage of IO pad is selected from external power: 2'b00: 3.3V from external power; 2'b01: 2.5V from external power; 2'b10: 1.8V from external power; 2'b11: 1.5V from external power.
CFG_LDO0	33	O/LI/PU	
CFG_LDO1	34	O/LI/PD	

6.9 LED Interface

Table 6-9 LED Interface

Pin Name	Pin No.	Type	Description
LED0	32	O/LI/PD	Link Status LED Indicator 0. High: Link up at 10Mbps; Blinking: Transmitting or receiving.
LED1	33	O/LI/PU	Link Status LED Indicator 1. Low: Link up at 100Mbps; Blinking: Transmitting or receiving.
LED2	34	O/LI/PD	Link Status LED Indicator 2. High: Link up at 1000Mbps; Blinking: Transmitting or receiving.

Note 1: High/Low active depends on the hardware configuration setting.
Note 2: See section 7.11 for more LED setting details.

6.10 Power Supply Interface

Table 6-10 Power Supply Interface

Pin Name	Pin No.	Type	Description
RSET	39	O	Reference Resistance. A 2.49KΩ±1% external resistor should be connected to this pin.
REG_OUT	30	O	Switching Regulator 1.1V Output. Connect to an external 2.2uH or 4.7uH inductor.
DVDD33	29	P	3.3V digital non-RGMII and non-SMI I/O Pad Power.
DVDD_RG	28	P	Digital RGMII and SMI I/O Pad Power. When pulling CFG_EXT pin high during hardware configuration (External power mode), connect this pin with external power source for 3.3/2.5/1.8/1.5V I/O pads.
DVDD10	21	P	1.1V Digital Core Power.
AVDD33	11, 40	P	3.3V Analog Power.
AVDD10	3, 8, 38	P	1.1V Analog Power.
GND	41	G	Ground. Exposed Pad (E-pad) is Analog and Digital Ground.

7 Function Description

7.1 Transmit and Receive Functions

7.1.1 1000Mbps Mode

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D-PAM5 symbols, transmitted onto the CAT.5 cable at 125Mbps through a D/A converter.

The input signal from the media is passed through hybrid circuit to reduce the near-end echo. Then the received signal is processed with adaptive equalization, baseline wander correction, crosstalk cancellation, echo cancellation, timing recovery, error correction and 4D-PAM5 decoding. The 8-bit-wide data is recovered and sent to the RGMII interface at a clock of 125MHz.

7.1.2 100Mbps Mode

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion and MLT-3 encoding and transmission onto the media with the D/A converter.

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion with the data presented on the RGMII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

7.1.3 10Mbps Mode

The transmit 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz, are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

The received differential signal is converted into a Manchester-encoded stream. Then the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles presented onto the RGMII interface.

7.2 MAC Interface

The MAE0621A adopts Reduced Gigabit Media Independent Interface (RGMII) as MAC interface. This interface can be used to implement 10/100/1000Mbps by reducing the clock rate to 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps. While it is used to implement 1000 Mbps, the clock rate is 125MHz. The TXC signal is always generated by the MAC and the RXC signal is generated by the PHY. During packet reception, RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulse is allowed. No glitch of the clocks is allowed during speed transition.

The MAC must hold TXCTL low until the MAC has ensured that TXCTL is operating at the same speed as the PHY.

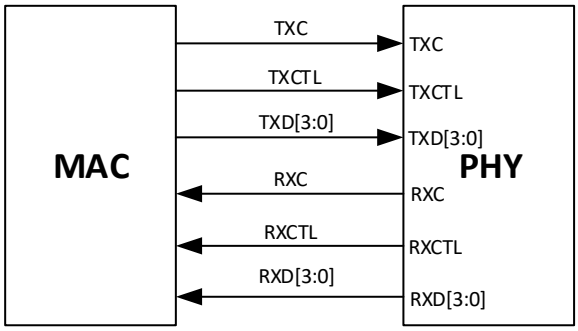


Figure 7-1 RGMII Interface

7.3 Serial Management Interface

The management interface is used to access the internal registers through the MDC and MDIO serial interface that is compliant with IEEE 802.3 clause 22. MDC is the management CLK input. MDIO is the management data input/output which is a bi-directional signal that runs synchronously to MDC. The MDIO pin requires a pull-up resistor of 1.5kΩ that pulls the MDIO high during the idle and turn around.

The MAE0621A share the same MDIO bus and can be distinguished by the unique address that is assigned during the hardware reset. Refer to section 7.9 for more information on how to configure PHY addresses.

The frame structure of read or write instruction for management interface contains following:

- **Preamble**: 32 contiguous logic 1 sent to MDIO pin, along with 32 corresponding cycles on MDC. This provides synchronization for the PHY.
- **Start**: The value of 01 indicates the start of an instruction.
- **Opcode**: A read instruction is 10, while a write instruction is 01.
- **PHY address**: 5 bit PHY address follows with the most significant bit (MSB) transmitted first. 3-bit field of 5-bit PHY address is allowed by the MAE0621A to be assigned for a MDIO bus accessing multiple PHY chips.
- **Register address**: A 5-bit PHY address follows with the MSB transmitted first. The address for the registers used by the MAE0621A are show in Table 8-2.
- **Turnaround**: An idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. When a write operation is being performed, a 10 must be sent to MAE0621A during these 2-bit times. When a read operation is being performed, the MDIO pin of the MAC must be put in high-impedance state during these bit times. The MAE0621A transceiver drives the MDIO pin to during the second bit time.
- **Data**: The last 16 bits of the instruction are the actual data bits.
- **Idle**: No true part of management frame. This is a high impedance state and pull-up resistor will pull MDIO line to logic 1, a minimum of one idle bit is required between operations.

The time sequence of read and write operation is shown in Figure 7-2 and Figure 7-3.

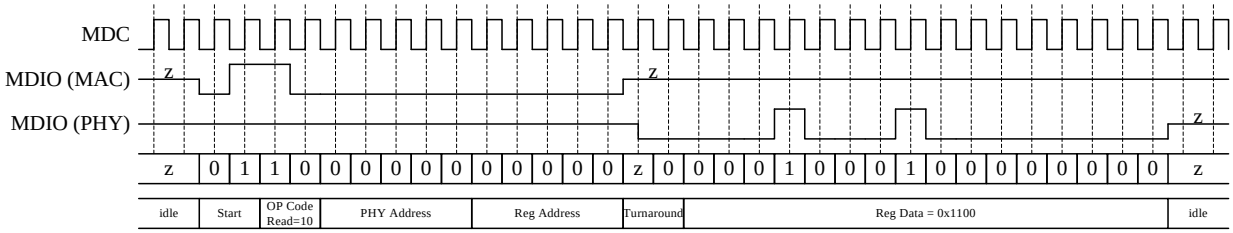


Figure 7-2 MDIO/MDC Read Timing

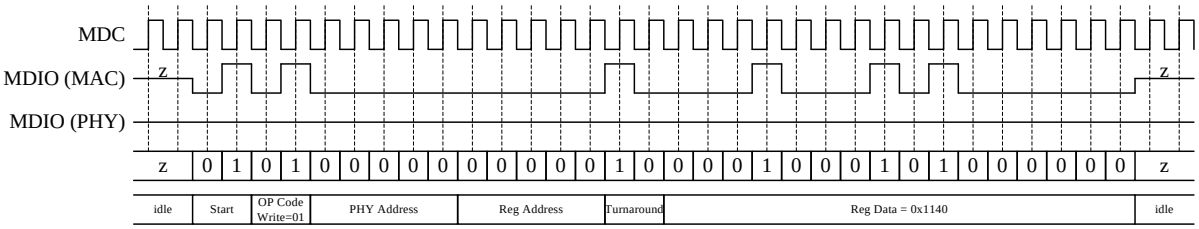


Figure 7-3 MDIO/MDC Write Timing

7.4 MDC/MDIO Register Access

7.4.1 Change Page

The following shows the set MDIO commands in order for the desired Page 0xXYZ (in Hex).

1) To register 31, write Data = 0xXYZ (Page 0xXYZ)
2) Read/Write the target Register Data
3) To register 31, write Data = 0x0000 or 0xa42 (switch back to IEEE 802.3 Standard Registers)

7.4.2 Access to MDIO Manageable Device (MMD)

The MAE0621A supports MMD registers to extend the ability of more device registers access, defined in section 8.3 MMD Register Mapping and Definitions. Access to registers in MMD space is provided via registers 13 and 14.

1) Write to the MMD's register:
   a) Write Function filed to 00(address mode) and DEVAD filed to the device address value for the desired MMD's register. (Register 13)
   b) Write the desired address value to the MMD's register. (Register 14)
   c) Write Function filed to 01 (data mode; no post increment) and DEVAD filed to the same device address for the desired MMD's register. (Register 13)
   d) Write the content to the selected register in MMD's register. (Register 14)

2) Read from the MMD's register:
   a) Write Function filed to 00 (address mode) and DEVAD filed to the device address value for the desired MMD's register. (Register 13)
   b) Write the desired address value to the MMD's register. (Register 14)
   c) Write Function filed to 01 (data mode; no post increment) and DEVAD filed to the same device address for the desired MMD's register. (Register 13)
   d) Read the content from the selected MMD's register. (Register 14)

7.5 Auto-Negotiation

The MAE0621A supports auto-negotiation in compliance with IEEE 802.3 clause 28, 40 and IEEE 802.3az. Auto-negotiation is used to negotiate speed/duplex/flow control and MASTER/SLAVE mode for 1000BASE-T over UTP twisted pair cable. It performs auto-negotiation priority resolution, pause/asymmetric pause resolution, and/or 1000BASE-T MASTER/SLAVE resolution based on the information exchanged between the local and remote devices to determine the best possible operating mode. Auto-negotiation can also advertise the capability of crossover MDI/MDI-X and EEE power saving between the local device and its link partner.

Auto-negotiation and auto MDI/MDI-X can be enabled and disabled independently. Auto-negotiation can be enabled and/or disabled manually via Register 0.12. If auto-negotiation is disabled, the PHY speed and duplex can be set via Register 0.6, 0.8 and 0.13. If auto-negotiation is enabled, the ability of operating 10/100/1000BASE-T mode can be set via Register 4 and 9.

Auto-negotiation process will be triggered automatically whenever any one of the following occurs:

- Power-up
- Hardware reset
- Software reset (Register 0.15)
- Restart auto-negotiation (Register 0.9)
- Change from power down to power up (Register 0.11)
- Copper link goes down (e.g., entering the link fail state)

7.5.1 Auto-Negotiation Resolution

1) Priority Resolution

Since the MAE0621A has the multiple abilities of 10/100/1000BASE-T speeds and full/half duplex modes, auto-negotiation process follows the IEEE802.3 prioritization resolution scheme to ensure the highest common denominator ability, which is selected through the information carried in the link code word. Table 7-1 shows the order of priority from high to low.

Table 7-1 Prioritization Resolution

Priority	Speed	Duplex mode	Note
Highest	1000BASE-T	Full	
	1000BASE-T	Half	Not support
	100BASE-TX	Full	
	100BASE-TX	Half	
	10BASE-T	Full	
Lowest	10BASE-T	Half	

2) MASTER/SLAVE Resolution

The MAE0621A operating in 1000BASE-T mode supports auto-negotiation and being capable of operating as MASTER or SLAVE. The PHY automatically transmits next pages or extended next pages to advertise the ability.

The decision priority of master depends on both the port type and whether it is manually set:

- Manual has a higher priority than non-manual.

- The multi-port PHY has priority over the signal-port PHY.

The following four equations are used to determine the relationships:

- Manual MASTER = U0*U1
- Manual SLAVE = U0*U1
- Single port device=!U0*!U2
- Multiport device=!U0*U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1
See Table 7-2 for detailed definition.

Table 7-2 1000BAST-T U0-U2 Bit Assignment of Next Page

U2	1000BASE-T port type bit (1 = multiport device and 0 = single-port device)	GMII Register 9.10 (MASTER-SLAVE Control Register)
U1	1000BASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE) This bit is ignored if Register 9.12 = 0.	GMII Register 9.11 (MASTER-SLAVE Control Register)
U0	1000BAST-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable) This bit intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with Register 9.11.	

3) PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame has been defined. A new ASYMMETRIC PAUSE control frame was defined in IEEE 802.3ab.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting ANAR Register 4, bits10 and 11. Link partner PAUSE capabilities can be determined from ANLPAR Register 5, bits 10 and 11. A PHY layer device is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established and is responsible for correct flow control actions thereafter.

7.5.2 Parallel Detection

Auto-negotiation may not be supported by the link partner. In this case the MAE0621A uses the parallel detection function to judge the speed of its partner and operates at half duplex mode only.

The MAE0621A automatically enables the parallel detection and does not need the additional configuration.

7.6 Crossover detection and auto-correction

Crossover detection and auto-correction can adapt crossover cables between devices, such as two computers connect with CAT.5 Ethernet cable. The initial state is MDI mode, if no link is established in a certain time, it will switch to crossover mode and repeat the process until the link is established.

When the MAE0621A interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the MAE0621A follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the MAE0621A uses signal detect to determine whether or not to crossover. Refer to Page 0xA43, Register 0x18 for manual configuration of crossover function.

7.7 Polarity correction

The MAE0621A automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T mode. In 100BASE-TX mode, the polarity is irrelevant.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

7.8 PHY Reset

PHYRSTB pin is used to reset the chip. When it is asserted low, all registers will restore to default values. For a complete reset, it should be asserted low for at least 10ms and wait for at least 72ms before accessing the PHY register.

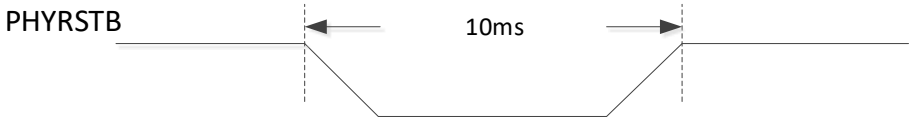


Figure 7-4 PHY Reset Timing

7.9 Hardware Configuration

The I/O pad voltage, interface mode and PHY address can be set by CONFIG pins. Using external pull-high or pull-low resistor to set the CONFIG pins, the configurable functions are shown in Table 7-3.

Table 7-3 CONFIG Pins, Configuration Function Definition

CONFIG PIN	Configuration	description
RXD3	PHYAD[0]	PHYAD[2:0] is used to set PHY address. The MAE0621A supports addresses from 0x01 to address 0x07.
RXC	PHYAD[1]	

RXCTL	PHYAD[2]	
RXD2	PLLOFF	ALDPS Mode PLL Off Configuration 1: Stop PLL when entering ALDPS mode. (connecting 4.7kΩ to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode. (connecting 4.7kΩ to GND)
RXD1	TXDLY	RGMII Transmit Clock Timing Control 1: Add 2ns delay to TXC for TXD latching. (connecting 4.7kΩ to DVDD_RG) 0: No delay. (connecting 4.7kΩ to GND)
RXD0	RXDLY	RGMII Receive Clock Timing Control 1: Add 2ns delay to RXC for RXD latching. (connecting 4.7kΩ to DVDD_RG) 0: no delay. (connecting 4.7kΩ to GND)
LED0	CFG_EXT	RGMII I/O Pad External Power Source Mode Configuration 1: Use the external power source for the RGMII I/O pad. (connecting 4.7kΩ to 3.3V) 0: Use the integrated LDO to transform the desired voltage for the RGMII I/O pad. (connecting 4.7kΩ to GND)
LED1	CFG_LDO[0]	LDO Output Voltage Selection for the RGMII I/O pad or External power Source Voltage Selection for the RGMII I/O pad When CFG_EXT pin = 0, CFG_LDO[1:0] represent LDO output voltage setting for the RGMII I/O pad. (0 means connecting 4.7kΩ to GND; 1 means connecting 4.7kΩ to 3.3V) 00: reserved 01: 2.5V 10: 1.8V 11: 1.5V When CFG_EXT pin = 1, CFG_LDO[1:0] represent external power voltage selection for the RGMII I/O pad 00: 3.3V 01: 2.5V 10: 1.8V 11: 1.5V
LED2	CFG_LDO[1]	

7.10 LED and LDO Configuration

The LED pins are multiplexed with CFG_EXT and CFG_LDO [1:0] to reduce the pin count of the MAE0621A. As the Hardware Configuration shares the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. When the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding CFG_EXT/CFG_LDO[1:0] inputs upon power-on-reset.

As Table 7-1 (left side) shows, when a given CFG_EXT/CFG_LDO[1:0] inputs are pulled high then the corresponding LED outputs will be configured as an active low driver. On the right side, when a given CFG_EXT/CFG_LDO[1:0] inputs are pulled down then the corresponding output will be configured as an active high driver.

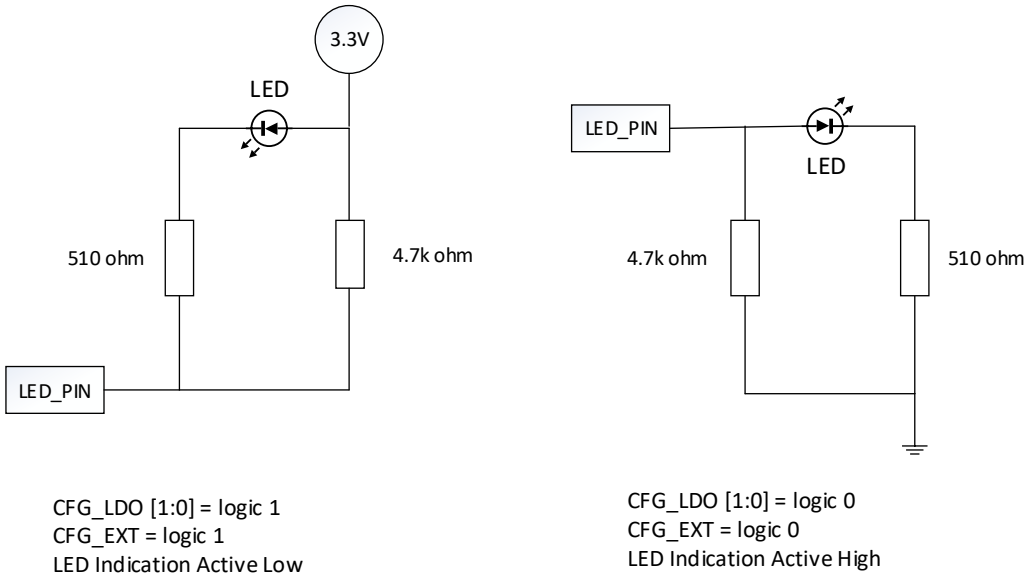


Figure 7-5 LED and LDO Configuration

7.11 LED Configuration

The MAE0621A has three led pins which are called LED0, LED1 and LED2. The led pins can be driven for multiple types of applications by setting Register 16 in Page 0xd04. The register table is shown in Table 7-4.

Table 7-4 LED Register Table

	Link Speed			Active (TX/RX)
	10Mbps	100Mbps	1000Mbps	
LED0	Register 16 Bit0	Register 16 Bit1	Register Bit3	Register 16 Bit4
LED1	Register 16 Bit5	Register 16 Bit6	Register 16 Bit8	Register 16 Bit9
LED2	Register 16 Bit10	Register 16 Bit11	Register 16 Bit13	Register 16 Bit14

Two LED configuration modes are provided by the PHY and each mode has 16 configuration types (See Table 7-5 for Mode A and Table 7-6 for Mode B). To switch between these two modes, set Page 0xd04, Register 16, bit [15] to 0 (Mode A) or 1 (Mode B).

Table 7-5 LED Configuration Table – Mode A

Pin	Link Bit			Active (TX/RX)	Description
	10Mbps	100Mbps	1000Mbps		
LED0 LED1 LED2	0	0	0	0	N/A
	0	0	0	1	N/A
	0	0	1	0	Link 1000Mbps
	0	0	1	1	Link 1000Mbps + Active 1000Mbps
	0	1	0	0	Link 100Mbps
	0	1	0	1	Link 100Mbps + Active 100Mbps
	0	1	1	0	Link 100/1000Mbps

	0	1	1	1	Link 100/1000Mbps + Active 100/1000 Mbps
	1	0	0	0	Link 10Mbps
	1	0	0	1	Link 10Mbps + Active 10Mbps
	1	0	1	0	Link 10/1000Mbps
	1	0	1	1	Link 10/1000Mbps + Active 10/1000Mbps
	1	1	0	0	Link 10/100Mbps
	1	1	0	1	Link 10/100Mbps + Active 10/100Mbps
	1	1	1	0	Link 10/100/1000Mbps
	1	1	1	1	Link 10/100/1000Mbps + Active 10/100/1000Mbps

Table 7-6 LED Configuration Table – Mode B

Pin	Link Bit			Active	Description
	10Mbps	100Mbps	1000Mbps	(TX/RX)	
LED0 LED1 LED2	0	0	0	0	N/A
	0	0	0	1	Active 10/100/1000Mbps
	0	0	1	0	Link 1000Mbps
	0	0	1	1	Link 1000 Mbps + Active 10/100/1000Mbps
	0	1	0	0	Link 100Mbps
	0	1	0	1	Link 100Mbps + Active 10/100/1000Mbps
	0	1	1	0	Link 100/1000Mbps
	0	1	1	1	Link 100/1000 Mbps + Active 10/100/1000Mbps
	1	0	0	0	Link 10Mbps
	1	0	0	1	Link 10Mbps + Active 10/100/1000Mbps
	1	0	1	0	Link 10/1000Mbps
	1	0	1	1	Link 10/1000Mbps + Active 10/100/1000Mbps
	1	1	0	0	Link 10/100Mbps
	1	1	0	1	Link 10/100Mbps + Active 10/100/1000Mbps
	1	1	1	0	Link 10/100/1000Mbps
	1	1	1	1	Link 10/100/1000Mbps + Active 10/100/1000Mbps

The default configuration LED pins is shown as Table 7-7.

Table 7-7 LED Default Definitions

Pin	Description
LED0	10Mbps Link and Active (Transmitting or Receiving)
LED1	100Mbps Link and Active (Transmitting or Receiving)
LED2	1000Mbps Link and Active (Transmitting or Receiving)

7.12 INTB/PMEB Pin Usage

The INTB/PMEB pin is designed to indicate interrupt and WOL events. When Page 0xd40, Register 22, bit [5] = 0, it is used for INTB; when Page 0xd40, Register 22, bit [5] = 1, it is used for PMEB. The default mode of this pin is INTB.

When WOL events occurs, PMEB will be triggered. The interrupts can be individually enabled or disabled by setting Register INER (Page0, Address, 0x12, bit [7]).

If the pin is worked in INTB mode, the Pulse Low waveform format is not supported. It will output an active low level when PHY status change. All interrupt conditions are represented by the read-only general status register INSR (Page 0x043, Address 0x1d). The interrupts can be individually enabled or disabled by setting Register INER (Page 0xA42, Address 0x12).

7.13 Wake-On-LAN (WOL) Event

The MAE0621A can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; ‘B’ means low active) pin when such a packet or event occurs. Then the system can be restored to a normal operation state.

The MAE0621A supports 6-byte verification password for magic packet. In any part of a valid Ethernet packet, the matched magic packet format should be: Misc. + 6*FF + 16*DID (Destination ID) + password (Option) + Misc.

8 Register Description

8.1 Register Access Types

Table 8-1 Register Access Types

Type	Description
LH	Latch high. If the status is high, this field is set to '1' and remains set.
RC	Read-cleared. The register field is cleared after read.
RO	Read only.
RW	Read and Write.
SC	Self-cleared. Writing a '1' to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0'.

8.2 Register Mapping and Definitions

Table 8-2 Register Mapping and Definitions

Page	Offset	Access	Name	Description
0	0	RW	BMCR	Basic Mode Control Register
0	1	RO	BMSR	Basic Mode Status Register
0	4	RW	ANAR	Auto-Negotiation Advertising Register
0	5	RO	ANLPAR	Auto-Negotiation Link Partner Ability Register
0	6	RO	ANER	Auto-Negotiation Expansion Register
0	7	RW	ANNPTR	Auto-Negotiation Next Page Transmit Register
0	8	RO	ANNPRR	Auto-Negotiation Next Page Receive Register
0	9	RW	GBCR	1000BASE-T Control Register
0	10	RO	GBSR	1000BASE-T Status Register
0	11~12	RO	RSVD	Reserved
0	13	WO	MACR	MMD Access Control Register
0	14	RW	MAADR	MMD Access Address Data Register
0	15	RO	GBESR	1000BASE-T Extended Status Register
0xA42	16~17	RO	RSVD	Reserved
0xA42	18	RW	INER	Interrupt Enable Register
0xA42	19~23	RO	RSVD	Reserved
0xA43	24	RW	PHYCR1	PHY Specific Control Register 1
0xA43	25	RW	PHYCR2	PHY Specific Control Register 2
0xA43	26	RO	PHYSR	PHY Specific Status Register
0xA43	27~28	RO	RSVD	Reserved
0xA43	29	RO	INSR	Interrupt Status Register
0xA43	30	RO	RSVD	Reserved
0xA43	31	RW	PAGSR	Page Select Register
0xA46	20	RW	PHYSCR	PHY Special Configure Register
0xD04	16	RW	LCR	LED Control Register
0xD04	17	RW	EEELCR	EEE LED Control Register
0xD08	21	RW	MIICR	MII Control Register
0xD40	22	RW	INTBCR	INTB Pin Control Register

Note 1: To access the IEEE Standard Registers 0 to 15, the Page Select Register (PAGSR, Register 31) should be set as '0' or '0xA42'(default value).

Note 2: For example, to switch to Page 0xD04, set Register 31 Data=0x0D04 (change to Page 0xD04). After LED setting, switch back to the PHY's IEEE Standard Registers, i.e. Page 0 or Page 0xA42 (Register 31 Data = 0 or 0xA42).

8.3 MMD Register Mapping and Definitions

Table 8-3 MMD Register Mapping and Definitions

Device	Offset	Access	Name	Description
3	0	RW	PC1R	PCS Control 1 Register
3	1	RW	PS1R	PCS Status 1 Register
3	20	RO	EEECR	EEE Capability Register
3	22	RC	EEEWER	EEE Wake Error Register
7	60	RW	EEEAR	EEE Advertisement Register
7	61	RO	EEELPAR	EEE Link Partner Ability Register

8.4 Register Tables

8.4.1 BMCR (Basic Mode Control Register, Address 0x00)

Table 8-4 BMCR (Basic Mode Control Register, Address 0x00)

<table>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Default</th><th>Description</th></tr>
<tr><td>0.15</td><td>Reset</td><td>RW, SC</td><td>0</td><td>Reset.
1: PHY reset
0: Normal operation
Register 0 (BMCR) and Register 1 (BMSR) will return to default values after a software reset. This action may change the internal PHY state and the state of the physical link associated with the PHY.</td></tr>
<tr><td>0.14</td><td>Loopback</td><td>RW</td><td>0</td><td>Loopback Mode.
1: Enable PCS loopback mode
0: Disable PCS loopback mode
The loopback function enables RGMII transmit data to be routed to the RGMII receive data path</td></tr>
<tr><td>0.13</td><td>Speed[0]</td><td>RW</td><td>0</td><td>Speed Select Bit 0.
In forced mode, i.e., when Auto-Negotiation is disabled, bits 0.6 and 0.13 determine the selection of device speed.
<table>
<tr><th>Speed[1]</th><th>Speed[0]</th><th>Speed Enabled</th></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1000Mbps</td></tr>
<tr><td>0</td><td>1</td><td>100Mbps</td></tr>
<tr><td>0</td><td>0</td><td>10Mbps</td></tr>
</table></td></tr>
<tr><td>0.12</td><td>ANE</td><td>RW</td><td>1</td><td>Auto-Negotiation Enable.
1: Enable Auto-Negotiation
0: Disable Auto-Negotiation</td></tr>
</table>

Bit	Name	Type	Default	Description
0.11	PWD	RW	0	Power Down. 1: Power down (only Management Interface and logic are active; link is down.) 0: Normal operation
0.10	Isolate	RW	0	Isolate. 1: RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the MAE0621A ignores TXD[3:0] and TXCTL inputs, presents a high impedance on RXC, RXCTL, RXD[3:0]. 0: Normal operation
0.9	Restart_AN	RW, SC	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation
0.8	Duplex	RW	1	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode.
0.7	Collision Test	RW	0	Collision Test. 1: Enable the collision test mode 0: Disable the collision test mode
0.6	Speed[1]	RW	1	Speed Select Bit 1. Work in conjunction with bit 13.
0.5	Uni-directional enable	RW	0	Uni-Directional Enable. 1: Enable packet transmit regardless of whether the PHY has determined that a valid link has been established. 0: Packet transmit permitted when the PHY determined that a valid link has been established.
0.4:0	RSVD	RO	00000	Reserved

Note 1: Changes to Registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power-down to normal operation.
Note 2: Auto-Negotiation is enabled when speed is set to 1000BASE-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6 and 0.8. Otherwise, Register 4, bit[8:5] and Register 9, bit[9:8] take effect.
Note 3: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.

8.4.2 BMSR (Basic Mode Status Register, Address 0x01)

Table 8-5 BMSR (Basic Mode Status Register, Address 0x01)

Bit	Name	Type	Default	Description
1.15	100BASE-T4	RO	0	100BASE-T4 Capability. The MAE0621A does not support 100BASE-T4 mode. This bit should always be 0.

Bit	Name	Type	Default	Description
1.14	100BASE-TX (full)	RO	1	100BASE-TX Full Duplex Capability. 1: Device is able to perform 100BASE-TX in full duplex mode 0: Device is not able to perform 100BASE-TX in full duplex mode
1.13	100BASE-TX (half)	RO	1	100BASE-TX Half Duplex Capability. 1: Device is able to perform 100BASE-TX in half duplex mode 0: Device is not able to perform 100BASE-TX in half duplex mode
1.12	10BASE-T (full)	RO	1	10BASE-T Full Duplex Capability. 1: Device is able to perform 10BASE-T in full duplex mode 0: Device is not able to perform 10BASE-T in full duplex mode
1.11	10BASE-T (half)	RO	1	10BASE-T Half Duplex Capability. 1: Device is able to perform 10BASE-T in half duplex mode 0: Device is not able to perform 10BASE-T in half duplex mode
1.10	10BASE-T2 (full)	RO	0	10BASE-T2 Full Duplex Capability. The MAE0621A does not support 10BASE-T2 mode. This bit should always be 0
1.9	10BASE-T2 (half)	RO	0	10BASE-T2 Half Duplex Capability. The MAE0621A does not support 10BASE-T2 mode. This bit should always be 0
1.8	1000BASE-T Extended Status	RO	1	1000BASE-T Extended Status Register. 1: Device supports Extended Status Register 15 Always set to 1.
1.7	Uni-directional ability	RO	0	Uni-directional ability. 1: PHY able to transmit from RGMII regardless of whether the PHY has determined that a valid link has been established. 0: PHY only able to transmit from RGMII only when the PHY determined that a valid link has been established.
1.6	Preamble Suppression	RO	1	Preamble Suppression Capability. 0: PHY will not accept management frames with preamble suppressed. 1: PHY will accept management frames with preamble suppressed.
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid. 0: Auto-Negotiation process not complete.
1.4	Remote Fault	RC, LH	0	Remote Fault.

Bit	Name	Type	Default	Description
				1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner. 0: No remote fault condition detected.
1.3	Auto-Negotiation Ability	RO	1	Auto-negotiation capability. 1: Device is able to perform auto-negotiation. 0: Device is not able to perform auto-negotiation.
1.2	Link Status	RO	0	Link Status. 1: Link is up. 0: Link is down. This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read Page 0xA43 Register 26, bit[2] Link (Real Time).
1.1	Jabber Detect	RC, LH	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1.

8.4.3 ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Table 8-6 ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	Type	Default	Description
4.15	NextPage	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved
4.13	Remote Fault	RW	0	1: Set Remote Fault bit 0: Do not set remote fault bit
4.12	RSVD	RO	0	Reserved
4.11	Asymmetric PAUSE	RW	0	1: Advertise asymmetric pause 0: Advertise no asymmetric pause
4.10	PAUSE	RW	0	1: Advertise support of pause frames 0: No pause frames
4.9	100BASE-T4	RO	0	1: 100BASE-T4 support 0: 100BASE-T4 not supported
4.8	100BASE-TX (Full)	RW	1	1: Advertise support of 100BASE-TX full-duplex mode 0: Not advertised
4.7	100BASE-TX (Half)	RW	1	1: Advertise support of 100BASE-TX half-duplex mode 0: Not advertised
4.6	10BASE-T (Full)	RW	1	1: Advertise support of 10BASE-TX full-duplex mode 0: Not advertised

Bit	Name	Type	Default	Description
4.5	10BASE-T (Half)	RW	1	1: Advertise support of 10BASE-TX half-duplex mode 0: Not advertised
4.4:0	Selector Field	RO	00001	Indicates IEEE 802.3

Note 1: The setting of Register 4 has no effect unless Auto-Negotiation is restarted or the link goes down, i.e., software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.
Note 2: If 1000BASE-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.

8.4.4 ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 8-7 ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	Type	Default	Description
5.15	Next Page	RO	0	Next Page Indication. 1: Link partner has Next Page ability. 0: Link partner does not have Next Page ability.
5.14	ACK	RO	0	Acknowledge. 1: Link partner has received link code word. 0: Link partner has not received link code word.
5.13	Remote Fault	RO	0	Remote Fault indicated by Link Partner. 1: Link partner has detected remote fault. 0: Link partner has not detected remote fault.
5.12	RSVD	RO	0	Reserved
5.11:5	Technology Ability Field	RO	0000000	Received Code Word Bit 11:5.
5.4:0	Selector Field	RO	00000	Received Code Word Bit 4:0.

Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates it is completed.

8.4.5 ANER (Auto-Negotiation Expansion Register, Address 0x06)

Table 8-8 ANER (Auto-Negotiation Expansion Register, Address 0x06)

Bit	Name	Type	Default	Description
6.15:5	RSVD	RO	0x000	Reserved
6.4	Parallel Detection Fault	RC, LH	0	1: A fault has been detected via the Parallel Detection function. 0: The fault has not been detected via the Parallel Detection function.
6.3	Link Partner Next Page Able	RO	0	1: Link Partner has Next Page capability. 0: Link Partner does not have Next Page capability.
6.2	Local Next Page Able	RO	1	1: Local Device is able to send Next Page. Always 1.
6.1	Page Received	RC, LH	0	1: A New Page has been received from link partner.

Bit	Name	Type	Default	Description
				0: A New Page has not been received.
6.0	Link Partner Auto-Negotiation capable	RO	0	1: Link Partner supports Auto-Negotiation. 0: Link Partner does not support Auto-Negotiation.

Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates it is completed.

8.4.6 ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Table 8-9 ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Bit	Name	Type	Default	Description
7.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
7.14	RSVD	RO	0	Reserved
7.13	Message Page	RW	1	0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
7.12	Acknowledge 2	RW	0	0: Cannot comply with the message received. 1: Comply with the message received. Transmit Code Word Bit 12.
7.11	Toggle	RO	0	Toggle Bit Transmit Code Word Bit 11.
7.10:0	Message/Unformatted Field	RW	0x001	Content of Message/Unformatted Page Transmit Code Word Bit 10:0.

8.4.7 ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Table 8-10 ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Bit	Name	Type	Default	Description
8.15	Next Page	RO	0	1: Additional next pages follow 0: Sending last next page Received Link Code Word Bit 15.
8.14	Acknowledge	RO	0	1: Acknowledge 0: No acknowledge Received Link Code Word Bit 14.
8.13	Message Page	RO	0	1: Formatted page 0: Unformatted page Received Link Code Word Bit 13.
8.12	Acknowledge 2	RO	0	1: Comply with message 0: Cannot comply with message Received Link Code Word Bit 12.
8.11	Toggle	RO	0	Toggle Bit. Received Link Code Word Bit 11.

Bit	Name	Type	Default	Description
8.10:0	Message/Unformatted Field	RO	0x00	Content of Message/Unformatted Page. Received Link Code Word Bit 10:0.

Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates it is completed.

8.4.8 GBCR (1000BASE-T Control Register, Address 0x09)

Table 8-11 GBCR (1000BASE-T Control Register, Address 0x09)

Bit	Name	Type	Default	Description
9.15:13	Test Mode	RW	000	Test Mode Select. 000: Normal Mode 001: Test Mode 1 - Transmit Waveform Test¨ 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved
9.12	MASTER/SLAVE Manual Configuration Enable	RW	0	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE configuration
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
9.10	Port Type	RW	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)
9.9	1000BASE-T Full Duplex	RW	1	1: Advertise 1000BASE-T full-duplex capability 0: Advertise no 1000BASE-T full-duplex capability
9.8	RSVD	RO	0	Reserved
9.7:0	RSVD	RO	0x00	Reserved

Note 1: Values set in register 9.12:9 have no effect unless Auto-Negotiation is restarted (Register 0.9) or the link goes down.
Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12=0.

8.4.9 GBSR (1000BASE-T Status Register, Address 0x0A)

Table 8-12 GBSR (1000BASE-T Status Register, Address 0x0A)

Bit	Name	Type	Default	Description
10.15	MASTER/SLAVE Configuration Fault	RO, RC, LH	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected

Bit	Name	Type	Default	Description
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local transmitter is MASTER 0: Local transmitter is SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local receiver OK 0: Local receiver not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote receiver OK 0: Remote receiver not OK
10.11	Link Partner 1000BASE-T Full Duplex Capability	RO	0	Link Partner 1000BASE-T Full Duplex Capability. 1: Link partner is capable of 1000BASE-T full duplex 0: Link partner is not capable of 1000BASE-T full duplex
10.10	Link Partner 1000BASE-T Half Duplex Capability	RO	0	Link Partner 1000BASE-T Half Duplex Capability. 1: Link partner is capable of 1000BASE-T half duplex 0: Link Partner is not capable of 1000BASE-T half duplex
10.9:8	RSVD	RO	00	Reserved
10.7:0	Idle Error Count	RO	0x00	Idle Error Counter. The counter stops automatically when it reaches 0xff.

Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.
Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

8.4.10 MACR (MMD Access Control Register, Address 0x0D)

Table 8-13 MACR (MMD Access Control Register, Address 0x0D)

Bit	Name	Type	Default	Description
13.15:14	Function	WO	00	00: Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	0x000	Reserved
13.4:0	DEVAD	WO	0x00	Device Address.

Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.
Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.
Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.

8.4.11 MAADR (MMD Access Address Data Register, Address 0x0E)

Table 8-14 MAADR (MMD Access Address Data Register, Address 0x0E)

Bit	Name	Type	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14 = 00 ▪ MMD DEVAD's address register 13.15:14 = 01, 10, or 11 ▪ MMD DEVAD's data register as indicated by the contents of its address register

Note: This register is used in conjunction with the MACR (Register 13; Table 8-13) to provide access to the MMD address space.

8.4.12 GBESR (1000BASE-T Extended Status Register, Address 0x0F)

Table 8-15 GBESR (1000BASE-T Extended Status Register, Address 0x0F)

Bit	Name	Type	Default	Description
15.15	1000BASE-X FD	RO	0	0: Not 1000BASE-X full duplex capable
15.14	1000BASE-X HD	RO	0	0: Not 1000BASE-X half duplex capable
15.13	1000BASE-T FD	RO	1	1: 1000BASE-T full duplex capable
15.12	1000BASE-T HD	RO	0	0: Not 1000BASE-T half duplex capable
15.11:0	RSVD	RO	0x000	Reserved

8.4.13 INER (Interrupt Enable Register, Page 0xA42, Address 0x12)

Table 8-16 INER (Interrupt Enable Register, Page 0xA42, Address 0x12)

Bit	Name	Type	Default	Description
18.15:11	RSVD	RO	00000	Reserved
18.10	Jabber Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[10] always reflects the jabber interrupt behavior.
18.9	ALDPS State Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the ALDPS state change interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[9] always reflects the ALDPS state change interrupt behavior.
18.8	RSVD	RO	0	Reserved
18.7	PME (Power Management Event of WOL)	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PME interrupt event in the INTB pin. Page 0xA43, Reg29 Bit[7] always reflects the PME interrupt behavior.

Bit	Name	Type	Default	Description
18.6	RSVD	RO	0	Reserved
18.5	PHY Register Accessible Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PHY register access interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[5] always reflects the PHY register access interrupt behavior.
18.4	Link Status Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the link status change interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[4] always reflects the link change interrupt behavior.
18.3	Auto-Negotiation Completed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto-negotiation completed interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[3] always reflects the auto-negotiation completed interrupt behavior.
18.2	Page Received Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the page received interrupt event in the INTB pin. Page 0xa43, Register 29 Bit[2] always reflects the page received interrupt behavior.
18.1	RSVD	RO	0	Reserved
18.0	Auto Negotiation Error Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto negotiation error interrupt event in the INTB pin. Page 0xA43, Register 29 Bit[0] always reflects the auto-negotiation error interrupt behavior.

8.4.14 PHYCR1 (PHY Specific Control Register 1, Page 0xA43, Address 0x18)

Table 8-17 PHYCR1 (PHY Specific Control Register 1, Page 0xA43, Address 0x18)

Bit	Name	Type	Default	Description
24.15:14	RSVD	RO	00	Reserved
24.13	PHYAD_0 Enable	RW	1	1: A broadcast from MAC (A command with PHY address = 0) is valid. MDC/MDIO will respond to this command.
24.12	RSVD	RO	0	Reserved
24.11:10	RSVD	RO	00	Reserved

Bit	Name	Type	Default	Description
24.9	MDI Mode Manual Configuration Enable	RW	0	1: Enable Manual Configuration of MDI mode
24.8	MDI Mode	RW	1	Set the MDI/MDIX mode. 1: MDI 0: MDIX This bit will take effect only when Bit 24.9 = 1.
24.7	TX CRS Enable	RW	0	1: Assert CRS on transmit 0: Never assert CRS on transmit
24.6	PHYAD Non-zero Detect	RW	0	1: The MAE0621A with PHYAD[2:0] = 000 will latch the first non-zero PHY address as its own PHY address
24.5	RSVD	RO	0	Reserved
24.4	Preamble Check Enable	RW	1	1: Check preamble when receiving an MDC/MDIO command 0: Do not check preamble
24.3	Jabber Detection Enable	RW	1	1: Enable Jabber Detection
24.2	ALDPS Enable	RW	0	1: Enable Link Down Power Saving Mode
24.1	ALDPS PLL OFF Enable	RW	0	1: Enable PLL off when in ALDPS mode (valid when Bit 24.2= 1)
24.0	RSVD	RO	0	Reserved

Note: The method to disable auto crossover and force MDI or MDIX mode is as follows:
Step 1: Set Bit 24.9=1 (Manual Configuration of MDI mode) and set Bit24.8=1 (MDI) or 0 (MDIX).
Step 2: Perform a PHY reset, i.e., set Page 0, Register 0 bit[15]=1.

8.4.15 PHYCR2 (PHY Specific Control Register 2, Page 0xA43, Address 0x19)

Table 8-18 PHYCR2 (PHY Specific Control Register 2, Page 0xA43, Address 0x19)

Bit	Name	Type	Default	Description
25.15:14	RSVD	RO	00	Reserved
25.13:12	CLKOUT SSC Capability	RW	00	CLKOUT SSC Capability Select. 00: Normal CLKOUT 11: CLKOUT with SSC capability Others: Reserved
25.11	CLKOUT Frequency Select	RW	0	Frequency Select of the CLKOUT Pin Clock Output. 0: 25MHz 1: 125MHzs
25.10:8	RSVD	RO	000	Reserved
25.7	CLKOUT SSC Enable	RW	0	1: Enable Spread-Spectrum Clocking (SSC) on CLKOUT output clock.
25.6	RSVD	RO	0	Reserved
25.5	RSVD	RO	1	Reserved
25.4	RSVD	RO	0	Reserved

Bit	Name	Type	Default	Description
25.3	RSVD	RO	0	Reserved
25.2	RSVD	RO	0	Reserved
25.1	RXC Enable	RW	1	1: RXC Clock Output Enabled.
25.0	CLKOUT Enable	RW	1	1: CLKOUT Clock Output Enabled.

Note 1: A PHY reset should be issued (set Page 0, Register 0, bit[15]=1) after setting these bits in PHYCR2 register.

8.4.16 PHYSR (PHY Specific Status Register, Page 0xA43, Address 0x1A)

Table 8-19 PHYSR (PHY Specific Status Register, Page 0xA43, Address 0x1A)

Bit	Name	Type	Default	Description
26.15	RSVD	RO	0	Reserved
26.14	ALDPS State	RO	0	Link Down Power Saving Mode. 1: Reflects local device entered Link Down Power Saving Mode, i.e., cable is not plugged in (reflected after 3 sec). 0: With cable plugged in
26.13	RSVD	RO	0	Reserved
26.12	Auto-Negotiation Enable	RO	1	Auto Negotiation Status. 1: Enable 0: Disable
26.11	Master Mode	RO	0	Device is in Master/Slave Mode. 1: Master mode 0: Slave mode
26.10:9	RSVD	RO	00	Reserved
26.8	EEE capability	RO	0	1: Both local and link-partner have EEE capability of current speed.
26.7	Rxflow Enable	RO	0	Rx Flow Control. 1: Enable 0: Disable
26.6	Txflow Enable	RO	0	Tx Flow Control. 1: Enable 0: Disable
26.5:4	Speed	RO	11	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
26.3	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
26.2	Link (Real Time)	RO	0	Real Time Link Status. 1: Link is OK 0: Link is not OK
26.1	MDI Crossover Status	RO	0	MDI/MDI Crossover Status. 1: MDI Crossover

Bit	Name	Type	Default	Description
				0: MDI
26.0	Jabber (Real Time)	RO	0	Real Time Jabber Indication. 1: Jabber Indication 0: No Jabber Indication

Note 1: Bit 26.11 valid only when in Gigabit mode.

8.4.17 INSR (Interrupt Status Register, Page 0xA43, Address 0x1D)

Table 8-20 INSR (Interrupt Status Register, Page 0xA43, Address 0x1D)

Bit	Name	Type	Default	Description
29.15:11	RSVD	RO	00000	Reserved
29.10	Jabber	RO, RC	0	1: Jabber detected 0: No jabber detected
29.9	ALDPS State Change	RO, RC	0	1: ALDPS state changed 0: ALDPS state not changed
29.8	RSVD	RO	0	Reserved
29.7	PME (Power Management Event of WOL)	RO, RC	0	1: WOL event occurred 0: WOL event did not occur
29.6	RSVD	RO	0	Reserved
29.5	PHY Operation Status	RO, RC	0	1: Normal Operation 0: Abnormal
29.4	Link Status Change	RO, RC	0	1: Link status changed 0: Link status not changed
29.3	Auto-Negotiation Completed	RO, RC	0	1: Auto-Negotiation is completed 0: Auto-Negotiation is not completed
29.2	Page Received	RO, RC	0	1: Page received 0: Page not received
29.1	RSVD	RO	0	Reserved
29.0	Auto-Negotiation Error	RO, RC	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error

8.4.18 PHYSCR (PHY Special Configure Register, Page 0xA46, Address 0x14)

Table 8-21 PHYSCR (PHY Special Configure Register, Page 0xA46, Address 0x14)

Bit	Name	Type	Default	Description
20.15:2	RSVD	RO	0x0000	Reserved
20.1	PHY Special Configure Done	RW	0	1: Write 1 to indicate the special PHY parameter configuration has been done.
20.0	RSVD	RO	0	Reserved

8.4.19 LCR (LED Control Register, Page 0xD04, Address 0x10)

Table 8-22 LCR (LED Control Register, Page 0xD04, Address 0x10)

Bit	Name	Type	Default	Description
16.15	LED_MODE	RW	0	0: LED Mode A is selected. 1: LED Mode B is selected.
16.14	LED2_ACT	RW	1	LED2 Active (Transmitting or Receiving) Indication
16.13	LED2_LINK_1000	RW	1	LED2 Link Indication: 1000Mbps
16.12	RSVD	RO	0	Reserved
16.11	LED2_LINK_100	RW	0	LED2 Link Indication: 100Mbps
16.10	LED2_LINK_10	RW	0	LED2 Link Indication: 10Mbps
16.9	LED1_ACT	RW	1	LED1 Active (Transmitting or Receiving) Indication
16.8	LED1_LINK_1000	RW	0	LED1 Link Indication: 1000Mbps
16.7	RSVD	RO	0	Reserved
16.6	LED1_LINK_100	RW	1	LED1 Link Indication: 100Mbps
16.5	LED1_LINK_10	RW	0	LED1 Link Indication: 10Mbps
16.4	LED0_ACT	RW	1	LED0 Active (Transmitting or Receiving) Indication
16.3	LED0_LINK_1000	RW	0	LED0 Link Indication: 1000Mbps
16.2	RSVD	RO	0	Reserved
16.1	LED0_LINK_100	RW	0	LED0 Link Indication: 100Mbps
16.0	LED0_LINK_10	RW	1	LED0 Link Indication: 10Mbps

8.4.20 EEELCR (EEE LED Control Register, Page 0xD04, Address 0x11)

Table 8-23 EEELCR (EEE LED Control Register, Page 0xD04, Address 0x11)

Bit	Name	Type	Default	Description
17.15:4	RSVD	RO	0x000	Reserved
17.3	LED2 EEE Enable	RW	1	1: Enable EEE LED indication of LED2.
17.2	LED1 EEE Enable	RW	1	1: Enable EEE LED indication of LED1.
17.1	LED0 EEE Enable	RW	1	1: Enable EEE LED indication of LED0.
17.0	RSVD	RO	0	Reserved

8.4.21 MIICR (MII Control Register, Page 0xD08, Address 0x15)

Table 8-24 MIICR (MII Control Register, Page 0xD08, Address 0x15)

Bit	Name	Type	Default	Description
21.15:7	RSVD	RO	0x000	Reserved
21.6	RGMII In-band CRS Enable	RW	0	1: Enable in-band CRS Status in RGMII Rx flow
21.5:0	RSVD	RO	0x00	Reserved

8.4.22 INTBCR (INTB Pin Control Register, Page 0xD40, Address 0x16)

Table 8-25 INTBCR (INTB Pin Control Register, Page 0xD40, Address 0x16)

Bit	Name	Type	Default	Description
22.15:6	RSVD	RO	0x000	Reserved
22.5	INTB/PMEB Selection	RW	0	Pin 31 of the MAE0621A functions as: 1: PMEB 0: INTB
22.4:0	RSVD	RO	0x00	Reserved

8.4.23 PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Table 8-26 PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bit	Name	Type	Default	Description
3.0.15:11	RSVD	RO	0x00	Reserved
3.0.10	Clock Stop Enable	RW	0	1: PHY stops RXC when receiving LPI 0: RXC not stoppable
3.0.9:0	RSVD	RO	0x000	Reserved

8.4.24 PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

Table 8-27 PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

Bit	Name	Type	Default	Description
3.1.15:12	RSVD	RO	0x0	Reserved
3.1.11	TX LPI Received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3.1.10	RX LPI Received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received
3.1.9	TX LPI Indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3.1.8	RX LPI Indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3.1.7	RSVD	RO	0	Reserved
3.1.6	Clock Stop Capable	RO	1	1: MAC stops TXC in LPI 0: TXC is not stoppable
3.1.5:0	RSVD	RO	0x00	Reserved

8.4.25 EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Table 8-28 EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Bit	Name	Type	Default	Description
3.20.15:3	RSVD	RO	0x0000	Reserved
3.20.2	1000BASE-T EEE	RO	1	1: EEE is supported for 1000BASE-T EEE 0: EEE is not supported for 1000BASE-T EEE

Bit	Name	Type	Default	Description
3.20.1	100BASE-TX EEE	RO	1	1: EEE is supported for 100BASE-TX EEE 0: EEE is not supported for 100BASE-TX EEE
3.20.0	RSVD	RO	0	Reserved

8.4.26 EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Table 8-29 EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Bit	Name	Type	Default	Description
3.22.15:0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

8.4.27 EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3C)

Table 8-30 EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3C)

Bit	Name	Type	Default	Description
7.60.15:3	RSVD	RO	0x0000	Reserved
7.60.2	1000BASE-T EEE	RW	0	Advertise 1000BASE-T EEE Capability. 1: Advertise 0: Do not advertise
7.60.1	100BASE-TX EEE	RW	0	Advertise 100BASE-TX EEE Capability. 1: Advertise 0: Do not advertise
7.60.0	RSVD	RO	0	Reserved

8.4.28 EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3D)

Table 8-31 EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3D)

Bit	Name	Type	Default	Description
7.61.15:3	RSVD	RO	0x0000	Reserved
7.61.2	LP 1000BASE-T EEE	RO	0	1: Link Partner is capable of 1000BASE-T EEE 0: Link Partner is not capable of 1000BASE-T EEE
7.61.1	LP 100BASE-TX EEE	RO	0	1: Link Partner is capable of 100BASE-TX EEE 0: Link Partner is not capable of 100BASE-TX EEE
7.61.0	RSVD	RO	0	Reserved

9 Regulators and Power Sequence

9.1 Switching Regulator

The MAE0621A incorporates a switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot.

The switching regulator 1.1V output pin REG_OUT should be connected only to DVDD10 and AVDD10. An X5R/X7R low-ESR ceramic capacitor is required to enhance switching regulator stability.

9.2 Power Sequence

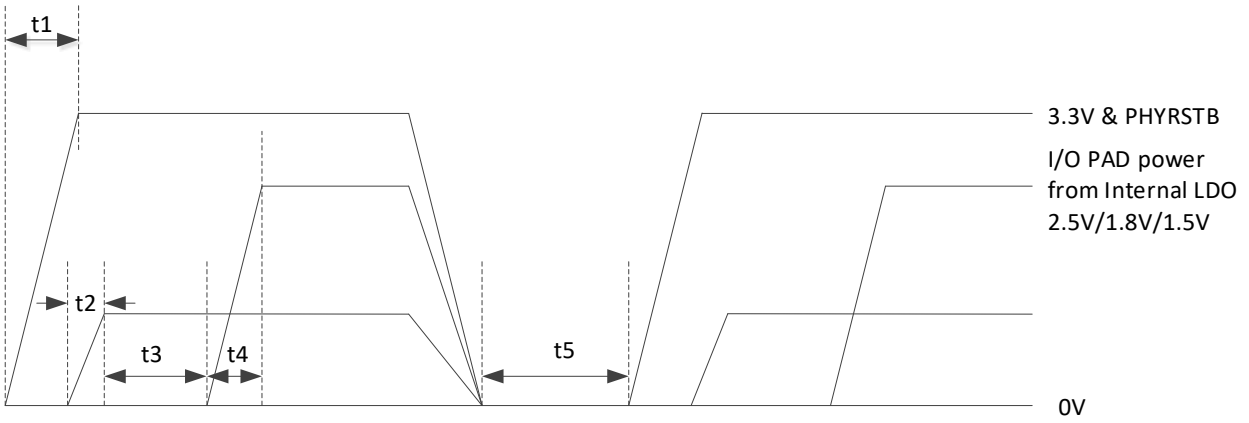


Figure 9-1 Power Sequence (Internal DCDC and Internal LDO)

Table 9-1 Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Unit
t1	3.3V Rise Time	0.5	-	20	ms
t2	DCDC Ready Time	-	-	0.5	ms
t3	Core Logic Ready Time	-	45	-	ms
t4	LDO Ready Time	-	-	3	ms
t5	3.3V Off Time	100	-	-	ms

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Table 10-1 Absolute Maximum Rating

Symbol	Description	Min	Max	Unit
DVDD33, AVDD33	Supply Voltage 3.3V	-0.3	3.6	V
DVDD10, AVDD10	Supply Voltage 1.1V	-0.3	1.2	V
3.3V DVDD_RG	Supply Voltage 3.3V	-0.3	3.6	V
2.5V DVDD_RG	Supply Voltage 2.5V	-0.3	2.8	V
1.8V DVDD_RG	Supply Voltage 1.8V	-0.3	2.0	V
1.5V DVDD_RG	Supply Voltage 1.5V	-0.3	1.7	V
$T_{STORAGE}$	Storage Temperature	-55	+125	℃

Note: These specifications indicate levels where permanent damage to the device can occur. Functionality at or above limits is not guaranteed. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

10.2 Recommended Operation Condition

Table 10-2 Recommended Operation Condition

Symbol	Description	Min	Typical	Max	Unit
DVDD33, AVDD33	Supply Voltage 3.3V	3.14	3.3	3.46	V
DVDD10, AVDD10	Supply Voltage 1.1V	1.05	1.1	1.18	V
3.3V DVDD_RG	Supply Voltage 3.3V	3.14	3.3	3.46	V
2.5V DVDD_RG	Supply Voltage 2.5V	2.38	2.5	2.62	V
1.8V DVDD_RG	Supply Voltage 1.8V	1.71	1.8	1.89	V
1.5V DVDD_RG	Supply Voltage 1.5V	1.43	1.5	1.57	V
T_A	Ambient Operation Temperature (MAE0621A-Q3C)	0	-	70	℃
	Ambient Operation Temperature (MAE0621A-Q3I)	-40	-	85	℃
T_J	Junction Temperature	-	-	125	℃

10.3 25Mz Clock Source Requirement

10.3.1 Crystal Requirements

Table 10-3 Crystal Requirements

Symbol	Description	Min	Typical	Max	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type	-	25	-	MHz
F_{ref} Tolerance	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type, AT-Cut Type. T_a =0℃~70℃.	-50	-	50	ppm

Symbol	Description	Min	Typical	Max	Unit
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	50	Ω
DL	Drive Level.	-	-	0.5	mW
V_{ih} CKTAL	Crystal Output High Level	2.3	-	-	V
V_{il} CKTAL	Crystal Output Low Level	-	-	0.4	V

Note 1: F_{ref} Tolerance +/- 50ppm including effects of aging of the first year, crystal capacitors and PCB layout.

10.3.2 Oscillator/External Clock Requirements

Table 10-4 Oscillator/External Clock Requirements

Symbol	Min	Typical	Max	Unit
Frequency	-	25	-	MHz
Frequency Tolerance	-50	-	50	ppm
Duty Cycle	40	-	60	%
Broadband Peak-to-Peak Jitter	-	-	200	ps
V_{ih}	2.3	-	-	V
V_{il}	-	-	0.4	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns
Operating Temperature	-40	-	85	℃

Note 1: TIE standard deviation <9ps.
Note 2: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitor and PCB layouts.

10.4 DC Characteristics

Table 10-5 DC Characteristics

Symbol	Description	Min	Typical	Max	Unit
Voh(3.3V)	High Level Output Voltage	2.4	-	-	V
Voh(2.5V)	High Level Output Voltage	2.0	-	-	V
Voh(1.8V)	High Level Output Voltage	1.4	-	-	V
Voh(1.5V)	High Level Output Voltage	1.3	-	-	V
Vol(3.3V)	Low Level Output Voltage	-	-	0.4	V
Vol(2.5V)	Low Level Output Voltage	-	-	0.4	V
Vol(1.8V)	Low Level Output Voltage	-	-	0.2	V
Vol(1.5V)	Low Level Output Voltage	-	-	0.2	V
Vih(3.3V)	Input High Voltage	2.0	-	-	V
Vih(2.5V)	Input High Voltage	1.7	-	-	V
Vih(1.8V)	Input High Voltage	1.2	-	-	V
Vih(1.5V)	Input High Voltage	1.0	-	-	V
Vil(3.3V)	Input Low Voltage	-	-	0.8	V
Vil(2.5V)	Input Low Voltage	-	-	0.7	V
Vil(1.8V)	Input Low Voltage	-	-	0.5	V
Vil(1.5V)	Input Low Voltage	-	-	0.3	V

10.5 AC Characteristics

10.5.1 SMI Timing

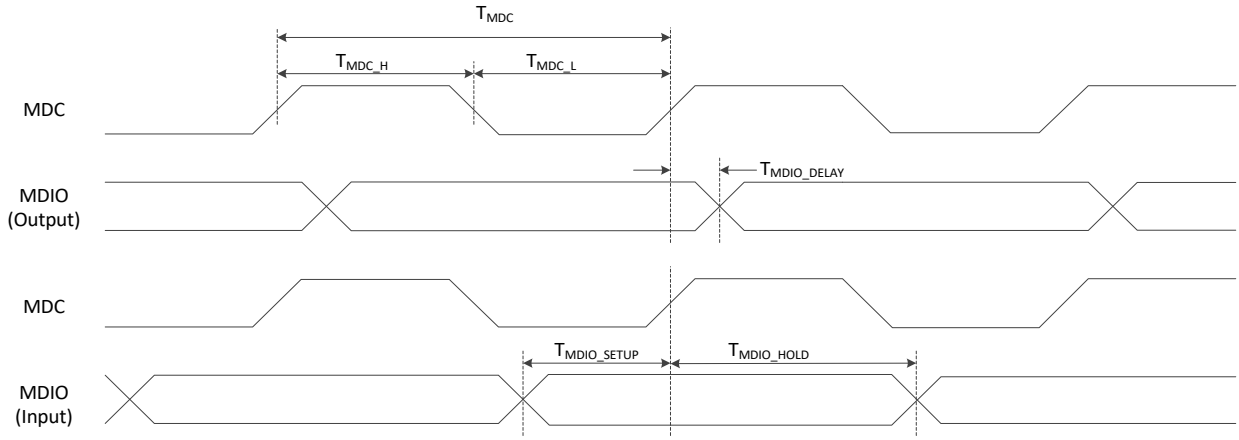


Figure 10-1 SMI MDC & MDIO Timing Diagram

Table 10-6 SMI- MDC & MDIO Timing Parameters

Symbol	Description	Min	Max	Unit
T_{MDC}	MDC Period	80	-	ns
T_{MDC_H}	MDC High Pulse Width	32	-	ns
T_{MDC_L}	MDC Low Pulse Width	32	-	ns
T_{MDIO_DELAY}	MDIO Valid from MDC Rising Edge	0	60	ns
T_{MDIO_SETUP}	MDIO Setup Time to MDC Rising Edge	10	-	ns
T_{MDIO_HOLD}	MDIO Hold Time from MDC Rising Edge	10	-	ns

10.5.2 RGMII Timing

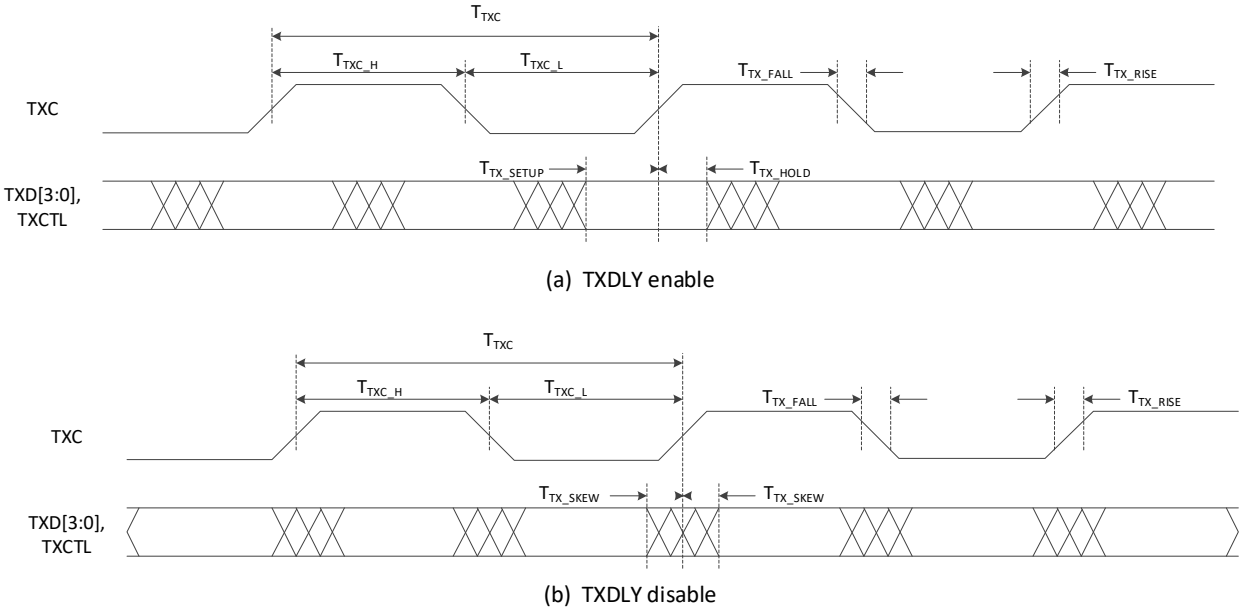
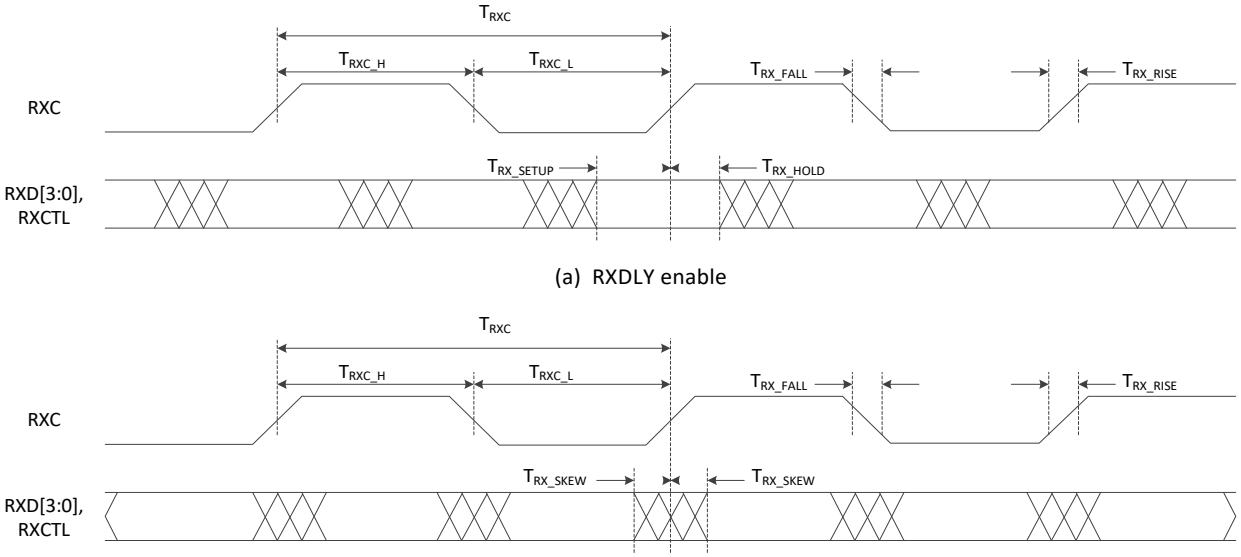


Figure 10-2 RGMII- TX Timing Diagram

Table 10-7 RGMII- TX Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
T_{TXC}	TXC Period (1000Mbps)	7.2	8	8.8	ns
T_{TXC_H}	TXC High Pulse Width (1000Mbps)	3.6	4	4.4	ns
T_{TXC_L}	TXC Low Pulse Width (1000Mbps)	3.6	4	4.4	ns
T_{TXC_RISE}	TXC Rise Time (20% ~ 80%)	-	-	0.75	ns
T_{TXC_FALL}	TXC Fall Time (20% ~ 80%)	-	-	0.75	ns
T_{TXC_SKEW}	TXD/TXCTL to TXC Skew Time	-	0	0.5	ns
T_{TXC_SETUP}	TXD/TXCTL to TXC Setup Time	1	2	-	ns
T_{TXC_HOLD}	TXD/TXCTL to TXC Hold Time	1	2	-	ns



(a) RXDLY enable

(b) RXDLY disable

Figure 10-3 RGMII- RX Timing Diagram

Table 10-8 RGMII- RX Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
T_{RXC}	RXC Period (1000Mbps)	7.2	8	8.8	ns
T_{RXC_H}	RXC High Pulse Width (1000Mbps)	3.6	4	4.4	ns
T_{RXC_L}	RXC Low Pulse Width (1000Mbps)	3.6	4	4.4	ns
T_{RXC_RISE}	RXC Rise Time (20% ~ 80%)	-	-	0.75	ns
T_{RXC_FALL}	RXC Fall Time (20% ~ 80%)	-	-	0.75	ns
T_{RXC_SKEW}	RXD/RXCTL to RXC Skew Time	-	0	0.5	ns
T_{RXC_SETUP}	RXD/RXCTL to RXC Setup Time	1	2	-	ns
T_{RXC_HOLD}	RXD/RXCTL to RXC Hold Time	1	2	-	ns

11 Mechanical Dimensions

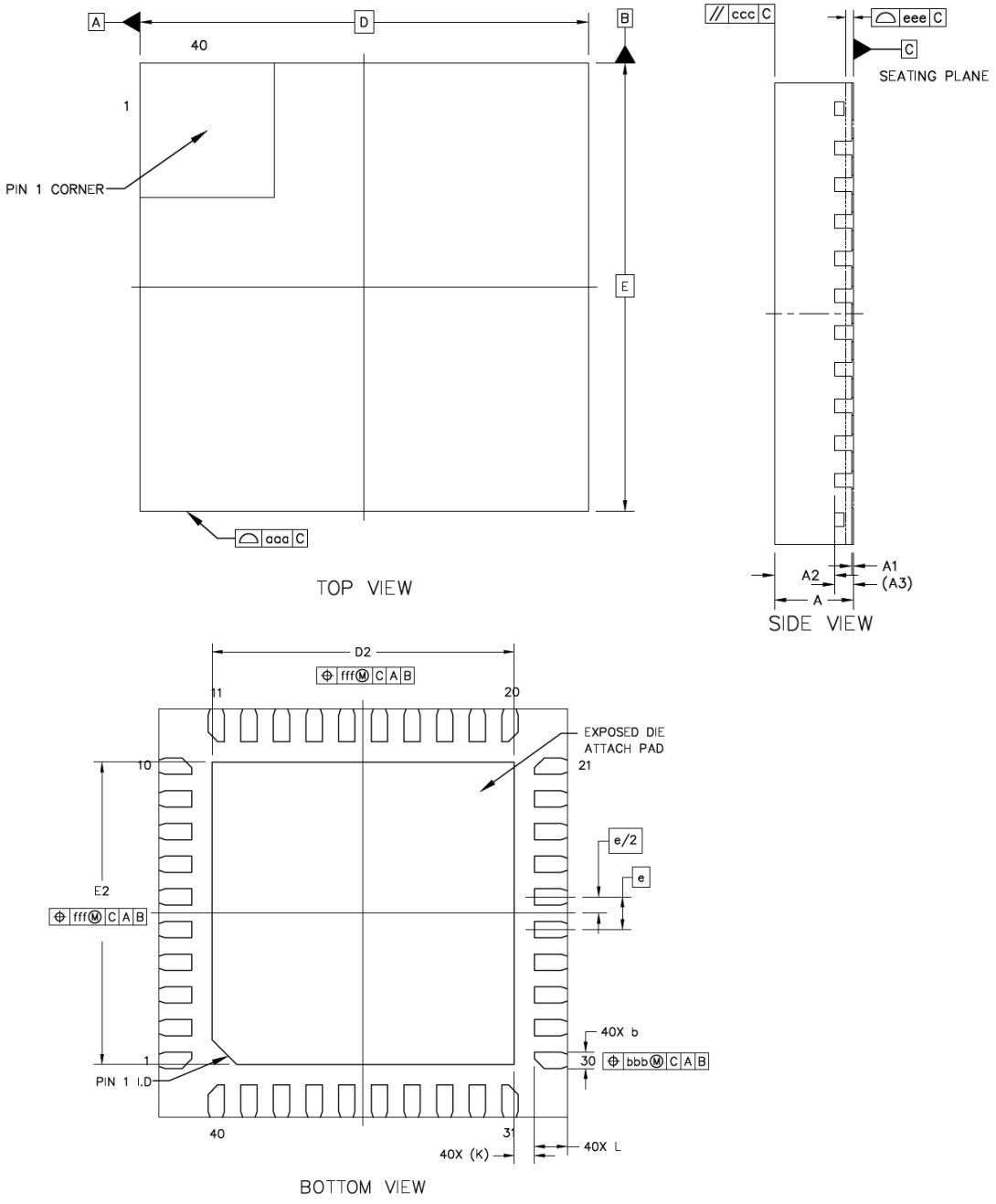


Figure 11-1 **Mechanical Dimensions**

Table 11-1 Mechanical Dimensions

	Symbol	Min	Nom	Max
Total Thickness	A	0.8	0.85	0.9
Stand Off	A1	0	0.02	0.05
Mold Thickness	A2	-	0.65	-

L/F Thickness		A3	0.203 REF		
Lead Width		b	0.15	0.20	0.25
Body Size	**X**	D	5 BSC		
	Y	E	5 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	**X**	D2	3.5	3.6	3.7
	Y	E2	3.5	3.6	3.7
Lead Length		L	0.3	0.4	0.5
Lead Tip To Exposed Pad Edge		K	0.3 REF		

Note1: CONTROLLING DIMENSION: MILLIMETER (mm).

12 Ordering Information

Table 12-1 Ordering Information

Part Number	Package	Ambient Temperature
MAE0621A-Q3C	QFN40	0℃ to 70℃
MAE0621A-Q3I	QFN40	-40℃ to 85℃